



ISO2-CMOS MT8870C/MT8870C-1 Integrated DTMF Receiver

T-75-27-07

Features

- Complete DTMF Receiver
- Low Power Consumption
- Internal Gain Setting Amplifier
- Adjustable Guard Time
- Central Office Quality
- Power-down Mode
- Inhibit Mode

Applications

- Receiver System for British Telecom (BT) or CEPT Spec (MT8870C-1)
- Paging Systems
- Repeater Systems/Mobile Radio
- Credit Card Systems
- Remote Control
- Personal Computers
- Telephone Answering Machine

9161-002-094-NA

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Pin Connections

IN +	1	18	VDD
IN -	2	17	S/GT
GS	3	16	EST
VRef	4	15	STD
INH	5	14	Q4
PWDN	6	13	Q3
OSC1	7	12	Q2
OSC2	8	11	Q1
VSS	9	10	TOE

Ordering Information

- MT8870CE/MT8870CE-1 Plastic DIP
- MT8870CC/MT8870CC-1 Cerdip
- MT8870CS/MT8870CS-1 SOIC
- 40 °C to + 85 °C

Description

The MT8870C/MT8870C-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions, fabricated in Mitel's double poly ISO2-CMOS technology. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses

digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three-state bus interface.

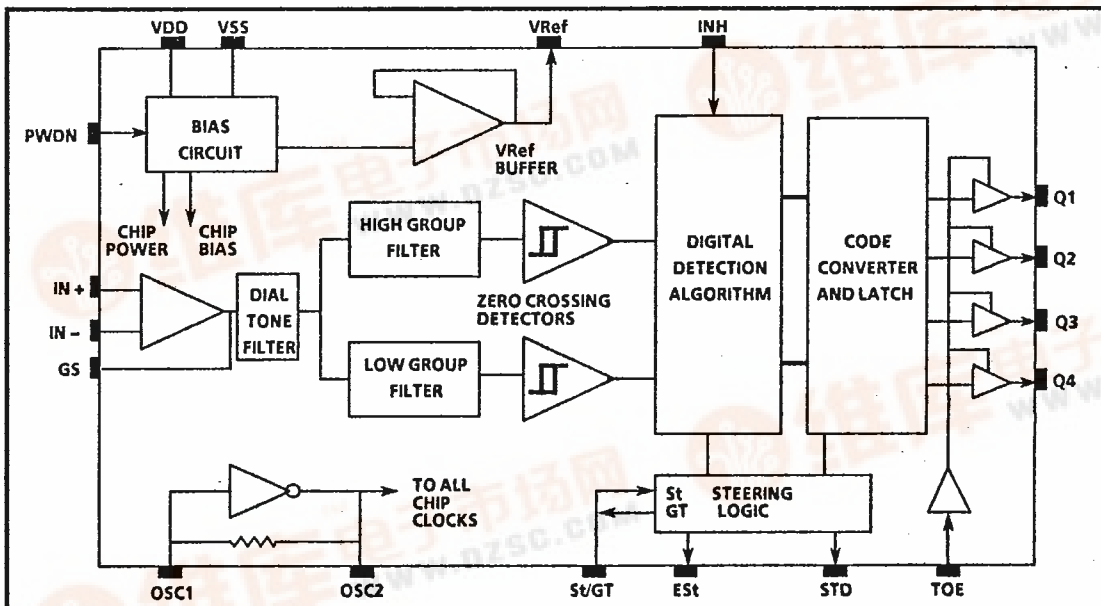


Figure 1 - Functional Block Diagram



Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	DC Power Supply Voltage	V _{DD}		6	V
2	Voltage on any pin	V _I	V _{SS} - 0.3	V _{DD} + 0.3	V
3	Current at any pin (other than supply)	I _I		10	mA
4	Storage temperature	T _{STG}	- 65	+ 150	°C
5	Package power dissipation	P _D		1000	mW

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
 Derate above 75 °C at 16 mW/°C. All leads soldered to board.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Parameter	Sym	Min	Typ†	Max	Units	Test Conditions
1	DC Power Supply Voltage	V _{DD}	4.75	5.0	5.25	V	
2	Operating Temperature	T _O	- 40		+ 85	°C	
3	Crystal/Clock Frequency	f _c		3.579545		MHz	
4	Crystal/Clock Freq. Tolerance	Δf _c		± 0.1		%	

† Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - V_{DD} = 5.0V ± 5%, V_{SS} = 0V, -40°C ≤ T_O ≤ +85°C, unless otherwise stated

	Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions	
1	S U P P L Y	Standby supply current	I _{DDQ}		100	μA	PWDN = V _{DD}	
2		Operating supply current	I _{DD}	3.0	9.0	mA		
3		Power consumption	P _O		15	50	mW	f _c = 3.579545 MHz
4	I N P U T S	High level input	V _{IH}	3.5		V	V _{DD} = 5.0V	
5		Low level input voltage	V _{IL}			1.5	V	V _{DD} = 5.0V
6		Input leakage current	I _{IH} /I _{IL}		0.1		μA	V _{IN} = V _{SS} or V _{DD}
7		Pull up (source) current	I _{SO}		7.5	20	μA	TOE (pin 10) = 0, V _{DD} = 5.0V
8		Pull down (sink) current	I _{SI}		15	45	μA	INH = 5.0V, PWDN = 5.0V, V _{DD} = 5.0V
9		Input impedance (IN +, IN -)	R _{IN}		10		MΩ	@ 1 kHz
10		Steering threshold voltage	V _{TSt}	2.2		2.5	V	V _{DD} = 5.0V
11	O U T P U T S	Low level output voltage	V _{OL}		V _{SS} + 0.03	V	No load	
12		High level output voltage	V _{OH}	V _{DD} - 0.03			V	No load
13		Output low (sink) current	I _{OL}	1.0	2.5		mA	V _{OUT} = 0.4 V
14		Output high (source) current	I _{OH}	0.4	0.8		mA	V _{OUT} = 4.6 V
15		V _{Ref} output voltage	V _{Ref}	2.4		2.7	V	No load, V _{DD} = 5.0V
16		V _{Ref} output resistance	R _{OR}		10		kΩ	

† Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

T-75-27-07

Operating Characteristics - $V_{DD} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $-40^\circ C \leq T_O \leq +85^\circ C$, unless otherwise stated
Gain Setting Amplifier

	Characteristics	Sym	Min	Typ [†]	Max	Units	Test Conditions
1	Input leakage current	I_{IN}			100	nA	$V_{SS} \leq V_{IN} \leq V_{DD}$
2	Input resistance	R_{IN}	10			M Ω	
3	Input offset voltage	V_{OS}			25	mV	
4	Power supply rejection	PSRR	50			dB	1 kHz
5	Common mode rejection	CMRR	40			dB	$-3.0V \leq V_{IN} \leq 3.0V$
6	DC open loop voltage gain	A_{VOL}	32			dB	
7	Unity gain bandwidth	f_C	0.30			MHz	
8	Output voltage swing	V_O	4.0			V_{pp}	Load ≥ 100 k Ω to V_{SS}
9	Maximum capacitive load (GS)	C_L			100	pF	
10	Maximum resistive load (GS)	R_L			50	k Ω	
11	Common mode range	V_{CM}	2.5			V_{pp}	No Load

MT8870C AC Electrical Characteristics[†] - $V_{DD} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $-40^\circ C \leq T_O \leq +85^\circ C$, using Test Circuit shown in Figure 2

	Characteristics	Sym	Min	Typ [†]	Max	Units	Notes [*]
1	Valid input signal levels (each tone of composite signal)		-29			dBm	1,2,3,5,6,9
			-27.5			mV _{RMS}	1,2,3,5,6,9
					+1	dBm	1,2,3,5,6,9
					869	mV _{RMS}	1,2,3,5,6,9
2	Negative twist accept				6	dB	2, 3, 6, 9
3	Positive twist accept				6	dB	2, 3, 6, 9
4	Frequency deviation accept		$\pm 1.5\% \pm 2$ Hz				2, 3, 5, 9
5	Frequency deviation reject		$\pm 3.5\%$				2, 3, 5, 9
6	Third tone tolerance			-16		dB	2, 3, 4, 5, 9, 10
7	Noise tolerance			-12		dB	2, 3, 4, 5, 7, 9, 10
8	Dial tone tolerance			+22		dB	2, 3, 4, 5, 8, 9, 11

[†]Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

***NOTES**

- dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
- Digit sequence consists of all DTMF tones.
- Tone duration = 40 ms, tone pause = 40 ms.
- Signal condition consists of nominal DTMF frequencies.
- Both tones in composite signal have an equal amplitude.
- Tone pair is deviated by $\pm 1.5\% \pm 2$ Hz.
- Bandwidth limited (3 kHz) Gaussian noise.
- The precise dial tone frequencies are (350 Hz and 440 Hz) $\pm 2\%$.
- For an error rate of better than 1 in 10,000.
- Referenced to lowest level frequency component in DTMF signal.
- Referenced to the minimum valid accept level.

MT8870C-1 AC Electrical Characteristics[†] - $V_{DD} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $-40^{\circ}C \leq T_0 \leq +85^{\circ}C$, using Test Circuit shown in Figure 2

	Characteristics	Sym	Min	Typ [†]	Max	Units	Notes [*]
1	Valid input signal levels (each tone of composite signal)		- 31		+ 1	dBm	$V_{DD} = 5.0V$ 1,2,3,5,6,9
			21.8		869	mV _{RMS}	
2	Input Signal Level Reject		- 37			dBm	$V_{DD} = 5.0V$ 1,2,3,5,6,9
			10.9			mV _{RMS}	
3	Negative twist accept				6	dB	2, 3, 6, 9
4	Positive twist accept				6	dB	2, 3, 6, 9
5	Frequency deviation accept		$\pm 1.5\% \pm 2$ Hz				2, 3, 5, 9
6	Frequency deviation reject		$\pm 3.5\%$				2, 3, 5, 9
7	Third tone tolerance		- 18.5			dB	2, 3, 4, 5, 9, 12
8	Noise tolerance			- 12		dB	2, 3, 4, 5, 7, 9, 10
9	Dial tone tolerance			+ 22		dB	2, 3, 4, 5, 8, 9, 11

[†]Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

***NOTES**

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration = 40 ms, tone pause = 40 ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by $\pm 1.5\% \pm 2$ Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) $\pm 2\%$.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. Referenced to Fig. 10 input DTMF tone level at -25dBm (-28dBm at GS Pin) interference frequency range between 480-3400Hz.

AC Electrical Characteristics - $V_{DD} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $-40^{\circ}C \leq T_o \leq +85^{\circ}C$, using Test Circuit shown in Figure 2

	Characteristics	Sym	Min	Typ [‡]	Max	Units	Test Conditions
T I M I N G	Tone present detect time	t_{DP}	5	11	14	ms	see Figure 3
	Tone absent detect time	t_{DA}	0.5	4	8.5	ms	see Figure 3
	Tone duration accept	t_{REC}			40	ms	User adjustable
	Tone duration reject	t_{REC}	20			ms	User adjustable
	Interdigit pause accept	t_{ID}			40	ms	User adjustable
	Interdigit pause reject	t_{DO}	20			ms	User adjustable
O U T P U T S	Propagation delay (St to Q)	t_{PQ}		8	11	μs	TOE = V_{DD}
	Propagation delay (St to StD)	t_{PStD}		12	16	μs	TOE = V_{DD}
	Output data set up (Q to StD)	t_{QStD}		3.4		μs	TOE = V_{DD}
	Propagation delay (TOE to Q ENABLE)	t_{PTE}		50		ns	load of 10 k Ω , 50 pF
	Propagation delay (TOE to Q DISABLE)	t_{PTD}		300		ns	load of 10 k Ω , 50 pF
C L O C K	Crystal /clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
	Clock input rise time	t_{LHCL}			110	ns	Ext. clock
	Clock input fall time	t_{HLCL}			110	ns	Ext. clock
	Clock input duty cycle	DCCL	40	50	60	%	Ext. clock
	Capacitive load (OSC2)	C_{LO}			30	pF	

[‡] Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

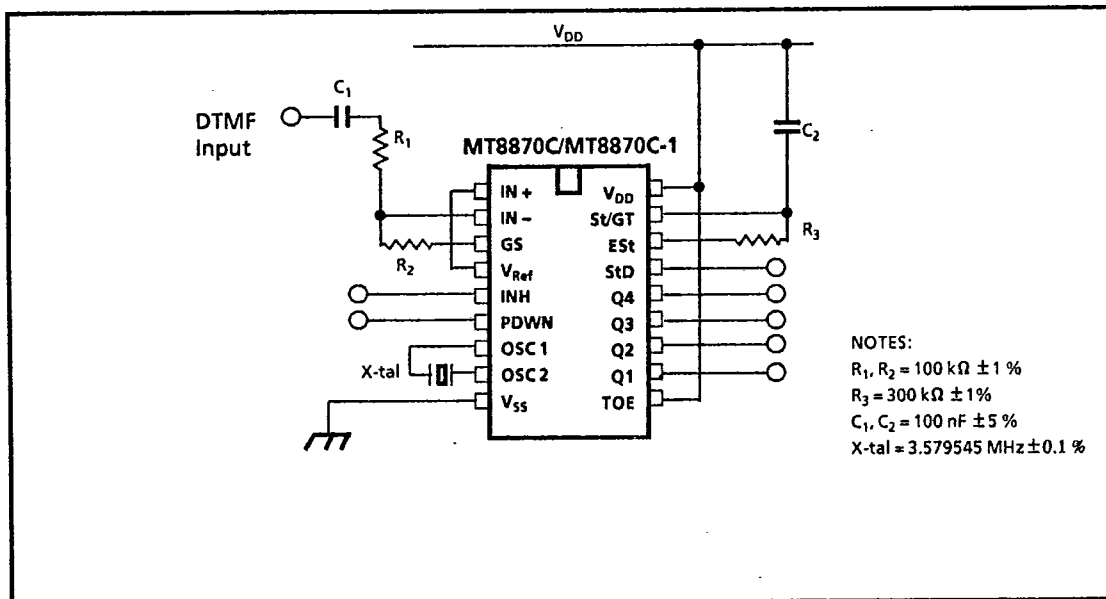


Figure 2 - Single-Ended Input Configuration

Pin Description

Pin #	Name	Description
1	IN +	Non-Inverting Op-Amp (Input).
2	IN -	Inverting Op-Amp (Input).
3	GS	Gain Select. Gives access to output of front end differential amplifier for connection of feedback resistor.
4	V _{Ref}	Reference Voltage (Output), Nominally V _{DD} /2 is used to bias inputs at mid-rail (see Fig.2).
5	INH	Inhibit (Input). Logic high inhibits the detection of tones representing characters A, B, C and D. This pin input is internally pulled down.
6	PWDN	Power Down (Input). Active high. Powers down the device and inhibits the oscillator. This pin input is internally pulled down.
7	OSC1	Clock (Input).
8	OSC2	Clock (Output). A 3.579545 MHz crystal connected between pins OSC1 and OSC2 completes the internal oscillator circuit.
9	V _{SS}	Negative Power Supply (Input).
10	TOE	Three State Output Enable (Input). Logic high enables the outputs Q1-Q4. This pin is pulled up internally.
11-14	Q1-Q4	Three State Data (Output). When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Table 1). When TOE is logic low, the data outputs are high impedance.
15	StD	Delayed Steering (Output). Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below V _{Tst} .
16	ES _t	Early Steering (Output). Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ES _t to return to a logic low.
17	St/GT	Steering Input/Guard time (Output) Bidirectional. A voltage greater than V _{Tst} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V _{Tst} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ES _t and the voltage on St.
18	V _{DD}	Positive power supply (Input).

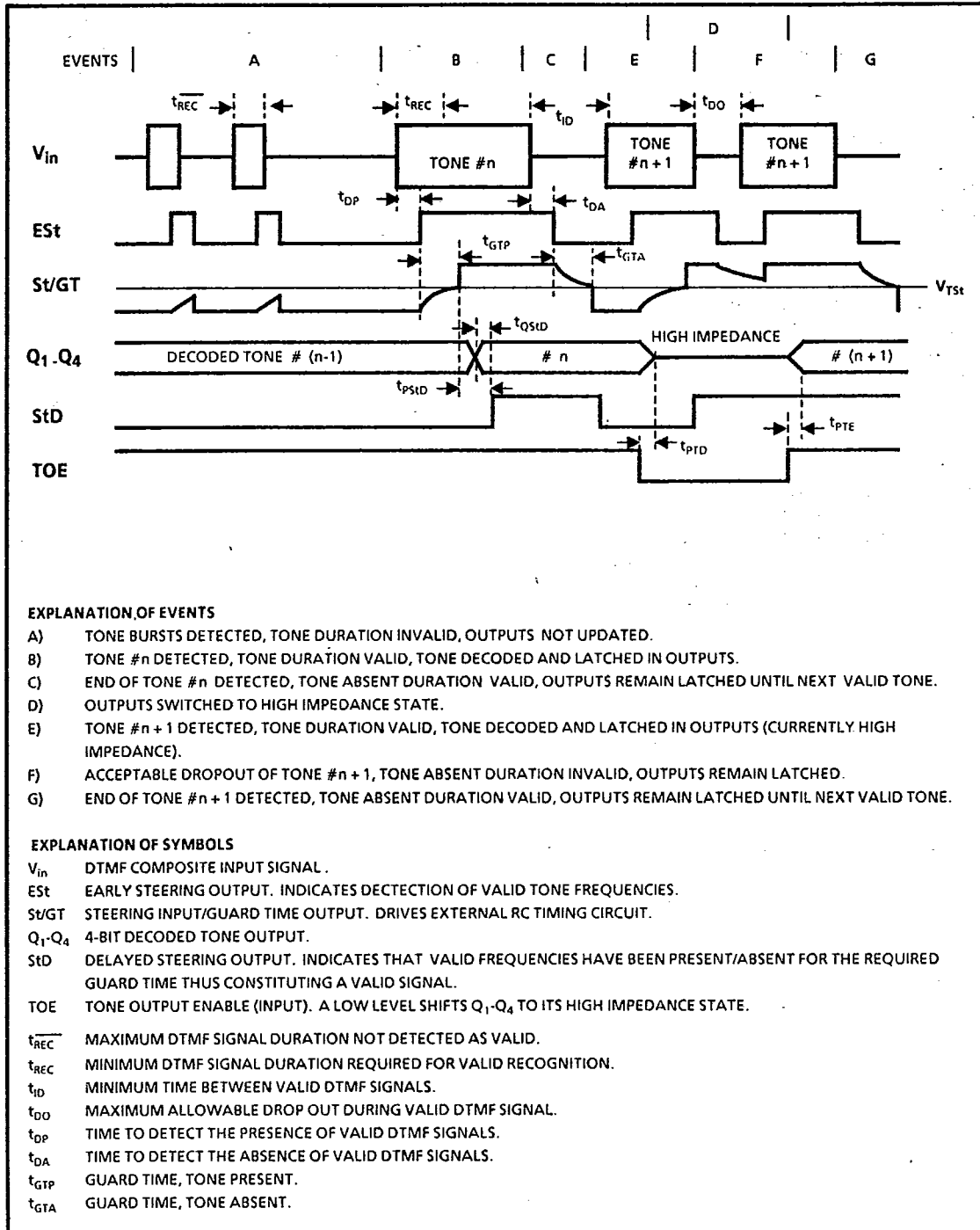


Figure 3- Timing Diagram

Functional Description

The MT8870C/MT8870C-1 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which separates the high and low group tones, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Separation of the low-group and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection (see Figure 4). Each filter output is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

Decoder Section

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone

simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state (see "Steering Circuit").

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes v_c (see Figure 5) to rise as the capacitor discharges. Provided signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), v_c reaches the threshold (V_{TST}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Table 1) into the output latch. At this point the GT output is activated and drives v_c to V_{DD} . GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag (StD) goes high, signalling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three state control input (TOE) to a logic high. The steering circuit works in reverse to validate

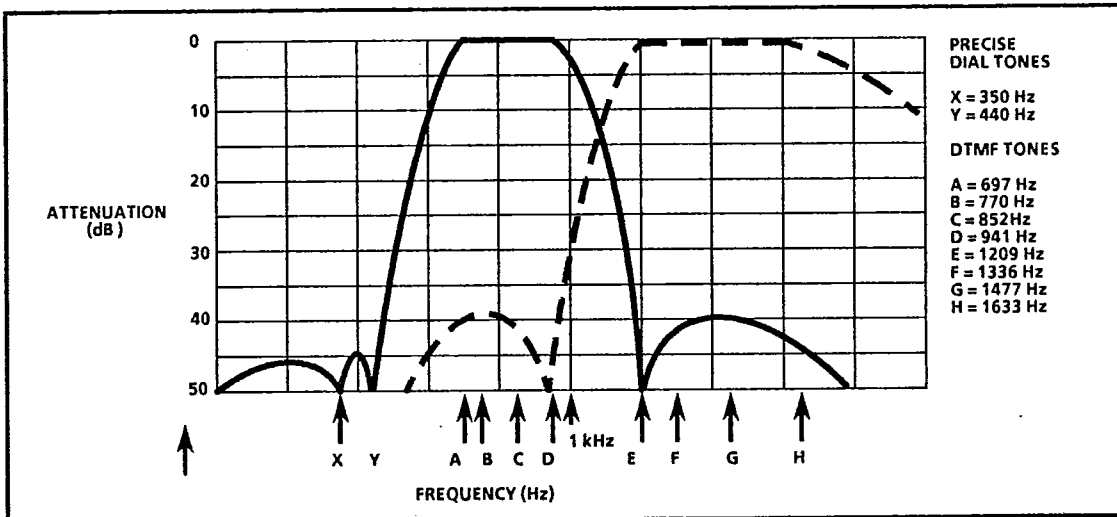


Figure 4- Filter Response

T-75-27-07

Digit	TOE	INH	EST	Q ₄	Q ₃	Q ₂	Q ₁
ANY	L	X	-	Z	Z	Z	Z
1	H	L	H	0	0	0	1
2	H	L	H	0	0	1	0
3	H	L	H	0	0	1	1
4	H	L	H	0	1	0	0
5	H	L	H	0	1	0	1
6	H	L	H	0	1	1	0
7	H	L	H	0	1	1	1
8	H	L	H	1	0	0	0
9	H	L	H	1	0	0	1
0	H	L	H	1	0	1	0
*	H	L	H	1	0	1	1
#	H	L	H	1	1	0	0
A	H	L	H	1	1	0	1
B	H	L	H	1	1	1	0
C	H	L	H	1	1	1	1
D	H	L	H	0	0	0	0
1	H	H	H	0	0	0	1
2	H	H	H	0	0	1	0
3	H	H	H	0	0	1	1
4	H	H	H	0	1	0	0
5	H	H	H	0	1	0	1
6	H	H	H	0	1	1	0
7	H	H	H	0	1	1	1
8	H	H	H	1	0	0	0
9	H	H	H	1	0	0	1
0	H	H	H	1	0	1	0
*	H	H	H	1	0	1	1
#	H	H	H	1	1	0	0
A	H	H	L	undetected, the output code will remain the same as the previous detected code			
B	H	H	L				
C	H	H	L				
D	H	H	L				

L = LOGIC LOW, H = LOGIC HIGH, Z = HIGH IMPEDANCE

Table 1 - Functional Decode Table

the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop out) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

In many situations not requiring selection of tone duration and interdigit pause, the simple steering

circuit shown in Figure 5 is applicable. Component values are chosen according to the formula:

$$t_{REC} = t_{DP} + t_{GTP}$$

$$t_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a device parameter (see Figure 3) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 μ F is recommended for most applications, leaving R to be selected by the designer.

Different steering arrangements may be used to select independently the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigit pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure 6.

Power-down and Inhibit Mode

A logic high applied to pin 6 (PWDN) will power down the device to minimize the power consumption in a standby mode. It stops the oscillator and the functions of the filters.

Inhibit mode is enabled by a logic high input to the pin 5 (INH). It inhibits the detection of tones representing characters A,B,C and D. The output code will remain the same as the previous detected code (see Table 1).

Differential Input Configuration

The input arrangement of the MT8870C/MT8870C-1 provides a differential-input operational amplifier as well as a bias source (V_{REF}) which is used to bias the inputs at mid-rail. Provision is made for connection of a feedback resistor to the op-amp output (G5) for adjustment of gain. In a single-ended configuration, the input pins are connected as shown in Figure 2 with the op-amp connected for unity gain and V_{REF} biasing the input at $\frac{1}{2}V_{DD}$. Figure 7 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R_5 .

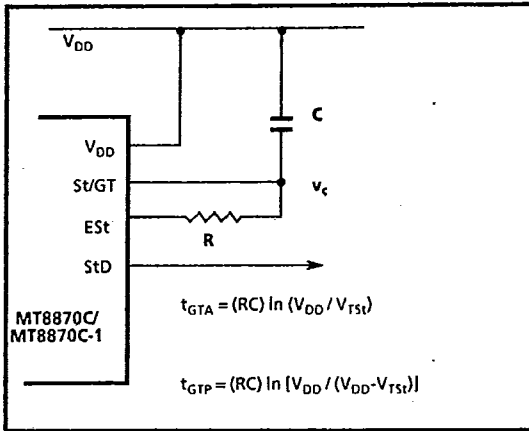


Figure 5- Basic Steering Circuit

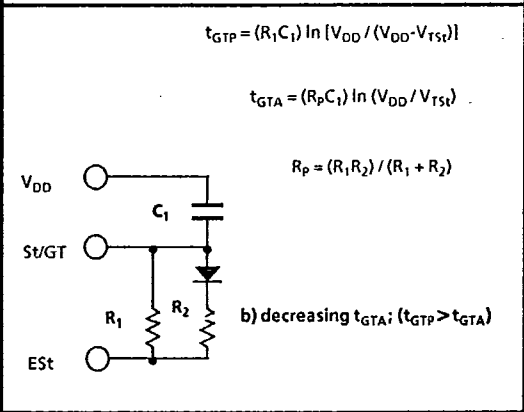
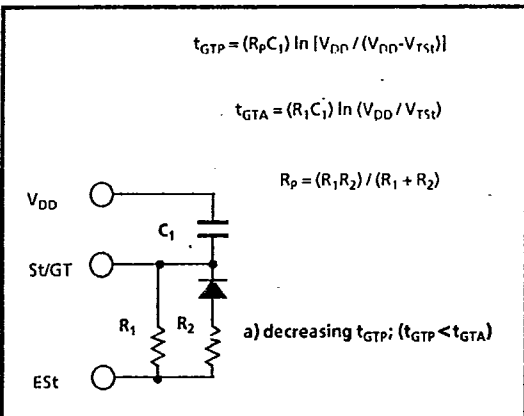
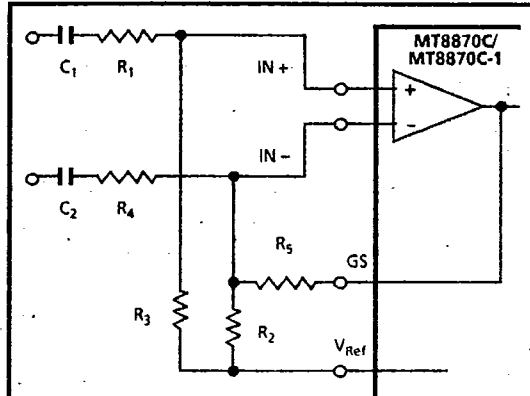


Figure 6- Guard Time Adjustment



DIFFERENTIAL INPUT AMPLIFIER

$C_1 = C_2 = 10 \text{ nF}$
 $R_1 = R_4 = R_5 = 100 \text{ k}\Omega$ All resistors are $\pm 1\%$ tolerance.
 $R_2 = 60 \text{ k}\Omega, R_3 = 37.5 \text{ k}\Omega$ All capacitors are $\pm 5\%$ tolerance.

$$R_3 = \frac{R_2 R_5}{R_2 + R_5}$$

$$\text{VOLTAGE GAIN } (A_v \text{ diff}) = \frac{R_5}{R_1}$$

INPUT IMPEDANCE

$$(Z_{\text{INDIFF}}) = 2 \sqrt{R_1^2 + \left(\frac{1}{\omega C}\right)^2}$$

Figure 7- Differential Input Configuration

to configure several MT8870C/MT8870C-1 devices employing only a single oscillator crystal. The oscillator output of the first device in the chain is coupled through a 30 pF capacitor to the oscillator input (OSC1) of the next device. Subsequent devices are connected in a similar fashion. Refer to Figure 8 for details. The problems associated with unbalanced loading are not a concern with the arrangement shown, ie; precision balancing capacitors are not required.

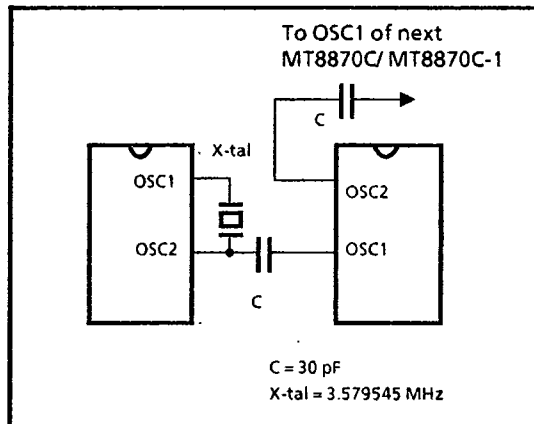


Figure 8- Oscillator Connection

Crystal Oscillator

The internal clock circuit is completed with the addition of an external 3.579545 MHz crystal and is normally connected as shown in Figure 2 (Single Ended Input Configuration). However, it is possible

APPLICATION

RECEIVER SYSTEM FOR BRITISH TELECOM SPEC POR 1151

The circuit shown in Fig. 10 illustrates the use of MT8870C-1 device in a typical receiver system. BT Spec defines the input signals less than -34 dBm as the non-operate level. This condition can be attained by choosing a suitable values of R_1 and R_2 to provide 3 dB attenuation, such that -34 dBm input signal will correspond to -37 dBm at the gain setting pin GS of MT8870C-1. As shown in the diagram, the component values of R_3 and C_2 are the guard time requirements when the total component tolerance is 6%. For better performance, it is recommended to use the non-symmetric guard time circuit in Fig. 9.

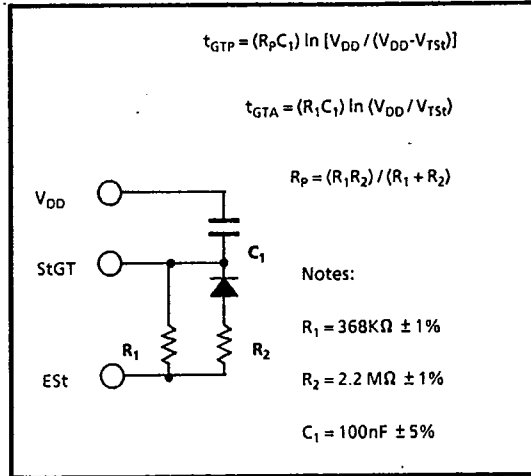


Figure 9 - Non-Symmetric Guard Time Circuit

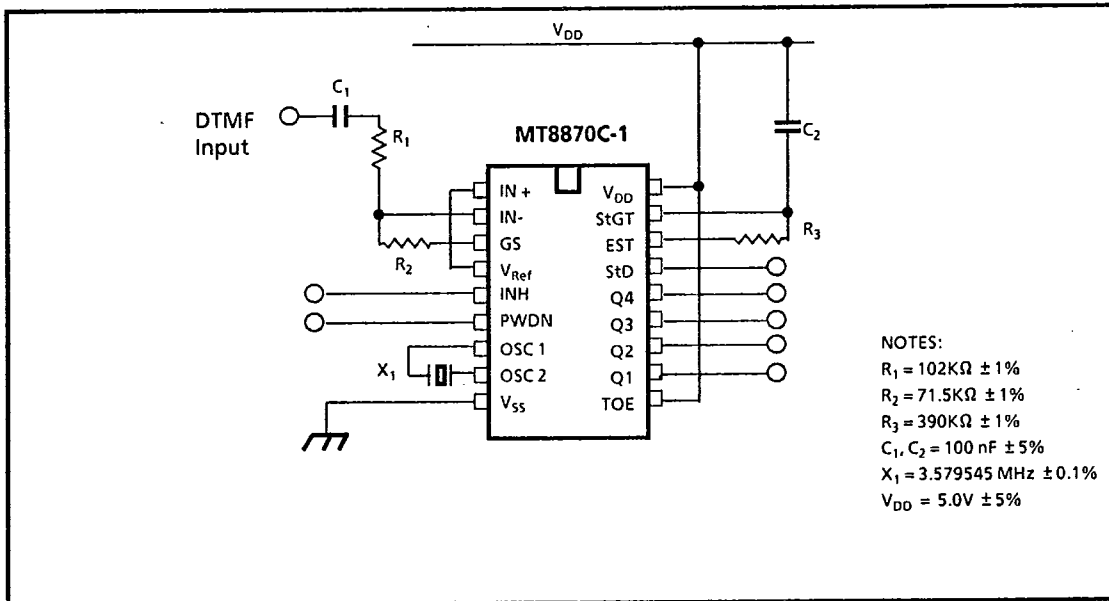


Figure 10 - Single-Ended Input Configuration for BT or CEPT Spec