



CS5361

114 dB, 192 kHz, Multi-Bit Audio A/D Converter

Features

- Advanced Multi-bit Delta-Sigma Architecture
- 24-Bit Conversion
- 114 dB Dynamic Range
- -100 dB THD+N
- System Sampling Rates up to 192 kHz
- Less than 150 mW Power Consumption
- High Pass Filter or DC Offset Calibration
- Supports Logic Levels Between 5 and 1.8V
- Differential Analog Architecture
- Linear Phase Digital Anti-Alias Filtering

General Description

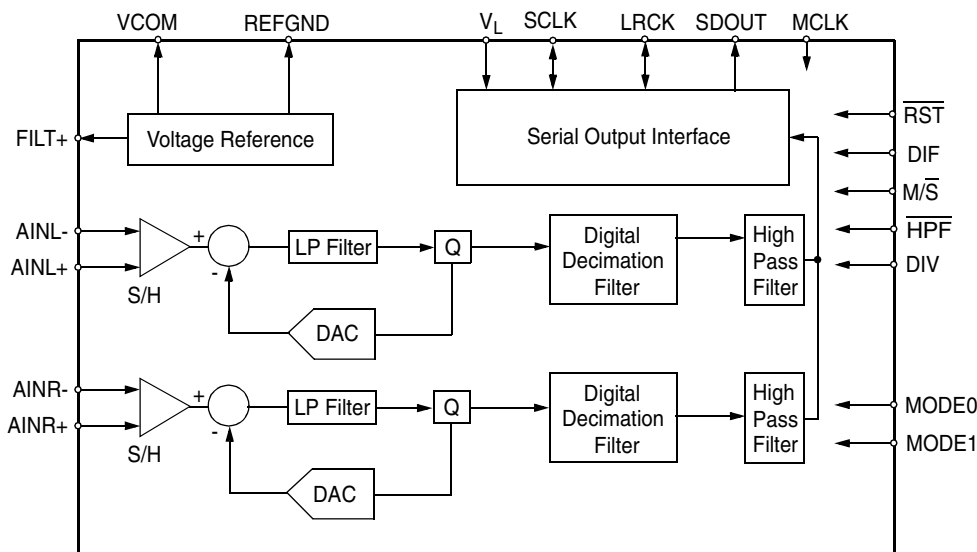
The CS5361 is a complete analog-to-digital converter for digital audio systems. It performs sampling, analog-to-digital conversion and anti-alias filtering, generating 24-bit values for both left and right inputs in serial form at sample rates up to 192 kHz per channel.

The CS5361 uses a 5th-order, multi-bit delta-sigma modulator followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The ADC uses a differential architecture which provides excellent noise rejection.

The CS5361 is ideal for audio systems requiring wide dynamic range, negligible distortion and low noise, such as A/V receivers, DVD-R, CD-R, digital mixing consoles, effects processors, and automotive applications.

ORDERING INFORMATION

CS5361-KS	-10° to 70° C	24-pin SOIC
CS5361-BS	-40° to 85° C	24-pin SOIC
CDB5361	Evaluation Board	



Advance Product Information

This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

TABLE OF CONTENTS

1 CHARACTERISTICS AND SPECIFICATIONS	4
ANALOG CHARACTERISTICS	4
DIGITAL FILTER CHARACTERISTICS.....	5
POWER AND THERMAL CHARACTERISTICS.....	6
DIGITAL CHARACTERISTICS	6
ABSOLUTE MAXIMUM RATINGS	7
RECOMMENDED OPERATING CONDITIONS	7
SWITCHING CHARACTERISTICS	8
2 TYPICAL CONNECTION DIAGRAM	10
3 PIN DESCRIPTIONS	11
4 APPLICATIONS	13
4.1 General Description	13
4.2 High Pass Filter	13
4.3 Analog Connections	13
4.4 Power-up	13
4.5 Synchronization of Multiple Devices	13
4.6 Master/Slave Mode Operation	14
4.7 High Pass Filter and DC Offset Calibration	14
4.8 Grounding and Power Supply Decoupling	15
4.9 Digital Filter	15
5 PARAMETER DEFINITIONS	18
6 REFERENCES	19
7 PACKAGE DIMENSIONS.....	20

Contacting Cirrus Logic Support

For a complete listing of Direct Sales, Distributor, and Sales Representative contacts, visit the Cirrus Logic web site at:
<http://www.cirrus.com/corporate/contacts>

Preliminary product information describes products which are in production, but for which full characterization data is not yet available. Advance product information describes products which are in development and subject to development changes. Cirrus Logic, Inc. has made best efforts to ensure that the information contained in this document is accurate and reliable. However, the information is subject to change without notice and is provided "AS IS" without warranty of any kind (express or implied). Customers are advised to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability. No responsibility is assumed by Cirrus Logic, Inc. for the use of this information, including use of this information as the basis for manufacture or sale of any items, nor for infringements of patents or other rights of third parties. This document is the property of Cirrus Logic, Inc. and by furnishing this information, Cirrus Logic, Inc. grants no license, express or implied under any patents, mask work rights, copyrights, trademarks, trade secrets or other intellectual property rights of Cirrus Logic, Inc. Cirrus Logic, Inc., copyright owner of the information contained herein, gives consent for copies to be made of the information only for use within your organization with respect to Cirrus Logic integrated circuits or other parts of Cirrus Logic, Inc. The same consent is given for similar information contained on any Cirrus Logic website or disk. This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale. The names of products of Cirrus Logic, Inc. or other vendors and suppliers appearing in this document may be trademarks or service marks of their respective owners which may be registered in some jurisdictions. A list of Cirrus Logic, Inc. trademarks and service marks can be found at <http://www.cirrus.com>.

LIST OF FIGURES

Figure 1. Master Mode, Left Justified (DIF low)	9
Figure 2. Slave Mode, Left Justified (DIF low)	9
Figure 3. Master Mode, I ² S Format (DIF high).....	9
Figure 4. Slave Mode, I ² S Format (DIF high).....	9
Figure 5. Typical Connection Diagram.....	10
Figure 6. CS5361 Master Mode: LRCK Generation.....	14
Figure 7. CS5361 Master Mode: SCLK Generation.....	14
Figure 8. Left Justified Format, DIF Low	15
Figure 9. I ² S Format, DIF High	15
Figure 10. Full Scale Input Voltage	15
Figure 11. Single Speed Mode Stopband Rejection	16
Figure 12. Single Speed Mode Transition Band.....	16
Figure 13. Single Speed Mode Transition Band (Detail).....	16
Figure 14. Single Speed Mode Passband Ripple	16
Figure 15. Double Speed Mode Stopband Rejection.....	16
Figure 16. Double Speed Mode Transition Band	16
Figure 17. Double Speed Mode Transition Band (Detail)	17
Figure 18. Double Speed Mode Passband Ripple	17
Figure 19. Quad Speed Mode Stopband Rejection	17
Figure 20. Quad Speed Mode Transition Band.....	17
Figure 21. Quad Speed Mode Transition Band (Detail).....	17
Figure 22. Quad Speed Mode Passband Ripple.....	17

LIST OF TABLES

Table 1. CS5361 Common Master Clock Frequencies	12
Table 2. CS5361 Mode Control	12
Table 3. CS5361 SCLK/LRCK Ratios	14
Table 4. CS5361 MCLK/LRCK Ratios.....	14

1 CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS ($T_A = 25^\circ \text{C}$; Logic "0" = GND = 0 V; Logic "1" = VL = 5V; MCLK = 12.288 MHz, Fs for Single Speed Mode = 48 kHz, Fs for Double Speed Mode = 96 kHz, Fs for Quad Speed Mode = 192 kHz, SCLK = 64 Fs, Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Input is 997Hz sine wave.)

Parameter	Symbol	CS5361KS			CS5361BS			Unit	
		Min	Typ	Max	Min	Typ	Max		
Single Speed Mode									
Dynamic Range	A-weighted	TBD	114	-	TBD	114	-	dB	
	unweighted	TBD	111	-	TBD	111	-	dB	
Total Harmonic Distortion + Noise	THD+N	-	-100	TBD	-	-100	TBD	dB	
	-1 dB	-	-91	-	-	-91	-	dB	
	-20 dB	-	-51	-	-	-51	-	dB	
	-60 dB	-	-	-	-	-	-	dB	
Double Speed Mode									
Dynamic Range	A-weighted	TBD	114	-	TBD	114	-	dB	
	unweighted	TBD	111	-	TBD	111	-	dB	
Total Harmonic Distortion + Noise	THD+N	-	-100	TBD	-	-100	TBD	dB	
	-1 dB	-	-91	-	-	-91	-	dB	
	-20 dB	-	-51	-	-	-51	-	dB	
	-60 dB	-	-	-	-	-	-	dB	
Quad Speed Mode									
Dynamic Range	A-weighted	TBD	114	-	TBD	114	-	dB	
	unweighted	TBD	111	-	TBD	111	-	dB	
Total Harmonic Distortion + Noise	THD+N	-	-100	TBD	-	-100	TBD	dB	
	-1 dB	-	-91	-	-	-91	-	dB	
	-20 dB	-	-51	-	-	-51	-	dB	
	-60 dB	-	-	-	-	-	-	dB	
Dynamic Performance for All Modes									
Interchannel Isolation		-	110	-	-	110	-	dB	
Interchannel Phase Deviation		-	0.0001	-	-	0.0001	-	Degree	
DC Accuracy									
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB	
Gain Error		-	-	TBD	-	-	TBD	%	
Gain Drift		-	+/-100	-	-	+/-100	-	ppm/°C	
Offset Error	with HPF active	-	0	-	-	0	-	LSB	
Analog Input Characteristics									
Full-scale Input Voltage		TBD	2.0	TBD	TBD	2.0	TBD	Vrms	
Input Impedance (Differential)*		37	-	-	37	-	-	kΩ	
Common Mode Rejection Ratio	CMRR	-	82	-	-	82	-	dB	

* Measured between AIN+ and AIN-

DIGITAL FILTER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Single Speed Mode (2kHz to 50kHz sample rates)					
Passband (-0.1 dB)		0	-	22.5	kHz
Passband Ripple		-	-	±0.035	dB
Stopband		27.8	-	-	kHz
Stopband Attenuation		-95	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	12/Fs	-	s
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0.0	μs
Double Speed Mode (50kHz to 100kHz sample rates)					
Passband (-0.1 dB)		0	-	43.2	kHz
Passband Ripple		-	-	±0.035	dB
Stopband		64.3	-	-	kHz
Stopband Attenuation		-92	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	9/Fs	-	s
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0.0	μs
Quad Speed Mode (100kHz to 192kHz sample rates)					
Passband (-0.1 dB)		0	-	47	kHz
Passband Ripple		-	-	±0.035	dB
Stopband		148.8	-	-	kHz
Stopband Attenuation		-97	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	5/Fs	-	s
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0.0	μs
High Pass Filter Characteristics					
Frequency Response -3.0 dB		-	1	-	Hz
-0.13 dB (Note 1)		-	20	-	Hz
Phase Deviation @ 20Hz (Note 1)		-	10	-	Deg
Passband Ripple		-	-	0	dB

Notes: 1. Response shown is for Fs equal to 48 kHz. Filter characteristics scale with Fs.

POWER AND THERMAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$; $V_A = 5\text{V}$; $\text{MCLK} = 12.288\text{ MHz}$; Master Mode)

Parameter	Symbol	CS5361-KS			CS5361-BS			Unit	
		Min	Typ	Max	Min	Typ	Max		
Power Supply Current (Normal Operation)	V_A	I_A	-	15	TBD	-	15	TBD	mA
	$V_L, V_D = 5\text{V}$	I_D	-	12	TBD	-	12	TBD	mA
	$V_L, V_D = 3.3\text{V}$	I_D	-	TBD	TBD	-	TBD	TBD	mA
Power Supply Current (Power-Down Mode) (Note 2)	V_A	I_A	-	2	-	-	2	-	mA
	$V_D = 5\text{V}$	I_D	-	2	-	-	2	-	mA
Power Consumption (Normal Operation)	$V_D = 5\text{V}$	-	-	135	TBD	-	135	TBD	mW
	$V_D = 3.3\text{V}$	-	-	TBD	-	-	TBD	-	mW
	(Power-Down Mode)	-	-	20	-	-	20	-	mW
Power Supply Rejection Ratio (1 kHz) (Note 3)	PSRR	-	65	-	-	65	-	dB	
Allowable Junction Temperature		-	-	135	-	-	135	$^\circ\text{C}$	
Junction to Ambient Thermal Impedance	θ_{JA}	-	TBD	-	-	TBD	-	$^\circ\text{C/W}$	

DIGITAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$; $V_D = 5\text{V} \pm 5\%$)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (% of V_L)	V_{IH}	70%	-	-	V
Low-Level Input Voltage (% of V_L)	V_{IL}	-	-	30%	V
High-Level Output Voltage at $I_o = 20\text{ }\mu\text{A}$	V_{OH}	$V_L - 1.0$	-	-	V
Low-Level Output Voltage at $I_o = 20\text{ }\mu\text{A}$	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	± 10	μA

- Notes: 2. Power Down Mode is defined as $\overline{\text{RST}} = \text{Low}$ with all clocks and data lines held static.
3. Valid with the recommended capacitor values on FILT+ and VCOM as shown in the Typical Connection Diagram.

ABSOLUTE MAXIMUM RATINGS (GND = 0V, All voltages with respect to ground.)

Parameter	Symbol	Min	Typ	Max	Units	
DC Power Supplies:	Analog	VA	-0.3	-	+6.0	V
	Logic	VL	-0.3	-	+6.0	V
	Digital	VD	-0.3	-	+6.0	V
Input Current	(Note 4)	I_{in}	-	-	± 10	mA
Analog Input Voltage	(Note 5)	V_{IN}	GND-0.7	-	VA+0.7	V
Digital Input Voltage	(Note 5)	V_{IND}	-0.7	-	VL+0.7	V
Ambient Operating Temperature (Power Applied)		T_A	-55	-	+70	°C
Storage Temperature		T_{stg}	-65	-	+150	°C

- Notes: 4. Any pin except supplies. Transient currents of up to ± 100 mA on the analog input pins will not cause SCR latch-up.
5. The maximum over/under voltage is limited by the input current.

WARNING: Operation beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (GND = 0V, all voltages with respect to ground.)

Parameter	Symbol	Min	Typ	Max	Units	
DC Power Supplies:	Positive Analog	VA	4.75	5.0	5.25	V
	Positive Digital	VD	3.1	-	5.25	V
	Positive Logic	VL	1.7	-	5.25	V
Ambient Operating Temperature (Power Applied)	CS5361-KS	T_A	-10	-	+70	°C
	CS5361-BS	T_A	-40	-	+85	°C

SWITCHING CHARACTERISTICS ($T_A = 25^\circ \text{C}$; Logic "0" = GND = 0 V; Logic "1" = VL = VA = VD = 5 V, $C_L = 20 \text{ pF}$)

Parameter	Symbol	Min	Typ	Max	Unit	
Input Sample Rate	Single Speed Mode	Fs	2	-	50	kHz
	Double Speed Mode	Fs	50	-	100	kHz
	Quad Speed Mode	Fs	100	-	192	kHz
MCLK Specifications						
MCLK Period	t_{clkw}	40	-	1953	ns	
MCLK Pulse Width High	t_{clkh}	15	-	-	ns	
MCLK Pulse Width Low	t_{ckl}	15	-	-	ns	
Master Mode						
SCLK falling to LRCK	t_{mslr}	-20	-	20	ns	
SCLK falling to SDOOUT valid	t_{sdo}	0	-	40	ns	
SCLK Duty Cycle		-	50	-	%	
SCLK Output Frequency		-	$64 \bullet F_s$	-	Hz	
LRCK Output Frequency (Fs)		-	MCLK+256	-	Hz	
Slave Mode						
Single Speed						
LRCK Duty Cycle		40	50	60	%	
SCLK Period	t_{sclkw}	163	-	-	ns	
SCLK High/Low	t_{sclkh}	20	-	-	ns	
SCLK falling to SDOOUT valid	t_{dss}	-	-	40	ns	
SCLK falling to LRCK edge	t_{slrd}	-20	-	20	ns	
Double Speed						
LRCK Duty Cycle		40	50	60	%	
SCLK Period	t_{sclkw}	163	-	-	ns	
SCLK High/Low	t_{sclkh}	20	-	-	ns	
SCLK falling to SDOOUT valid	t_{dss}	-	-	40	ns	
SCLK falling to LRCK edge	t_{slrd}	-20	-	20	ns	
Quad Speed						
LRCK Duty Cycle		40	50	60	%	
SCLK Period	t_{sclkw}	81	-	-	ns	
SCLK High/Low	t_{sclkh}	20	-	-	ns	
SCLK falling to SDOOUT valid	t_{dss}	-	-	20	ns	
SCLK falling to LRCK edge	t_{slrd}	-10	-	10	ns	

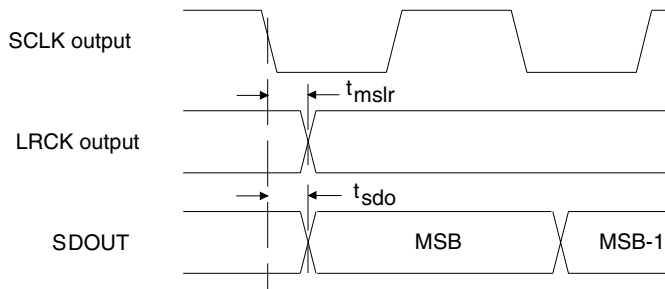


Figure 1. Master Mode, Left Justified (DIF low)

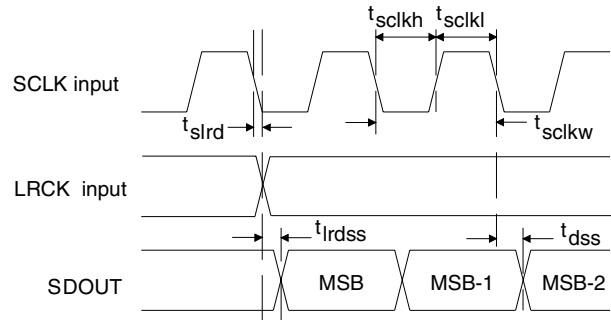


Figure 2. Slave Mode, Left Justified (DIF low)

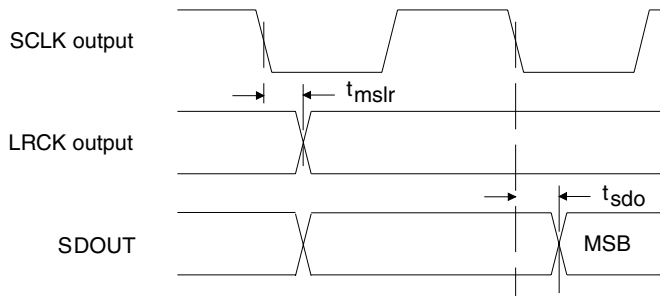


Figure 3. Master Mode, I²S Format (DIF high)

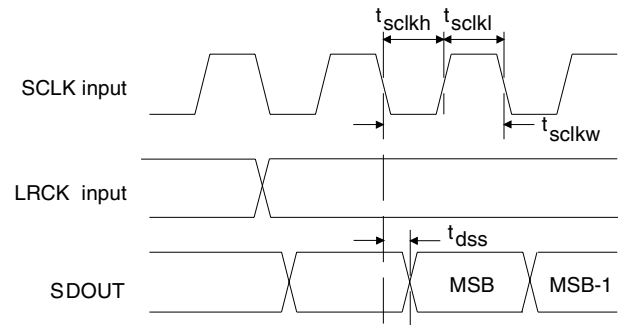
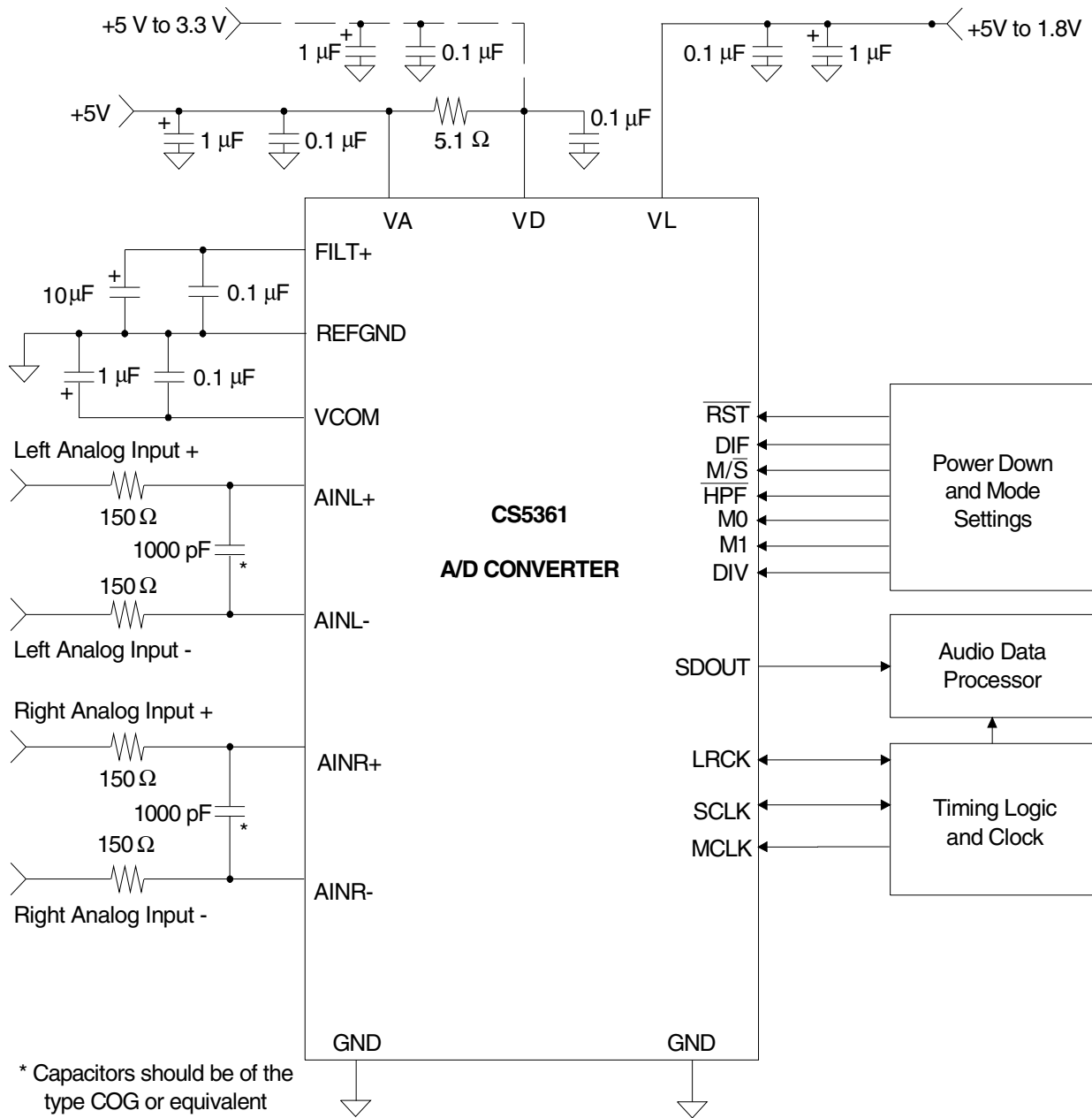


Figure 4. Slave Mode, I²S Format (DIF high)

2 TYPICAL CONNECTION DIAGRAM

Figure 5. Typical Connection Diagram

3 PIN DESCRIPTIONS

Reset	RST	□ 1	24 □	FILT+	Voltage Reference
Master/Slave Mode	M/S	□ 2	23 □	REFGND	Reference Ground
Left/Right Clock	LRCK	□ 3	22 □	VCOM	Common Mode Voltage
Serial Data Clock	SCLK	□ 4	21 □	AINR+	Right Channel Analog Input+
Master Clock	MCLK	□ 5	20 □	AINR-	Right Channel Analog Input-
Digital Power	VD	□ 6	19 □	VA	Analog Power
Ground	GND	□ 7	18 □	GND	Ground
Logic Level	VL	□ 8	17 □	AINL-	Left Channel Analog Input-
Serial Data	SDOUT	□ 9	16 □	AINL+	Left Channel Analog Input+
MCLK Divider	DIV	□ 10	15 □	TST	Test Pin
High Pass Filter Enable	HPF	□ 11	14 □	M1	Mode Select
Digital Interface Format	DIF	□ 12	13 □	M0	Mode Select

Power Supply and Ground

Pin Name	#	Pin Description
RST	1	Reset (Input) - The device enters a low power mode when low.
M/S	2	Master/Slave Mode (Input) - In Master mode, SCLK and LRCK are outputs. Internal dividers divide the master clock to generate the serial clock and the left/right clock. In Slave mode, LRCK and SCLK become inputs.
LRCK	3	Left Right Clock (Input/Output) - Determines which channel, Left or Right, is currently active on the serial audio data line. The frequency of the left/right clock must be at the audio sample rate, Fs.
SCLK	4	Serial Clock (Input/Output) - Serial clock for the serial audio interface.
MCLK	5	Master Clock (Input) - Clock source for the delta-sigma modulator and digital filters. Table 1 illustrates several standard audio sample rates and the required master clock frequency.
VD	6	Digital Power (Input) - Positive power supply for the digital section. Refer to the Recommended Operating Conditions for appropriate voltages.
GND	7, 18	Ground (Input) - Ground reference. Must be connected to analog ground.
VL	8	Logic Power (Input) - Determines the required signal level for the digital input/output. Refer to the Recommended Operating Conditions for appropriate voltages.
SDOUT	9	Serial Audio Data Output (Output) - Output for two's complement serial audio data.
DIV	10	MCLK Divider (Input) - When high, the externally supplied MCLK is divided by two prior to all other chip circuitry.
HPF	11	High Pass Filter Enable (Input) - The device includes a high pass filter after the decimator to remove the indeterminate DC offsets introduced by the analog buffer stage and the analog modulator. The first-order high pass filter response characteristics are detailed in the Digital Filter specifications table. The filter response scales linearly with sample rate.
DIF	12	Digital Interface Format (Input) - The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format selection. Refer to Figures 8 and 9.
M0 M1	13, 14	Mode Selection (Input) - Determines the operational mode of the device as detailed in Table 2.
TST	15	Test Pin (Input) - This pin needs to be connected to GND.
AINL+ AINL-	16, 17	Differential Left Channel Analog Input (Input) - Signals are presented differentially to the delta-sigma modulators via the AINL+/- pins. The full scale differential analog input level is specified in the Analog Characteristics Specification table.

VA	19	Analog Power (Input) - Positive power supply for the analog section. Refer to the Recommended Operating Conditions for appropriate voltages.
AINR+ AINR-	20, 21	Differential Right Channel Analog Input (Input) - Signals are presented differentially to the delta-sigma modulators via the AINR+/- pins. The full scale differential analog input level is specified in the Analog Characteristics Specification table.
VCOM	22	Common Mode Voltage (Output) - Nominally 2.5 volts; can be used to bias the analog input circuitry to the common mode voltage of the CS5361. VCOM is not buffered and the maximum current is 10 uA.
REF_GND	23	Reference Ground (Input) - Ground reference for the internal sampling circuits and must be connected to analog ground.
FILT+	24	Positive Voltage Reference (Output) - Positive reference voltage for the internal sampling circuits. Requires the capacitive decoupling to GND as shown in the Typical Connection Diagram.

SAMPLE RATE (kHz)	DIV = 1 MCLK (MHz)	DIV = 0 MCLK (MHz)
32	8.192	16.384
44.1	11.2896	22.5792
48	12.288	24.576
64	8.192	16.384
88.2	11.2896	22.5792
96	12.288	24.576
176.4	11.2896	22.5792
192	12.288	24.576

Table 1. CS5361 Common Master Clock Frequencies

Mode 1	Mode 0	MODE
0	0	Single Speed Mode
0	1	Double Speed Mode
1	0	Quad Speed Mode
1	1	Reserved

Table 2. CS5361 Mode Control

4 APPLICATIONS

4.1 General Description

The CS5361 is a 24-bit, stereo A/D converter designed for digital audio applications. The analog input channels are simultaneously sampled by separate, 5th-order delta-sigma modulators. The resulting serial bit streams are digitally filtered, yielding pairs of 24-bit values at output sample rates (F_s) of up to 192 kHz. This technique yields nearly ideal conversion performance independent of input frequency and amplitude.

The converter does not require anti-alias filters, external sample-and-hold amplifiers or voltage references. Only normal power supply decoupling components, voltage reference bypass capacitors and a single resistor and capacitor on each input for anti-aliasing are required, as shown in Figure 5. Output data is available in serial form, coded as 2's complement 24-bit numbers. For more information on delta-sigma modulation techniques see the references at the end of this data sheet.

4.2 High Pass Filter

The CS5361 includes a digital high pass filter after the decimator to remove the indeterminate DC offsets introduced by the analog buffer stage and the CS5361 analog modulator. The first-order high pass filter is detailed in the Digital Filter specifications table. The filter response scales linearly with the sample rate.

4.3 Analog Connections

The analog modulator samples the input at 6.144 MHz ($MCLK=12.288$ MHz). The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are $(n \times 6.144$ MHz) the digital passband frequency, where $n=0,1,2,\dots$. Refer to the Typical Connection Diagram which shows the suggested filter that will attenuate any noise energy at

6.144 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these can degrade signal linearity. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the AINR and AINL pins.

4.4 Power-up

Reliable power-up can be accomplished by keeping the device in reset until the power supplies, clocks and configuration pins are stable. It is also recommended that reset be activated if the analog or digital supplies drop below the recommended operating condition to prevent power glitch related issues.

Due to the presence of external capacitance on the FILT+ pin, a time delay of approximately $10\text{ns}/\mu\text{F}$ is required after applying power to the device or after exiting a reset state for the reference to come up. The delta-sigma modulators settle in a matter of microseconds after the analog section is powered, either through the application of power or by setting the reset pin high.

4.5 Synchronization of Multiple Devices

In systems where multiple ADCs are required, care must be taken to achieve simultaneous sampling. To ensure synchronous sampling, the MCLK and LRCK must be the same for all CS5361's in the system. If only one master clock source is needed, one solution is to place one CS5361 in Master mode, and slave all of the other CS5361's to the one master. If multiple master clock sources are needed, a possible solution would be to supply all clocks from the same external source and time the CS5361 reset with the inactive edge of MCLK. This will ensure that all of the CS5361's in the system will begin sampling on the same clock edge.

4.6 Master/Slave Mode Operation

The CS5361 can operate in Master or Slave mode, which is selectable via pin 2 (M/\bar{S}). In Master mode, LRCK and SCLK are outputs. The CS5361 will produce an LRCK that is equal to the output sample rate, F_s , and an SCLK that is $64x F_s$.

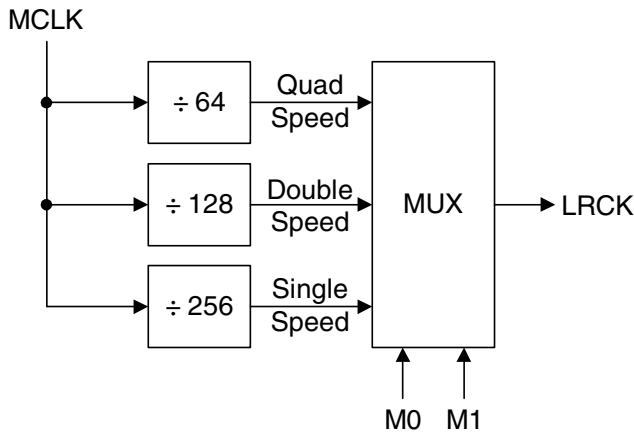


Figure 6. CS5361 Master Mode: LRCK Generation

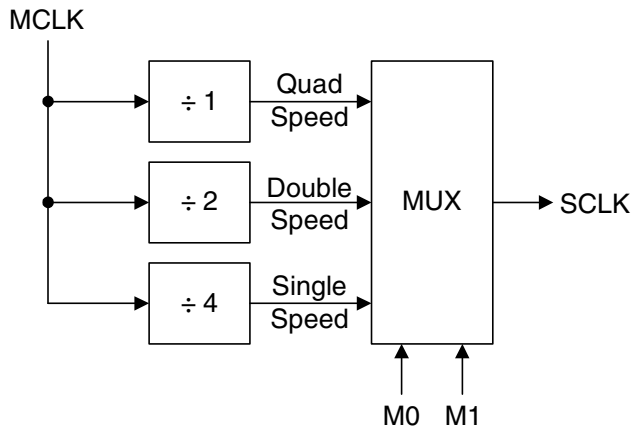


Figure 7. CS5361 Master Mode: SCLK Generation

In Slave mode, LRCK and SCLK become inputs. The LRCK must be equal to the sample rate, F_s . The SCLK must be equal to $128x$, $64x$, or $32x F_s$. It is recommended that SCLK be equal to $64x F_s$ to avoid potential interference effects which may degrade system performance. See Table 3 for more details.

	Mode0 (SSM)	Mode1 (DSM)	Mode2 (QSM)
Master Mode	64x	64x	64x
Slave Mode	32x, 64x, 128x	32x, 64x	64x

Table 3. CS5361 SCLK/LRCK Ratios

The MCLK/LRCK ratio requirements for Master and Slave mode operation is described in Table 4.

	Mode0 (SSM)	Mode1 (DSM)	Mode2 (QSM)
Master Mode	256x	128x	64x
Slave Mode	256x	128x	128x

Table 4. CS5361 MCLK/LRCK Ratios

4.7 High Pass Filter and DC Offset Calibration

The operational amplifiers in the input circuitry driving the CS5361 may generate a small DC offset into the A/D converter. The CS5361 includes a high pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding "clicks" when switching between devices in a multichannel system. The high pass filter can be removed from the signal path by keeping the \overline{HPF} pin high as the part comes out of reset.

The high pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. If the \overline{HPF} pin is taken high during normal operation, the current value of the DC offset register is frozen and this DC offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

- 1) running the CS5361 with the high pass filter enabled for approximately 1 second until the filter settles followed by
- 2) disabling the high pass filter and freezing the stored DC offset.

A system calibration performed in this way will eliminate offsets anywhere in the signal path between the calibration point and the CS5361.

4.8 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS5361 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 5 shows the recommended power arrangements, with VA and VL connected to clean supplies. VD, which powers the digital filter, may be run from the system logic supply or may be powered from the analog supply via a ferrite bead. In this case, no additional devices should be powered from VD. Please refer to the Recommended Operating Conditions for supply voltage ranges. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest. All signals, especially clocks, should be kept away from the FILT+ and VCOM pins in order to avoid unwanted coupling into the modulators. The FILT+ and VCOM decoupling capacitors, particularly the 0.1 μ F, must be positioned to minimize the electrical path from FILT+ and pin 23, REFGND. The CDB5361

evaluation board demonstrates the optimum layout and power supply arrangements. To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

4.9 Digital Filter

Figures 11-22 show the performance of the digital filter included in the CS5361. All plots are normalized to F_s . Assuming a sample rate of 48 kHz, the 0.5 frequency point on the plot refers to 24 kHz. The filter frequency response scales precisely with F_s .

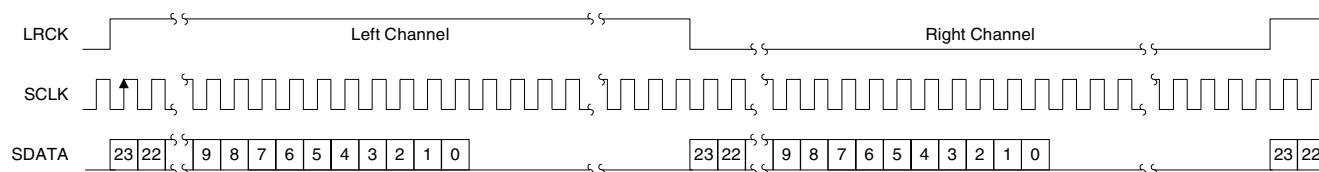
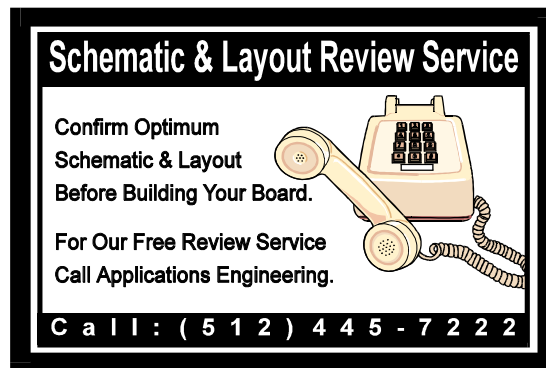


Figure 8. Left Justified Format, DIF Low

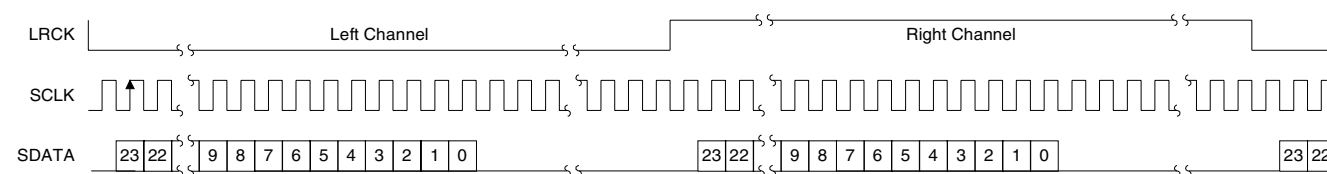
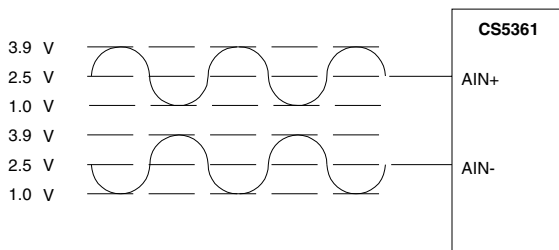
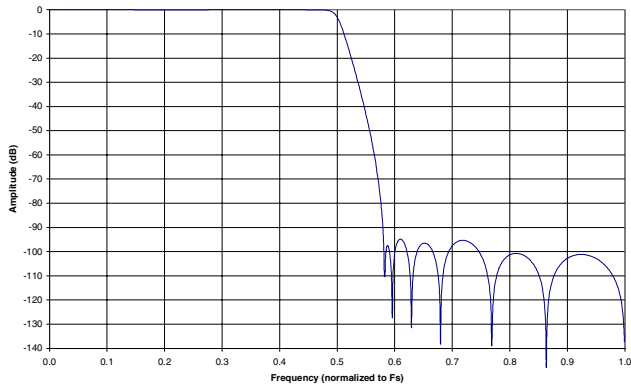
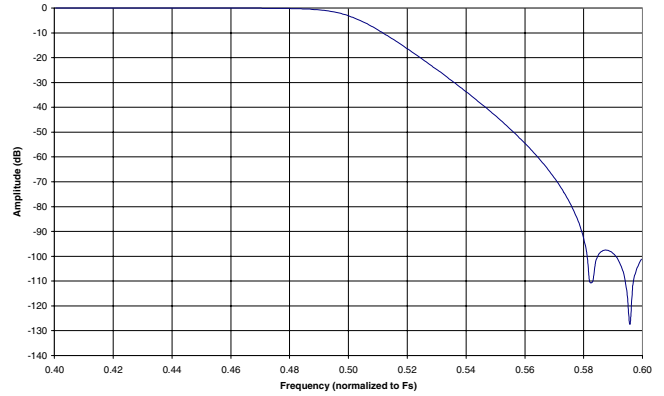
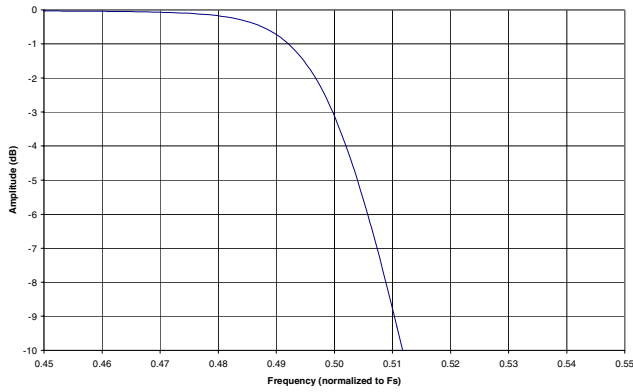
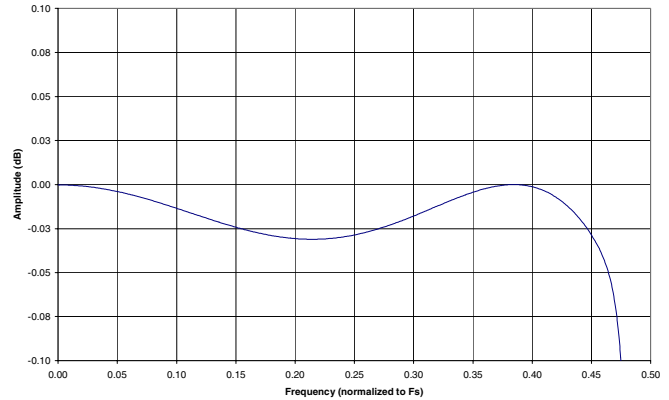
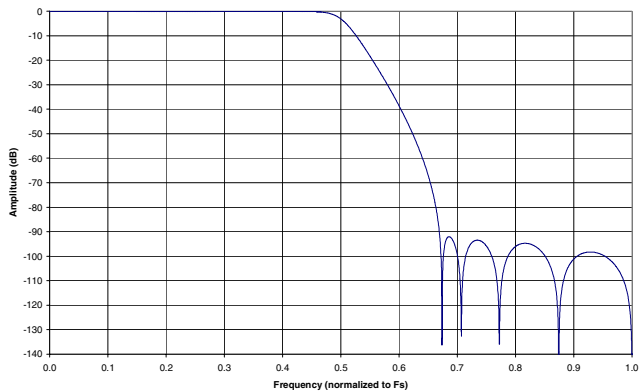
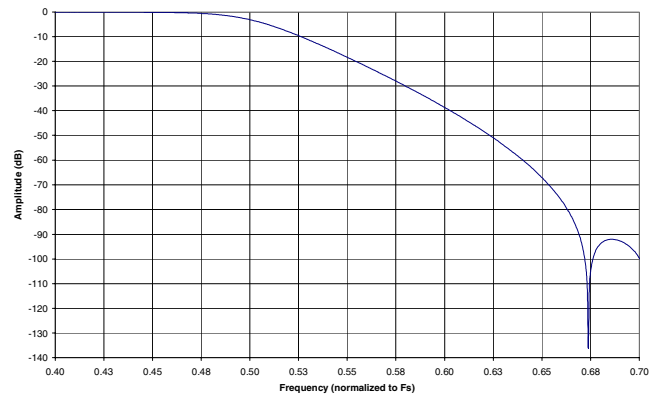


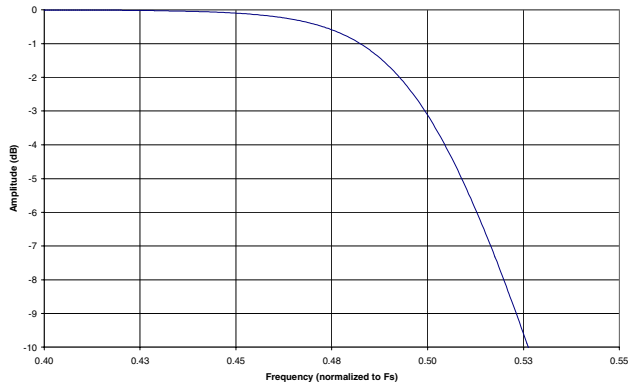
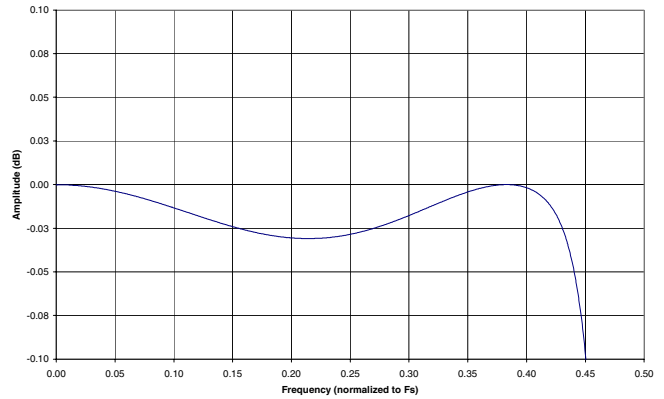
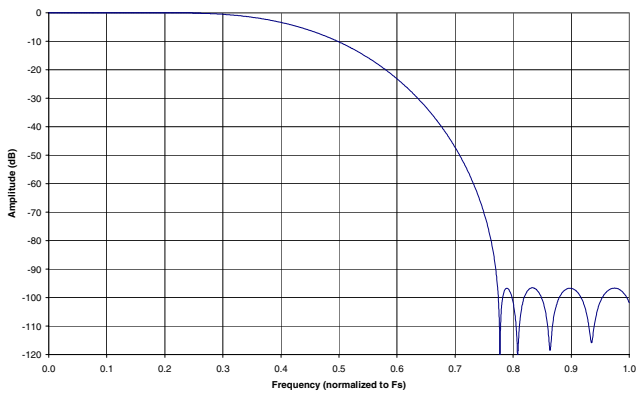
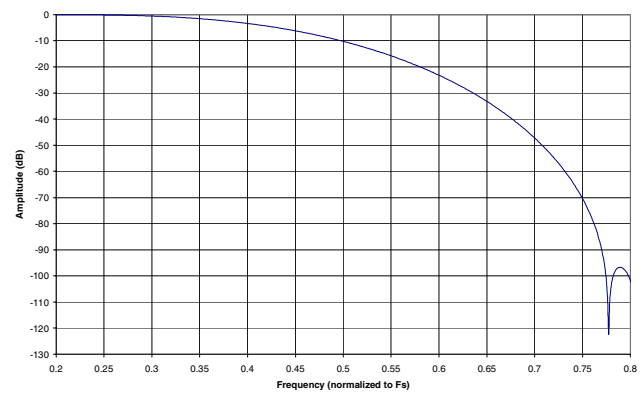
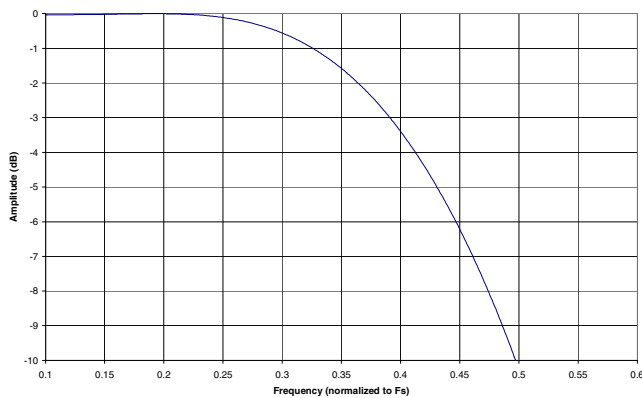
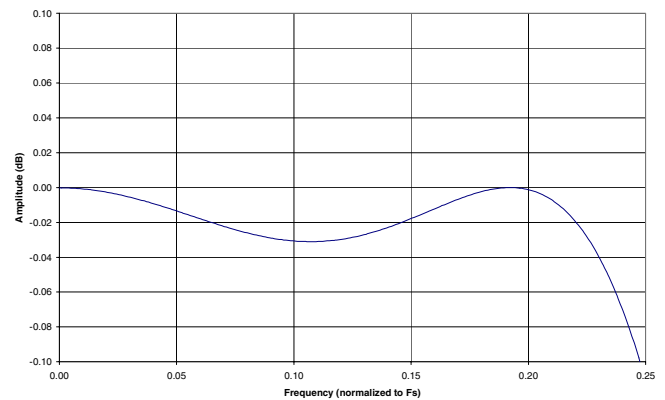
Figure 9. I²S Format, DIF High



$$\text{Full Scale Input level} = (\text{AIN}+) - (\text{AIN}-) = 5.6 \text{ Vpp}$$

Figure 10. Full Scale Input Voltage


Figure 11. Single Speed Mode Stopband Rejection

Figure 12. Single Speed Mode Transition Band

Figure 13. Single Speed Mode Transition Band (Detail)

Figure 14. Single Speed Mode Passband Ripple

Figure 15. Double Speed Mode Stopband Rejection

Figure 16. Double Speed Mode Transition Band


Figure 17. Double Speed Mode Transition Band (Detail)

Figure 18. Double Speed Mode Passband Ripple

Figure 19. Quad Speed Mode Stopband Rejection

Figure 20. Quad Speed Mode Transition Band

Figure 21. Quad Speed Mode Transition Band (Detail)

Figure 22. Quad Speed Mode Passband Ripple

5 PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

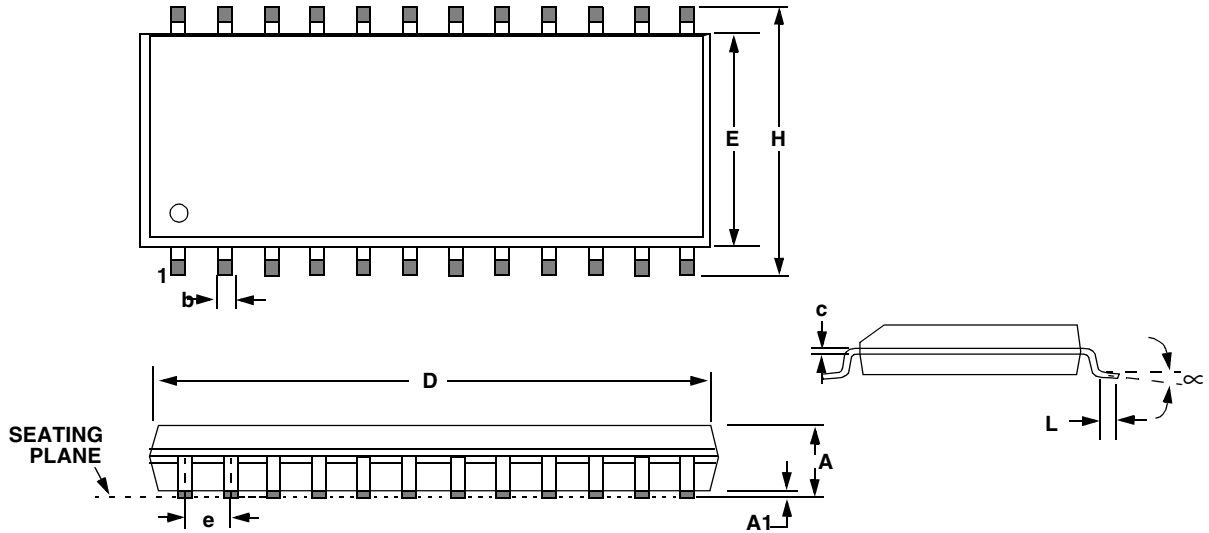
The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

6 REFERENCES

- 1) "Techniques to Measure and Maximize the Performance of a 120 dB, 96 kHz A/D Converter Integrated Circuit" by Steven Harris, Steven Green and Ka Leung. Presented at the 103rd Convention of the Audio Engineering Society, September 1997.
- 2) "A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio" by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.
- 3) "The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's" by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.
- 4) "An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example" by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.
- 5) "How to Achieve Optimum Performance from Delta-Sigma A/D and D/A Converters" by Steven Harris. Presented at the 93rd Convention of the Audio Engineering Society, October 1992.

7 PACKAGE DIMENSIONS
24L SOIC (300 MIL BODY) PACKAGE DRAWING


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.598	0.614	15.20	15.60
E	0.291	0.299	7.40	7.60
e	0.040	0.060	1.02	1.52
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
∞	0°	8°	0°	8°

• **Notes** •

SMART
Analog™