Ordering number : EN 3270B

CMOS LSI

SANYO

No.3270B

LC7480, 7480M

Video A/D Converter with 3-Input Multiplexer

Overview

The LC7480 is a video 6-bit flash type A/D converter implemented in CMOS process technology. It has an internal clamp voltage generation circuit for video component signals (Y, R-Y, and B-Y) and a multiplexer.

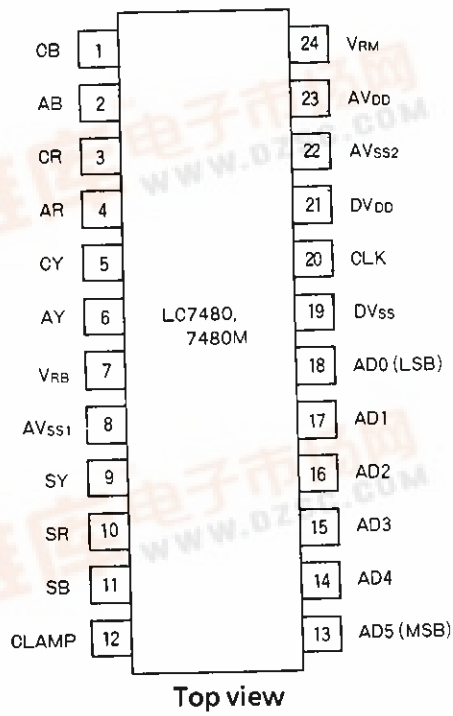
Functions

- Clamp voltage generation circuit (CY, CR, and CB)
- Three-input multiplexer
- Reference voltage source

Features

· Resolution	6 bits
· Nonlinearity error	±1/2 LSB
· Maximum conversion rate	20MSPS
· Analog input voltage range	1Vpp
· Digital input/output voltage	CMOS level
· Single power source	5±0.5V
· Power dissipation	135mW (typ)
· Package	DIP24S(LC7480)
	MFP24S(LC7480M)

Pin Assignment

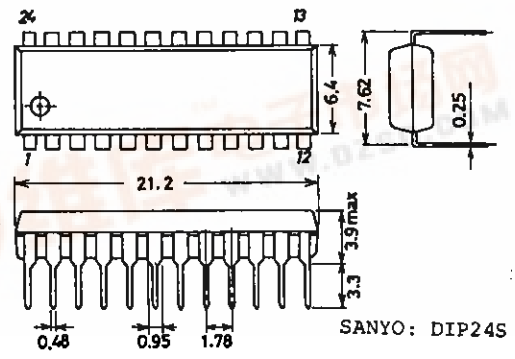


Top view

Package Dimensions

(unit :mm)

3067 [LC7480]

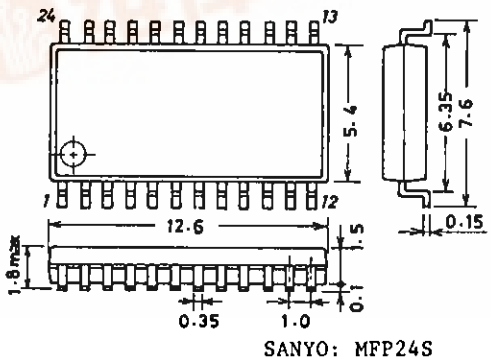


SANYO: DIP24S

Package Dimensions

(unit :mm)

3112 [LC7480M]



SANYO: MFP24S

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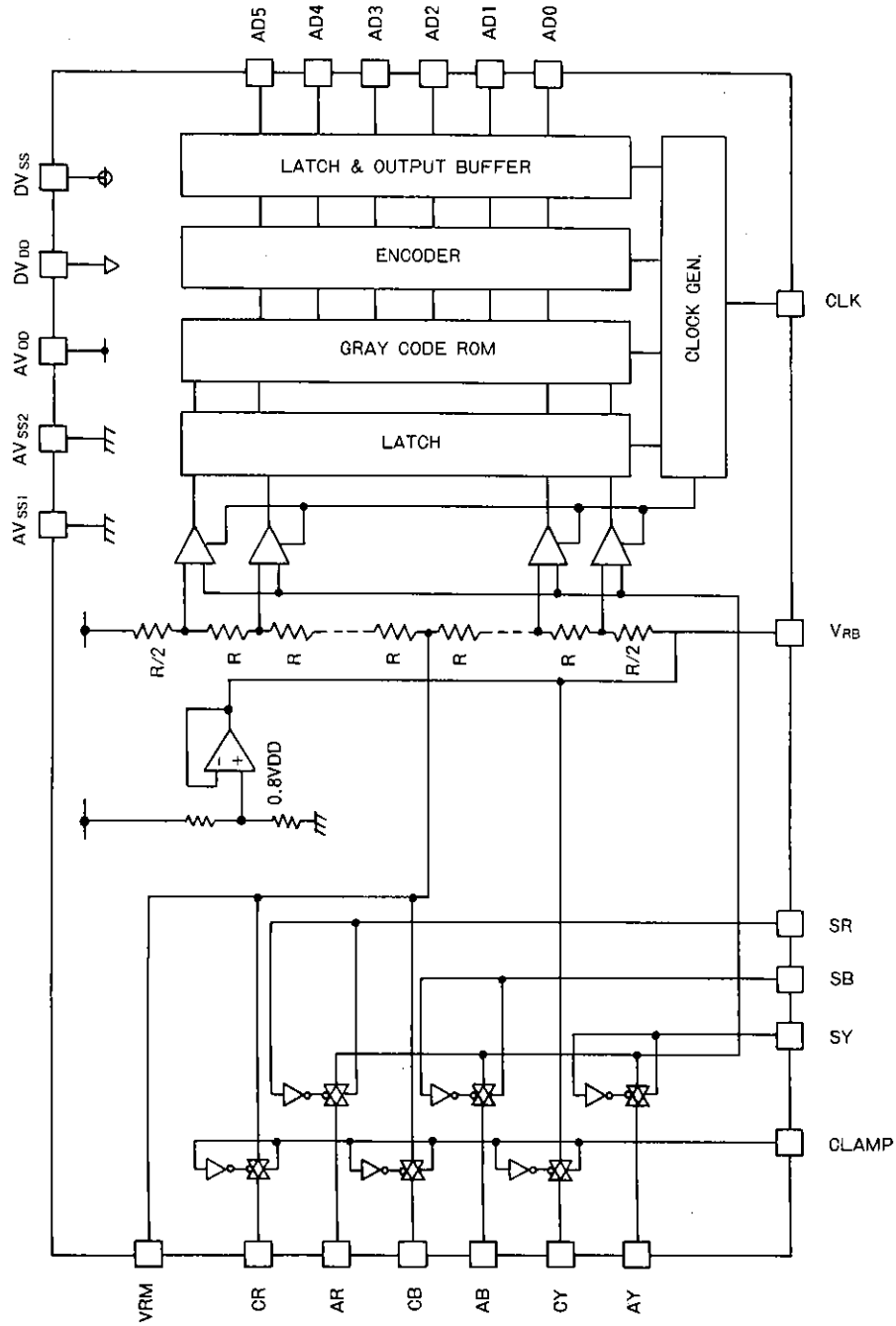
Block Diagram



Pin Functions

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	CB	Clamp voltage output for B-Y signal	13	AD5	Digital output [MSB]
2	AB	B-Y signal input	14	AD4	Digital output
3	CR	Clamp voltage output for R-Y signal	15	AD3	Digital output
4	AR	R-Y signal input	16	AD2	Digital output
5	CY	Clamp voltage output for Y signal	17	AD1	Digital output
6	AY	Y signal input	18	AD0	Digital output [LSB]
7	V_{RB}	Reference voltage (B)	19	DV_{SS}	Digital GND
8	$AV_{SS}1$	Analog GND	20	CLK	Clock input
9	SY	Multiplexer SW (for Y signal)	21	DV_{DD}	Digital power supply
10	SR	Multiplexer SW (for R-Y signal)	22	$AV_{SS}2$	Analog GND
11	SB	Multiplexer SW (for B-Y signal)	23	AV_{DD}	Analog power supply
12	CLAMP	Clamp SW	24	V_{RM}	Reference voltage (M)

Absolute Maximum Ratings at Ta = 25 ± 2°C, V_{SS} (= DV_{SS}, $AV_{SS}1$, $AV_{SS}2$) = 0V

				unit	Applicable pins
Supply Voltage	V_{DD} ($=AV_{DD}, DV_{DD}$)		−0.3 to +7.0	V	AV_{DD}, DV_{DD}
I/O Pin Voltage	V_{IN}, V_{OUT}		−0.3 to V_{DD} + 0.3	V	I/O pins
Analog Reference Voltage	V_{RM}, V_{RB}		−0.3 to V_{DD} + 0.3	V	V_{RM}, V_{RB}
Allowable Power Dissipation	Pd max	Ta ≦ 70°C	300	mW	
Operating Temperature	Topr		−30 to +70	°C	
Storage Temperature	Tstg		−55 to +125	°C	

(Note) The LSI should be used on the condition that $AV_{DD} = DV_{DD}$ and $AV_{SS1} = AV_{SS2} = DV_{SS}$.

Allowable Operating Conditions at Ta = −30 to +70°C, V_{SS} = 0V

		min	typ	max	unit	Applicable pins
Supply Voltage	V_{DD}	4.5	5.0	5.5	V	AV_{DD}, DV_{DD}
Analog Input Voltage	V_{INA}		$V_{DD} - V_{RB}$		Vpp	AY, AR, AB
Digital Input Voltage	V_{IHD}	0.7V_{DD}			V	CLK, SY, SR,
	V_{ILD}			0.3V_{DD}	V	SB, CLAMP
Sampling Clock	f_{CLK}	1.0		20.0	MHz	CLK
Sampling Clock Pulse Width	t_{CLKH} (H level)	25.0			ns	CLK
	t_{CLKL} (L level)	25.0			ns	CLK
Clamp Pulse Width	t_{CLPH} (H level)	2.0			μs	CLAMP
MPX Set up	t_{MSU}	25.0			ns	SY, SR, SB
MPX Hold	t_{MHD}	0.0			ns	SY, SR, SB
MPX Off	t_{MOFF}	0.0			ns	SY, SR, SB

Electrical Characteristics at Ta = 25 ± 2°C, V_{DD} = 5V ± 10%, V_{SS} = 0V

			min	typ	max	unit	Applicable pins
Power Dissipation (Analog)	$I_{DD}A$	V_{DD} = 5V,		20.0		mA	AV_{DD}
Power Dissipation (Digital)	$I_{DD}D$	f_{CLK} = 14.3MHz, input signal = 3.58MHz (sine wave)		7.0		mA	DV_{DD}
Resolution					6.0	bit	
Linearity Error	SINL				±1/2	LSB	
Differential Linearity Error	SDNL				±1/2	LSB	
Reference Voltage (M)	V_{RM}			0.9V_{DD}		V	V_{RM}
Reference Voltage (B)	V_{RB}			0.8V_{DD}		V	V_{RB}
Digital Output Voltage	V_{OH}	Io = −1.6mA	V_{DD} − 0.4			V	AD0 to AD5
	V_{OL}	Io = +1.6mA			0.4	V	

Switching Characteristics at Ta = 25 ± 2°C, V_{DD} = 5V ± 10%, V_{SS} = 0V

			min	typ	max	unit	Applicable pins
Digital Output Delay Time	t_{Pd}	Load capacitance : 50pF			40.0	ns	

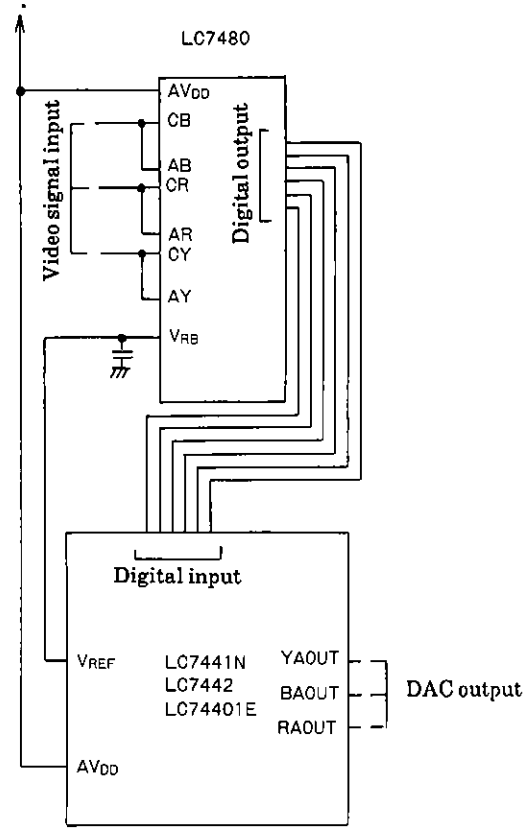
Output Code Example

STEP	Analog Input Voltage (V)		Digital I/O Code	AOUT (V)
0	3.992	4.000	000000	3.992
1	4.000	4.016	000001	4.008
2	4.016	4.032	000010	4.024
31	4.480	4.496	011111	4.488
32	4.496	4.512	100000	4.504
33	4.512	4.528	100001	4.520
61	4.960	4.976	111101	4.968
62	4.976	4.992	111110	4.984
63	4.992	5.000	111111	5.000

V_{DD}=5.000V, V_{RB}=V_{REF}=3.992V

1LSB=16mV

Application Circuit



Timing Chart