HYUNDAI

# HY5DU28822

## 4 Banks x 4M x 8Bit Double Data Rate SDRAM

***PRELIMINARY***

## DESCRIPTION

The Hyundai HY5DU28822 is a 134,217,728-bit CMOS Double Data Rate(DDR) Synchronous DRAM, ideally suited for the main memory applications which require large memory density and high bandwidth. HY5DU28822 is organized as 4 banks of 4,194,304x8.

HY5DU28822 offers fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the clock(falling edges of the CLK), Data(DQ), Data strobes(DQS) and Write data masks(DM) inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL_2.

Mode Register set options include the length of pipeline ($\overline{\text{CAS}}$ latency of 2 / 2.5), the number of consecutive read or write cycles initiated by a single control command (Burst length of 2 / 4 / 8), the burst count sequence(sequential or interleave), DQ FET Control (/QFC) and Output Driver types (Full / Half Strength Driver). Because data rate is doubled through reading and writing at both rising and falling edges of the clock, 2X higher data bandwidth can be achieved than that of traditional (single data rate) Synchronous DRAM.

## FEATURES

- 2.5V $V_{DD}$ and $V_{DDQ}$ power suppliy
- All inputs and outputs are compatible with SSTL_2 interface
- JEDEC standard 400mil 66pin TSOP-II with 0.65mm pin pitch
- Fully differential clock operations(CLK & $\overline{\text{CLK}}$) with 100MHz/125MHz/133MHz
- All addresses and control inputs except Data, Data strobes and Data masks latched on the rising edges of the clock
- Data(DQ) and Write masks(DM) latched on both rising and falling edges of the Data Stobe
- Data outputs on DQS edges when read (edged DQ) Data inputs on DQS centers when write (centered DQ)
- Delay Locked Loop(DLL) installed with DLL reset mode
- Write mask byte controlled by DM
- Programmable $\overline{\text{CAS}}$ Latency 2 and 2.5 supported
- Write Operations with 1 Clock Write Latency
- /QFC & Half Strength Driver controlled by EMRS
- Programmable Burst Length 2 / 4 / 8 with both sequential and interleave mode
- Internal four bank operations with single pulsed $\overline{\text{RAS}}$
- Auto refresh and self refresh supported
- 4096 refresh cycles / 64ms

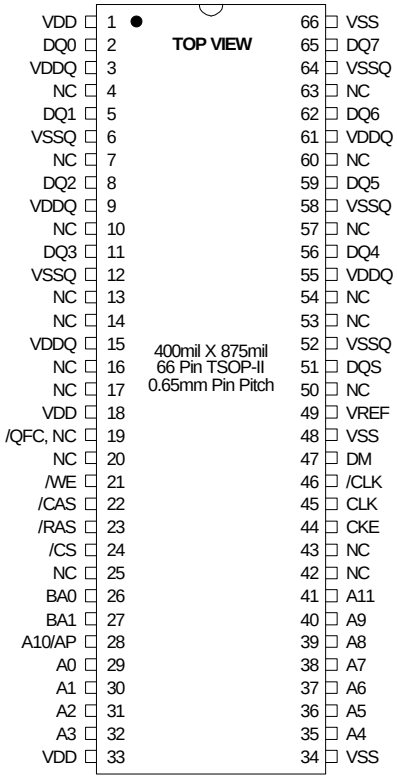
## ORDERING INFORMATION

| Part No. | Power Suppy | Clock Frequency | Organization | Interface | Package |
|---|---|---|---|---|---|
| HY5DU28822(L)T-K | $V_{DD}$=2.5V<br>$V_{DDQ}$=2.5V | 143MHz (*PC266A) | 4Banks<br>x 4Mbit x 8 | SSTL_2 | 400mil 66pin<br>TSOP II |
| HY5DU28822(L)T-H | | 133MHz (*PC266B) | | | |
| HY5DU28822(L)T-L | | 125MHz (*PC200) | | | |

* *(L) Low Power Part*

* *JEDEC Defined Specifications compliant*

## PIN CONFIGURATION

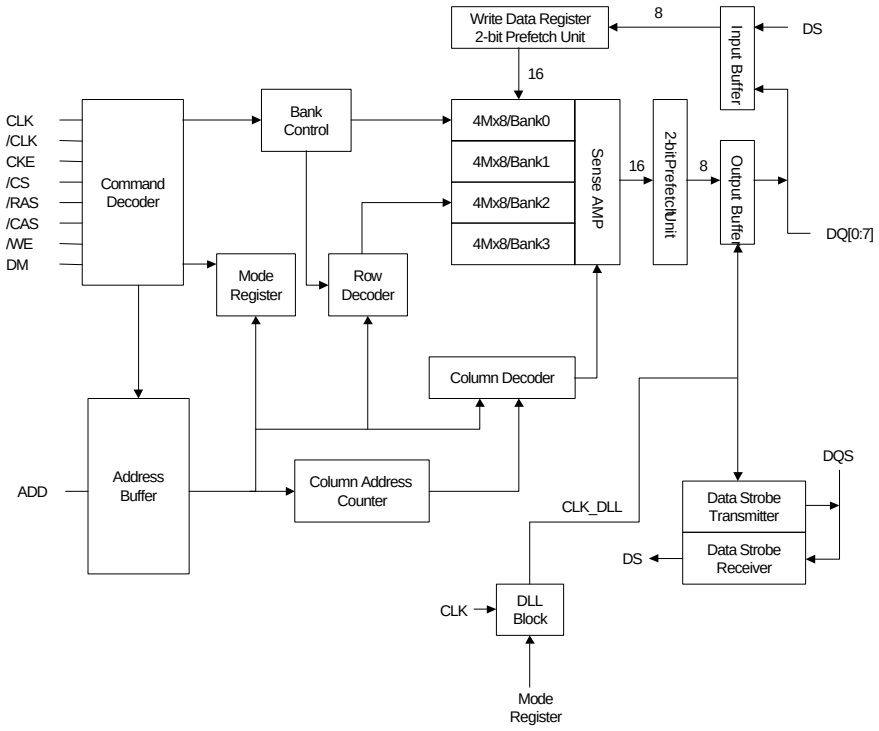



## PIN DESCRIPTION

| PIN | PIN NAME | DESCRIPTION |
|---|---|---|
| CLK, $\overline{CLK}$ | Differential Clock Input | The system clock input. All of the inputs are latched on the rising edges of the clock except DQi, DQS and DM that are sampled on the both. |
| CKE | Clock Enable | Controls internal clock signal and when deactivated, the DDR SDRAM will be one of the states among power down, suspend or self refresh. |
| $\overline{CS}$ | Chip Select | Enables or disables all inputs except CLK/$\overline{CLK}$, CKE, DQS and DM. |
| BA0, BA1 | Bank Select Address | Selects bank to be activated during either $\overline{RAS}$ or $\overline{CAS}$ activity.<br>Selects bank to be read/written during either $\overline{RAS}$ or $\overline{CAS}$ activity. |
| A0 ~ A11 | Address | Row Address : A0 ~ A11, Column Address : A0 ~ A9, AP Flag : A10 |
| $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | Row Address Strobe,<br>Column Address Strobe,<br>Write Enable | $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operations.<br>Refer function truth table for details. |
| DM | Write Mask | Masks input data in write mode. |
| DQS | Data Input/Output Strobe | Active on the both edges for Data Input and Output. |
| DQ0 ~ DQ7 | Data Input/Output | Multiplexed data input / output pin. |
| $V_{DD}/V_{SS}$ | Power Supply/Ground | Power supply for internal circuits and input buffers. |
| $V_{DDQ}/V_{SSQ}$ | Data Output Power/Ground | Power supply for output buffers for Noise immunity. |
| $V_{REF}$ | Reference Voltage | Reference voltage for inputs for SSTL interface. |
| /QFC (optional) | DQ FET Switch Control | Controls FET Switches on DQs used for reduction of Impedance. |
| NC | No Connection | No connection. |

## FUNCTIONAL BLOCK DIAGRAM

4banks x 4Mbit x 8 I/O Double data rate Synchronous DRAM




## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Ambient Temperature | $T_A$ | 0 ~ 70 | $^oC$ |
| Storage Temperature | $T_{STG}$ | -55 ~ 125 | $^oC$ |
| Voltage on Any Pin relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | -0.5 ~ 3.6 | V |
| Voltage on $V_{DD}$ relative to $V_{SS}$ | $V_{DD}$ | -0.5 ~ 3.6 | V |
| Voltage on $V_{DDQ}$ relative to $V_{SS}$ | $V_{DDQ}$ | -0.5 ~ 3.6 | V |
| Output Short Circuit Current | $I_{OS}$ | 50 | mA |
| Power Dissipation | $P_D$ | 1 | W |
| Soldering Temperature · Time | $T_{SOLDER}$ | 260 · 10 | $^oC$ · Sec |

**Note :** Operation at above absolute maximum rating can adversely affect device reliability.

## DC OPERATING CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

| Parameter | Symbol | Min | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Power Supply Voltage | VDD | 2.3 | 2.5 | 2.7 | V | |
| Power Supply Voltage | VDDQ | 2.3 | 2.5 | 2.7 | V | 1 |
| Input High Voltage | VIH | VREF + 0.15 | - | VDDQ + 0.3 | V | |
| Input Low Voltage | VIL | -0.3 | - | VREF - 0.15 | V | 2 |
| Termination Voltage | VTT | VREF - 0.04 | VREF | VREF + 0.04 | V | |
| Reference Voltage | VREF | 1.15 | 1.25 | 1.35 | V | 3 |

**Note :**
1. VDDQ must not exceed the level of VDD.
2. VIL (min) is acceptable -1.5V AC pulse width with ≤ 5ns of duration.
3. The value of VREF is approximately equal to 0.5VDDQ.

## AC OPERATING CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Input High (Logic 1) Voltage, DQ, DQS and DM signals | VIH(AC) | VREF + 0.31 | | V | |
| Input Low (Logic 0) Voltage, DQ, DQS and DM signals | VIL(AC) | | VREF - 0.31 | V | |
| Input Differential Voltage, CK and /CK inputs | VID(AC) | 0.7 | VDDQ + 0.6 | V | 1 |
| Input Crossing Point Voltage, CK and /CK inputs | VIX(AC) | 0.5*VDDQ-0.2 | 0.5*VDDQ+0.2 | V | 2 |

**Note :**
1. VID is the magnitude of the difference between the input level on CK and the input on CK.
2. The value of VIX is expected to equal 0.5*V DDQ of the transmitting device and must track variations in the DC level of the same.

## AC OPERATING TEST CONDITIONS (TA=0 to 70°C, Voltage referenced to VSS = 0V)

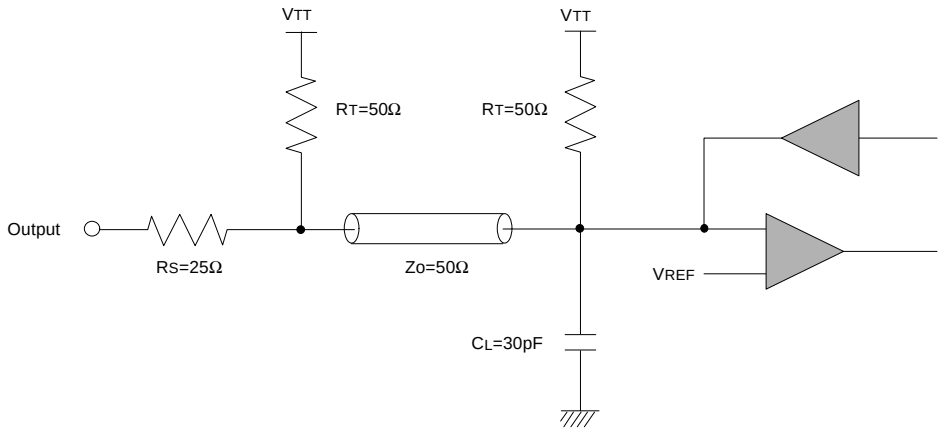
| Parameter | Value | Unit |
|---|---|---|
| Reference Voltage | VDDQ x 0.5 | V |
| Termination Voltage | VDDQ x 0.5 | V |
| AC Input High Level Voltage (VIH, min) | VREF + 0.31 | V |
| AC Input Low Level Voltage (VIL, max) | VREF - 0.31 | V |
| Input Timing Measurement Reference Level Voltage | VREF | V |
| Output Timing Measurement Reference Level Voltage | VTT | V |
| Input Signal maximum peak swing | 1.5 | V |
| Input minimum Signal Slew Rate | 1 | V/ns |
| Termination Resistor (RT) | 50 | Ω |
| Series Resistor (RS) | 25 | Ω |
| Output Load Capacitance for Access Time Measurement (CL) | 30 | pF |

## CAPACITANCE ($T_A$=25°C, f=100MHz )

| Parameter | Pin | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Input Capacitance | A0 ~ A11, BA0 ~ BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | $C_{IN}$ | 2.0 | 3.0 | pF |
| Clock Capacitance | CLK, $\overline{CLK}$ | $C_{CLK}$ | 2.0 | 3.0 | pF |
| Data Input / Output Capacitance | DQ0 ~ DQ7, DQS, DM | $C_{IO}$ | 4.0 | 5.0 | pF |

**Note :**
1. VDD = min. to max., VDDQ = 2.3V to 2.7V, VODC = VDDQ/2, $V_{O}$peak-to-peak = 0.2V
2. Pins not under test are tied to GND.
3. These values are guaranteed by design and are tested on a sample basis only.

## OUTPUT LOAD CIRCUIT



## DC CHARACTERISTICS I (TA=0 to 70°C, Voltage referenced to $V_{SS}$ = 0V)

| Parameter | Symbol | Min. | Max | Unit | Note |
|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | -5 | 5 | uA | 1 |
| Output Leakage Current | $I_{LO}$ | -5 | 5 | uA | 2 |
| Output High Voltage | $V_{OH}$ | $V_{TT}$ + 0.76 | - | V | $I_{OH}$ = -15.2mA |
| Output Low Voltage | $V_{OL}$ | - | $V_{TT}$ - 0.76 | V | $I_{OL}$ = +15.2mA |

**Note :**
1.$V_{IN}$ = 0 to 3.6V, All other pins are not tested under $V_{IN}$ =0V
2.$D_{OUT}$ is disabled, $V_{OUT}$=0 to 2.7V

## DC CHARACTERISTICS II (TA=0 to 70°C, Voltage referenced to $V_{SS}$ = 0V)

| Parameter | Symbol | Test Condition | | Speed | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| | | | | -K | -H | -L | | |
| Operating Current | $I_{DD1}$ | Burst length=2, One bank active<br>$t_{RC} \geq t_{RC}$(min), $I_{OL}$=0mA | | 150 | 140 | 130 | mA | 1 |
| Precharge Standby Current in Power Down Mode | $I_{DD2P}$ | CKE ≤ $V_{IL}$(max), $t_{CK}$ = min | | 20 | | | mA | |
| Precharge Standby Current in Non Power Down Mode | $I_{DD2N}$ | CKE ≥ $V_{IH}$(min), $\overline{CS}$ ≥ $V_{IH}$(min), $t_{CK}$ = min<br>Input signals are changed one time during 2clks | | 40 | | | mA | |
| Active Standby Current in Power Down Mode | $I_{DD3P}$ | CKE ≤ $V_{IL}$(max), $t_{CK}$ = min | | 25 | | | mA | |
| Active Standby Current in Non Power Down Mode | $I_{DD3N}$ | CKE ≥ $V_{IH}$(min), $\overline{CS}$ ≥ $V_{IH}$(min), $t_{CK}$ = min<br>Input signals are changed one time during 2clks | | 50 | | | mA | |
| Burst Mode Operating Current | $I_{DD4}$ | $t_{CK} \geq t_{CK}$(min), $I_{OL}$=0mA<br>All banks active | CL=2.5 | 270 | 260 | 250 | mA | 1 |
| | | | CL=2 | 230 | 210 | 190 | | |
| Auto Refresh Current | $I_{DD5}$ | $t_{RC} \geq t_{RFC}$(min), All banks active | | 320 | | | mA | 2 |
| Self Refresh Current | $I_{DD6}$ | CKE ≤ 0.2V | | 2 | | | mA | 3 |
| | | | | TBD | | | mA | 4 |

**Note :**
1. $I_{DD1}$, $I_{DD4}$ and $I_{DD5}$ depend on output loading and cycle rates. Specified values are measured with the output open.
2. Min. of $t_{RFC}$ (Auto Refresh Row Cycle Time) is shown at AC Characteristics.
3. HY5DU28822T
4. HY5DU28822LT, Self refresh low power

## AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

| Parameter | | Symbol | -K(PC266A) | | -H(PC266B) | | -L(PC200) | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | | |
| Row Cycle Time | | tRC | 65 | - | 65 | - | 70 | - | ns | |
| Auto Refresh Row Cycle Time | | tRFC | 75 | - | 75 | - | 80 | - | ns | |
| Row Active Time | | tRAS | 45 | 120K | 48 | 120K | 50 | 120K | ns | |
| Row Address to Column Address Delay | | tRCD | 20 | - | 20 | - | 20 | - | ns | |
| Row Active to Row Active Delay | | tRRD | 15 | - | 15 | - | 15 | - | ns | |
| Column Address to Column Address Delay | | tCCD | 1 | - | 1 | - | 1 | - | CLK | |
| Row Precharge Time | | tRP | 20 | - | 20 | - | 20 | - | ns | |
| Write Recovery Time | | tWR | 15 | - | 15 | - | 15 | - | ns | |
| Last Data-In to Read Command | | tDRL | 1 | - | 1 | - | 1 | - | CLK | |
| Auto Precharge Write Recovery + Precharge Time | | tDAL | 35 | - | 35 | - | 35 | - | ns | |
| System Clock Cycle Time | $\overline{CAS}$ Latency = 2.5 | tCK | 7 | 15 | 7.5 | 15 | 8 | 15 | ns | |
| | $\overline{CAS}$ Latency = 2 | | 7.5 | 15 | 10 | 15 | 10 | 15 | ns | |
| Clock High Level Width | | tCH | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | CLK | |
| Clock Low Level Width | | tCL | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | CLK | |
| Data-Out edge to Clock edge Skew | | tAC | -0.75 | 0.75 | -0.75 | 0.75 | -0.8 | 0.8 | ns | |
| DQS-Out edge to Clock edge Skew | | tDQSCK | -0.75 | 0.75 | -0.75 | 0.75 | -0.8 | 0.8 | ns | |
| DQS-Out edge to Data-Out edge Skew | | tDQSQ | - | 0.5 | - | 0.5 | - | 0.6 | ns | |
| Data-Out hold time from DQS | | tQH | tHPmin -0.75ns | - | tHPmin -0.75ns | - | tHPmin -0.75ns | - | ns | 1 |
| Clock Half Period | | tHP | tCH/L min | - | tCH/L min | - | tCH/L min | - | ns | 1 |
| Input Setup Time (fast slew rate) | | tIS | 0.9 | - | 0.9 | - | 1.0 | - | ns | 2,3,5,6 |
| Input Hold Time (fast slew rate) | | tIH | 0.9 | - | 0.9 | - | 1.0 | - | ns | 2,3,5,6 |
| Input Setup Time (slow slew rate) | | tIS | 1.1 | - | 1.1 | - | 1.1 | - | ns | 2,4,5,6 |
| Input Hold Time (slow slew rate) | | tIH | 1.1 | - | 1.1 | - | 1.1 | - | ns | 2,4,5,6 |
| Input Pulse Width | | tIPW | 2.2 | | 2.2 | | - | | | 6 |
| Write DQS High Level Width | | tDQSH | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | CLK | |
| Write DQS Low Level Width | | tDQSL | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | CLK | |
| CLK to First Rising edge of DQS-In | | tDQSS | 0.75 | 1.25 | 0.75 | 1.25 | 0.75 | 1.25 | CLK | |
| Data-In Setup Time to DQS-In (DQ & DM) | | tDS | 0.5 | - | 0.5 | - | 0.6 | - | ns | 7 |
| Data-in Hold Time to DQS-In (DQ & DM) | | tDH | 0.5 | - | 0.5 | - | 0.6 | - | ns | 7 |

## AC CHARACTERISTICS (AC operating conditions unless otherwise noted) *- continued -*

| Parameter | Symbol | -K(PC266A) | | -H(PC266B) | | -L(PC200) | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| DQ & DM Input Pulse Width | tDIPW | 1.75 | - | 1.75 | - | 2 | - | ns | |
| Read DQS Preamble Time | tRPRE | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | CLK | |
| Read DQS Postamble Time | tRPST | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | CLK | |
| Write DQS Preamble Setup Time | tWPRES | 0 | - | 0- | - | 0 | - | CLK | |
| Write DQS Preamble Hold Time | tWPREH | 0.25 | - | 0.25 | - | 0.25 | - | CLK | |
| Write DQS Postamble Time | tWPST | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | CLK | |
| Mode Register Set Delay | tMRD | 2 | - | 2 | - | 2 | - | CLK | |
| Power Down Exit Time | tPDEX | 10 | - | 10 | - | 10 | - | ns | |
| Exit Self Refresh to Non-Read Command | tXSNR | 75 | - | 75 | - | 80 | - | ns | |
| Exit Self Refresh to Read Cimmand | tXSRD | 200 | - | 200 | - | 200 | - | CLK | 8 |
| Average Periodic Refresh Interval | tREFI | - | 15.6 | - | 15.6 | - | 15.6 | us | |

**Note :**
1. This calculation accounts for tDQSQ(max), the pulse width distortion of on-chip circuit and jitter.
2. Data sampled at the rising edges of the clock : A0~A11, BA0~BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$.
3. For command/address input slew rate >=1.0V/ns
4. For command/address input slew rate >=0.5V/ns and <1.0V/ns
5. CK, /CK slew rates are >=1.0V/ns
6. These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester correlation.
7. Data latched at both rising and falling edges of Data Strobes(DQS) : DQ, DM
8. Minimum of 200 cycles of stable input clocks after Self Refresh Exit command, where CKE is held high, is required to complete Self Refresh Exit and lock the internal DLL circuit of DDR SDRAM.

## WRITE MASK TRUTH TABLE

| Function | CKEn-1 | CKEn | $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | DM | ADDR | A10/ AP | BA | Note |
|---|---|---|---|---|---|---|---|---|
| Data Write | H | X | X | L | X | | | 1 |
| Data-In Mask | H | X | X | H | X | | | 1 |

**Note :**
1. Write Mask command masks burst write data with reference to DQS(Data Strobes) and it is not related with read data.

## SIMPLIFIED COMMAND TRUTH TABLE

| Command | | CKEn-1 | CKEn | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | ADDR | A10/AP | BA | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Extended Mode Register Set | | H | X | L | L | L | L | OP code | | | 1,2 |
| Mode Register Set | | H | X | L | L | L | L | OP code | | | 1,2 |
| Device Deselect | | H | X | H | X | X | X | X | | | 1 |
| No Operation | | | | L | H | H | H | | | | |
| Bank Active | | H | X | L | L | H | H | RA | | V | 1 |
| Read | | H | X | L | H | L | H | CA | L | V | 1 |
| Read with Autoprecharge | | | | | | | | | H | | 1,3 |
| Write | | H | X | L | H | L | L | CA | L | V | 1 |
| Write with Autoprecharge | | | | | | | | | H | | 1,4 |
| Precharge All Banks | | H | X | L | L | H | L | X | H | X | 1,5 |
| Precharge selected Bank | | | | | | | | | L | V | 1 |
| Read Burst Stop | | H | X | L | H | H | L | X | | | 1 |
| Auto Refresh | | H | H | L | L | L | H | X | | | 1 |
| Self Refresh | Entry | H | L | L | L | L | H | X | | | 1 |
| | Exit | L | H | H | X | X | X | | | | 1 |
| | | | | L | H | H | H | | | | |
| Precharge Power Down Mode | Entry | H | L | H | X | X | X | X | | | 1 |
| | | | | L | H | H | H | | | | 1 |
| | Exit | L | H | H | X | X | X | | | | 1 |
| | | | | L | H | H | H | | | | 1 |
| Active Power Down Mode | Entry | H | L | H | X | X | X | X | | | 1 |
| | | | | L | V | V | V | | | | 1 |
| | Exit | L | H | X | | | | | | | 1 |

( H=Logic High Level, L=Logic Low Level, X=Dont Care, V=Valid Data Input, OP Code=Operand Code, NOP=No Operation )

**Note :**

1. DM states are "Dont Care". Refer to below Write Mask Truth Table.
2. OP Code(Operand Code) consists of $A_0$~$A_{11}$ and $BA_0$~$BA_1$ used for Mode Registering duing Extended MRS or MRS. Before entering Mode Register Set mode, all banks must be in a precharge state and MRS command can be issued after tRP period from Prechagre command.
3. If a Read with Autoprecharge command is detected by memory component in CLK(n), then there will be no command presented to activated bank until CLK(n+BL/2+$t_{RP}$).
4. If a Write with Autoprecharge command is detected by memory component in CLK(n), then there will be no command presented to activated bank until CLK(n+BL/2+1+$t_{DPL}$+$t_{RP}$). Last Data-In to Prechage delay($t_{DPL}$) which is also called Write Recovery Time (tWR) is needed to guarantee that the last data has been completely written.
5. If $A_{10}$/AP is "High" when Row Precharge command being issued, $BA_0$/$BA_1$ are ignored and all banks are selected to be precharged.

## PACKAGE INFORMATION

### 400mil 66pin Thin Small Outline Package