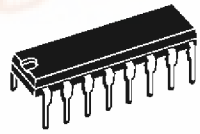
SGS-THOMSON MICROELECTRONICS

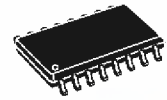
TDA7479

SINGLE CHIP RDS DEMODULATOR + FILTER

- VERY HIGH RDS DEMODULATION QUALITY WITH IMPROVED DIGITAL SIGNAL PROCESSING
- HIGH PERFORMANCE, 57KHz BANDPASS FILTER (8th ORDER)
- FILTER ADJUSTMENT FREE AND WITHOUT EXTERNAL COMPONENTS
- PURELY DIGITAL RDS DEMODULATION WITHOUT EXTERNAL COMPONENTS
- ARI (SK INDICATION) AND RDS SIGNAL QUALITY OUTPUT
- 4.332MHz CRYSTAL OSCILLATOR (8.664 and 17.328MHz OPTIONAL)
- LOW NOISE CMOS TECHNOLOGY
- LOW RADIATION



DIP16



SO16

ORDERING NUMBERS:

TDA7479 TDA7479D

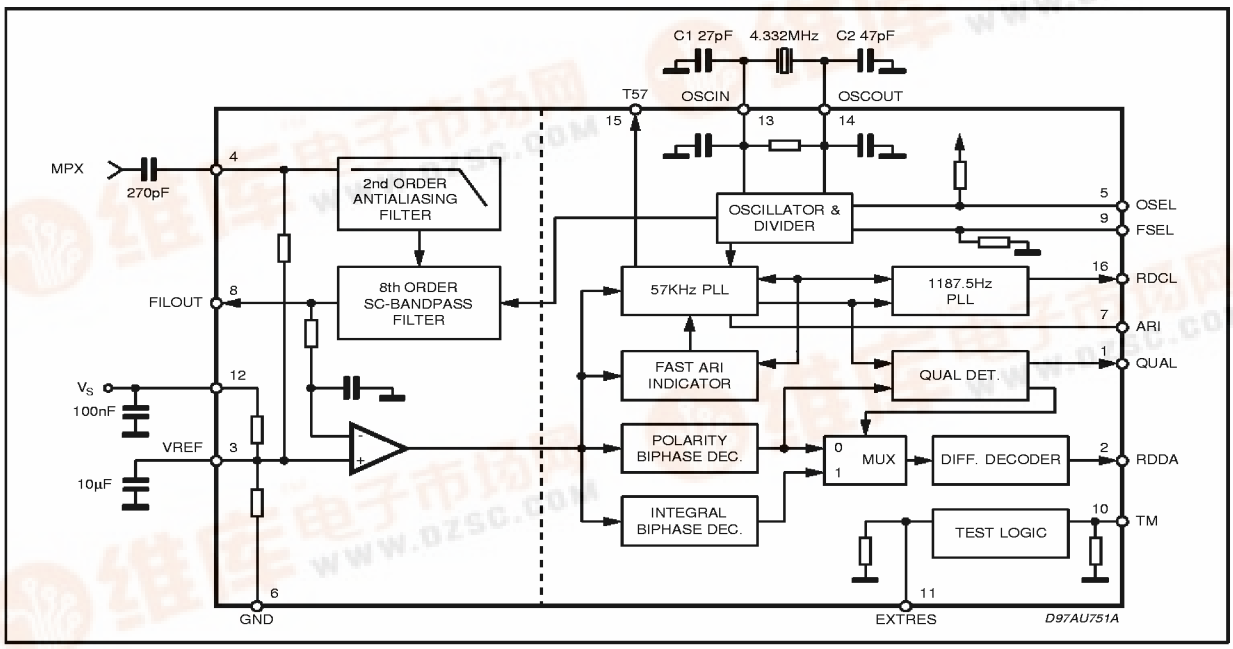
DESCRIPTION

The TDA7479 recovers the additional inaudible RDS information which is transmitted by FM radio broadcasting stations and operates in accordance with the EBU (European Broadcasting Union) specifications.

The device is made up of two sections: a cascaded antialiasing + switched capacitors bandpass filter for precise RDS band selection and a demodulating section that performs the extraction od RDS data stream (RDDA) and clock (RDCL), to be furher processed by a suitable RDS decoder.

Outputs for RDS signal quality and ARI indication are also present.

BLOCK DIAGRAM AND TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	-0.3 to 7	V
T_{op}	Operating Temperature Range	-40 to 85	°C
T_{stg}	Storage Temperature	-55 to 150	°C

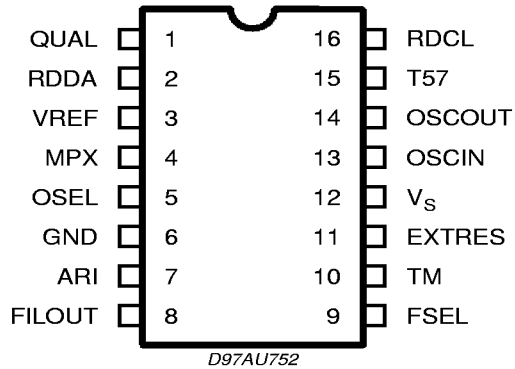
THERMAL DATA

Symbol	Description		DIP16	SO16	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	100	200	°C/W

PIN DESCRIPTION

N° pin	Name	Description
1	QUAL	Output for signal quality indication (High = good)
2	RDDA	RDS data output
3	VREF	Reference voltage
4	MPX	RDS input signal
5	OSEL	Oscillator selector pin: - open, closed to V_S = quartz oscillator - closed to GND=external driven
6	GND	Ground
7	ARI	Output for ARI indication: - high when RDS+ARI are present - high when only ARI is present
8	FILOUT	Filter output
9	FSEL	Frequency selector pin: -100K to V_S = 17.328MHz - open = 4.332MHz - closed to V_S = 8.664MHz
10	TM	Test mode pin: - open = normal RUN - closed to V_S = testmode
11	EXTRES	Reset pin: - open=run mode - closed to V_S = reset condition
12	V_S	Supply voltage
13	OSCIN	Oscillator input
14	OSCOUT	Oscillator output
15	T57	Testing output pin: 57kHz clock output
16	RDCL	RDS clock output 1187.5Hz

PIN CONNECTION (Top View)



D97AU752

THERMAL DATA

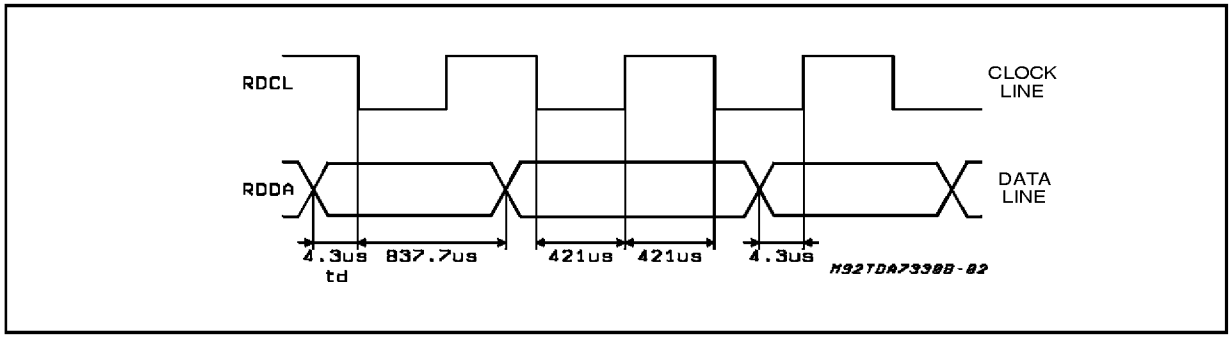
Symbol	Description		DIP20	SO20	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-Ambient	Max	100	200	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_S = 5V, unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply voltage		4.5	5	5.5	V
I_S	Supply current			7.5	11.0	mA
FILTER						
f_C	Center frequency		56.5	57	57.5	kHz
BW	3dB Bandwidth		2.5	3	3.5	kHz
G	Gain	f = 57kHz	18	20	22	dB
A	Attenuation	$\Delta f \pm 4$kHz	18	22		dB
		f = 38kHz	50	60		dB
		f = 67kHz	35	45		dB
R_I	Input impedance of MPX		80	120	150	KΩ
R_L	Load impedance on FILOUT		1			MΩ
S/N	Signal to noise ratio	V_{IN} = 3mV_{RMS}	30	40		dB
V_{IN}	MPX input signal	f = 19kHz; T3 ≤ 40dB(1) f = 57kHz (RDS+ ARI)			1000 50	mV_{RMS} mV_{RMS}
V_{REF}	Reference			V_S/2		V
DEMODULATOR						
Input pins (EXTRES, FSEL, TM) **Input pin (OSEL)**			**all with internal pull down resistor** **with internal pull up resistor**			
I_{PD}	Input Current	V_{IN} = 5V (pull-down input)	15		30	µA
I_{PU}	Input Current	V_{IN} = 0V (pull-up input)	-25		-10	µA
V_{IH}	Input voltage high		0.7 · V_S	0.8 · V_S		V
V_{IL}	Input voltage low			0.2 · V_S	0.3 · V_S	V
Output pins (RDCL, RDDA, ARI, QUAL, T57)						
V_{OH}	Ouput voltage high	I_L = 0.5mA	4	4.6		V
V_{OL}	Output voltage low	I_L = 0.5mA		0.4	1	V
OSCILLATOR						
VCLL	Input level OSCIN pin	OSEL = open circuit			1	V
VCLH	Input level OSCIN pin	OSEL = open circuit	4			V
	Amplitude OSCOUT	OSEL = open circuit		4.5		V
V_{PP}	Amplitude OSCIN (for external drive)	OSEL = GND, f = 4.332MHz		100		mVpp
		OSEL = GND, f = 8.664MHz		120		mVpp
		OSEL = GND, f = 17.328MHz		150		mVpp

(1) The 3rd harmonic (57kHz) must be less than -40dB with respect to the input signal plus gain.

Figure 1. RDS timing diagram



OUTPUT TIMING

The RDS (1187.5Hz) output clock on RDCL line is synchronized to the incoming data.
According to the internal PLL lock condition data change can result on the falling or on the rising clock edge. (see Fig. 1)
Whichever clock edge is used by the decoder (rising or falling edge) the data will remain valid for 416.7 µsec after the clock transition.

OSCILLATOR CONTROLS (FSEL, OSEL)

Three different crystal frequencies can be used. The adaption of the internal clock divider to the external crystal is achieved via the input pin FSEL. See the following table for reference:

Crystal	**FSEL** (pin configuration)
4.332MHz	connected to GND or open
8.664MHz	connected to Vs
17.328MHz	external resistor of 100K to Vs

A special mode is introduced to reduce EMI. With pin OSEL connected to GND the internal oscillator is switched off and an external sinusoidal frequency could be applied on OSCIN. The peak to peak voltage of this signal can be reduced down to 60mV.

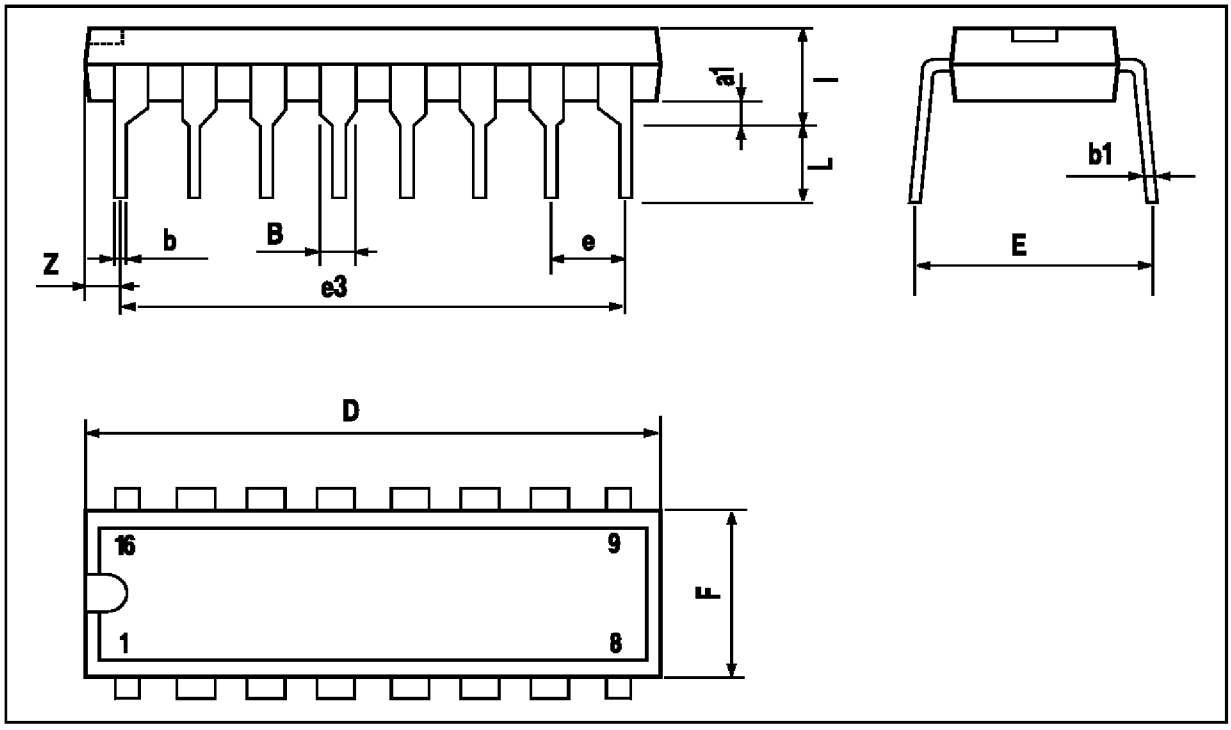
In this mode the frequency selection via FSEL is still active.

Suggested values of C1 and C2 are shown in the following table:

Crystal	C1	C2
4.332MHz	27pF	47pF
8.664MHz	27pF	-
17.328MHz	27pF	-

DIP16 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



SO16 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	10.1		10.5	0.398		0.413
E	10.0		10.65	0.394		0.419
e		1.27			0.050	
e3		8.89			0.350	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8° (max.)