



# Serial Input Voltage Output, 12/14 Bit DACs

## Preliminary Technical Data

## AD5530/AD5531

### FEATURES

- Pin Compatible 12 and 14 Bit DACs
- Serial Input, Voltage Output
- Maximum Output Voltage Range of  $\pm 10V$
- Data Readback
- 3 Wire Serial Interface
- Clear Function to a User Defined Voltage
- Power Down Function
- Serial Data Output for Daisy Chaining
- 16 Lead TSSOP Packages

### APPLICATIONS

- Industrial Automation
- Automatic Test Equipment
- Process Control
- General Purpose Instrumentation

### GENERAL DESCRIPTION

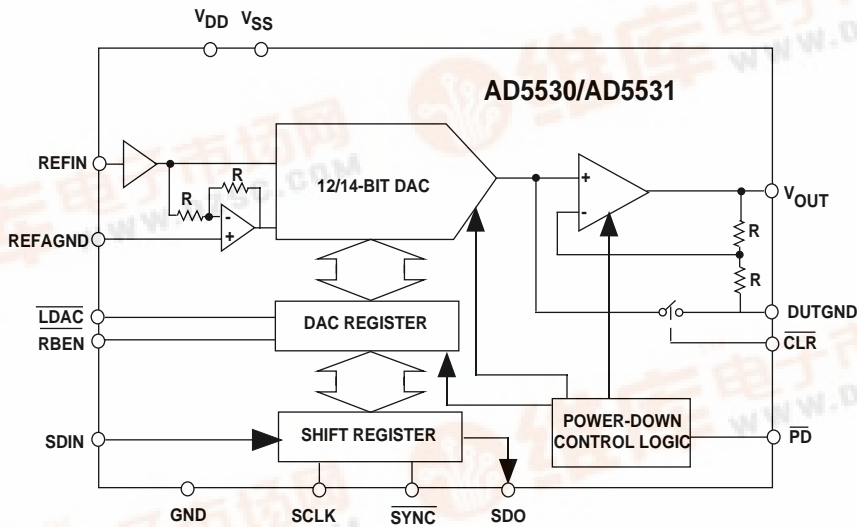
The AD5530 and AD5531 are single 12/14 bit serial input, voltage output DAC's respectively.

They utilize a versatile three-wire interface that is compatible with SPI™, QSPI™, MICROWIRE™ and DSP interface standards. Data is presented to the part in the format of a sixteen bit serial word. Serial data is available on the SDO pin for daisy chaining purposes. Data Readback allows the user to read the contents of the DAC register via the SDO pin.

The DAC output is buffered by a gain of two amplifier and referenced to the potential at DUTGND.  $\overline{LDAC}$  may be used to update the output of the DAC. A Power Down ( $\overline{PD}$ ) pin allows the DAC to be put into a low power state, and a  $\overline{CLR}$  pin allows the output to be cleared to a user defined voltage, the potential at DUTGND.

The AD5530 and AD5531 are available in 16 lead TSSOP packages.

### FUNCTIONAL BLOCK DIAGRAM



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MICROWIRE is a trademark of National Semiconductor Corporation.

REV. PrK, March, 2002

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# AD5530/AD5531—SPECIFICATIONS<sup>1</sup>

( $V_{DD} = +15\text{ V} \pm 10\%$ ;  $V_{SS} = -15\text{ V} \pm 10\%$ ;  $GND = 0\text{ V}$ ;  $R_L = 5\text{ k}\Omega$  and  $C_L = 220\text{ pF}$  to  $GND$ , All specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted)

Parameter	AD5530	AD5531	Units	Test Conditions/Comments
<b>ACCURACY</b>				
Resolution	12	14	Bits	
Relative Accuracy	$\pm 1$	$\pm 2$	LSB max	
Differential Nonlinearity	$\pm 1$	$\pm 1$	LSB max	Guaranteed Monotonic Over Temperature
Zero-Scale Error	$\pm 2$	$\pm 8$	LSB max	Typically within $\pm 1$ LSB
Full-Scale Error	$\pm 2$	$\pm 8$	LSB max	Typically within $\pm 1$ LSB
Gain Error	$\pm 1$	$\pm 8$	LSB typ	
Gain Temperature Coefficient <sup>2</sup>	20	20	ppm FSR/ $^{\circ}\text{C}$ typ	
	40	40	ppm FSR/ $^{\circ}\text{C}$ max	
<b>REFERENCE INPUTS<sup>2</sup></b>				
Reference Input Range	0/5	0/5	V min/V max	Max output range $\pm 10\text{V}$
DC Input Resistance	100	100	M $\Omega$ typ	
Input Current	$\pm 1$	$\pm 1$	$\mu\text{A}$ max	Per Input. Typically $\pm 20\text{ nA}$
<b>DUTGND INPUT<sup>2</sup></b>				
DC Input Impedance	60	60	k $\Omega$ typ	
Max Input Current	$\pm 0.3$	$\pm 0.3$	mA typ	
Input Range	-5/+5	-5/+5	V min/V max	Max output range $\pm 10\text{V}$
<b>O/P CHARACTERISTICS</b>				
Output Voltage Swing	$\pm 10$	$\pm 10$	V max	
Short Circuit Current <sup>2</sup>	15	15	mA max	
Resistive Load	5	5	k $\Omega$ min	To 0 V
Capacitive Load	220	220	pF max	To 0 V
DC Output Impedance <sup>2</sup>	0.5	0.5	$\Omega$ max	
<b>DIGITAL I/O</b>				
$V_{INH}$ , Input High Voltage	2.4	2.4	V min	
$V_{INL}$ , Input Low Voltage	0.8	0.8	V max	
$I_{INH}$ , Input Current	$\pm 10$	$\pm 10$	$\mu\text{A}$ max	Total for All Pins
$C_{IN}$ , Input Capacitance <sup>2</sup>	10	10	pF max	
SDO $V_{OL}$ Output Low Voltage	0.4	0.4	V max	$I_{SINK} = 1\text{ mA}$
<b>POWER REQUIREMENTS</b>				
$V_{DD}/V_{SS}$	+15/-15	+15/-15	V nom	$\pm 10\%$ For Specified Performance
Power Supply Sensitivity				
$\Delta$ Full Scale/ $\Delta V_{DD}$	110	110	dB typ	
$\Delta$ Full Scale/ $\Delta V_{SS}$	100	100	dB typ	
$I_{DD}$	2	2	mA max	Outputs Unloaded. $I_{DD}$ in power down $< 50\mu\text{A}$
$I_{SS}$	2	2	mA max	Outputs Unloaded.

## NOTES

<sup>1</sup>Temperature range for B Version:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

<sup>2</sup>Guaranteed by design.

Specifications subject to change without notice.

## AC PERFORMANCE CHARACTERISTICS<sup>1</sup>

( $V_{DD} = +10.8\text{V}$  to  $16.5\text{V}$ ,  $V_{SS} = -10.8\text{V}$  to  $-16.5\text{V}$ ;  $GND = 0\text{ V}$ ;  $R_L = 5\text{ k}\Omega$  and  $C_L = 220\text{ pF}$  to  $GND$ , All specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted)

Parameter	A	Units	Test Conditions/Comments
<b>DYNAMIC PERFORMANCE</b>			
Output Voltage Settling Time	20	$\mu\text{s}$ typ	Full-Scale Change to $\pm 1/2$ LSB. DAC Latch Contents Alternately Loaded with All 0s and All 1s
Slew Rate	1.5	V/ $\mu\text{s}$ typ	
Digital-to-Analog Glitch Impulse	120	nV-s typ	DAC Latch Alternately Loaded with 0FFF Hex and 1000 Hex. Not Dependent on Load Conditions
Digital Feedthrough	0.5	nV-s typ	Effect of Input Bus Activity on DAC Output Under Test
Output Noise Spectral Density @ 1 kHz	130	nV/(Hz) <sup>1/2</sup> typ	All 1s Loaded to DAC.

## NOTES

<sup>1</sup>Specifications subject to change without notice. Guaranteed by design, not subject to production test.

# SPECIFICATIONS<sup>1</sup>

## AD5530/AD5531

( $V_{DD} = +12\text{ V} \pm 10\%$ ;  $V_{SS} = -12\text{ V} \pm 10\%$ ;  $GND = 0\text{ V}$ ;  $R_L = 5\text{ k}\Omega$  and  $C_L = 220\text{ pF}$  to  $GND$ ,  $T_A^1 = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted)

Parameter	AD5530	AD5531	Units	Test Conditions/Comments
<b>ACCURACY</b>				
Resolution	12	14	Bits	
Relative Accuracy	$\pm 1$	$\pm 2$	LSB max	
Differential Nonlinearity	$\pm 1$	$\pm 1$	LSB max	Guaranteed Monotonic Over Temperature
Zero-Scale Error	$\pm 2$	$\pm 8$	LSB max	Typically within $\pm 1$ LSB
Full-Scale Error	$\pm 2$	$\pm 8$	LSB max	Typically within $\pm 1$ LSB
Gain Error	$\pm 1$	$\pm 8$	LSB typ	
Gain Temperature Coefficient <sup>2</sup>	20	20	ppm FSR/ $^{\circ}\text{C}$ typ	
	40	40	ppm FSR/ $^{\circ}\text{C}$ max	
<b>REFERENCE INPUTS<sup>2</sup></b>				
Reference Input Range	0/4.096	0/4.096	V min/V max	Max output range $\pm 8.192\text{V}$
DC Input Resistance	100	100	M $\Omega$ typ	
Input Current	$\pm 1$	$\pm 1$	$\mu\text{A}$ max	Per Input. Typically $\pm 20\text{ nA}$
<b>DUTGND INPUT<sup>2</sup></b>				
DC Input Impedance	60	60	k $\Omega$ typ	
Max Input Current	$\pm 0.3$	$\pm 0.3$	mA typ	
Input Range	-5/+5	-5/+5	V min/V max	Max output range $\pm 8.192\text{V}$
<b>O/P CHARACTERISTICS</b>				
Output Voltage Swing	$\pm 8.192$	$\pm 8.192$	V max	
Short Circuit Current <sup>2</sup>	15	15	mA max	
Resistive Load	5	5	k $\Omega$ min	To 0 V
Capacitive Load	220	220	pF max	To 0 V
DC Output Impedance <sup>2</sup>	0.5	0.5	$\Omega$ max	
<b>DIGITAL I/O</b>				
$V_{INH}$ , Input High Voltage	2.4	2.4	V min	
$V_{INL}$ , Input Low Voltage	0.8	0.8	V max	
$I_{INH}$ , Input Current	$\pm 10$	$\pm 10$	$\mu\text{A}$ max	Total for All Pins
$C_{IN}$ , Input Capacitance <sup>2</sup>	10	10	pF max	
SDO $V_{OL}$ Output Low Voltage	0.4	0.4	V max	$I_{SINK} = 1\text{ mA}$
<b>POWER REQUIREMENTS</b>				
$V_{DD}/V_{SS}$	+12/-12	+12/-12	V nom	$\pm 10\%$ For Specified Performance
Power Supply Sensitivity				
$\Delta$ Full Scale/ $\Delta V_{DD}$	110	110	dB typ	
$\Delta$ Full Scale/ $\Delta V_{SS}$	100	100	dB typ	
$I_{DD}$	2	2	mA max	Outputs Unloaded. $I_{DD}$ in power down $< 50\mu\text{A}$
$I_{SS}$	2	2	mA max	Outputs Unloaded.

### NOTES

<sup>1</sup>Temperature range for B Version:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

<sup>2</sup>Guaranteed by design.

Specifications subject to change without notice.

# AD5530/AD5531

## STAND ALONE TIMING CHARACTERISTICS<sup>1,2</sup>

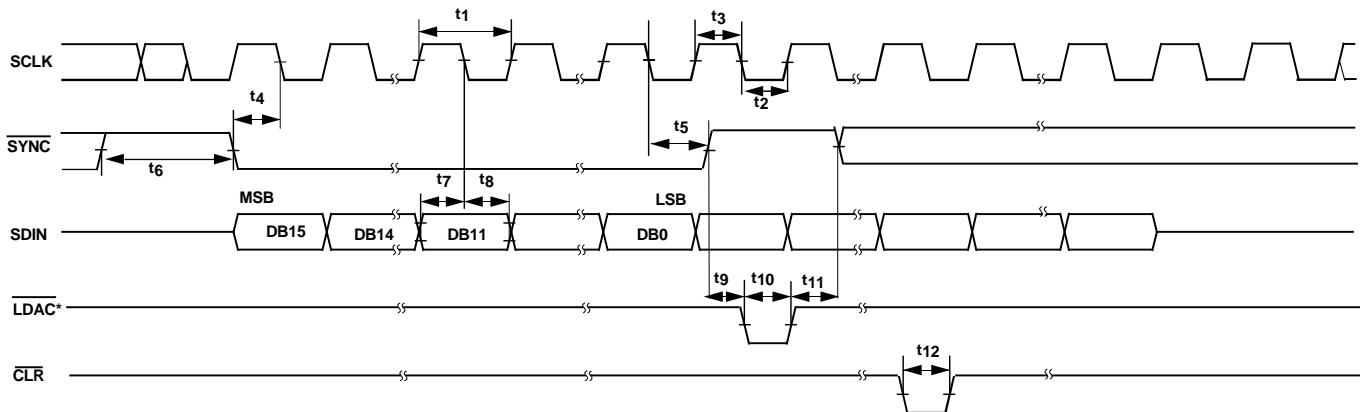
( $V_{DD} = +10.8V$  to  $16.5V$ ,  $V_{SS} = -10.8V$  to  $-16.5V$ ;  $GND = 0V$ ;  $R_L = 5k\Omega$  and  $C_L = 220pF$  to  $GND$ , All specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted)

Parameter	Limit at $T_{MIN}$ , $T_{MAX}$	Units	Description
$f_{MAX}$	8	MHz max	SCLK Frequency
$t_1$	125	ns min	SCLK cycle time
$t_2$	50	ns min	SCLK low time
$t_3$	50	ns min	SCLK high time
$t_4$	40	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
$t_5$	40	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
$t_6$	40	ns min	Min $\overline{SYNC}$ high time
$t_7$	30	ns min	Data setup time
$t_8$	10	ns min	Data hold time
$t_9$	0	ns min	$\overline{SYNC}$ high to $\overline{LDAC}$ low
$t_{10}$	40	ns min	$\overline{LDAC}$ pulse width
$t_{11}$	0	ns min	$\overline{LDAC}$ high to $\overline{SYNC}$ low
$t_{12}$	40	ns min	$\overline{CLR}$ pulse width

<sup>1</sup>Guaranteed by design. Not production tested.

<sup>2</sup>Sample tested during initial release and after any redesign or process change that may affect this parameter. All input signals are measured with  $t_r = t_f = 5ns$  (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH})/2$ .

Specifications subject to change without notice.



\*LDAC may be tied permanently low if required.

Figure 1. Timing Diagram for Stand Alone Mode

## DAISY CHAINING AND READBACK TIMING CHARACTERISTICS<sup>1,2,3</sup>

( $V_{DD} = +10.8V$  to  $16.5V$ ,  $V_{SS} = -10.8V$  to  $-16.5V$ ;  $V_{SS} = -15V \pm 10\%$ ;  $GND = 0V$ ;  $R_L = 5k\Omega$  and  $C_L = 220pF$  to  $GND$ , All specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted)

Parameter	Limit at $T_{MIN}$ , $T_{MAX}$	Units	Description
$f_{MAX}$	2	MHz max	SCLK Frequency
$t_1$	500	ns min	SCLK cycle time
$t_2$	200	ns min	SCLK low time
$t_3$	200	ns min	SCLK high time
$t_4$	40	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
$t_5$	40	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
$t_6$	40	ns min	Min $\overline{SYNC}$ high time
$t_7$	30	ns min	Data setup time
$t_8$	10	ns min	Data hold time
$t_{12}$	40	ns min	CLR pulse width
$t_{13}$	60	ns max	SCLK Falling edge to SDO Valid
$t_{14}$	20	ns min	SCLK Falling edge to SDO Invalid
$t_{15}$	40	ns min	$\overline{RBEN}$ to SCLK falling edge setup time
$t_{16}$	20	ns min	$\overline{RBEN}$ hold time
$t_{17}$	100	ns min	$\overline{RBEN}$ falling edge to SDO valid

<sup>1</sup>Guaranteed by design. Not production tested.

<sup>2</sup>Sample tested during initial release and after any redesign or process change that may affect this parameter. All input signals are measured with  $t_r = t_f = 5ns$  (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH})/2$ .

<sup>3</sup>SDO;  $R_{PULLUP} = 5k\Omega$ ,  $C_L = 15pF$ .

Specifications subject to change without notice.

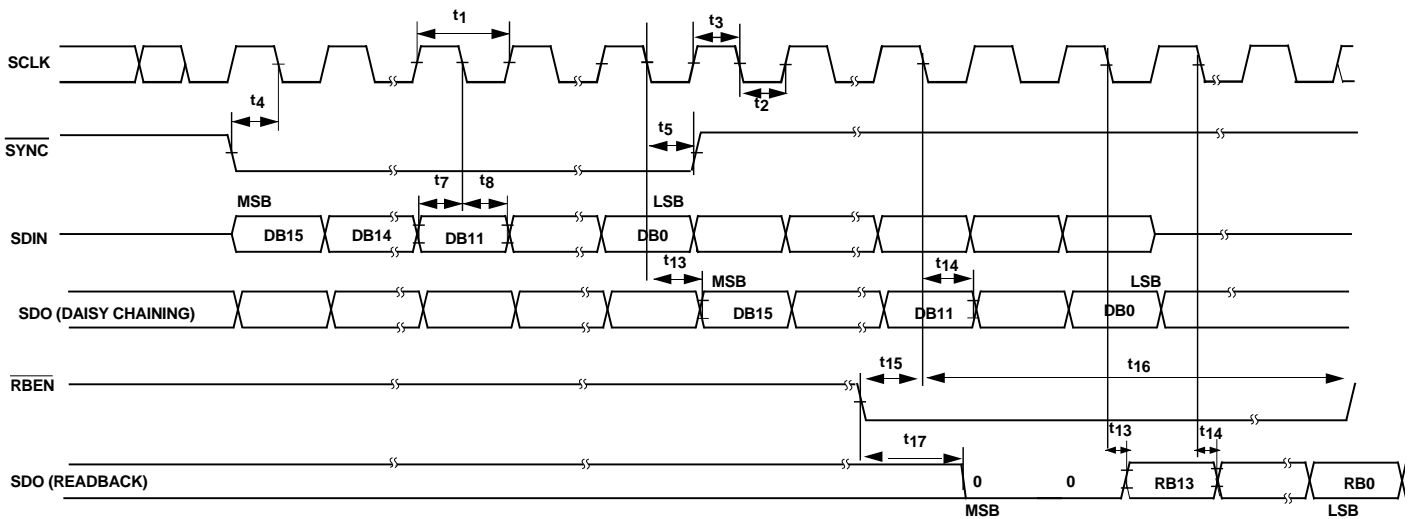


Figure 2. Timing Diagram for Daisy Chaining and Readback

# AD5530/AD5531

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = +25°C unless otherwise noted)

V <sub>DD</sub> to GND	-0.3 V, +17 V
V <sub>SS</sub> to GND	+0.3 V, -17 V
Digital Inputs to GND	-0.3V to V <sub>DD</sub> +0.3 V
SDO to GND	-0.3V to +6.5 V
REFIN to REFAGND	-0.3V, +17 V
REFIN to GND	V <sub>SS</sub> - 0.3V, V <sub>DD</sub> + 0.3V
REFAGND to GND	V <sub>SS</sub> - 0.3V, V <sub>DD</sub> + 0.3V
DUTGND to GND	V <sub>SS</sub> - 0.3V, V <sub>DD</sub> + 0.3V
Operating Temperature Range Industrial (B Version)	-40°C to +85°C

Storage Temperature Range	-65°C to +150°C
Maximum Junction Temperature, (T <sub>J</sub> max)	+150°C
Package Power Dissipation	(T <sub>J</sub> max - T <sub>A</sub> )/θ <sub>JA</sub>
Thermal Impedance θ <sub>JA</sub> TSSOP(RU-16)	150.4°C/W
Lead Temperature (Soldering 10s)	300°C
IR Reflow, Peak Temperature	220°C

### NOTES

<sup>1</sup>Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ORDERING GUIDE

Model	Temperature Range	INL (LSBs)	DNL(LSBs)	Package Option*
AD5530BRU	-40 °C to +85 °C	± 1	± 1	RU-16
AD5531BRU	-40 °C to +85 °C	± 2	± 1	RU-16

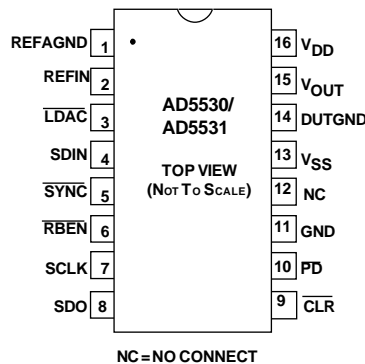
\*RU = Thin Shrink Small Outline Package.

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5530/5531 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESDprecautions are recommended to avoid performance degradation or loss of functionality.



## PIN CONFIGURATION 16 Lead TSSOP



## AD5530/AD5531 PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Description
1	REFAGND	For bipolar $\pm 10$ V output range, this pin should be tied to 0V.
2	REFIN	This is the voltage reference input for the DAC. Connect to external +5V reference for specified bipolar $\pm 10$ V output.
3	$\overline{\text{LDAC}}$	Load DAC logic input (active low). When taken low, the contents of the shift register is transferred to the DAC register. $\overline{\text{LDAC}}$ may be tied permanently low enabling the outputs to be updated on the rising edge of $\overline{\text{SYNC}}$ .
4	SDIN	Serial data input. This device accepts 16-bit words. Data is clocked into the input register on the falling edge of SCLK.
5	$\overline{\text{SYNC}}$	Logic Input signal used to frame the serial data input.
6	$\overline{\text{RBEN}}$	Readback enable function. This function allows the contents of the DAC register to be read. Data from the DAC register will be shifted out on SDO pin on each rising edge of SCLK.
7	SCLK	Clock input. Data is clocked into the input register on the falling edge of SCLK.
8	SDO	Serial Data out. This pin is used to clock out the serial data previously written to the input shift register or may be used in conjunction with $\overline{\text{RBEN}}$ to read back the data from the DAC register. This is an open drain output, it should be pulled high with an external pull up resistor. In stand alone mode, SDO should be tied to GND or left high impedance.
9	$\overline{\text{CLR}}$	Level sensitive, active low input. A falling edge of $\overline{\text{CLR}}$ resets $V_{\text{OUT}}$ to DUTGND. The contents of the registers are untouched. When $\overline{\text{CLR}}$ is brought high again, the DAC output reverts to the original output as determined by the data in the DAC register.
10	$\overline{\text{PD}}$	This allows the DAC to be put into a power down state.
11	GND	Ground reference.
12	NC	Do not connect anything to this pin.
13	$V_{\text{SS}}$	Negative analog supply voltage, $-12$ V $\pm 10\%$ or $-15$ V $\pm 10\%$ for specified performance.
14	DUTGND	$V_{\text{OUT}}$ is referenced to the voltage applied to this pin.
15	$V_{\text{OUT}}$	DAC output.
16	$V_{\text{DD}}$	Positive analog supply voltage, $+12$ V $\pm 10\%$ or $+15$ V $\pm 10\%$ for specified performance.

**TERMINOLOGY****Relative Accuracy**

Relative accuracy or endpoint linearity is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

**Differential Nonlinearity**

Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of  $\pm 1$  LSB maximum ensures monotonicity.

**Gain Error**

Gain error is the difference between the actual and ideal analog output range, expressed as a percent of the full-scale range. It is the deviation in slope of the DAC transfer characteristic from ideal.

**Zero Scale Error**

Zero code error is a measure of the output error when all 0s are loaded to the DAC latch.

**Full Scale Error**

This is the error in DAC output voltage when all 1s are loaded into the DAC latch. Ideally the output voltage, with all 1s loaded into the DAC latch, should be  $2 V_{\text{REF}} - 1 \text{ LSB}$ .

**Output Voltage Settling time**

This is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

**Digital-to-Analog Glitch Impulse**

Digital-to-Analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is specified as the area of the glitch in nV-s and is measured when the digital input code is changed by 1 LSB at the major carry transition.

**Digital Feedthrough**

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-s and is measured with a full-scale code change on the data bus, i.e., from all 0s to all 1s and vice versa.

# AD5530/AD5531

## TYPICAL PERFORMANCE CHARACTERISTICS

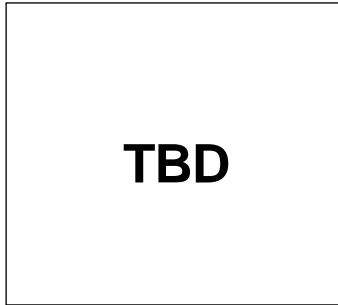


Figure 3. Typical INL Plot

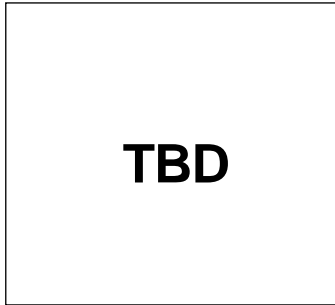


Figure 4. Typical DNL Plot

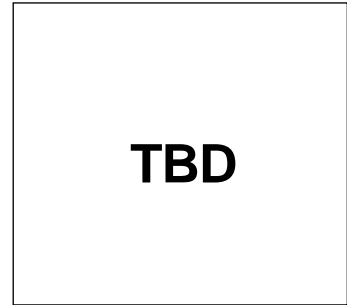


Figure 5. Typical INL Error vs. Temperature

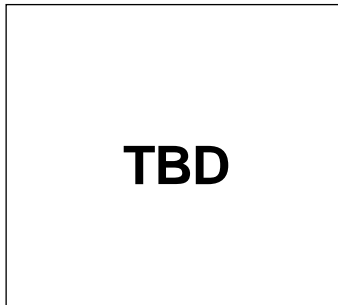


Figure 6. Typical DNL error vs. Temperature

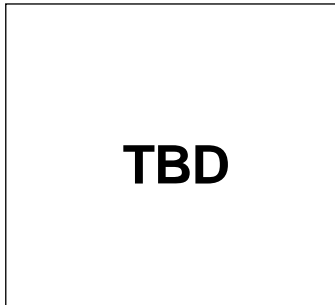


Figure 7. Zero Scale and Full Scale Error vs. Temperature

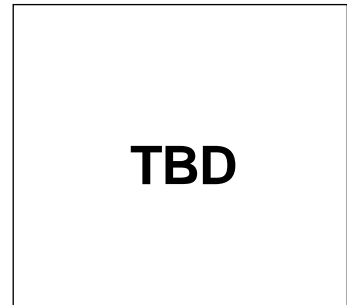


Figure 8. Typical Digital to Analog Glitch Impulse

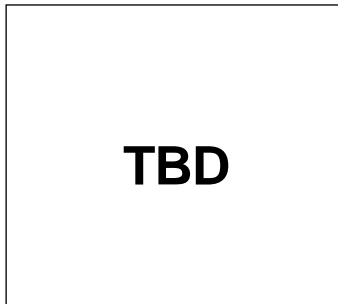


Figure 9. Settling Time

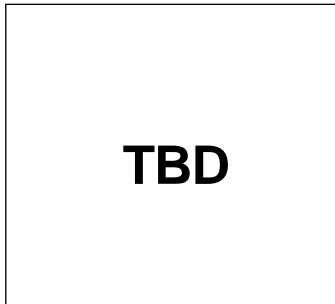


Figure 10.  $I_{DD}$ ,  $I_{SS}$  vs. Temperature

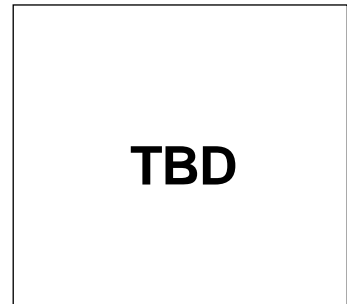


Figure 11. Power On Reset



## GENERAL DESCRIPTION

### DAC Architecture

The AD5530/AD5531 are pin compatible 12/14 bit DACs. The AD5530 consists of a straight 12 bit R-2R voltage mode DAC, while the AD5531 consists of a 14 bit R-2R section. Using a +5 V reference connected to the REFIN pin and REFAGND tied to 0V, a bipolar  $\pm 10V$  voltage output results. The DAC coding is straight binary.

### Serial Interface

Serial data on the SDIN input is loaded to the input register under the control of SCLK,  $\overline{\text{SYNC}}$  and  $\overline{\text{LDAC}}$ . A write operation transfers a 16 bit word to the AD5530/AD5531. Figure 1 and 2 show the timing diagrams. Figure 12 shows the contents of the input shift register. 12 or 14 bits of the serial word are data bits, the rest are don't cares.

The serial word is framed by the signal,  $\overline{\text{SYNC}}$ . After a high to low transition on  $\overline{\text{SYNC}}$ , data is latched into the input shift register on the falling edges of SCLK. There are two ways in which the DAC register and output may be updated. The  $\overline{\text{LDAC}}$  signal is examined on the falling edge of  $\overline{\text{SYNC}}$ , depending on its status, either a synchronous or asynchronous update is selected. If  $\overline{\text{LDAC}}$  is low, then the DAC register and output are updated on the low to high transition of  $\overline{\text{SYNC}}$ . Alternatively, if  $\overline{\text{LDAC}}$  is high upon sampling, the DAC register is not loaded with the new data on a rising edge of  $\overline{\text{SYNC}}$ . The contents of the DAC register and the output voltage will be updated by bringing  $\overline{\text{LDAC}}$  low any time after the 16 bit data transfer is complete.  $\overline{\text{LDAC}}$  may be tied permanently low if required. A simplified diagram of the input loading circuitry is illustrated in Figure 13.

Data written to the part via SDIN is available on the SDO pin 16 clocks later if the readback function is not used. SDO data is clocked out on the falling edge of the serial clock with some delay.

### $\overline{\text{PD}}$ Function

The PD pin allows the user to place the device into power down mode. While in this mode, power consumption is at a minimum, the device draws only 50 $\mu\text{A}$  of current. The PD function does not affect the contents of the DAC register.

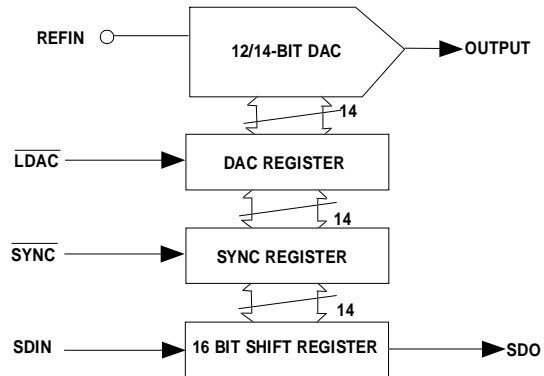


Figure 13. Simplified Serial Interface

### READBACK Function

The AD5530/AD5531 allows the data contained in the DAC register to be read back if required. The pins involved are the  $\overline{\text{RBEN}}$  and SDO (serial data out).  $\overline{\text{RBEN}}$  is first asserted low, on the next falling edge of SCLK, while  $\overline{\text{RBEN}}$  is still low, the contents of the DAC register are transferred to the shift register.  $\overline{\text{RBEN}}$  may be used to frame the readback data by leaving it low for 16 clock cycles, or it may be asserted high after the required hold time. The shift register contains the DAC register data and this is shifted out on the SDO line on each falling edge of SCLK with some delay. This ensures the data on the serial data output pin is valid for the falling edge of the receiving part. The two MSBs of the 16-bit word will be '0's.

### $\overline{\text{CLR}}$ function

The falling edge of  $\overline{\text{CLR}}$  causes  $V_{\text{OUT}}$  to be reset to the same potential as DUTGND. The contents of the registers remain unchanged, so the user can reload the previous data with  $\overline{\text{LDAC}}$  after  $\overline{\text{CLR}}$  is asserted high. Alternatively, if  $\overline{\text{LDAC}}$  is tied low, the output will be loaded with the contents of the DAC register automatically after  $\overline{\text{CLR}}$  is brought high.

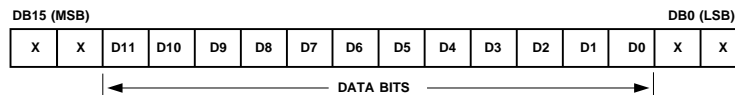


Figure 12a. AD5530 Input Shift register contents

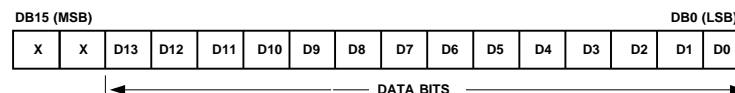


Figure 12b. AD5531 Input Shift register contents

# AD5530/AD5531

## Output Voltage

The DAC transfer function is as follows

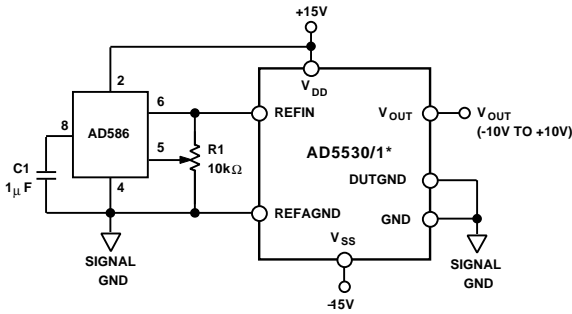
$$V_{OUT} = 2[2*(REFIN - REFAGND) * D / 2^N + 2*RefAGND - REFIN] - DUTGND$$

where :

D is the decimal data word loaded to the DAC register,  
N is the resolution of the DAC.

## Bipolar Configuration

Figure 14 shows the AD5530/AD5531 in a bipolar circuit configuration. REFIN is driven by the AD586, +5V reference, while the REFAGND and DUTGND pins are tied to GND. This results in a bipolar output voltage ranging from -10 V to +10 V. Resistor R1 is provided (if required) for gain adjust. Figure 15 shows the transfer function of the DAC when REFAGND is tied to 0V.



\*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 14. Bipolar +/-10 V operation.

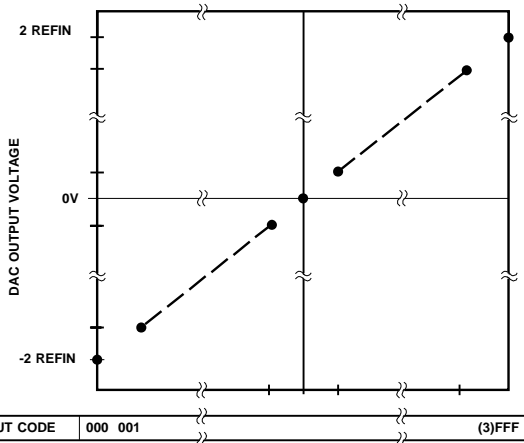


Figure 15. Output Voltage vs. DAC input codes (Hex).

## MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5530/AD5531 is via a serial bus that uses standard protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire (minimum) interface consisting of a clock signal, a data signal and a synchronization signal. The AD5530/AD5531 requires a 16-bit data word with data valid on the falling edge of SCLK.

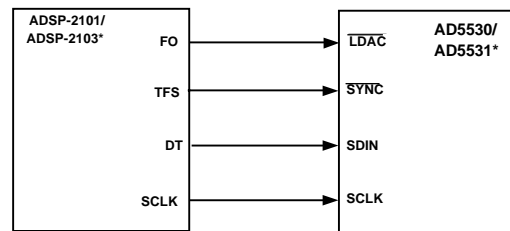
For all the interfaces, the DAC output update may be done automatically when all the data is clocked in or it may be done under the control of LDAC.

The contents of the DAC register may be read using the Readback function. RBEN is used to frame the readback data which is clocked out on SDO. The following figures illustrate these DACs interfacing with a simple 4 wire interface. The serial interface of the AD5530/AD5531 may be operated from a minimum of three wires.

### AD5530/AD5531 to ADSP-21xx

An interface between the AD5530/AD5531 and the ADSP-21xx is shown in Figure 17. In the interface example shown, SPORT0 is used to transfer data to the DAC. The SPORT control register should be configured as follows : internal Clock operation, alternate framing mode; active low framing signal.

Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. As the data is clocked out of the DSP on the rising edge of SCLK, no glue logic is required to interface the DSP to the DAC. In the interface shown, the DAC output is updated using the LDAC pin via the DSP. Alternatively, the LDAC input could be tied permanently low and then the update takes place automatically when TFS is taken high.



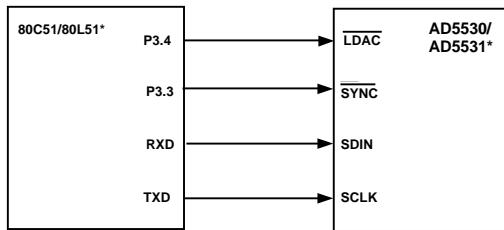
\*ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 16. AD5530/AD5531 to ADSP-21xx interface.

### AD5530/AD5531 to 8051 Interface

A serial interface between the AD5530/AD5531 and the 8051 is shown in Figure 16. TXD of the 8051 drives SCLK of the AD5530/AD5531, while RXD drives the serial data line, SDIN. P3.3 and P3.4 are bit programmable pins on the serial port and are used to drive SYNC and LDAC respectively.

The 8051 provides the LSB of its SBUF register as the first bit in the data stream. The user will have to ensure that the data in the SBUF register is arranged correctly as the DAC expects MSB first.



\*ADDITIONAL PINS OMITTED FOR CLARITY.

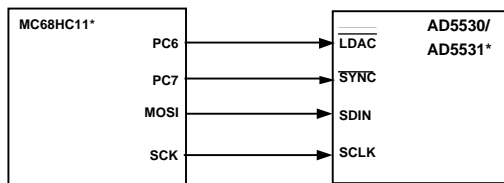
Figure 17. AD5530/AD5531 to 8051 Interface.

When data is to be transmitted to the DAC, P3.3 is taken low. Data on RXD is clocked out of the microcontroller on the rising edge of TXD and is valid on the falling edge. As a result no glue logic is required between this DAC and microcontroller interface.

The 8051 transmits data in 8-bit bytes with only 8 falling clock edges occurring in the transmit cycle. As the DAC expects a 16 bit word, P3.3 must be left low after the first eight bits are transferred. After the second byte has been transferred, the P3.3 line is taken high. The DAC may be updated using  $\overline{\text{LDAC}}$  via P3.4 of the 8051.

### AD5530/AD5531 to MC68HC11 Interface

Figure 18 shows an example of a serial interface between the AD5530/AD5531 and the MC68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC, while the MOSI output drives the serial data lines, SDIN.  $\overline{\text{SYNC}}$  is driven from one of the port lines, in this case PC7.



\*ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 18. AD5530/AD5531 to MC68HC11 interface.

The 68HC11 is configured for master mode; MSTR=1, CPOL=0 and CPHA = 1. When data is transferred to the part, PC7 is taken low, data is transmitted MSB first. Data appearing on the MOSI output is valid on the falling edge of SCK. Eight falling clock edges occur in the transmit cycle, so in order to load the required 16 bit word, PC7 is not brought high until the second eight bit word has been transferred to the DACs input shift register.

$\overline{\text{LDAC}}$  is controlled by the PC6 port output. The DAC can be updated after each two byte transfer by bringing  $\overline{\text{LDAC}}$  low. This example does not show other serial lines for the DAC. If  $\overline{\text{CLR}}$  were used, it could be controlled by port output PC5. In order to read data back from the DAC register, the SDO line could be connected to MISO of the MC68HC11, with  $\overline{\text{RBEN}}$  tied to another port output controlling and framing the readback data transfer.

## APPLICATIONS

### Optocoupler Interface

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled. Opto-isolators can provide voltage isolation in excess of 3kV. The serial loading structure of the AD5530/AD5531 makes it ideal for opto-isolated interfaces as the number of interface lines is kept to a minimum. Figure 19 shows a 4 channel isolated interface to the AD5530/AD5531. To reduce the number of opto-isolators, if the simultaneous updating of the DAC is not required, then the  $\overline{\text{LDAC}}$  pin may be tied permanently low.

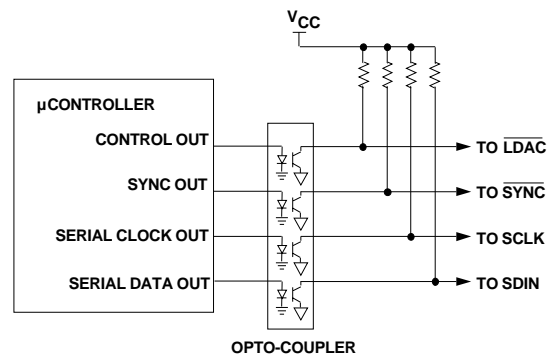


Figure 19. Opto-Isolated Interface.

### Serial Interface to Multiple AD5530s or AD5531s

Figure 20 shows how the  $\overline{\text{SYNC}}$  pin is used to address multiple AD5530/AD5531s. All devices receive the same serial clock and serial data, but only one device will receive the  $\overline{\text{SYNC}}$  signal at any one time. The DAC addressed will be determined by the decoder. There will be some feedthrough from the digital input lines, the effects of which can be minimized by using a burst clock.

# AD5530/AD5531

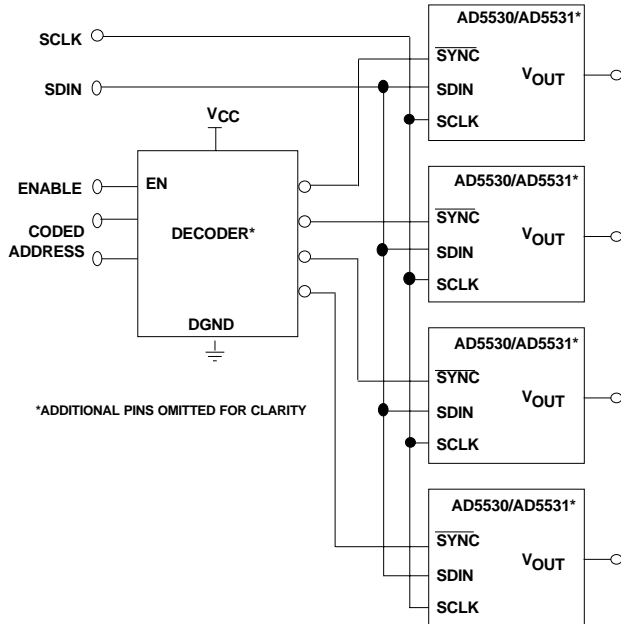


Figure 20. Addressing Multiple AD5530/AD5531s.

## Daisy Chaining Interface with Multiple AD5530s or AD5531s

A number of these DAC parts may be daisy chained together using the SDO pin. Figure 21 illustrates such a configuration.

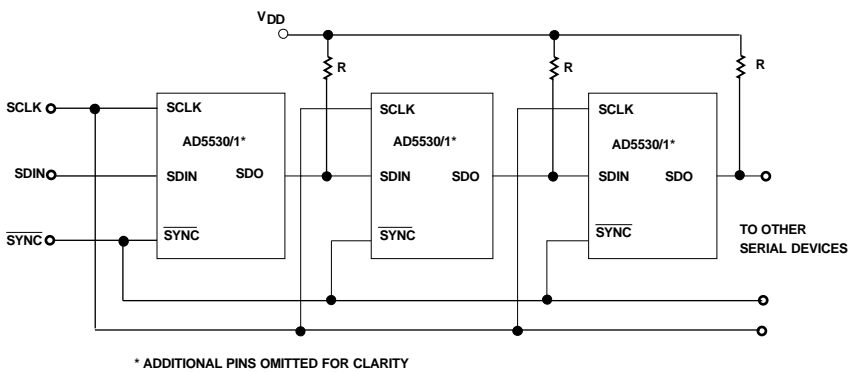


Figure 27. Daisy Chaining Multiple AD5530/1s.

**OUTLINE DIMENSIONS**  
Dimensions shown in inches and (mm).

**16-Lead TSSOP**  
**(RU-16)**

