S5920
32-Bit PCI Bus Target Interface

February 12, 1997 Revised October 1998

FEATURES

- PCI 2.2 Compliant Target/Slave Device
- Full 132 Mbytes/sec Transfer Rate
- PCI Bus Operation DC to 33 Mhz
- Add-On Bus 8 MHz to 40 Mhz
- Programmable Prefetch and Wait States
- 8/16/32 Bit Add-On User Bus
- Four Definable Pass-Thru Regions
- 32 Byte Burstable PCI Bus FIFO
- Active/Passive Add-On Bus Operation
- Mail Box Registers w/Byte Level Status
- Direct Mail Box Data Strobe/Interrupt Pin
- Mail Box Read/Write Interrupts
- Direct PCI & Add-On Interrupt Pins
- S5933 PCI Target Mode Replacement
- S5933 Software Compatible
- Plug-N-Play Compatible
- Two Wire Serial Bus nvRAM Support
- Optional External BIOS
- 160 Pin PQFP

APPLICATIONS

- ISA to PCI Local Bus Conversions
- I/O Communications Ports
- High Speed Data Output
- General Purpose PCI Interfacing
- Data Communications
- Memory Interfaces
- Data Acquisition
- Data Encryption/Decryption

DESCRIPTION

The AMCC S5920 was developed to provide the designer with a single multi-function device offering a flexible and easy means to connect applications to the PCI Local Bus. Designers connecting to the PCI Local Bus through the S5920 eliminate the necessity to understand complex PCI Bus timing requirements and the time consuming task of assuring PCI specification compliance. The S5920's design incorporates years of design experience and system knowledge achieved through the popular S5933 PCI Matchmaker device.

The S5920 converts complex PCI bus signals into an easy-to-use 8-, 16- or 32-bit user bus referred to as the Add-On Local Bus. The S5920 Add-On signal pins, shown in Figure 2, provide the designer with a much simpler bus structure in which to interface I/O, memory or data acquisition applications and to port existent ISA-based designs over to the PCI Bus. The bus can be operated either synchronously or asynchronously to the PCI Local Bus with user definable clock speeds from 8 to 40 MHz.

Since the S5920 is a PCI 'Target' or 'Slave' device only, its cost is significantly less than PCI Bus Master solutions making it ideal for low cost applications. The S5920 is compliant with the PCI Local Bus Specification Revision 2.2. It is capable of 132 Mbytes/sec data transfer rates and supports both burst and single DWORD data transfers. The S5920 logic core is powered from a single 5 volt supply and utilizes advanced AMCC technology to achieve low system power consumption at clock speeds to 33 MHz. The S5920 block diagram is shown in Figure 1.

The S5920's superior feature set offers the designer multiple hardware and software design options for higher performance. Up to four Host bus memory or I/O space definable blocks, referred to as Pass-Thru regions, may be implemented providing multiple data channels. Data transfers via a Pass-Thru data channel can be performed through a single buffered to the application or through burstable FIFOs. Added read prefetch and programmable FIFO wait state features allow the user to fine tune system performance. The Pass-Thru data channels also supports an 'active or passive' mode bus interface. Passive mode requires the designer to transfer data by externally driving data onto the Add-On Bus. Active mode minimizes design components by enabling internal logic to drive or acquire the Add-On Bus for reading or writing data independently. Active mode also supports programmable wait state generation for slower Add-On designs.

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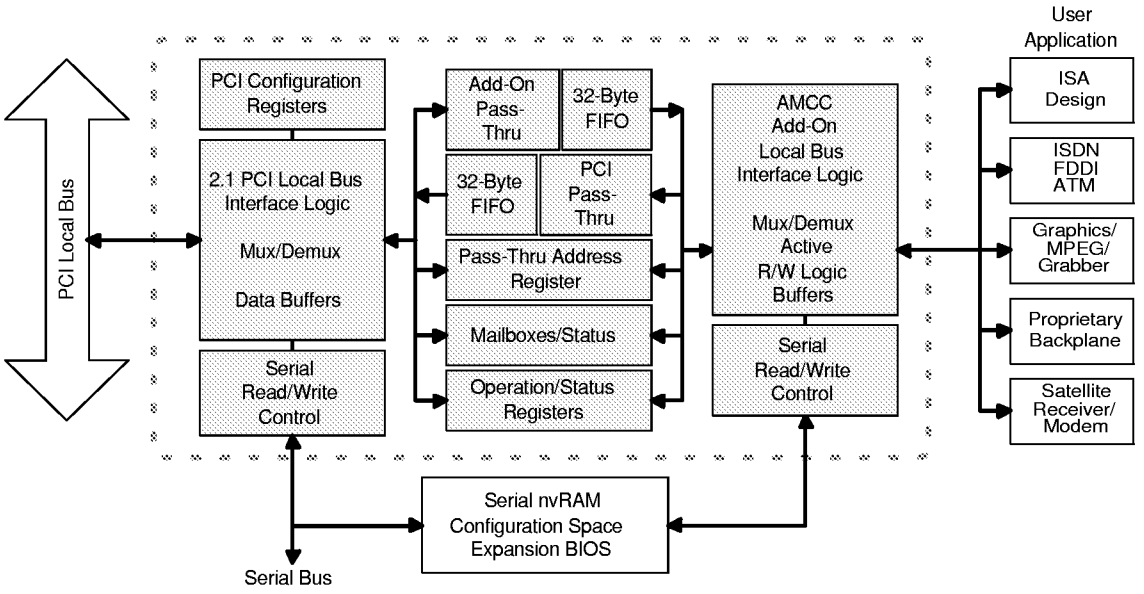


Figure 1

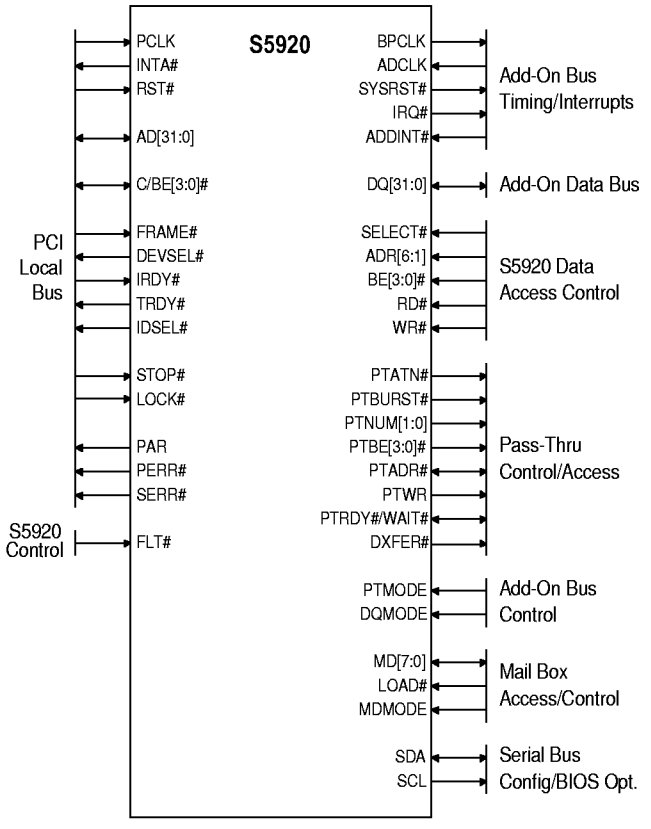


Figure 2

The S5920 signal pins are shown in Figure 2. The PCI Local Bus signals are detailed on the left side; Add-On Local Bus signal are detailed on the right side. All additional S5920 device control signals are shown on the lower right side.

The S5920 provides two 32-bit mailbox registers for data transfers or user definable status/command information transfer. Each mailbox may be examined for an empty or full status, at the byte level, through a mailbox status register. Mailbox transfers can be performed either by register style accesses (RD#/WR#, ADR[6:2], Select#, etc.) or hardware style accesses (MD[7:0] and Load#). The dedicated external mailbox data and strobe signal pins are provided for direct hardware read/writes with additional Add-On to PCI interrupt capabilities. A direct PCI to Add-On Bus interrupt pin is also provided adding further design flexibility.

The S5920 supports a two wire serial nvRAM bus. This allows the designer to customize the S5920 configuration by loading setup information during system power-up initialization from a single nvRAM and gain access to other devices on the serial bus.

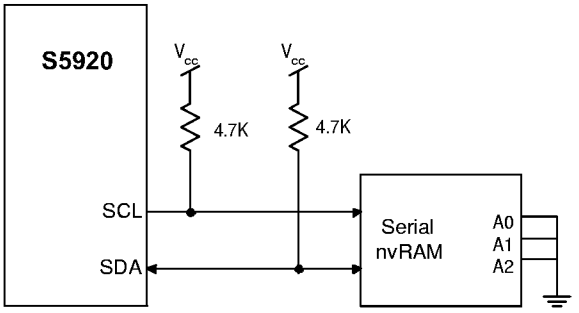


Figure 3

The S5920 supports boot loading of configuration data, Expansion BIOS and Power-On Self test code via the external nonvolatile serial memory device. The serial nvRAM may be programmed with user-defined configuration information which is loaded into the S5920 during power up initialization. Programming or reading the nvRAM may be done any time from dedicated S5920 operation registers. The utilization of the Expansion BIOS feature allows product identification banners or other user software code set-up requirements to be implemented during power up initalization. The serial nvRAM connections are shown in Figure 3.

The S5920 Register Architecture

All S5920 communications, control and configuration set up is performed through three groups of registers: PCI Configuration Registers, PCI Operation Registers and Add-On Operation Registers. All of these registers are user configurable through their associated buses with boot loadable registers configured from the external nvRAM. The following provides a brief overview of each register group.

PCI Configuration Registers

All PCI compliant devices are required to provide a group of PCI configuration registers. These registers are polled by the host system BIOS during power-up initialization. They contain specific device and product information such as Vendor ID, Device ID, Subsystem Vendor ID, memory requirements, etc. These registers are located in the S5920 and are either initialized with predefined default values or user customized definitions contained in the external nvRAM. Table 1 shows the S5920 PCI Configuration registers.

PCI Operation Registers

The second group of registers, shown in table 2, are the PCI Operation Registers. This group of registers is accessible via the PCI Bus. These are the primary registers through which the PCI Host configures the S5920 operation and communicates with the Add-On Bus. These registers encompass the PCI bus mailboxes, Pass-Thru/FIFO data channel and Status/Control registers.

Byte 3	Byte 2	Byte 1	Byte 0	Address
Device ID		Vendor ID		00h
PCI Status		PCI Command		04h
Class Code			Revision ID	08h
Built-In Self Test	Header Type	Latency Timer	CacheLine Size	0Ch
Base Address Register 0				10h
Base Address Register 1				14h
Base Address Register 2				18h
Base Address Register 3				1Ch
Base Address Register 4				20h
Base Address Register 5				24h
Reserved Space				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Expansion ROM Base Address				30h
Reserved Space				34h
Reserved Space				38h
Max. Latency	Min. Grant	Interrupt Pin	Interrupt Line	3Ch

Table 1

Add-On Bus Operation Registers

The last register group consists of the Add-On Operation Registers shown in table 3. This group of registers is accessible via the Add-On Bus. These are the primary registers through which the Add-On application configures S5920 operation and communicates with the PCI Bus. These registers encompass the Add-On bus mailboxes, Pass-Thru/FIFO Registers and Status/Control Registers.

PCI Operation Registers	Address Offset
Outgoing Mailbox Register (OMB)	0Ch
Incoming Mailbox Register (IMB)	1Ch
Mailbox Empty/Full Status Register (MBEF)	34h
Interrupt Control/Status Register (INTCSR)	38h
Reset Control Register (RCR)	3Ch
Pass-Thru Configuration Register (PTCR)	60h

Table 2

Add-On Bus Operation Registers	Address Offset
Add-On Incoming Mailbox Register (AIMB)	0Ch
Add-On Outgoing Mailbox Register (AOMB)	1Ch
Add-On Pass-Thru Address Register (APTA)	28h
Add-On Pass-Thru Data Register (APTD)	2Ch
Add-On Maibox Empty/Full Status Register (AMBEF	34h
Add-On Interrupt Control/Status Register (AINT)	38h
Add-On Reset Control Register (ARCR)	3Ch
Add-On Pass-Thru Configuration Register (APTCR)	60h

Table 3

Mailbox Operation

The mailbox registers are divided into two 4 byte sets. Each set is dedicated to one bus for data transfer to the other bus. Figure 4 shows a block diagram of the mailbox section of the S5920. The provision of mailbox registers provides data or user defined command/status transfer capability between two busses. An empty/full indication for each mailbox register, at the byte level, is determined by polling a status register accessible to both the PCI and Add-On busses. Providing mailbox byte level full indications allows greater flexibility in 8, 16 or 32 bit designs; i.e., transferring a single byte on a 32-bit Add-On bus without requiring the assembly or disassembly of 32 bit data.

A mailbox byte level interrupt feature for PCI or Add-On busses is provided. Bit locations configured within the S5920 operation registers can select which mailbox byte is to generate an interrupt when the mailbox is written to. Interrupts can

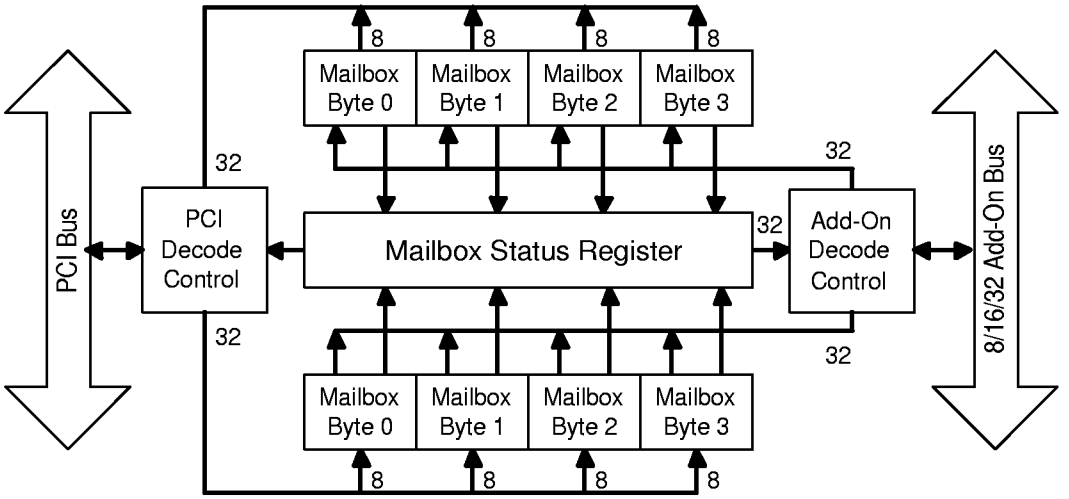


Figure 4

be generated to the PCI or Add-On buses. PCI Bus interrupts may also be generated from direct hardware interfacing due to a unique S5920 feature. The Add-On mailbox is hardware accessible via a set of dedicated device pins. A single load pulse latches data into the mailbox generating an interrupt, if enabled.

Pass-Thru Operation

Pass-Thru region accesses can execute PCI bus cycles in real time or through an internal FIFO. Real time operation allows the PCI bus to directly read or write to Add-On Bus resources. The S5920 allows the designer to declare up to four individual Pass-Thru regions. Each region may be defined as 8, 16 or 32 bits wide, mapped into memory or I/O system space and may be up to 512 MB in size. Figure 5 shows a block diagram of the S5920 Pass-Thru architecture.

Host communications to the Pass-Thru data channel utilizes dedicated Add-On Bus pins to signal that a PCI read or write

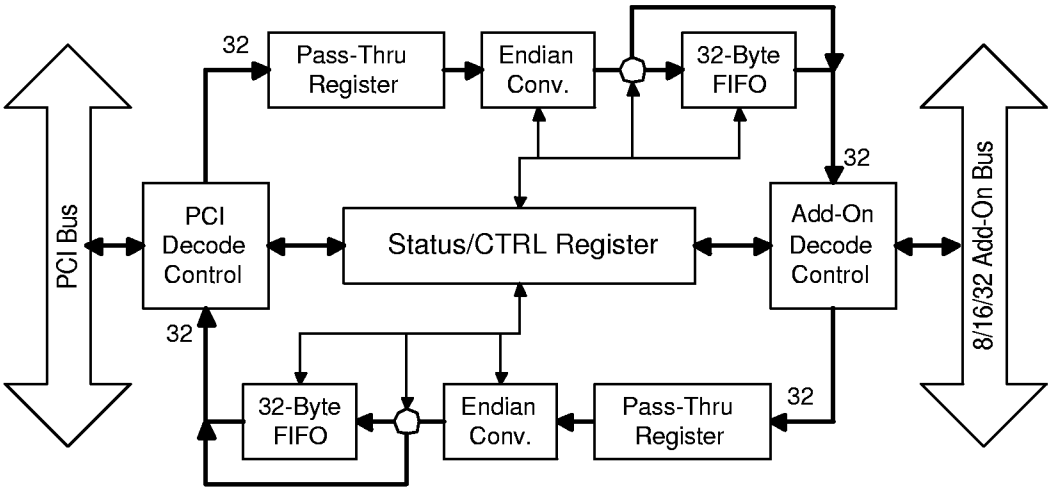


Figure 5

has been requested. User logic decodes these signals to determine if it must read or write data to the S5920 to satisfy the PCI request. Information decoded includes: PCI read/write transaction request, the byte lanes involved, the specific Pass-Thru region accessed and the request is a burst or single cycle access.

Pass-Thru operation supports single PCI data cycles and PCI data bursts. During PCI burst operations, the S5920 is capable of transferring data at the full PCI bandwidth. Should slower Add-On logic be implemented, the S5920 will issue a PCI bus retry until the requested transfer is completed.

To increase data throughput, the Pass-Thru channel incorporates two 32 byte FIFOs. One FIFO is dedicated to PCI read data while the other is dedicated to PCI write data. Enabling the write FIFO allows the S5920 to accept zero wait state bursts from the PCI bus regardless of the Add-On bus application design speed.

Enabling the read FIFO allows data to be optionally prefetched from the Add-On Bus. This can greatly improve performance of slow Add-On bus designs. PCI read cycles can be performed with zero wait states since data has been prefetched into the FIFO. Either of the write/read FIFOs can be disabled or enabled to tune system performance.

The Add-On bus can be operated in two different modes: active or passive. The passive mode of operation mimics that of the S5933 Add-On bus operation. The user design drives S5920 pins to read or write data. In active mode, the Add-On Bus is driven from an S5920 internal state machine. This reduces component count in cost sensitive designs. Active mode also incorporates programmable wait states from 0 to 7.

S5920 PIN DESCRIPTIONS

AD[31:0] t/s *Address/Data.* Address and data are multiplexed on the same PCI bus pins. A PCI Bus transaction consists of an address phase followed by one or more data phases. An address phase occurs on the PCLK cycle in which FRAME# is asserted. A data phase occurs on the PCLK cycles in which IRDY# and TRDY# are both asserted.

C/BE[3:0]# in *Command/Byte Enable.* Bus commands and byte enables are multiplexed on the same pins. These pins define the current bus command during an address phase. During a data phase, these pins are used as Byte Enables, with C/BE[0]# enabling byte 0 (LSB) and C/BE[3]# enabling byte 3 (MSB).

C/BE# [3	2	1	0]	Description
0	0	0	0	Interrupt Acknowledge
0	0	0	1	Special Cycle
0	0	1	0	I/O Read
0	0	1	1	I/O Write
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Memory Read
0	1	1	1	Memory Write
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Configuration Read
1	0	1	1	Configuration Write
1	1	0	0	Memory Read Multiple
1	1	0	1	Dual Address Cycle
1	1	1	0	Memory Read Line
1	1	1	1	Memory Write and Invalidate

PAR t/s *Parity.* Parity is always driven as even from all AD[31:0] and C/BE[3:0]# signals. The parity is valid during the clock following the address phase and is driven by the bus master. During a data phase for write transactions, the bus master sources this signal on the clock following IRDY# active; during a data phase for read transactions, this signal is driven by the target and is valid on the clock following TRDY# active. The PAR signal has the same timing as AD[31:0], delayed by one clock.

PCLK in *PCI Clock.* The rising edge of this signal is the reference upon which all other signals are based except for RST# and INTA#. The maximum PCLK frequency for the S5920 is 33 MHz and the minimum is DC (0 Hz).

RST# in *Reset* is used to bring the S5920 to a known state:
- All PCI Bus output signals tri-stated.
- All open drain signals (i.e. SERR#) floated.
- All registers set to their factory defaults.
- Pass-Thru is returned to an Idle state.
- All FIFOs emptied.

FRAME# in *Frame.* This signal is driven by the current bus master to indicate the beginning and duration of a bus transaction. When FRAME# is first asserted, it indicates a bus transaction is beginning with a valid addresses and bus command present on AD[31:0] and C/BE[3:0]. Data transfers continue while FRAME# is asserted. FRAME# de-assertion indicates the transaction is in a final data phase or has completed.

IRDY#	in	*Initiator Ready.* This signal is always driven by the bus master to indicate it's ability to complete the current data phase. During write transactions, it indicates AD[31:0] contains valid data.
TRDY#	s/t/s	*Target Ready.* This signal is driven by the selected target to indicate the target is able to complete the current data phase. During read transactions, it indicates AD[31:0] contains valid data. Wait states occur until both TRDY# and IRDY# are asserted together.
STOP#	s/t/s	*Stop.* The Stop signal is driven by a selected target and conveys a request to the bus master to stop the current transaction.
LOCK#	in	*Lock.* The lock signal provides for the exclusive use of a resource. The S5920 may be locked by one master at a time.
IDSEL	in	*Initialization Device Select.* This pin is used as a chip select during configuration read or write transactions.
DEVSEL#	s/t/s	*Device Select.* This signal is driven by a target decoding and recognizing its bus address. This signal informs a bus master whether an agent has decoded a current bus cycle.
INTA#	o/d	*Interrupt A.* This signal is defined as optional and level sensitive. Driving it low will interrupt to the host. The INTA# interrupt is to be used for any single function device requiring an interrupt capability.
PERR#	s/t/s	*Parity Error.* Only for reporting data parity errors for all bus transactions except for Special Cycles. It is driven by the agent receiving data two clock cycles after the parity was detected as an error. This signal is driven inactive (high) for one clock cycle prior to returning to the tri-state condition.
SERR#	o/d	*System Error.* Used to report address and data parity errors on Special Cycle commands and any other error condition having a catastrophic system impact. Special Cycle commands are not supported by the S5920.
SCL	o/d out	*Serial Clock.* This clock provides timing for all transactions on the two-wire serial bus. The S5920 drives this signal when performing as a serial bus master. SCL operates at the maximum allowable clock speed and enters the high Z state when FLT# is asserted or the serial bus is inactive.
SDA	o/d	*Serial Data/Address.* This bi-directional signal carries serial address and data information between nvRAMs and the S5920. This pin enters high Z state when FLT# is asserted or the serial bus is inactive.
MDMODE	in	*Mailbox Data Mode.* The MD[7:0] signal pins are always inputs when this signal is high. The MD[7:0] signal pins are defined as inputs and outputs under LOAD# control when MDMODE is low. This pin is provided for software compatibility with the S5933. New designs should permanently connect this signal low. This signal is connected to an internal pull-up.
LOAD#	in	MD[7:0] is defined as an input bus when this signal is low. The next rising edge of the ADCLK will latch MD[7:0] data into byte three of the Add-On outgoing mailbox. When LOAD# is high and MDMODE is low, MD[7:0] are defined as outputs displaying byte three of the PCI outgoing mailbox. This signal is connected to an internal pull-up.
MD[7:0]	t/s	*Mail Box Data Bus.* The mail box data registers can be directly accessed using the LOAD# and MDMODE signals. When configured as an input, data byte three of the PCI incoming mailbox is directly written to from these pins. When configured as an output, data byte three of the PCI outgoing mailbox is output to these pins. All MD[7:0] signals have an internal pull-up.

PTMODE in *Pass-Thru Mode*. Configures the Pass-Thru data channel operation. High configures the S5920 in Passive mode allowing other devices to read/write data bus data. Low configures the S5920 in Active mode. This mode allows the S5920 to actively drive signals and data onto the data bus. This signal is connected to an internal pull-up.

PTATN# out *Pass-Thru Attention*. Signals a decoded PCI to Pass-Thru region bus cycle. PTATN# is generated to signal Add-On logic Pass-Thru data must be read from or written to the S5920.

PTBURST# out *Pass-Thru Burst*. Informs the Add-On bus the current Pass-Thru region decoded PCI bus cycle is a burst access.

PTRDY#/WAIT# in *Pass-Thru Ready/Pass-Thru Wait*. During passive mode, the signal is referred to as PTRDY# and is asserted low to indicate Add-On logic has read/written data in response to a PTATN# signal. During active mode operation, the signal is referred to as WAIT# and can be driven high to insert wait states or hold the S5920 from clocking data onto the data bus. PTRDY# or WAIT# is synchronous to ADCLK. This signal is synchronous to ADCLK.

PTNUM[1:0] out *Pass-Thru Number*. Identifies which of the four Pass-Thru regions the PTATN# read/write is requesting. Only valid for the duration of PTATN# active. 00 = Base Address Register 1, 01 = Base Address Register 2, 10 = Base Address Register 3, 11 = Base Address Register 4.

PTBE[3:0]# out *Pass-Thru Byte Enables*. During a PCI to Pass-Thru read, Indicates which bytes of a DWORD is to be written into. During a PCI to Pass-Thru write, indicates which bytes of a DWORD are valid to read. PTBE[3:0]# are only valid while PTATN# is asserted.

PTADR# t/s *Pass-Thru Address*. Is an input when in passive mode. When asserted, the 32-bit Pass-Thru address register contents are driven onto the DQ[31:0] bus. All other Add-On control signals must be inactive during the assertion of PTADR# in passive mode. In active mode, becomes an output and indicates a Pass-Thru address is on the DQ bus. The DQMODE signal does not affect DQ bus width while the Pass-Thru address is driven.

PTWR out *Pass-Thru Write*. This signal indicates the current PCI to Pass-Thru bus transaction is a read or write cycle. Valid only when PTATN# is active.

DXFER# out *Data Transfer*. ACTIVE Transfer complete. When in ACTIVE mode, this output is asserted at the end of every 8, 16 or 32 bits data transfer cycle. This signal is not used in passive mode.

DQ[31:0] t/s *Address/Data Bus*. The 32 bit Add-On data bus. The DQMODE signal configures the bus width for either 32 or 16 bits. All DQ[31:0] signals have an internal pull-up.

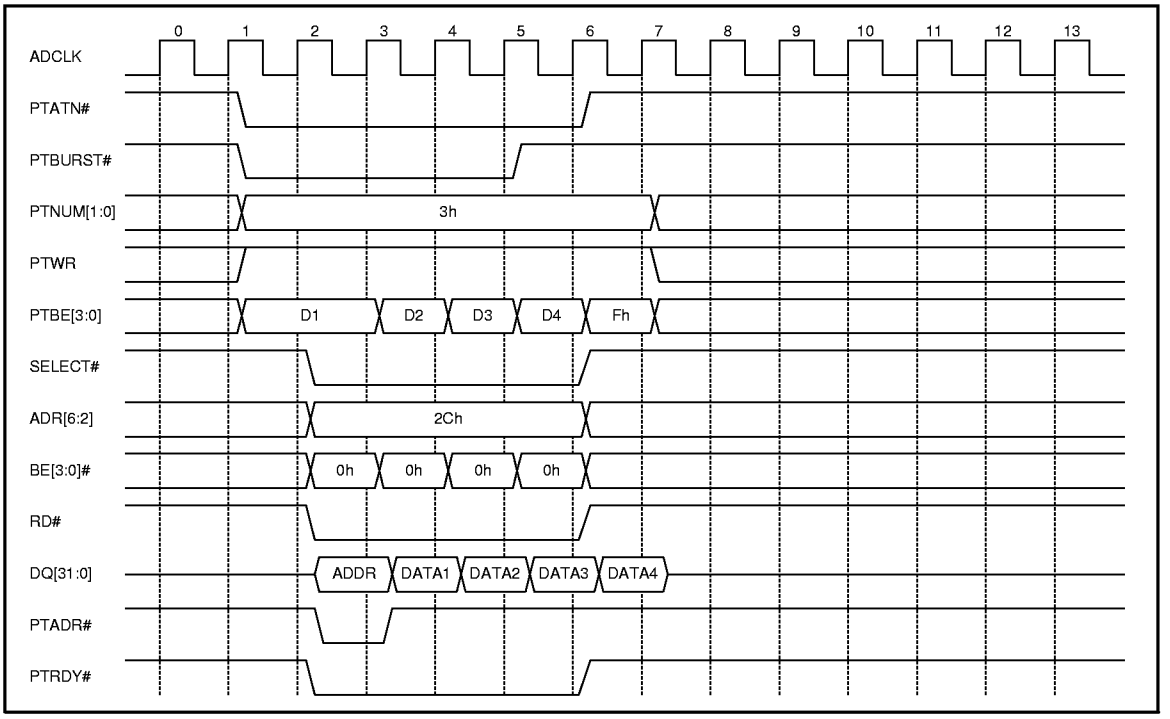
ADR{6:2} in Address [6:2]. These inputs select which S5920 register is to be read from or written to. To be used in conjunction with SELECT#, BE[3:0]# and WR# or RD#. The following table shows the register addresses.

ADR [6	5	4	3	2]	Description
0	0	0	1	1	Add-On Incoming Mailbox Register
0	0	1	1	1	Add-On Outgoing Mailbox Register
0	1	0	1	0	Add-On Pass-Thru Address Register
0	1	0	1	1	Add-On Pass-Thru Data Register
0	1	1	0	1	Add-On Mailbox Status Register
0	1	1	1	0	Add-On Interrupt Control Register
0	1	1	1	1	Add-On Reset Control Register
1	0	0	0	0	Pass-Thru/FIFO Configuration Register

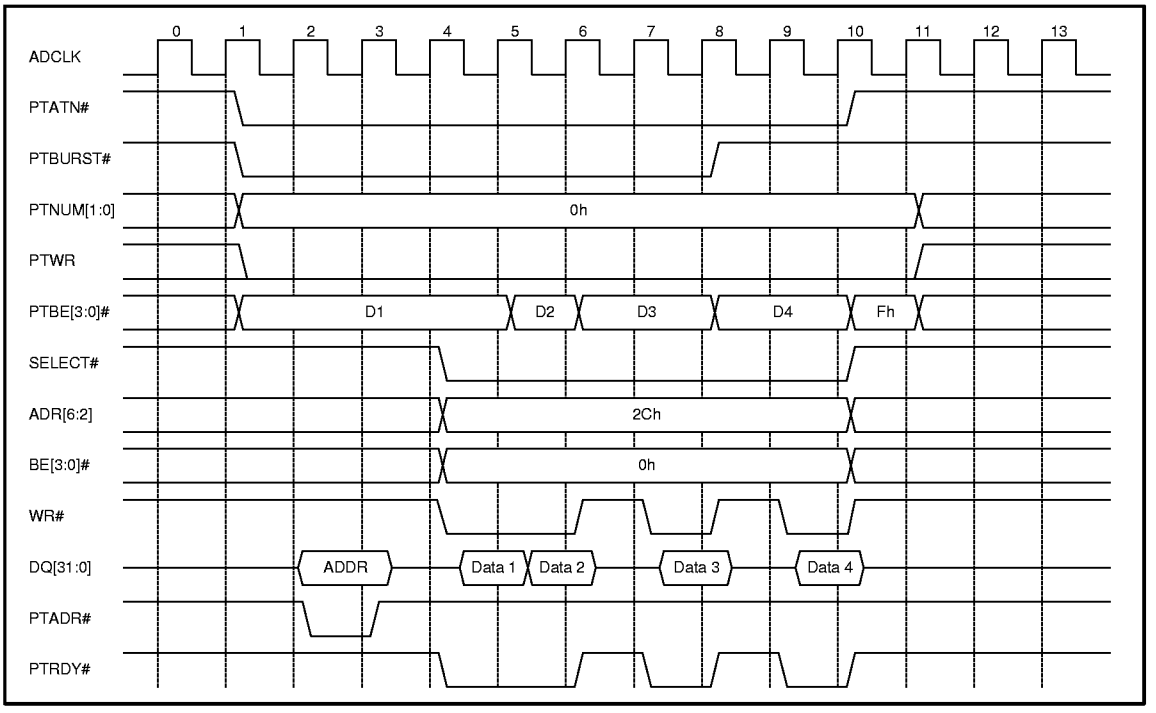
BE[2:0]#	in	*Byte Enable [2:0].* Provides individual read/write byte enabling during register read or write transactions. BE2# enables activity over DQ[23:16], BE1# enables DQ[15:8], and BE0# enables DQ[7:0]. During read transactions, enables the output driver for each byte lane; for write transactions, serves as an input enable to perform the write to each byte lane.
BE3#/ADR1	in	*Byte Enable 3/Address 1.* 32-bit bus width/16-bit bus width. BE3#, enables DQ[31:24] input drivers for writing data to registers identified by ADR[6:2] and enables DQ[31:24] output drivers to read registers identified by ADR[6:2]. To be used in conjunction with SELECT# and RD# or WR#. ADR1, selects the upper or lower WORD of a DWORD when a 16 bit wide bus is selected. 1 = lower, 0 = upper.
SELECT#	in	*Select.* Enables internal S5920 logic to decode WR#, RD# and ADR[6:2] when reading or writing to any Add-On register.
WR#	in	*Write Enable.* Asserting this signal writes DQ bus data byte(s) selected by BE[3:0]# into the S5920 register defined by SELECT# and ADR[6:2].
RD#	in	*Read Enable.* Asserting this signal drives data byte(s) selected by BE[3:0]# from the S5920 register defined by SELECT# and ADR[6:2] onto the DQ bus.
DQMODE	in	*DQ Mode.* Defines the DQ bus width when accessing data using WR#, RD#, SELECT# and ADR[6:2]#. Low = 32-bit wide DQ bus. High = 16-bit wide DQ bus. When high, the signal BE3# is re-assigned to the ADR1 signal and only DQ[15:0] is active.
SYSRST#	out	*System Reset.* An active-low buffered PCI bus RST# output signal. The signal is asynchronous and can be asserted through software from the PCI host interface.
BPCLK	out	*Buffered PCI Clock.* This output is a buffered form of the PCI bus clock and has all of the behavioral characteristics of the PCI clock (i.e., DC-to-33 MHz capability).
ADCLK	in	*Add-On Clock.* All internal S5920 Add-On bus logic is synchronous to this clock. The clock is asynchronous to the PCI bus logic unless connected to the BPCLK signal.
IRQ#	out	*Interrupt Request.* This output signals Add-On logic a significant event has occurred as a result of activity within the S5920.
ADDINT#	in	*Add-On Interrupt.* When enabled and asserted, this input will cause a PCI bus interrupt by driving INTA# low. The input is level sensitive and can be driven by multiple sources. This signal is connected to an internal pull-up.
FLT#	in	*Float.* Floats all S5920 output signals when asserted. This signal is connected to an internal pull-up.

TIMING DIAGRAMS

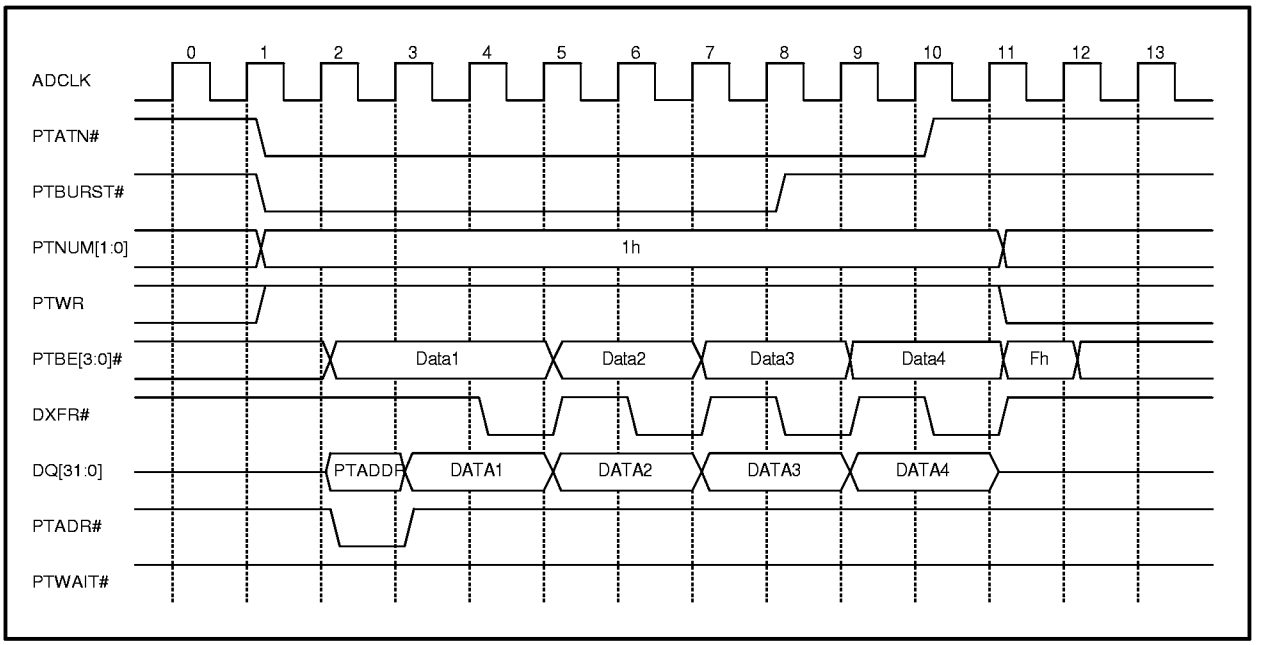
PCI to Add-On Passive Burst Write



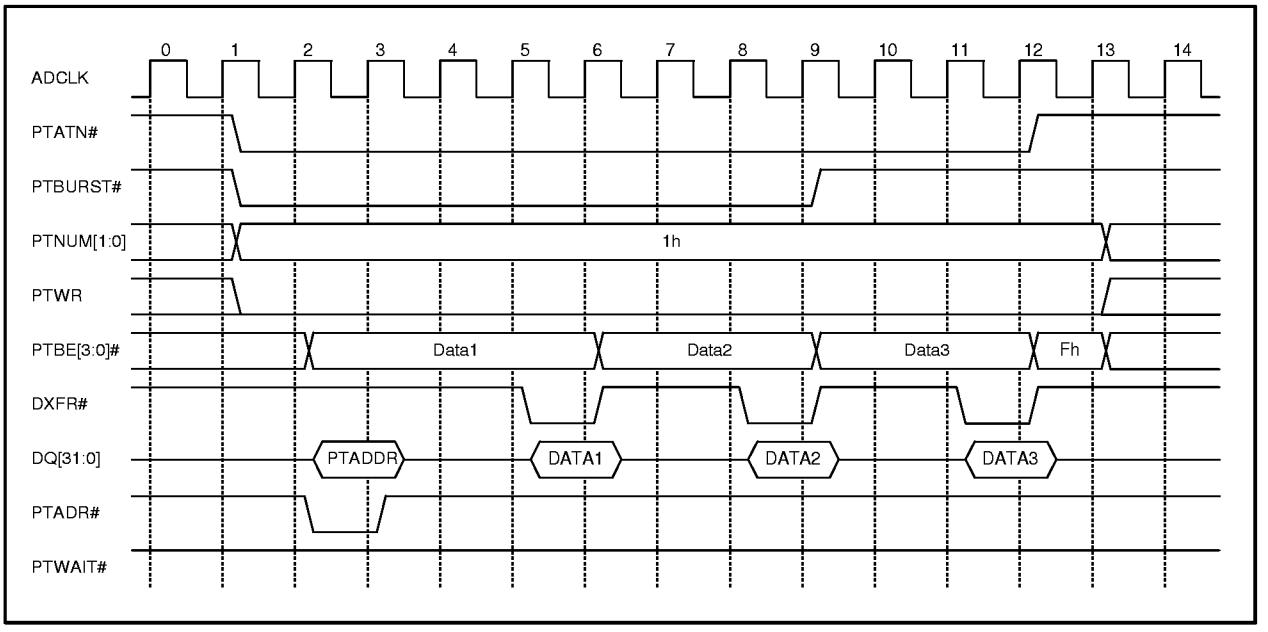
PCI to Add-On Passive Burst Read



Active Mode PCI Write Showing a One Wait State Programmed Delay



Active Mode PCI Write Showing a One Wait State Programmed Delay



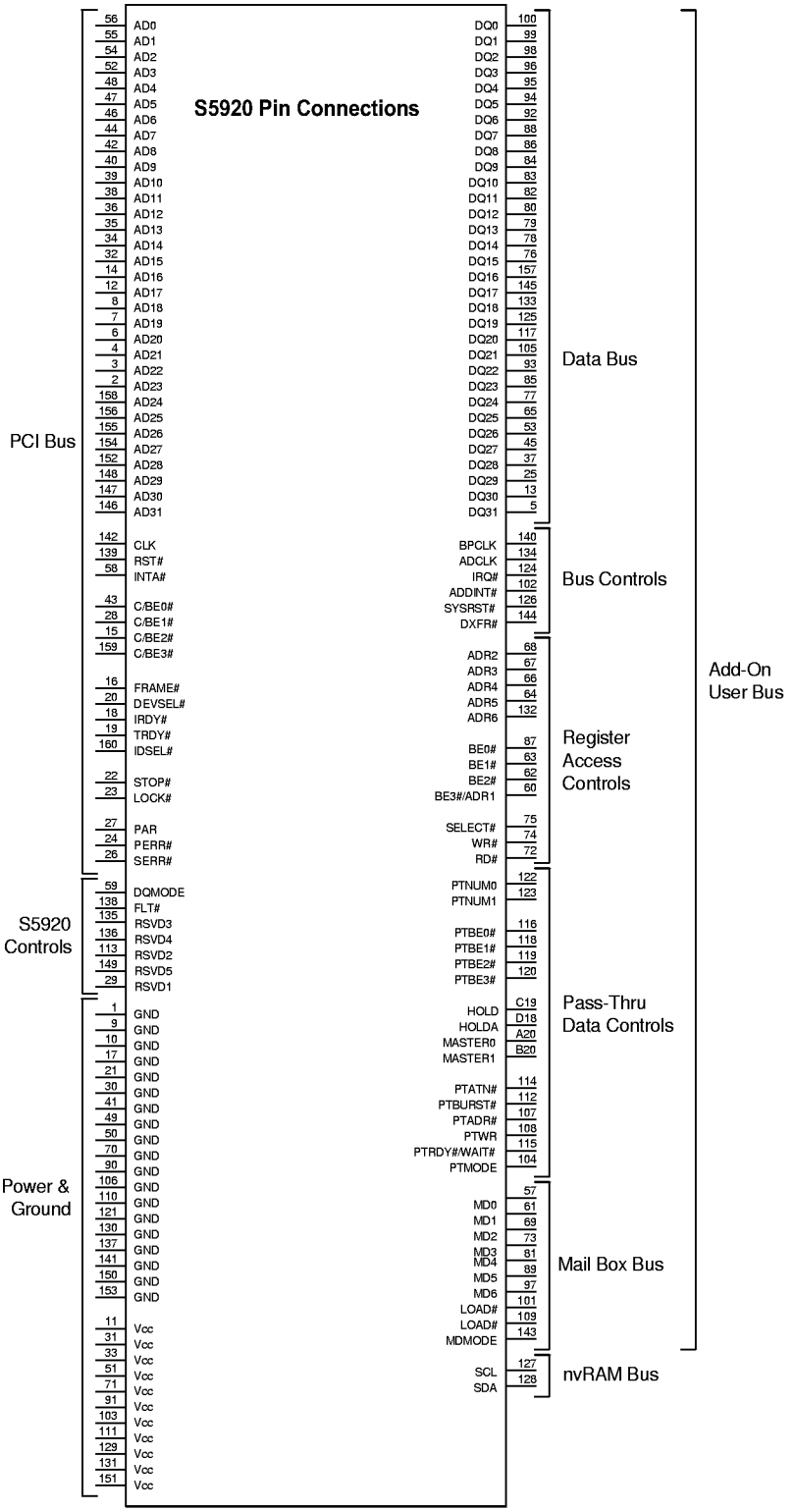
ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range (V_{CC} Core) . . . . . -0.3 V to 7.0 V
Input Pin Voltage Range . . . . . -0.5 V to VCC + 0.5 V
Storage Temperature Range. . . . . -55 to 125 °C
Operating Ambient Temperature Range . . . . . .0 to 70 °C
Virtual Junction Temperature. . . . . 150 °C
Soldering Lead Temperature . . . . . 300 °C 10 Seconds

⊗ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to this device. These are stress ratings only.

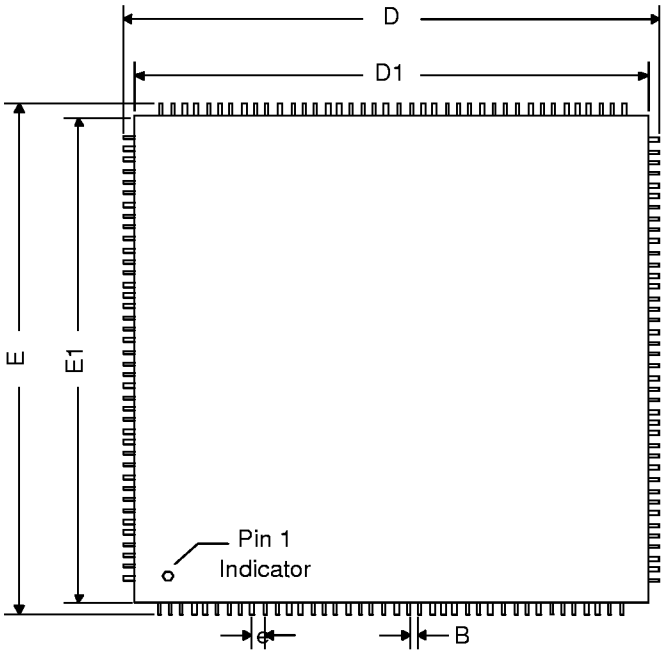
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	NOM	Max	Units	Test Conditions
V_{CC}	PCI Supply Voltage (core)	4.75		5.25	Volts	To PCI Spec 2.2
V_{ih}	High Level Input Voltage	2.0	-	V_{CC}	Volts	
V_{il}	Low Level Input Voltage	-0.5	-	0.8	Volts	
V_{oh}	High Level Output Voltage	2.4	-	-	Volts	I_{oh} = TBD
V_{ol}	Low Level Output Voltage	-	-	0.4	Volts	I_{ol} = TBD
I_{cc}	Supply Current (Static)	-		49	mA	
I_{cc}	Supply Current (Dynamic)	-		197	mA	@33 MHz
T_c	PCLK Cycle Time	25			ns	
T_w	PCLK High/Low Time	10			ns	
T_r	Rise/Fall Time			2.5	ns	
T_a	Ambient Temperature	0	-	70	°C	
P_{DD}	Power Dissipation	0	TBD	TBD	Watts	
C_{in}	Input Pin Capacitance	-	-	10	pF	
C_{CLK}	CLK Pin Capacitance	5	-	12	pF	
C_{IDSEL}	IDSEL Pin Capacitance	-	-	8	pF	

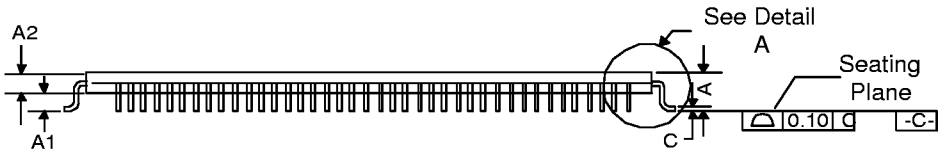

S5920 Pin Connections
PCI Bus
S5920 Controls
Power & Ground
Data Bus
Bus Controls
Register Access Controls
Pass-Thru Data Controls
Mail Box Bus
nvRAM Bus
Add-On User Bus
56 AD0
55 AD1
54 AD2
52 AD3
48 AD4
47 AD5
46 AD6
44 AD7
42 AD8
40 AD9
39 AD10
38 AD11
36 AD12
35 AD13
34 AD14
32 AD15
14 AD16
12 AD17
8 AD18
7 AD19
6 AD20
4 AD21
3 AD22
2 AD23
158 AD24
156 AD25
155 AD26
154 AD27
152 AD28
148 AD29
147 AD30
146 AD31
142 CLK
139 RST#
58 INTA#
43 C/BE0#
28 C/BE1#
15 C/BE2#
159 C/BE3#
16 FRAME#
20 DEVSEL#
18 IRDY#
19 TRDY#
160 IDSEL#
22 STOP#
23 LOCK#
27 PAR
24 PERR#
26 SERR#
59 DQMODE
138 FLT#
135 RSVD3
136 RSVD4
113 RSVD2
149 RSVD5
29 RSVD1
1 GND
9 GND
10 GND
17 GND
21 GND
30 GND
41 GND
49 GND
50 GND
70 GND
90 GND
106 GND
110 GND
121 GND
130 GND
137 GND
141 GND
150 GND
153 GND
11 Vcc
31 Vcc
33 Vcc
51 Vcc
71 Vcc
91 Vcc
103 Vcc
111 Vcc
129 Vcc
131 Vcc
151 Vcc
100 DQ0
99 DQ1
98 DQ2
96 DQ3
95 DQ4
94 DQ5
92 DQ6
88 DQ7
86 DQ8
84 DQ9
83 DQ10
82 DQ11
80 DQ12
79 DQ13
78 DQ14
76 DQ15
157 DQ16
145 DQ17
133 DQ18
125 DQ19
117 DQ20
105 DQ21
93 DQ22
85 DQ23
77 DQ24
65 DQ25
53 DQ26
45 DQ27
37 DQ28
25 DQ29
13 DQ30
5 DQ31
140 BPCLK
134 ADCLK
124 IRQ#
102 ADDINT#
126 SYSRST#
144 DXFR#
68 ADR2
67 ADR3
66 ADR4
64 ADR5
132 ADR6
87 BE0#
63 BE1#
62 BE2#
60 BE3#/ADR1
75 SELECT#
74 WR#
72 RD#
122 PTNUM0
123 PTNUM1
116 PTBE0#
118 PTBE1#
119 PTBE2#
120 PTBE3#
C19 HOLD
D18 HOLDA
A20 MASTER0
B20 MASTER1
114 PTATN#
112 PTBURST#
107 PTADR#
108 PTWR
115 PTRDY#/WAIT#
104 PTMODE
57 MD0
61 MD1
69 MD2
73 MD3
81 MD4
89 MD5
97 MD6
101 LOAD#
109 LOAD#
143 MDMODE
127 SCL
128 SDA

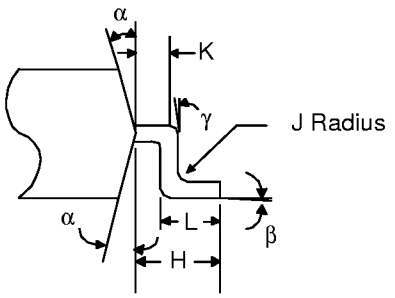
PACKAGE INFORMATION

160 PQFP



Symbol	MIN	NOM	MAX
A	-	-	4.07
A1	0.25	-	-
A2	3.17	-	-
D		31.90 BSC	
D1		28.00 BSC	
E		31.90 BSC	
E1		28.00 BSC	
L	0.65	0.80	1.03
e		0.65 BSC	
B	0.22	-	0.38
c	0.11	-	0.23
α	5	-	16
β	0	-	7
γ	0	-	-
G	0.13	-	-
H		1.95 BSC	
J	0.13	-	0.30
K	0.40	-	-
2H	-	3.9	-





Detail A

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