DATA SHEET

TDA8376; TDA8376A
I²C-bus controlled PAL/NTSC TV processors

Objective specification
File under Integrated Circuits, IC02

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1 FEATURES

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- Output signals of the video switch circuit for the teletext decoder and a Picture-In-Picture (PIP) processor
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- Integrated chrominance trap with pre-shoot compensation and bandpass filters (automatically calibrated)
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- Black stretcher circuit in the luminance channel
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- RGB control circuit with black-current stabilization and white point adjustment; to obtain a good grey scale tracking the black-current ratio of the 3 guns depends on the white point adjustment
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- Horizontal synchronization with two control loops and alignment-free horizontal oscillator
- Vertical count-down circuit
- Geometry correction by modulation of the vertical and E-W drive
- Vertical and horizontal zoom possibility for 16 : 9 applications (TDA8376A only)
- I²C-bus control of various functions
- Low dissipation (700 mW)
- Small amount of peripheral components compared with competition ICs
- Y, U and V inputs and outputs.

2 GENERAL DESCRIPTION

The TDA8376 and TDA8376A are alignment-free I²C-bus controlled video processors which contain a PAL/NTSC colour decoder, luminance processor, sync processor, RGB-control and deflection processor. The circuits have been designed for use with the baseband chrominance delay line TDA4665 and for DC-coupled vertical and East-West (E-W) output stages. Both ICs are pin compatible. The TDA8376A has a flexible horizontal and vertical zoom possibility for 16 : 9 applications.

The supply voltage for the ICs is 8 V. The ICs are available in an SDIP package with 52 pins and in a QFP package with 64 pins (see Chapter 4).

The pin numbers indicated in this document are referenced to the SDIP52; SOT247-1 package; unless otherwise indicated.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Supply					
V_P	supply voltage	–	8.0	–	V
I_P	supply current	–	75	–	mA
Input voltages					
$V_{9,13(p-p)}$	CVBS input voltage (peak-to-peak value)	–	1.0	–	V
$V_{27(p-p)}$	S-VHS luminance input voltage (peak-to-peak value)	–	1.0	–	V
$V_{6(p-p)}$	S-VHS chrominance input voltage (burst amplitude) (peak-to-peak value)	–	0.3	–	V
$V_{i(p-p)}$	RGB input voltage (peak-to-peak value)	–	0.7	–	V
Output voltages					
$V_{38(p-p)}$	TXT output voltage (peak-to-peak value)	–	1.0	–	V
$V_{11(p-p)}$	PIP output voltage (peak-to-peak value)	–	1.0	–	V
$V_{30(p-p)}$	–(R–Y) output voltage (peak-to-peak value)	–	525	–	mV
$V_{29(p-p)}$	–(B–Y) output voltage (peak-to-peak value)	–	675	–	mV
$V_{19,20,21(p-p)}$	RGB output signal voltage amplitudes (peak-to-peak value)	–	2.0	–	V
Output currents					
I_{40}	horizontal output current	10	–	–	mA
$I_{47,48}$	vertical output current	1	–	–	mA
I_{46}	E-W drive output current	0.5	–	–	mA

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8376	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1
TDA8376AH	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body $14 \times 20 \times 2.8$ mm	SOT319-2

5 BLOCK DIAGRAM

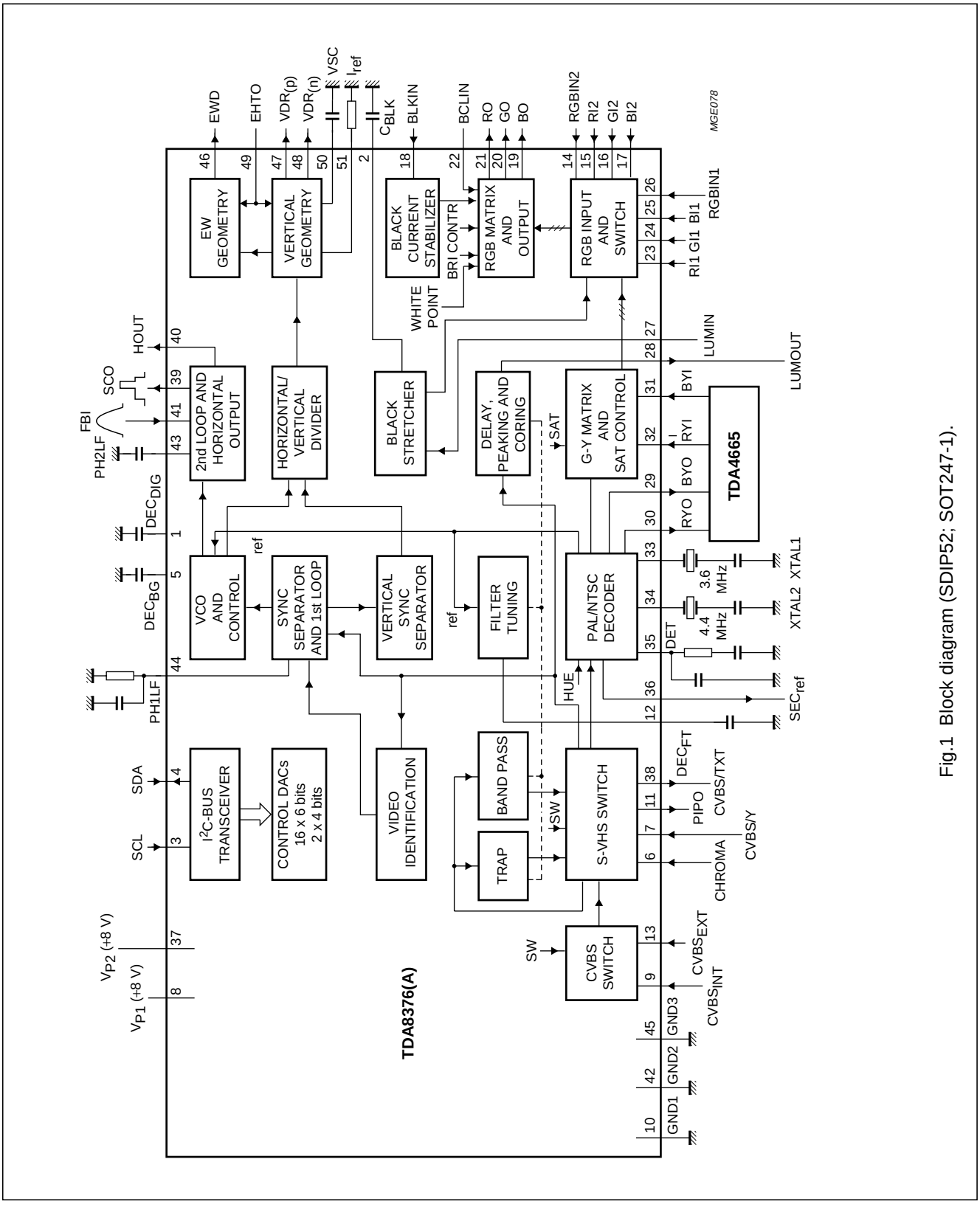


Fig.1 Block diagram (SDIP52; SOT247-1).

6 PINNING

SYMBOL	PIN		DESCRIPTION
	SDIP52	QFP64	
DEC_{DIG}	1	11	decoupling digital supply
C_{BLK}	2	12	black peak hold capacitor
SCL	3	13	I²C-bus serial clock input
SDA	4	14	I²C-bus serial data input/output
DEC_{BG}	5	16	band gap decoupling
CHROMA	6	17	chrominance input (S-VHS)
CVBS/Y	7	18	external CVBS/Y input
V_{P1}	8	20	main supply voltage (+8 V)
$CVBS_{INT}$	9	22	internal CVBS input
GND1	10	23	ground 1
PIPO	11	25	picture-in-picture output
DEC_{FT}	12	26	decoupling filter tuning
$CVBS_{EXT}$	13	27	external CVBS input
RGBIN2	14	28	RGB insertion input 2
RI2	15	29	red input 2
GI2	16	30	green input 2
BI2	17	31	blue input 2
BLKIN	18	32	black-current input
BO	19	34	blue output
GO	20	35	green output
RO	21	36	red output
BCLIN	22	37	beam current limiter input
RI1	23	38	red input 1
GI1	24	39	green input 1
BI1	25	40	blue input 1
RGBIN1	26	41	RGB insertion input 1
LUMIN	27	42	luminance input
LUMOUT	28	43	luminance output
BYO	29	44	–(B–Y) signal output
RYO	30	45	–(R–Y) signal output
BYI	31	46	–(B–Y) signal input
RYI	32	47	–(R–Y) signal input
XTAL1	33	49	3.58 MHz crystal connection
XTAL2	34	51	4.43/3.58 MHz crystal connection
DET	35	53	loop filter phase detector
SEC_{ref}	36	54	SECAM reference output
V_{P2}	37	55	horizontal oscillator supply voltage (+8 V)
CVBS/TXT	38	56	CVBS/TXT output

SYMBOL	PIN		DESCRIPTION
	SDIP52	QFP64	
SCO	39	57	sandcastle output
HOUT	40	58	horizontal output
FBI	41	59	flyback input
GND2	42	24	ground 2
PH2LF	43	62	phase-2 filter
PH1LF	44	63	phase-1 filter
GND3	45	60	ground 3
EWD	46	1	east-west drive output
$VDR_{(p)}$	47	3	vertical drive 1 positive output
$VDR_{(n)}$	48	4	vertical drive 2 negative output
EHTO	49	5	EHT/overvoltage protection input
VSC	50	7	vertical sawtooth capacitor
I_{ref}	51	8	reference current input
n.c.	52	2	not connected
n.c.	–	6	not connected
n.c.	–	9	not connected
n.c.	–	10	not connected
n.c.	–	15	not connected
n.c.	–	19	not connected
n.c.	–	33	not connected
n.c.	–	48	not connected
n.c.	–	50	not connected
n.c.	–	52	not connected
V_{P3}	–	21	supply voltage 3 (+8 V)
GND4	–	61	ground 4
GND5	–	64	ground 5

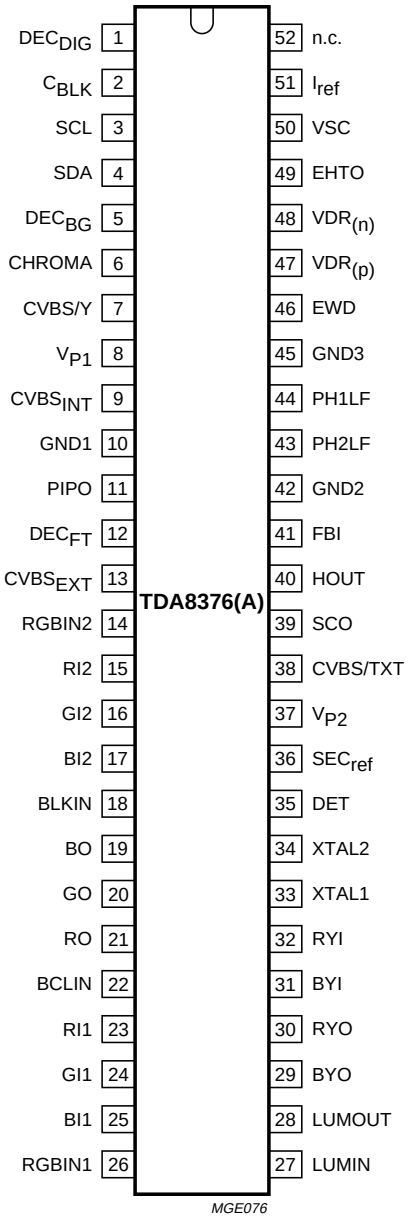


Fig.2 Pin configuration (SDIP52).

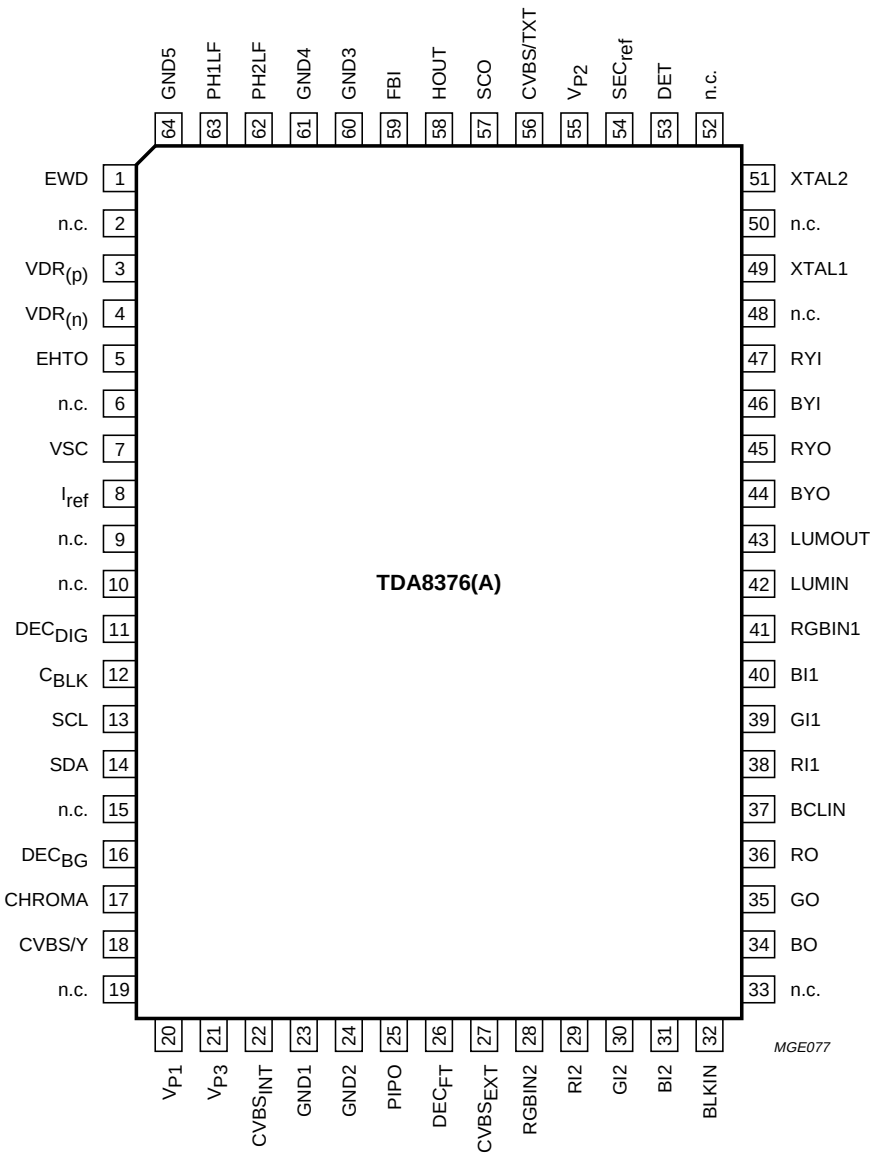


Fig.3 Pin configuration (QFP64).

7 FUNCTIONAL DESCRIPTION

7.1 Video switches

The circuit has two CVBS inputs and a Super-Video Home System (S-VHS) input. The input can be chosen by the I²C-bus. The input selector also has a position in which $CVBS_{EXT}$ is processed, unless there is a signal on the S-VHS input. When the input selector is in this position it switches to the S-VHS input if the S-VHS detector detects sync pulses on the S-VHS luminance input. The S-VHS detector output can be read by the I²C-bus. When the S-VHS option is not used the luminance input can be used as a second input for external CVBS signals. The choice is made via the CVS bit (see Table 1).

The video switch circuit has two outputs which can be programmed in a different way. The input signal for the decoder is also available on the TXT output. Therefore this signal can be used to drive the teletext decoder and the SECAM add-on decoder. The signal on the PIP output can be chosen independent of the TXT output. If S-VHS is selected for one of the outputs the luminance and chrominance signals are added so that a CVBS signal is obtained again.

The circuit contains a video identification circuit which checks whether a video signal is available at the selected video input. This circuit is independent of the synchronization circuit. The information of this identification circuit can also be used to switch the phase-1 (φ_1) loop to a low gain when no signal is received so that a stable OSD display is obtained. The video identification circuit can be switched on and off via the I²C-bus.

7.2 Integrated video filters, peaking and black stretcher

The circuit contains a chrominance bandpass and trap circuit. The chrominance trap filter in the luminance path is designed for a symmetrical step response behaviour. The filters are realized by gyrator circuits and they are automatically tuned by comparing the tuning frequency with the crystal frequency of the decoder. The luminance delay line and the delay for the peaking circuit are also realized by gyrator circuits. During SECAM reception the centre frequency of the chrominance trap is set to a value of approximately 4.2 MHz to obtain a better suppression of the SECAM carrier frequencies.

The peaking function is achieved by two luminance delay cells each with a delay of 165 ns. The resulting peaking frequency is 3 MHz. The peaking is asymmetrical so that the overshoots in the direction of ‘black’ are approximately two times higher than those in the direction of ‘white’. This provides a better picture impression than a symmetrical peaking. The circuit contains a coring circuit to prevent the noise content of the video signal being amplified by the peaking circuit. This coring circuit can be switched-off when required.

It is possible to connect a Colour Transient Improvement (CTI) or Picture Signal Improvement (PSI) IC to the TDA8376. The luminance signal which has passed the filter and delay line circuit is available externally. The output signal of the transient improvement circuit must be applied to the luminance input circuit. When the CTI function is not required the two pins must be AC-coupled.

The luminance signal below 50 IRE can be stretched in accordance with the difference between the peak black level and the blanking level of the back-porch of the video signal. The black level stretcher can be switched-off by connecting pin 2 to the positive supply line.

7.3 Synchronization circuit

The sync separator is preceded by a controlled amplifier which adjusts the sync pulse amplitude to a fixed level. These pulses are fed to the slicing stage which is operating at 50% of the amplitude.

The separated sync pulses are fed to the first phase detector and to the coincidence detector. This coincidence detector is only used to detect whether the line oscillator is synchronized and not for transmitter identification. The first Phase-Locked Loop (PLL) has a very high-statical steepness so that the phase of the picture is independent of the line frequency. To prevent the horizontal synchronization being disturbed by anti-copy signals such as Macrovision the phase detector is gated during the vertical retrace period so that pulses during scan have no effect on the output voltage. The position of this pulse is asymmetrical and the width is approximately 22 μs.

The horizontal output signal is generated by an oscillator which operates at twice the line frequency. Its frequency is divided-by-two to lock the first control loop to the incoming signal. The time-constant of the loop can be forced by the I²C-bus (fast or slow). If required the IC can select the time-constant depending on the noise content of the incoming video signal. The free-running frequency of the oscillator is determined by a digital control circuit which is locked to the reference signal of the colour decoder. When the IC is switched on the horizontal output signal is suppressed and the oscillator is calibrated as soon as all subaddress bytes have been sent. When the frequency of the oscillator is correct the horizontal drive signal is switched on.

To obtain a smooth switching-on and switching-off behaviour of the horizontal output stage the horizontal output frequency is doubled during switch-on and switch-off (slow start/stop). During that time the duty factor of the output pulse has such a value that maximum safety is obtained for the output stage

To protect the horizontal output transistor the horizontal drive is switched off when a power-on reset is detected. The drive signal is switched on again when the normal switch-on procedure is followed, i.e. all sub-address bytes must be sent and, after calibration, the horizontal drive signal will be released again via the slow start procedure.

When the coincidence detector indicates an out-of-lock situation the calibration procedure is repeated.

The circuit has a second control loop to generate the drive pulses for the horizontal driver stage. To prevent the horizontal output transistor being switched on during flyback the horizontal drive output is gated with the flyback pulse.

The vertical sawtooth generator drives the vertical output and E-W correction drive circuits. The geometry processing circuits provide control of horizontal shift, E-W width, E-W parabola/width ratio, E-W corner/parabola ratio, trapezium correction, vertical shift, vertical slope, vertical amplitude, and the S-correction. All these controls can be set via the I²C-bus. The geometry processor has a differential current output for the vertical drive signal and a single-ended output for the E-W drive. Both the vertical drive and the E-W drive outputs can be modulated for EHT compensation. The EHT compensation pin is also used for overvoltage protection.

The TDA8376A geometry processor also offers the possibility for a flexible vertical and horizontal zoom mode for 16 : 9 applications. Because of this feature an additional control can be added on the remote control so that the viewer can adjust the picture.

In addition the de-interlace of the vertical output can be set via the I²C-bus.

To avoid damage of the picture tube when the vertical deflection fails, the guard output current of the TDA8350 can be supplied to the sandcastle output. When a failure is detected the RGB-outputs are blanked and a bit is set (NDF) in the status byte of the I²C-bus. When no vertical deflection output stage is connected this guard circuit will also blank the output signals. This can be overruled by the EVG bit of subaddress 0A (see Table 1).

7.4 Colour decoder

The colour decoder contains an alignment-free crystal oscillator, a killer circuit and the colour difference demodulators. The 90° phase shift for the reference signal is made internally. The demodulation angle and gain ratio for the colour difference signals for PAL and NTSC are adapted to the standard.

The colour decoder is very flexible. Together with the SECAM decoder TDA8395 an automatic multistandard decoder can be designed. In the automatic mode the SECAM identification is accepted only when the vertical frequency is 50 Hz. In the forced mode the system can also identify signals with a vertical frequency of 60 Hz.

Which standard the IC can decode depends on the external crystals. If a 4.4 MHz and a 3.5 MHz crystal are used PAL 4.4, NTSC 4.4, NTSC 3.5 and PAL 3.5 can be decoded. If two 3.5 MHz crystals are used PAL N and M can be decoded. If one crystal is connected only PAL/NTSC 4.4 or PAL/NTSC 3.5 can be decoded. The crystal frequency of the decoder is used to tune the line oscillator. Therefore the value of the crystal frequency must be given to the IC via the I²C-bus. For a reliable calibration of the horizontal oscillator it is very important that the crystal indication bits (XA and XB) are not corrupted (see Table 6). For this reason the crystal bits (SXA and SXB) can be read in the output bytes so that the software can check the I²C-bus transmissions (see Table 38).

7.5 RGB output circuit and black-current stabilization

The colour-difference signals are matrixed with the luminance signal to obtain the RGB-signals. For the RGB-inputs linear amplifiers have been chosen so that the circuit is suited for signals coming from the SCART connector. The RGB2 inputs (pins 14 to 17) have priority over the RGB1 inputs (pins 23 to 26). Both fast blanking inputs can be blocked by I²C-bus controls. The contrast and brightness controls operate on internal and external signals.

The output signal has an amplitude of approximately 2 V black-to-white at nominal input signals and nominal settings of the controls.

The black current stabilization is realized by feedback from the video output amplifiers to the RGB control circuit. The 'black current' of the 3 guns of the picture tube is internally measured and stabilized. The black level control is active during 4 lines at the end of the vertical blanking. During the first line the leakage current is measured and the following 3 lines the 3 guns are adjusted to the required level. The maximum acceptable leakage current is ±100 μA.

The nominal value of the 'black current' is 10 μA. The ratio of the currents for the various guns automatically tracks with the white point adjustment so that the background colour is the same as the adjusted white point.

The input impedance of the 'black-current' measuring pin is 15 kΩ. Therefore the beam current during scan will cause the input voltage to exceed the supply voltage. The internal protection will start conducting so that the excessive current is bypassed.

When the TV receiver is switched on the black current stabilization circuit is not active, the RGB outputs are blanked and beam current limiting input pin is short-circuited. Only during the measuring lines will the outputs supply a voltage of 5 V to the video output stage so that it can be detected if the picture tube is warming up. These pulses are switched on after a waiting time of approximately 0.5 s. This ensures that the vertical deflection is activated so that the measuring pulses are not visible on the screen. As soon as the current supplied to the measuring input exceeds a value of 190 μA the stabilization circuit is activated. After a waiting time of approximately 0.8 s the blanking and the beam current limiting input pin are released. The remaining switch-on behaviour of the picture is determined by the external time constant of the beam current limiting network.

8 I²C-BUS SPECIFICATION

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	0	0	0	1	0	1	1/0

MLA743

Fig.4 Slave address (8A).

Valid subaddresses: 00 to 13 (TDA8376) or 00 to 16 (TDA8376A); subaddress FE is reserved for test purposes. Auto-increment mode is available for subaddresses.

8.1 Start-up procedure

Read the status bytes until POR = 0 and send all subaddress bytes. The horizontal output signal is switched on when the oscillator is calibrated.

Each time before the data in the IC is refreshed, the status bytes must be read. If POR = 1, the procedure previously mentioned must be carried out to restart the IC.

When this procedure is not followed the horizontal frequency may be incorrect after power-up or after a power dip.

8.2 Inputs

Table 1 Input status bits

FUNCTION	SUBADDRESS (HEX)	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Source select	00	INA	INB	INC	IND	FOA	FOB	XA	XB
Decoder mode	01	FORF	FORS	DL	STB	POC	CM2	CM1	CM0
Hue	02	0	0	A5	A4	A3	A2	A1	A0
Horizontal shift (HS)	03	0	0	A5	A4	A3	A2	A1	A0
E-W width (E-W)	04	0	0	A5	A4	A3	A2	A1	A0
E-W parabola/width (PW)	05	0	0	A5	A4	A3	A2	A1	A0
E-W corner parabola (CP)	06	0	0	A5	A4	A3	A2	A1	A0
E-W trapezium (TC)	07	0	0	A5	A4	A3	A2	A1	A0
Vertical slope (VS)	08	NCIN	0	A5	A4	A3	A2	A1	A0
Vertical amplitude (VA)	09	VID	LBM	A5	A4	A3	A2	A1	A0
S-correction (SC)	0A	HCO	EVG	A5	A4	A3	A2	A1	A0
Vertical shift (VSH)	0B	SBL	PRD	A5	A4	A3	A2	A1	A0
White point R	0C	EXP(1)	CL(1)	A5	A4	A3	A2	A1	A0
White point G	0D	0	CVS	A5	A4	A3	A2	A1	A0
White point B	0E	MAT	0	A5	A4	A3	A2	A1	A0
Peaking	0F	YD3	YD2	YD1	YD0	A3	A2	A1	A0
Brightness	10	RBL	COR	A5	A4	A3	A2	A1	A0
Saturation	11	IE1	IE2	A5	A4	A3	A2	A1	A0
Contrast	12	0	0	A5	A4	A3	A2	A1	A0
Spare	13	0	0	0	0	0	0	0	0
Spare	14	0	0	0	0	0	0	0	0
Spare	15	0	0	0	0	0	0	0	0
Vertical zoom (VX, 76A)	16	0	0	A5	A4	A3	A2	A1	A0

Note

1. The bits EXP and CL in subaddress 0C are only valid for the TDA8376. For the TDA8376A these two bits must be set to logic 0.

Table 2 Output status bits

FUNCTION	SUBADDRESS (HEX)	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Output status bytes	00	POR	FSI	STS	SL	XPR	CD2	CD1	CD0
	01	NDF	IN1	IN2	IFI	AFA	X(1)	SXA	SXB

Note

1. X = don’t care.

8.2.1 INPUT CONTROL BITS

Table 3 Source select 1

INA	INB	DECODER AND TXT
0	0	$CVBS_{INT}$
0	1	$CVBS_{EXT}$
1	0	S-VHS
1	1	S-VHS ($CVBS_{EXT}$)

Table 4 Source select 2

INC	IND	PIP
0	0	$CVBS_{INT}$
0	1	$CVBS_{EXT}$
1	0	S-VHS
1	1	S-VHS ($CVBS_{EXT}$)

Table 5 Phase 1 (φ_1) time constant

FOA	FOB	MODE
0	0	normal
0	1	slow
1	X(1)	fast

Note

1. X = don't care.

Table 6 Crystal indication XA and XB

XA	XB	CRYSTAL
0	0	two 3.6 MHz
0	1	one 3.6 MHz (pin 33)
1	0	one 4.4 MHz (pin 34)
1	1	3.6 MHz (pin 33) and 4.4 MHz (pin 34)

Table 7 Forced field frequency

FORF	FORS	FIELD FREQUENCY
0	0	auto (60 Hz when line not synchronized)
0	1	60 Hz; note 1
1	0	50 Hz; note 1
1	1	auto (50 Hz when line not synchronized)

Note

1. When the forced mode is selected the divider will only switch to that position when the horizontal oscillator is not synchronized.

Table 8 Interlace

DL	STATUS
0	interlace
1	de-interlace

Table 9 Standby

STB	MODE
0	standby
1	normal

Table 10 Synchronization mode

POC	MODE
0	active
1	not active

Table 11 Colour decoder mode

CM2	CM1	CM0	DECODER MODE
0	0	0	not forced, own intelligence
0	0	1	forced NTSC 3.6 MHz
0	1	0	forced PAL 4.4 MHz
0	1	1	forced SECAM
1	0	0	forced NTSC 4.4 MHz
1	0	1	forced PAL 3.6 MHz (pin 33)
1	1	0	forced PAL 3.6 MHz (pin 34)
1	1	1	no function

Table 12 Vertical divider mode

NCIN	VERTICAL DIVIDER MODE
0	normal operation
1	switched to search window

Table 13 Video identification mode

VID	VIDEO IDENTIFICATION MODE
0	φ_1 loop switched on and off
1	not active

Table 14 Long blanking mode

LBM	BLANKING MODE
0	adapted to standard (50 or 60 Hz)
1	fixed in accordance with 50 Hz standard

Table 15 EHT tracking mode

HCO	TRACKING MODE
0	EHT tracking only on vertical
1	EHT tracking on vertical and E-W

Table 16 Enable vertical guard (RGB blanking)

EVG	VERTICAL GUARD MODE
0	not active
1	active

Table 17 Service blanking

SBL	SERVICE BLANKING MODE
0	off
1	on

Table 18 Overvoltage input mode

PRD	OVERVOLTAGE MODE
0	detection mode
1	protection mode

Table 19 Vertical deflection mode (TDA8376 only)

EXP	CL	VERTICAL DEFLECTION MODE
0	0	normal
0	1	compress
1	0	expand
1	1	expand and lift

Table 20 Condition Y/C input

CVS	Y-INPUT MODE
0	switched to Y/C mode
1	switched to CVBS mode

Table 21 PAL/NTSC matrix

MAT	MATRIX
0	adapted to standard
1	PAL

Table 22 Y-delay adjustment; note 1

YD0 to YD3	Y-DELAY
YD3	YD3 × 160 ns +
YD2	YD2 × 80 ns +
YD1	YD1 × 40 ns +
YD0	YD0 × 40 ns

Note

1. For an equal delay of the luminance and chrominance signal the delay must be set at a value of 160 ns. This is only valid for a CVBS signal without group delay distortions.

Table 23 RGB blanking

RBL	RGB BLANKING
0	not active
1	active

Table 24 Noise coring (peaking)

COR	NOISE CORING
0	off
1	on

Table 25 Enable fast blanking RGB1

IE1	FAST BLANKING
0	not active
1	active

Table 26 Enable fast blanking RGB2

IE2	FAST BLANKING
0	not active
1	active

8.2.2 Output control bits

Table 27 Power-on reset

POR	MODE
0	normal
1	power-down

Table 28 Field frequency indication

FSI	FREQUENCY
0	50 Hz
1	60 Hz

Table 29 S-VHS status

STS	S-VHS INPUT
0	no signal
1	signal

Table 30 Phase 1 (φ_1) lock indication

SL	INDICATION
0	not locked
1	locked

Table 31 X-ray protection

XPR	OVERVOLTAGE
0	no overvoltage detected
1	overvoltage detected

Table 32 Colour decoder mode

CD2	CD1	CD0	STANDARD
0	0	0	no colour standard identified
0	0	1	NTSC 3.6 MHz
0	1	0	PAL 4.4 MHz
0	1	1	SECAM
1	0	0	NTSC 4.4 MHz
1	0	1	PAL 3.6 MHz (pin 33)
1	1	0	PAL 3.6 MHz (pin 34)
1	1	1	spare

Table 33 Output vertical guard

NDF	VERTICAL OUTPUT STAGE
0	OK
1	failure

Table 34 Indication RGB1 insertion

IN1	RGB INSERTION
0	no (pin 26 LOW)
1	yes (pin 26 HIGH)

Table 35 Indication RGB2 insertion

IN2	RGB INSERTION
0	no (pin 14 LOW)
1	yes (pin 14 HIGH)

Table 36 Output video identification

IFI	VIDEO SIGNAL
0	no video signal identified
1	video signal identified

Table 37 IC version indication

AFA	IC
0	TDA8376
1	TDA8376A

Table 38 Crystal indication SXA and SXB

SXA	SXB	CRYSTAL
0	0	two 3.6 MHz
0	1	one 3.6 MHz
1	0	one 4.4 MHz
1	1	3.6 and 4.4 MHz

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	9.0	V
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	operating ambient temperature		0	70	°C
T_{sol}	soldering temperature	for 5 s	–	260	°C
T_j	operating junction temperature		–	150	°C
V_{es}	electrostatic handling	all pins; notes 1 and 2	–2000	+2000	V
		all pins; notes 1 and 3	–200	+200	V

Notes

1. All pins are protected against ESD by means of internal clamping diodes.
2. Human Body Model (HBM): R = 1.5 kΩ; C = 100 pF.
3. Machine Model (MM): R = 0 Ω; C = 200 pF.

10 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SDIP52	40	K/W
	QFP64	50	K/W

11 QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611E"*. The number of the quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9398 510 63011.

11.1 Latch-up

At T_{amb} = 70 °C all pins meet the following specification.

- $I_{trigger} \geq 100$ mA or $\geq 1.5V_{DD(max)}$
- $I_{trigger} \leq -100$ mA or $\leq -0.5V_{DD(max)}$.

12 CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
MAIN SUPPLY (PIN 8)						
V_{P1}	supply voltage		7.2	8.0	8.8	V
I_{P1}	supply current		–	75	–	mA
P_{tot}	total power dissipation		–	650	–	W
HORIZONTAL OSCILLATOR SUPPLY (PIN 37)						
V_{P2}	supply voltage		7.2	8.0	8.8	V
I_{P2}	supply current		–	6	–	mA
CVBS and S-VHS input switch						
INTERNAL AND EXTERNAL CVBS INPUTS (PINS 9 AND 13)						
$V_{9(p-p)}$	CVBS input voltage (peak-to-peak value)	note 1	–	1.0	1.4	V
I_9	CVBS input current		–	4	–	µA
SS_{CVBS}	suppression of non-selected CVBS input signal	notes 2 and 3	50	–	–	dB
S-VHS INPUT (PINS 6 AND 7)						
$V_{7(p-p)}$	luminance input voltage (peak-to-peak value)		–	1.0	1.4	V
$I_{7(p-p)}$	luminance input current		–	4	–	µA
$V_{6(p-p)}$	chrominance input voltage (burst amplitude) (peak-to-peak value)	note 4	–	0.3	0.45	V
Z_i	chrominance input impedance		–	50	–	kΩ
TXT AND PIP OUTPUT SIGNALS (PINS 38 AND 11)						
$V_{o(p-p)}$	output signal voltage amplitude (peak-to-peak value)		–	1.0	–	V
Z_o	output impedance		–	–	250	Ω
V_{TS}	top sync voltage level		–	tbf	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB inputs, colour difference inputs, luminance inputs and outputs						
RGB INPUTS (PINS 15 TO 17 AND 23 TO 25); note 5						
$V_{i(p-p)}$	input signal voltage amplitude for an output signal of 2 V (black-to-white) at nominal controls (peak-to-peak value)	note 6	–	0.7	0.8	V
$V_{i(p-p)}$	input signal voltage amplitude before clipping occurs (peak-to-peak value)	note 2	1.0	–	–	V
ΔV_o	difference between black level of internal and external signals at the outputs		–	–	20	mV
I_i	input currents	no clamping; note 7	–	0.1	–	μA
Δt_d	delay difference for the three channels	note 2	–	0	20	ns
FAST BLANKING (PINS 14 AND 26)						
V_i	input voltage	no data insertion	–	–	0.4	V
		data insertion	0.9	–	–	V
$V_{14,26(max)}$	maximum input pulse	data insertion	–	–	3.0	V
t_d	delay time from RGB input to RGB output	data insertion; note 5	–	100	–	ns
Δt_d	delay difference between data insertion to RGB output and RGB input to RGB output	data insertion; note 5	–	50	–	ns
$I_{14,26}$	input current		–	–	0.2	mA
SS_{int}	suppression of internal RGB signals	notes 1 and 2; data insertion; f_i = 0 to 5 MHz	55	–	–	dB
SS_{ext}	suppression of external RGB signals	notes 1 and 2; no data insertion; f_i = 0 to 5 MHz	55	–	–	dB
V_{14}	input voltage to insert black level at the RGB outputs to facilitate OSD signals being applied to the outputs		4	–	–	V
COLOUR DIFFERENCE INPUT SIGNALS (PINS 31 AND 32)						
$V_{32(p-p)}$	input signal amplitude −(R−Y) (peak-to-peak value)	note 7	–	1.05	–	V
$V_{31(p-p)}$	input signal amplitude −(B−Y) (peak-to-peak value)	note 7	–	1.35	–	V
$I_{31,32}$	input current for both inputs	note 7	–	0.1	1.0	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LUMINANCE INPUTS AND OUTPUTS (PINS 27 AND 28)						
$V_{28(p-p)}$	output signal voltage amplitude (peak-to-peak value)	top sync to white	–	0.45	0.63	V
V_{TS}	top sync voltage level		–	2.5	–	V
Z_o	output impedance		–	250	–	Ω
$V_{27(p-p)}$	input signal voltage amplitude (peak-to-peak value)		–	0.45	–	V
I_{clamp}	clamping current during burst key pulse		–	200	–	µA
I_i	input current	no clamping	–	–	0.5	µA
Chrominance filters						
CHROMINANCE TRAP CIRCUIT						
f_{trap}	trap frequency		–	f_{osc}	–	MHz
		during SECAM reception	–	4.2	–	MHz
QF	trap quality factor	note 8	–	2	–	
SR	colour subcarrier rejection		20	–	–	dB
CHROMINANCE BAND-PASS CIRCUIT						
f_c	centre frequency		–	f_{osc}	–	MHz
QBP	band-pass quality factor		–	3	–	
Delay line, peaking circuit and black stretcher						
Y DELAY LINE						
t_d	delay time	note 2	–	480	–	ns
t_{d1}	tuning range delay time	8 steps	–160	–	+160	ns
B	bandwidth of internal delay line	note 2	5	–	–	MHz
PEAKING CONTROL; note 9						
$f_{c(p)}$	peaking centre frequency		–	3	–	MHz
t_W	width of preshoot or overshoot	at 50% of pulse; note 2	–	160	–	ns
OS	overshoot	positive	–	20	–	%
		negative	–	36	–	%
	peaking control curve	16 steps		see Fig.5		
G_W	wave gain	$\frac{\text{negative half wave gain}}{\text{positive half wave gain}}$	–	1.8	–	
CORING STAGE						
S	coring range		–	15	–	IRE
BLACK LEVEL STRETCHER (PIN 2); note 10						
BLS_{max}	maximum black level shift		15	21	27	IRE
LSH	level shift	100% of peak-white	–1	0	+1	IRE
		50% of peak-white	–1	–	+3	IRE
		15% of peak-white	6	8	10	IRE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Horizontal synchronization circuits						
SYNC VIDEO INPUTS (PINS 7, 9 AND 13)						
$V_{7,9,13}$	sync pulse voltage amplitude	note 7	50	300	–	mV
SL_{HS}	slicing level for horizontal sync	note 11	–	50	–	%
SL_{VS}	slicing level for vertical sync		–	30	–	%
HORIZONTAL OSCILLATOR						
f_{fr}	free running frequency		–	15625	–	Hz
Δf_{fr}	spread of free running frequency		–	–	±2	%
$\Delta f/\Delta V_P$	frequency variation with respect to the supply voltage	V_P = 8 V ±10%; note 2	–	0.2	0.5	%
$\Delta f_{(max)}$	maximum frequency variation with temperature	T_{amb} = 0 to 70 °C; note 2	–	–	80	Hz
FIRST CONTROL LOOP (FILTER CONNECTED TO PIN 44); note 12						
f_{HR}	frequency holding range PLL		–	±0.9	±1.2	kHz
f_{CR}	frequency catching range PLL	note 2	±0.6	±0.9	–	kHz
S/N	signal-to-noise ratio of the video input signal at which the time constant is switched		–	20	–	dB
HYS	hysteresis at the switching point		–	1	–	dB
SECOND CONTROL LOOP (CAPACITOR CONNECTED TO PIN 43)						
$\Delta\varphi_i/\Delta\varphi_o$	control sensitivity		–	150	–	µs/µs
t_{cr}	control range from start of horizontal output to flyback at nominal shift position		11	12	–	µs
t_{shift}	horizontal shift range	63 steps	±2	–	–	µs
φ_{dync}	control sensitivity for dynamic compensation		–	5.3	–	µs/V
V_{43}	voltage to switch on the 'flash' protection	note 13	6	–	–	V
I_{43}	input current during protection		–	–	1	mA
HORIZONTAL OUTPUT (PIN 40); note 14						
V_{OL}	LOW level output voltage	I_{OL} = 10 mA	–	–	0.3	V
$I_{O(max)}$	maximum allowed output current		10	–	–	mA
$V_{O(max)}$	maximum allowed output voltage		–	–	V_P	V
δ	duty factor	note 2	–	50	–	%
		note 2; V_{HOUT} = high; during switch-on/switch-off	–	75	–	%
f_{switch}	frequency during switch-on and switch-off		–	$2f_{HOUT}$	–	Hz
$t_{switch(on)}$	switch-on time		–	50	–	ms
$t_{switch(off)}$	switch-off time	RGB drive maximum	–	100	–	ms
		RGB drive minimum	–	50	–	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FLYBACK PULSE INPUT (PIN 41)						
V_{HSW}	switching voltage level for horizontal blanking		–	0.4	–	V
$V_{\varphi2(SW)}$	switching level for phase-2 loop		–	4.0	–	V
$V_{41(max)}$	maximum input voltage	note 7	–	8.0	–	V
Z_i	input impedance	note 7	–	10	–	MΩ
SANDCASTLE PULSE OUTPUT (PIN 39)						
V_{39}	output voltage	during burst key	4.8	5.3	5.8	V
		during blanking	1.8	2.0	2.2	V
t_W	pulse width	burst key pulse	3.3	3.5	3.7	µs
		vertical blanking (50 Hz)	–	25	–	lines
		vertical blanking (60 Hz)	–	21	–	lines
V_{clamp}	clamping voltage level for vertical guard detection		–	2.7	–	V
$I_{39(min)}$	minimum input current to activate guard detection		–	–	0.5	mA
$I_{39(max)}$	maximum allowable input current		2.5	–	–	mA
t_d	delay of start of burst key to start of sync		–	5.4	–	µs
Vertical synchronization and geometry correction						
VERTICAL OSCILLATOR; note 15						
f_{fr}	free running frequency		–	50/60	–	Hz
f_{lock}	locking frequency range		45	–	64.5	Hz
	divider value not locked		–	625/525	–	lines
LR	locking range		488	–	722	lines/ frame
VERTICAL RAMP GENERATOR (PIN 50)						
$V_{50(p-p)}$	sawtooth voltage amplitude (peak-to-peak value)	VS = 1FH; C = 100 nF; R = 39 kΩ	–	3.5	–	V
I_{dis}	discharge current		–	1	–	mA
I_{charge}	charge current set by external resistor	note 16	–	19	–	µA
VS	vertical slope control range	63 steps	–20	–	+20	%
ΔI_{50}	charge current increase	f = 60 Hz	–	20	–	%
V_{50L}	LOW level voltage of ramp		–	2.07	–	V
VERTICAL DRIVE OUTPUTS (PINS 47 AND 48)						
$I_{diff(p-p)}$	differential output current (peak-to-peak value)	VA = 1FH	–	0.95	–	mA
I_{CM}	common mode output current		–	400	–	µA
V_o	output voltage		0	–	4.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EHT TRACKING/OVERVOLTAGE PROTECTION (PIN 49); note 13						
V_{49}	input voltage		1.2	–	2.8	V
SMR	scan modulation range		–5	–	+5	%
φ_{vert}	vertical sensitivity		–	6.3	–	%/V
φ_{EW}	E-W sensitivity	when switched-on	–	–6.3	–	%/V
I_{eq}	E-W equivalent output current		+100	–	–100	µA
V_{49}	overvoltage detection level		–	3.9	–	V
DE-INTERLACE						
	first field delay		–	0.5H	–	
E-W WIDTH; note 17						
CR	control range	63 steps				
	TDA8376		100	–	80	%
	TDA8376A		100	–	65	%
I_{eq}	equivalent output current					
	TDA8376		0	–	400	µA
	TDA8376A		0	–	700	µA
V_o	E-W output voltage range		1.0	–	8.0	V
I_o	E-W output current range					
	TDA8376		0	–	900	µA
	TDA8376A		0	–	1200	µA
E-W PARABOLA/WIDTH						
CR	control range	63 steps	0	–	22	%
I_{eq}	equivalent output current	E-W = 3FH; CP = 00H	0	–	440	µA
E-W CORNER/PARABOLA						
CR	control range	63 steps	–43	–	0	%
I_{eq}	equivalent output current	PW = 3FH; E-W = 3FH	–190	–	0	µA
E-W TRAPEZIUM						
CR	control range	63 steps	–5	–	+5	%
I_{eq}	equivalent output current		–100	–	+100	µA
VERTICAL AMPLITUDE						
CR	control range	63 steps	80	–	120	%
$I_{eqdiff(p-p)}$	equivalent differential vertical drive output current (peak-to-peak value)	SC = 00H	760	–	1140	µA
VERTICAL SHIFT						
CR	control range	63 steps	–5	–	+5	%
$I_{eqdiff(p-p)}$	equivalent differential vertical drive output current (peak-to-peak value)		–50	–	+50	µA
S-CORRECTION						
CR	control range	63 steps	0	–	30	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VERTICAL EXPANSION (ZOOM) MODE (TDA8376A ONLY); note 18						
Output current variation compared with nominal scan:						
VEF	vertical expansion factor		0.75	–	1.38	%
	output current limiting and RGB blanking		–	1.06	–	%
Colour demodulation part						
CHROMINANCE AMPLIFIER						
ACC_{cr}	ACC control range	note 19	26	–	–	dB
ΔV	variation in amplitude of the output signals over the ACC range		–	–	2	dB
THR_{on}	threshold colour killer ON		–23	–26	–29	dB
HYS_{off}	hysteresis colour killer OFF	strong signal conditions; S/N ≥ 40 dB; note 2	–	+3	–	dB
		noisy input signals; note 2	–	+1	–	dB
REFERENCE PART						
Phase-locked loop; note 20						
f_{CR}	frequency catching range		±360	±600	–	Hz
$\Delta\varphi$	phase shift for a ±400 Hz deviation of the oscillator frequency	note 2	–	–	2	deg
Oscillator						
TC_{osc}	temperature coefficient of the oscillator frequency	note 2	–	–	tbf	Hz/K
Δf_{osc}	oscillator frequency deviation with respect to the supply	note 2; V_P = 8 V ±10%	–	–	tbf	Hz
$R_{i(min)}$	minimum negative input resistance		–	–	1	kΩ
$C_{L(max)}$	maximum load capacitance		–	–	15	pF
HUE CONTROL						
HUE_{cr}	hue control range	63 steps; see Fig.6	±35	±40	–	deg
ΔHUE	hue variation for ±10% V_P	note 2	–	0	–	deg
$\Delta HUE/\Delta T$	hue variation with temperature	T_{amb} = 0 to 70 °C; note 2	–	0	–	deg

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DEMODULATORS (PINS 29 AND 30)						
$V_{30(p-p)}$	–(R–Y) output voltage amplitude (peak-to-peak value)	note 21	–	0.525	–	V
$V_{29(p-p)}$	–(B–Y) output voltage amplitude (peak-to-peak value)	note 21	–	0.675	–	V
G	gain ratio between both demodulators G(B–Y) and G(R–Y)		1.60	1.78	1.96	
ΔV	spread of voltage amplitude ratio PAL/NTSC	note 2	–1	–	+1	dB
Z_o	output impedance –(R–Y)/–(B–Y) output	note 2	–	500	–	Ω
B	bandwidth of demodulators	–3 dB; notes 7 and 21	–	650	–	kHz
$V_{29,30(p-p)}$	residual carrier output (peak-to-peak value)	$f = f_{osc}$; –(R–Y) output	–	–	5	mV
		$f = f_{osc}$; –(B–Y) output	–	–	5	mV
		$f = 2f_{osc}$; –(R–Y) output	–	–	5	mV
		$f = 2f_{osc}$; –(B–Y) output	–	–	5	mV
$V_{30(p-p)}$	H/2 ripple at –(R–Y) output (peak-to-peak value)		–	–	25	mV
$\Delta V_o/\Delta T$	variation of output voltage amplitude with temperature	note 2	–	0.1	–	%/K
$\Delta V_o/\Delta V_P$	variation of output voltage amplitude with supply voltage	note 2	–	–	±0.1	dB
φ_e	phase error in the demodulated signals		–	–	±5	deg
COLOUR DIFFERENCE MATRICES IN CONTROL CIRCUIT						
PAL or (SECAM mode with TDA8395); –(R–Y) and –(B–Y) not affected						
(G–Y)/(R–Y)	ratio of demodulated signals		–	–0.51 ±10%	–	
(G–Y)/(B–Y)	ratio of demodulated signals		–	–0.19 ±25%	–	
NTSC mode; the colour-difference matrix results in the following signals (nominal hue setting)						
–(B–Y)	–(B–Y) signal			–(B–Y)		
–(R–Y)	–(R–Y) signal			1.39(R–Y) – 0.07(B–Y)		
–(G–Y)	–(G–Y) signal			–0.46(R–Y) – 0.15(B–Y)		

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
REFERENCE SIGNAL OUTPUT FOR TDA8395 (PIN 36); note 22						
f_{ref}	reference frequency		–	4.43	–	MHz
$V_{36(p-p)}$	output voltage amplitude (peak-to-peak value)		0.2	0.25	0.3	V
V_o	output voltage level	PAL/NTSC identified	–	1.5	–	V
		no PAL/NTSC identified; SECAM (by TDA8395) identified	–	5.0	–	V
I_{36}	required current to stop PAL/NTSC identification circuit during SECAM		150	–	–	μA
Control part						
SATURATION CONTROL; note 6						
SAT_{CR}	saturation control range	63 steps; see Fig.7	52	–	–	dB
CONTRAST CONTROL; note 6						
CON_{CR}	contrast control range	63 steps	–	20	–	dB
	tracking between the three channels over a control range of 10 dB	see Fig.8	–	–	0.5	dB
BRIGHTNESS CONTROL						
BRI_{CR}	brightness control range	63 steps; see Fig.9	–	±0.7	–	V
RGB OUTPUT SIGNALS (PINS 19, 20 AND 21)						
$V_{19,20,21(p-p)}$	output voltage amplitude (peak-to-peak value)	at nominal luminance input signal, nominal contrast and white-point adjustment; note 6	tbf	2.0	tbf	V
		at maximum white point setting	–	3.0	–	V
$V_{BWmax(p-p)}$	maximum voltage amplitude (black-to-white)	note 23	–	2.6	–	V
		at maximum white point setting	–	3.6	–	V
$V_{RED(p-p)}$	output voltage amplitude for the 'red' channel (peak-to-peak value)	at nominal settings for contrast and saturation control and no luminance signal to the input (R–Y, PAL)	tbf	2.1	tbf	V
V_{blank}	blanking level at the RGB outputs		0.7	0.8	0.9	V
I_{bias}	internal bias current of NPN emitter follower output transistor		–	1.5	–	mA
I_o	available output current		–	5	–	mA
Z_o	output impedance		–	150	–	Ω
CR_{bl}	control range of the black-current stabilization	nominal brightness and white-point adjustment (with respect to the measuring pulse); V_{blk} = 2.5 V	–	–	±1	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{bl}	black level shift with picture content	note 2	–	–	20	mV
V_o	output voltage of the 4-L pulse after switch-on		–	4.2	–	V
$\Delta bl/\Delta T$	variation of black level with temperature	note 2	–	1.0	–	mV/K
Δbl	relative variation in black level between the three channels during variations of	note 2				
	supply voltage (±10%)	nominal controls	–	–	tbf	mV
	saturation (50 dB)	nominal contrast	–	–	tbf	mV
	contrast (20 dB)	nominal saturation	–	–	tbf	mV
	brightness (±0.5 V)	nominal controls	–	–	tbf	mV
	temperature (range 40 °C)		–	–	tbf	mV
S/N	signal-to-noise ratio of the output signals	RGB input; note 24	60	–	–	dB
		CVBS input; note 24	50	–	–	dB
$V_{res(p-p)}$	residual voltage at the RGB outputs (peak-to-peak value)	at f_{osc}	–	–	15	mV
		at $2f_{osc}$ plus higher harmonics in RGB outputs	–	–	15	mV
B	bandwidth of output signals	RGB input; at –3 dB	8	–	–	MHz
		CVBS input; at –3 dB; f_{osc} = 3.58 MHz	–	2.8	–	MHz
		CVBS input; at –3 dB; f_{osc} = 4.43 MHz	–	3.5	–	MHz
		S-VHS input; at –3 dB	5	–	–	MHz
WHITE-POINT ADJUSTMENT						
	I²C-bus setting for nominal gain	HEX code	–	20H	–	
$G_{inc(max)}$	maximum increase of the gain	HEX code 3FH	40	50	60	%
$G_{dec(max)}$	maximum decrease of the gain	HEX code 00H	40	50	60	%
BLACK-CURRENT STABILIZATION (PIN 18); note 25						
I_{bias}	bias current for the picture tube cathode	nominal white point setting	–	10	–	μA
I_{leak}	acceptable leakage current		–	100	–	μA
$I_{scan(max)}$	maximum current during scan		–	0.3	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BEAM CURRENT LIMITING (PIN 22); note 23						
V_{CR}	contrast reduction starting voltage		–	3.5	–	V
V_{diffCR}	voltage difference for full contrast reduction		–	2.0	–	V
V_{BR}	brightness reduction starting voltage		–	2.5	–	V
V_{diffBR}	voltage difference for full brightness reduction		–	1.0	–	V
V_{bias}	internal bias voltage		–	4.5	–	V
$I_{ch(int)}$	internal charge current		–	25	–	µA
I_{disch}	discharge current due to ‘peak-white limiting’		–	200	–	µA

Notes

1. Signal with negative-going sync. Amplitude includes sync pulse amplitude.
2. This parameter is not tested during production but is guaranteed by the design and qualified by means of matrix batches which are made in the pilot production period.
3. This parameter is measured at nominal settings of the various controls.
4. Indicated is a signal for a colour bar with 75% saturation (chrominance : burst ratio = 2.2 : 1).
5. The RGB1 inputs (pins 14 to 17) have priority over the RGB2 inputs (pins 23 to 25).
6. Nominal contrast is specified with the DAC in position 20H. Nominal saturation as maximum –10 dB. In the nominal brightness setting the black level at the outputs is identical to the level of the black-current measuring pulses.
7. This parameter is not tested during production and is just given as application information for the designer of the television receiver.
8. The –3 dB bandwidth of the circuit can be calculated by means of the following equation:

$$f_{-3\ dB} = f_{osc}\left(1 - \frac{1}{2Q}\right)$$

9. Valid for a signal amplitude on the Y-input of 0.7 V black-to-white (100 IRE) with a rise time (10% to 90%) of 70 ns and the video switch in the Y/C mode. During production the peaking function is not tested by measuring the overshoots but by measuring the frequency response of the Y output.
10. For video signals with a black level which deviates from the back-porch blanking level the signal is ‘stretched’ to the blanking level. The amount of correction depends on the IRE value of the signal (see Fig.10). The black level is detected by the capacitor connected to pin 2. The black level stretcher can be made inoperative by connecting pin 2 to the positive supply line. The values given are valid only when the luminance input signal (pins 7, 9 and 13) has a value of 1 V (p-p).
11. The slicing level is independent of sync pulse amplitude. The given percentage is the distance between the slicing level and the black level (back porch).

12. To obtain a good performance for both weak signal and VCR playback the time constant of the first control loop is switched depending on the input signal condition and the condition of the I²C-bus. Therefore the circuit contains a noise detector and the time constant is switched to 'slow' when too much noise is present in the signal. In the 'fast' mode during the vertical retrace time the phase detector current is increased 50% so that phase errors due to head-switching of the VCR are corrected as soon as possible. Switching between the two modes can be automatically or overruled by the I²C-bus.

    The circuit contains a video identification circuit which is independent of first loop. This identification circuit can be used to close or open the first control loop when a video signal is present or not present on the input. This enables a stable On Screen Display (OSD) when just noise is present at the input. The coupling of the video identification circuit with the first loop can be defeated via the I²C-bus.

    To prevent that the horizontal synchronization being disturbed by anti-copy guard signals like Macrovision the phase detector is gated during the vertical retrace period so that pulses during scan have no effect on the output voltage. The width of the gate pulse is approximately 22 μs, the phase position around the sync pulse is asymmetrical. During weak signal conditions (noise detector active) the gating is active during the complete scan period and the width of the gate pulse is reduced to 5.7 μs so that the effect of the noise is reduced to a minimum.

    The output current of the phase detector in the various conditions are shown in Table 39.

13. The ICs have two protection inputs. The protection on pin 43 is intended to be used as 'flash' protection. When this protection is activated the horizontal drive pulse is switched-off immediately and then switched on again via the slow start procedure. The protection on pin 49 is intended for overvoltage (X-ray) protection. When this protection is activated the horizontal drive can be switched-off (via the slow stop procedure). It is also possible to continue the horizontal drive and to set the protection bit (XPR) in the output bytes of the I²C-bus. The choice between the two modes of operation is made via the PRD bit.

14. During switch-on the horizontal output starts with the double frequency and with a duty factor of 75% (V_{HOUT} = high). After approximately 50 ms the frequency is changed to the normal value. Because of the high frequency the peak currents in the horizontal output transistor are limited. Also during switch-off the frequency is switched to the double value and the RGB drive is set to maximum so that the EHT capacitor is discharged. After approximately 100 ms the RGB drive is set to minimum and 50 ms later the horizontal drive is switched-off.

15. The timing pulses for the vertical ramp generator are obtained from the horizontal oscillator via a divider circuit. This divider circuit has 3 modes of operation:

    a) Search mode 'large window'.

    This mode is switched on when the circuit is not synchronized or when a non-standard signal (number of lines per frame in the 50 Hz mode is between 311 and 314 and in the 60 Hz mode between 261 and 264). In the search mode the divider can be triggered between line 244 and line 361 (approximately 45 to 64.5 Hz).

    b) Standard mode 'narrow window'.

    This mode is switched on when more than 15 successive vertical sync pulses are detected in the narrow window. When the circuit is in the standard mode and a vertical sync pulse is missing the retrace of the vertical ramp generator is started at the end of the window. Consequently, the disturbance of the picture is very small. The circuit will switch back to the search window when, for 6 successive vertical periods, no sync pulses are found within the window.

    c) Standard TV-norm (divider ratio 525 (60 Hz) or 625 (50 Hz).

    When the system is switched to the narrow window it is checked whether the incoming vertical sync pulses are in accordance with the TV-norm. When 15 standard TV-norm pulses are counted the divider system is switched to the standard divider ratio mode. In this mode the divider is always reset at the standard value even if the vertical sync pulse is missing.

    When 3 vertical sync pulses are missed the system switches back to the narrow window and when also in this window no sync pulses are found (condition 3 missing pulses) the system switches over to the search window.

    The vertical divider requires some waiting time during channel-switching of the tuner. When a fast reaction of the divider is required during channel-switching the system can be forced to the search window by means of the NCIN bit in subaddress 08.

16. Conditions: frequency is 50 Hz; normal mode; VS = 1FH.
17. The E-W output current range of the TDA8376A is higher than that of the TDA8376 because of the horizontal zoom function of the TDA8376A. The output range percentages mentioned for E-W control parameters are based on the assumption that 400 μA variation in E-W output current is equivalent to 20% variation in picture width.
18. The TDA8376A has a zoom adjustment possibility for the vertical and horizontal deflection. For this reason an extra DAC has been added in the vertical amplitude control which controls the vertical scan amplitude between 75 to 138% of the nominal scan. At an amplitude of 106% of the nominal scan the output current is limited and the blanking of he RGB outputs is activated. This is illustrated in Fig.21. In addition to the variation of the vertical amplitude the vertical slope control range is also increased. This allows variation of the position of the bottom part of the picture independent of the upper part. The nominal scan height must be adjusted at a position of 19H of the vertical 'zoom' DAC.
19. At a chrominance input voltage of 660 mV (p-p) [colour bar with 75% saturation i.e. burst signal amplitude 300 mV (p-p)] the dynamic range of the ACC is +6 and −20 dB.
20. All frequency variations are referenced to a 3.58 or 4.43 MHz carrier frequency. All oscillator specifications are measured with the Philips crystal series 9922 520 with a series capacitance of 18 pF. The oscillator circuit is rather insensitive to the spurious responses of the crystal. Provided the resonance resistance of the third overtone is higher than that of the fundamental frequency the oscillator will operate at the correct frequency. The typical crystal parameters for the crystals are:
    a) load resonance frequency f_0 (C_L = 20 pF) = 4.433619 or 3.579545 MHz
    b) motional capacitance C_M = 20.6 fF (4.43 MHz crystal) or 14.7 fF (3.58 MHz crystal)
    c) parallel capacitance C_0 = 5 pF for both crystals.

    The minimum detuning range can only be specified if both the IC and the crystal tolerances are known and the figures given in are therefore valid for the specified crystal series. In this, tolerances of the crystal with respect to nominal frequency, motional capacitance and ageing have been taken into account and have been counted for by gaussic addition. Whenever different typical crystal parameters are used the following equation might be helpful for calculating the impact on the detuning capabilities:

    Detuning range: $\frac{C_M}{\left(1+\frac{C_0}{C_L}\right)^2}$

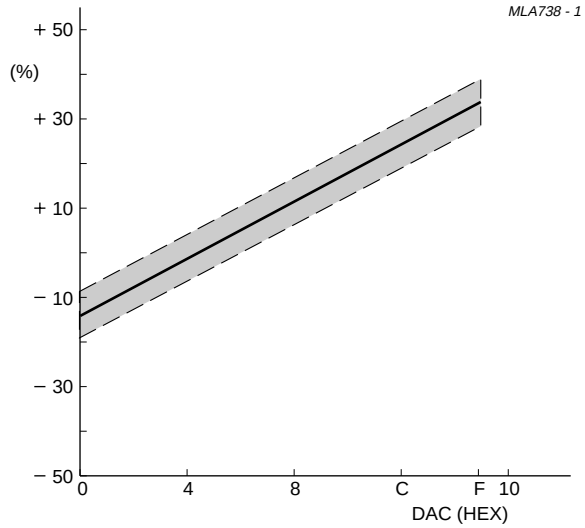
    The resulting detuning range should be corrected for temperature shift and supply deviation of both the IC and the crystal. The actual series capacitance in the application should be C_L = 18 pF to account for parasitic capacitances on and off chip. For 3-normal applications with two crystals connected to one pin the maximum parasitic capacitance of the crystal pin should not exceed 15 pF.
21. The −(R−Y) and −(B−Y) signals are demodulated with a phase difference of the reference carrier of 90° and a gain ratio $\frac{-(B-Y)}{-(R-Y)} = 1.78$. The matrixing to the required signals is achieved in the control part.
22. The subcarrier output signal can be supplied to the TDA8395 but it can also be used as drive signal for external comb filters. For this reason the signal is continuously available at the output. Only when SECAM has been identified the subcarrier signal is available only during the vertical retrace time. This is to avoid cross-talk between the SECAM input signal and the subcarrier signal. An external DC load on this pin is not allowed because this current will disturb the reliability of the communication between the TDA8376/TDA8376A and the TDA8395.
23. At nominal setting of the gain control. When this amplitude is exceeded the peak-white limiting circuit will reduce the contrast. The control voltage is generated via the external capacitor connected to the beam-current limiting input.
24. Signal-to-noise ratio (S/N) is specified as peak-to-peak signal with respect to RMS noise (bandwidth 5 MHz).
25. This is a current input. The indicated value of the nominal bias current is obtained at the nominal setting of the gain (white point) control. The actual value of the bias current depends on the gain control setting of each channel. As a result the 'black-current' of each gun is adapted to the white point setting so that the background colour will follow the white point adjustment.

Table 39 Output current of the phase detector in the various conditions

I²C-BUS COMMANDS				IC CONDITIONS			φ-1 CURRENT/MODE			
VID	POC	FOA	FOB	IDENT	COIN	NOISE	SCAN	V-RETR	GATING	MODE
–	0	0	0	yes	yes	yes	30	30	yes(1)	auto
–	0	0	0	yes	no	no	180	270	no	auto
–	0	0	1	yes	yes	yes	30	30	yes	slow
–	0	0	1	yes	yes	no	180	270	yes	fast
–	0	1	–	yes	–	–	180	270	no	fast
0	0	–	–	no	–	–	6	6	no	OSD
–	1	–	–	–	–	–	–	–	–	off

Note

1. Only during vertical retrace, pulse width 22 μs. In other conditions the pulse width is 5.7 μs and the gating is continuous.



Overshoot in direction ‘black’.

Fig.5 Peaking control curve.

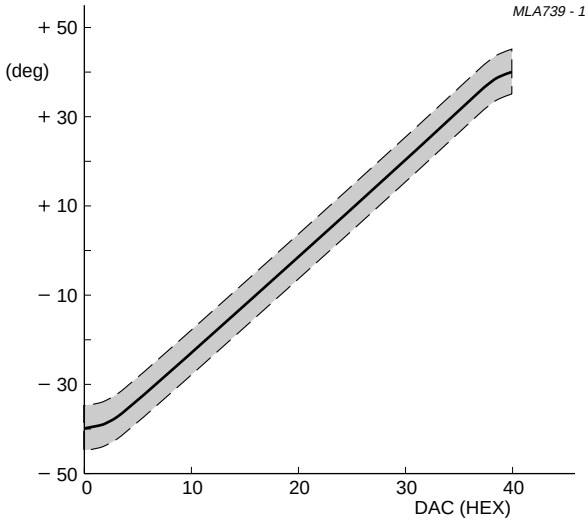


Fig.6 Hue control curve.

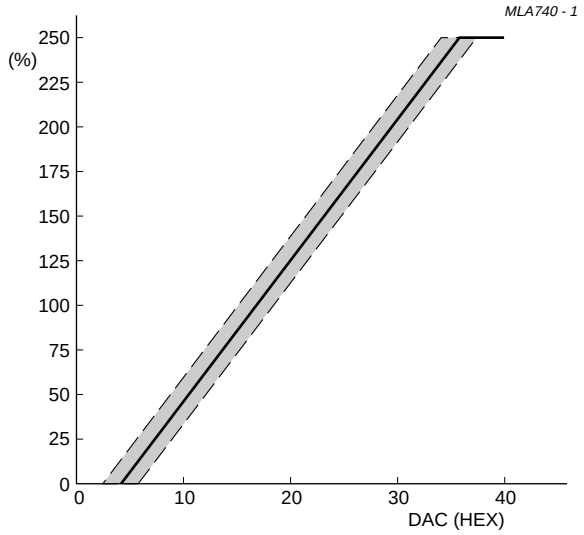


Fig.7 Saturation control curve.

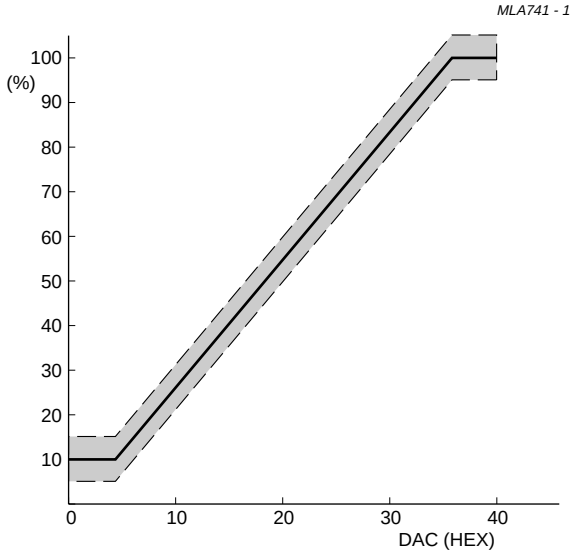
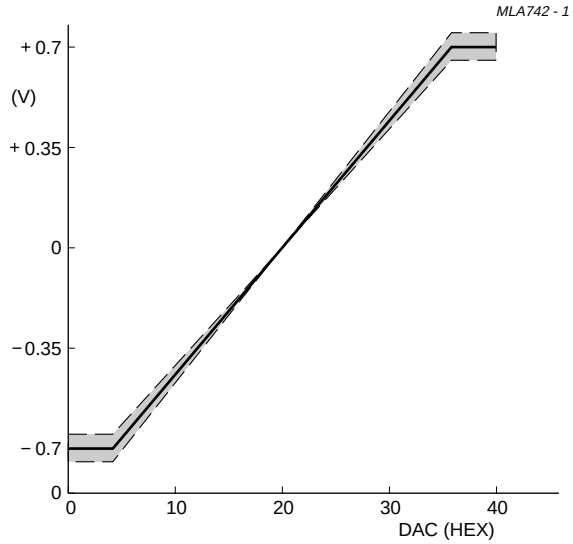
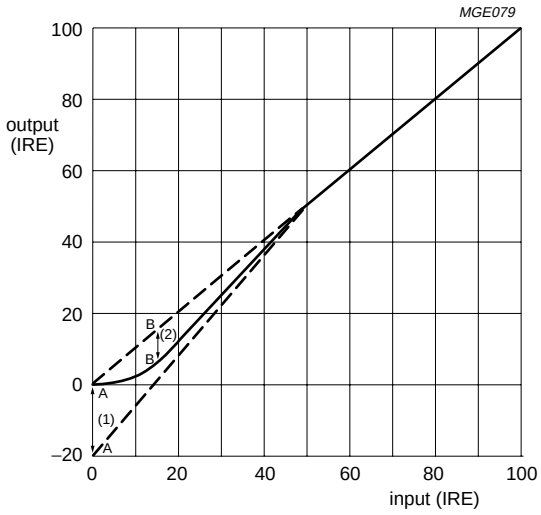


Fig.8 Contrast control curve.



Relative variation with respect to the measuring pulse.

Fig.9 Brightness control curve.



(1) Maximum black level shift.
(2) Level shift at 15% of peak white.

Fig.10 I/O relationship of the black level stretcher.

13 TEST AND APPLICATION INFORMATION

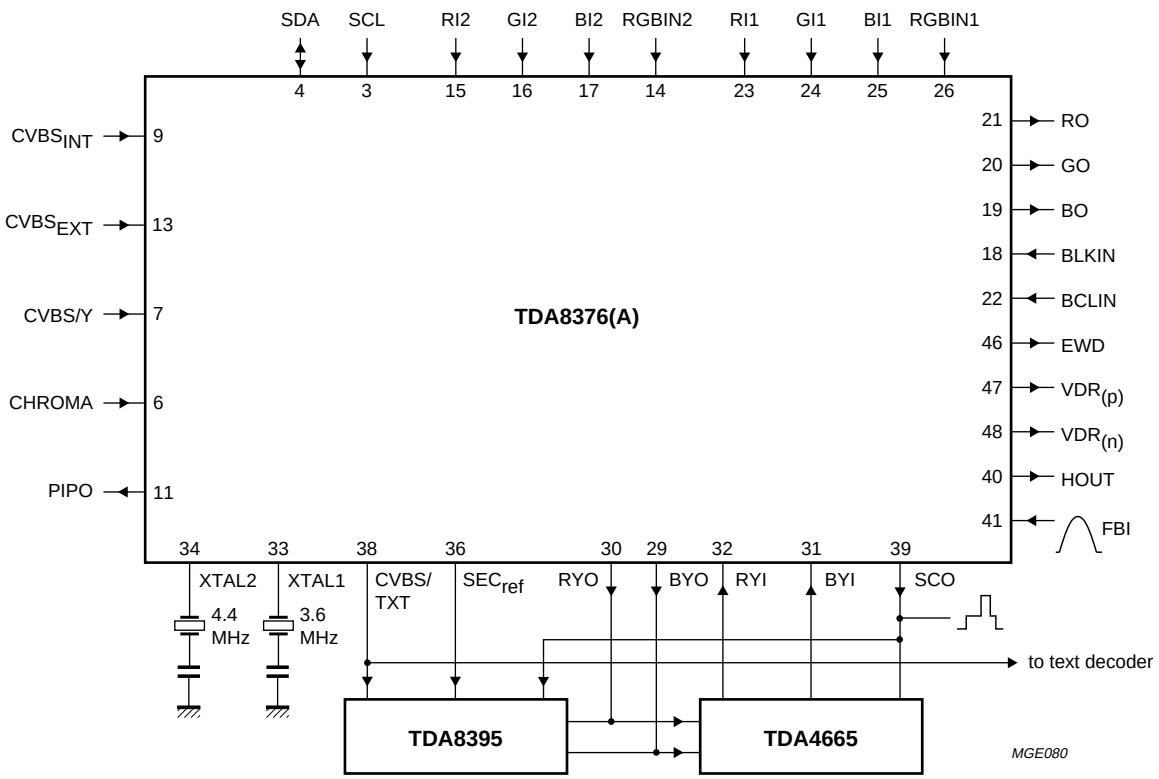


Fig.11 Application diagram.

13.1 East-West output stage

In order to obtain correct tracking of the vertical and horizontal EHT-correction, the E-W output stage should be dimensioned as illustrated in Fig.12.

Resistor R_{EW} determines the gain of the E-W output stage. Resistor R_c determines the reference current for both the vertical sawtooth generator and the geometry processor.

The preferred value of R_c is 39 kΩ which results in a reference current of 100 µA (V_{ref} = 3.9 V

The value of R_{EW} must be:

$$R_{EW} = R_c \times \frac{V_{scan}}{18 \times V_{ref}}$$

Example: With V_{ref} = 3.9 V R_c = 39 kΩ and V_{scan} = 120 V then R_{EW} = 68 kΩ.

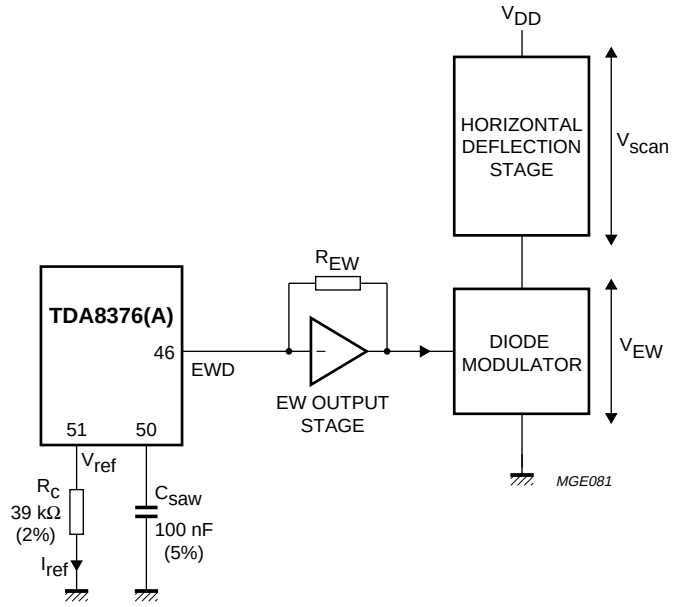
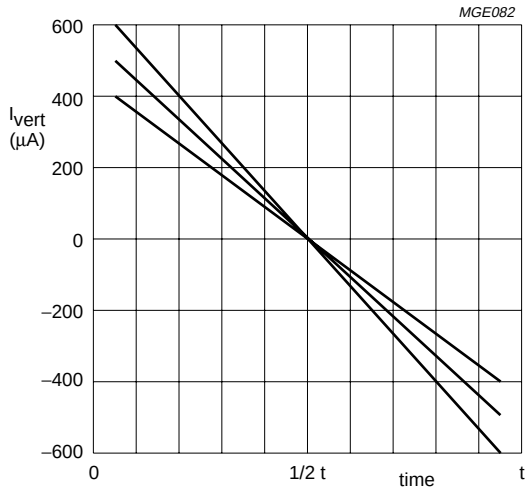
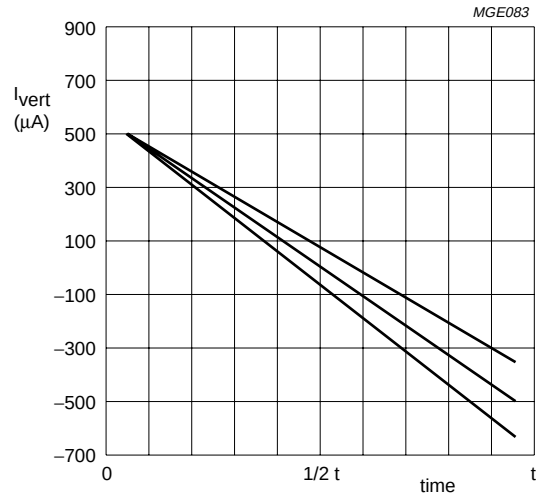


Fig.12 East-West output stage.



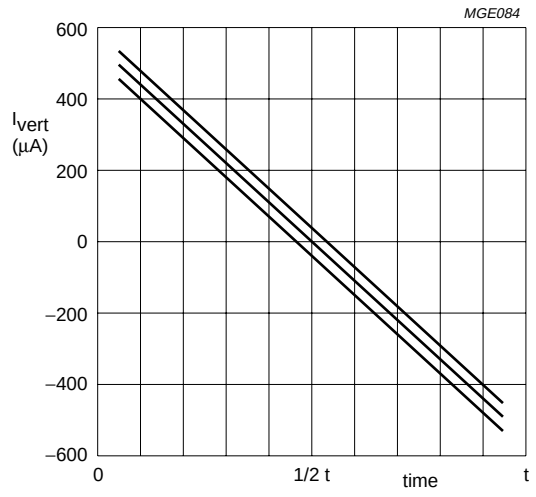
VA = 0, 31H and 63H; VSH = 31H; SC = 0.

Fig.13 Control range of vertical amplitude.



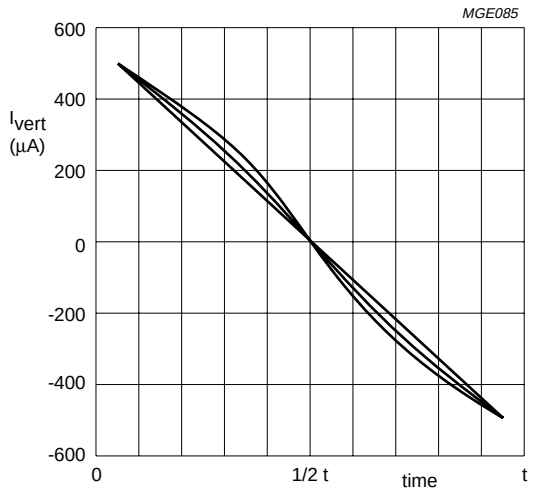
VS = 0, 31H and 63H; VA = 31H; VHS = 31H; SC = 0.

Fig.14 Control range of vertical slope.



VSH = 0, 31H and 63H; VA = 31H; SC = 0.

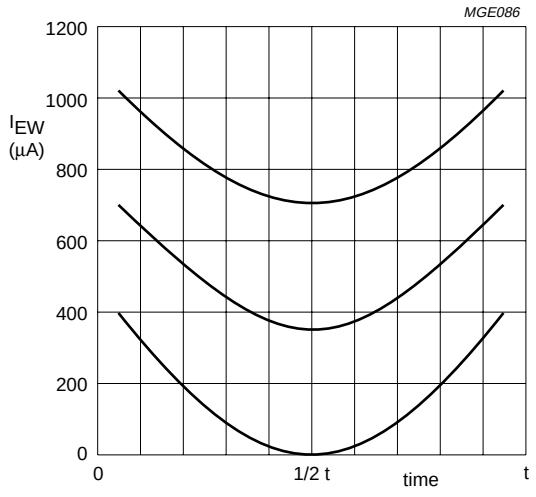
Fig.15 Control range of vertical shift.



SC = 0, 31H and 63H; VA = 31H; VHS = 31H.

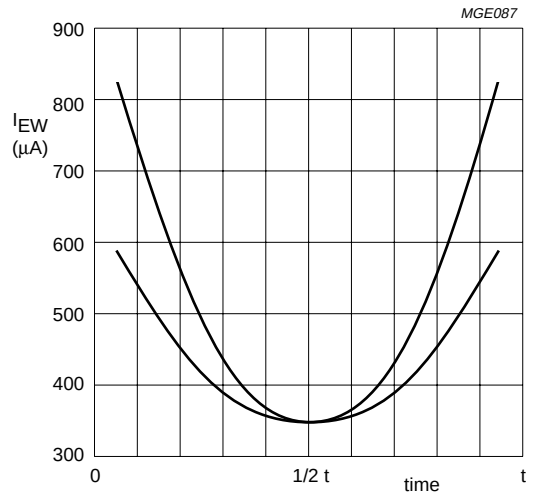
Picture height does not change with setting of S-correction for nominal vertical amplitude (VA = 31H).

Fig.16 Control range of S-correction.



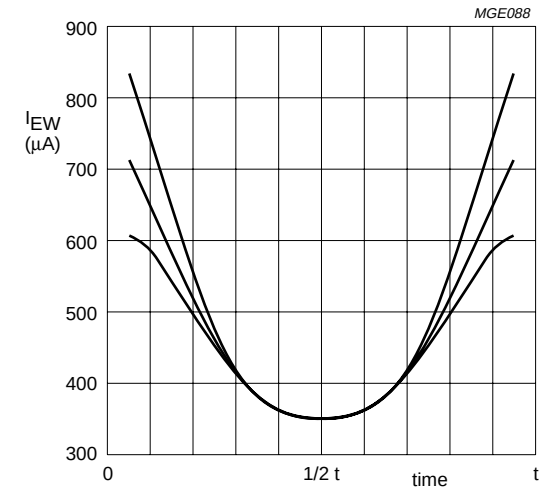
EW = 0, 31H and 63H; PW = 31H; CP = 31H.

Fig.17 Control range of E-W width.



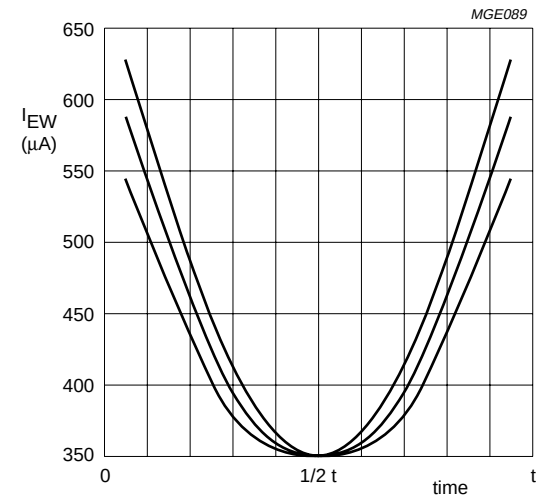
PW = 0, 31H and 63H; EW = 31H; CP = 31H.

Fig.18 Control range of E-W parabola/width ratio.



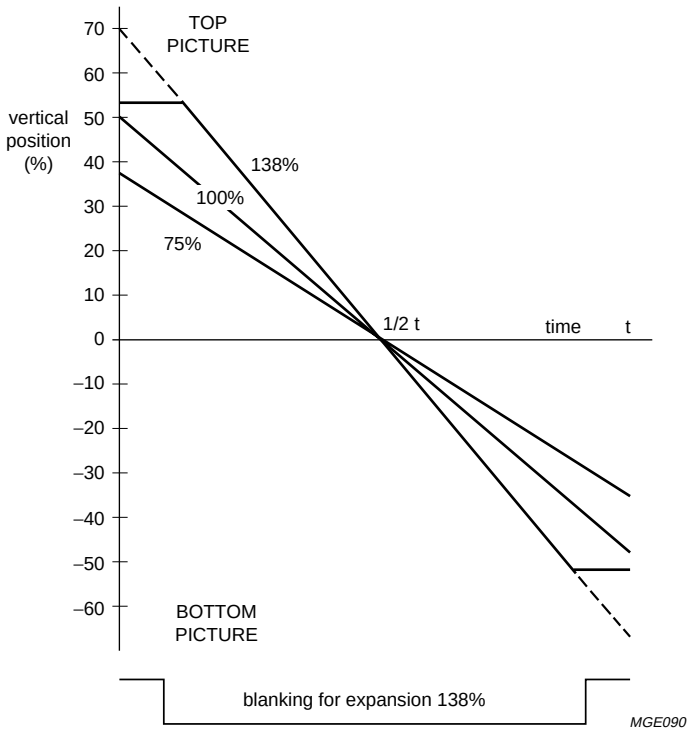
CP = 0, 31H and 63H; EW = 31H; PW = 63H.

Fig.19 Control range of E-W corner/parabola ratio.



TC = 0, 31H and 63H; EW = 31H; PW = 31H.

Fig.20 Control range of E-W trapezium correction.



TDA8376A only.

Fig.21 Sawtooth waveform and blanking pulse.

13.2 Adjustment of geometry control parameters

The deflection processor of the TDA8376/TDA8376A offers nine control parameters for picture alignment:

- Vertical picture alignment
  - S-correction
  - vertical amplitude
  - vertical slope
  - vertical shift
- Horizontal picture alignment
  - horizontal shift
  - E-W width
  - E-W parabola/width
  - E-W corner/parabola
  - E-W trapezium correction.

It is important to notice that the TDA8376/ TDA8376A is designed for use with a DC-coupled vertical deflection stage. This is the reason why a vertical linearity alignment is not necessary (and therefore not available).

For a particular combination of picture tube type, vertical output stage and E-W output stage it is determined which are the required values for the settings of S-correction, E-W parabola/width ratio and E-W corner/parabola ratio. These parameters can be preset via the I²C-bus, and do not need any additional adjustment. The remainder of the parameters are preset with the mid-value of their control range (i.e. 1FH), or with the values obtained by previous TV-set adjustments.

The vertical shift control is intended for compensation of off-sets in the external vertical output stage or in the picture tube. It can be shown that without compensation these off-sets will result in a certain linearity error, especially with picture tubes that need large S-correction. The total linearity error is in first order approximation proportional to the value of the off-set, and to the square of the S-correction required. The necessity to use the vertical shift alignment depends on the expected off-sets in vertical output stage and picture tube, on the required value of the S-correction, and on the demands upon vertical linearity.

For adjustment of the vertical shift and vertical slope independent of each other, a special service blanking mode can be entered by setting the SB-bit HIGH. In this mode the RGB-outputs are blanked during the second half of the picture. There are two different methods for alignment of the picture in vertical direction. Both methods make use of the service blanking mode.

The first method is recommended for picture tubes that have a marking for the middle of the screen. With the vertical shift control the last line of the visible picture is positioned exactly in the middle of the screen. After this adjustment the vertical shift should not be changed. The top of the picture is placed by adjustment of the vertical amplitude, and the bottom by adjustment of the vertical slope.

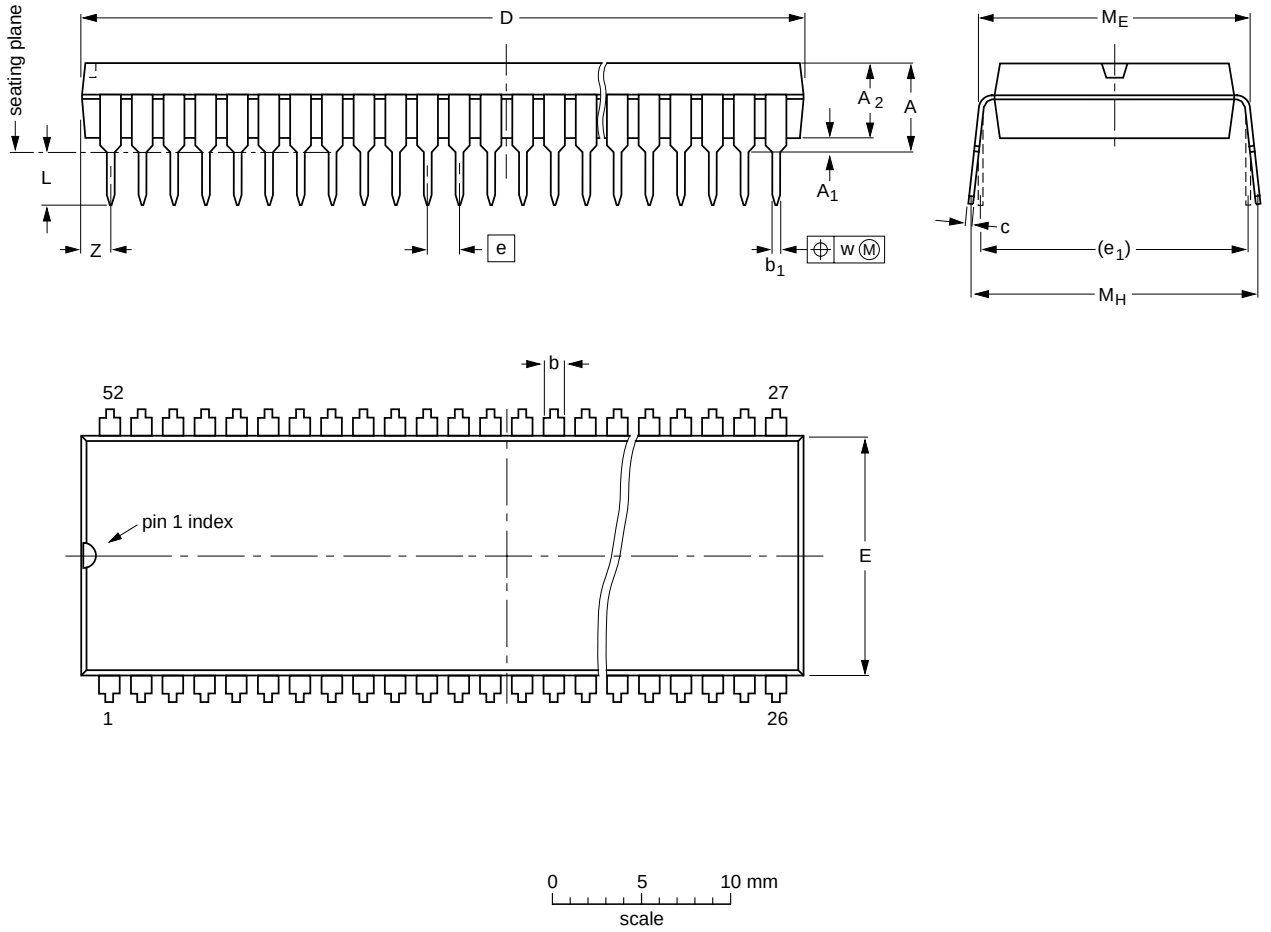
The second method is recommended for picture tubes that have no marking for the middle of the screen. For this method a video signal is required in which the middle of the picture is indicated (e.g. the white line in the circle test pattern). With the vertical slope control the beginning of the blanking is positioned exactly on the middle of the picture. Then the top and bottom of the picture are placed symmetrical with respect to the middle of the screen by adjustment of the vertical amplitude and vertical shift. After this adjustment the vertical shift has the correct setting and should not be changed.

If the vertical shift alignment is not required VSH should be set to its mid-value (i.e. VSH = 1FH). Then the top of the picture is placed by adjustment of the vertical amplitude and the bottom by adjustment of the vertical slope. After the vertical picture alignment the picture is positioned in the horizontal direction by adjustment of the E-W width and the horizontal shift. Finally (if necessary) the left and right-hand sides of the picture are aligned in parallel by adjusting the E-W trapezium control.

To obtain the full range of the vertical zoom function of the TDA8376A the adjustment of the vertical geometry should be carried out at a nominal setting of the zoom DAC at position 19H.

14 PACKAGE OUTLINES

SDIP52: plastic shrink dual in-line package; 52 leads (600 mil) **SOT247-1**



DIMENSIONS (mm are the original dimensions)

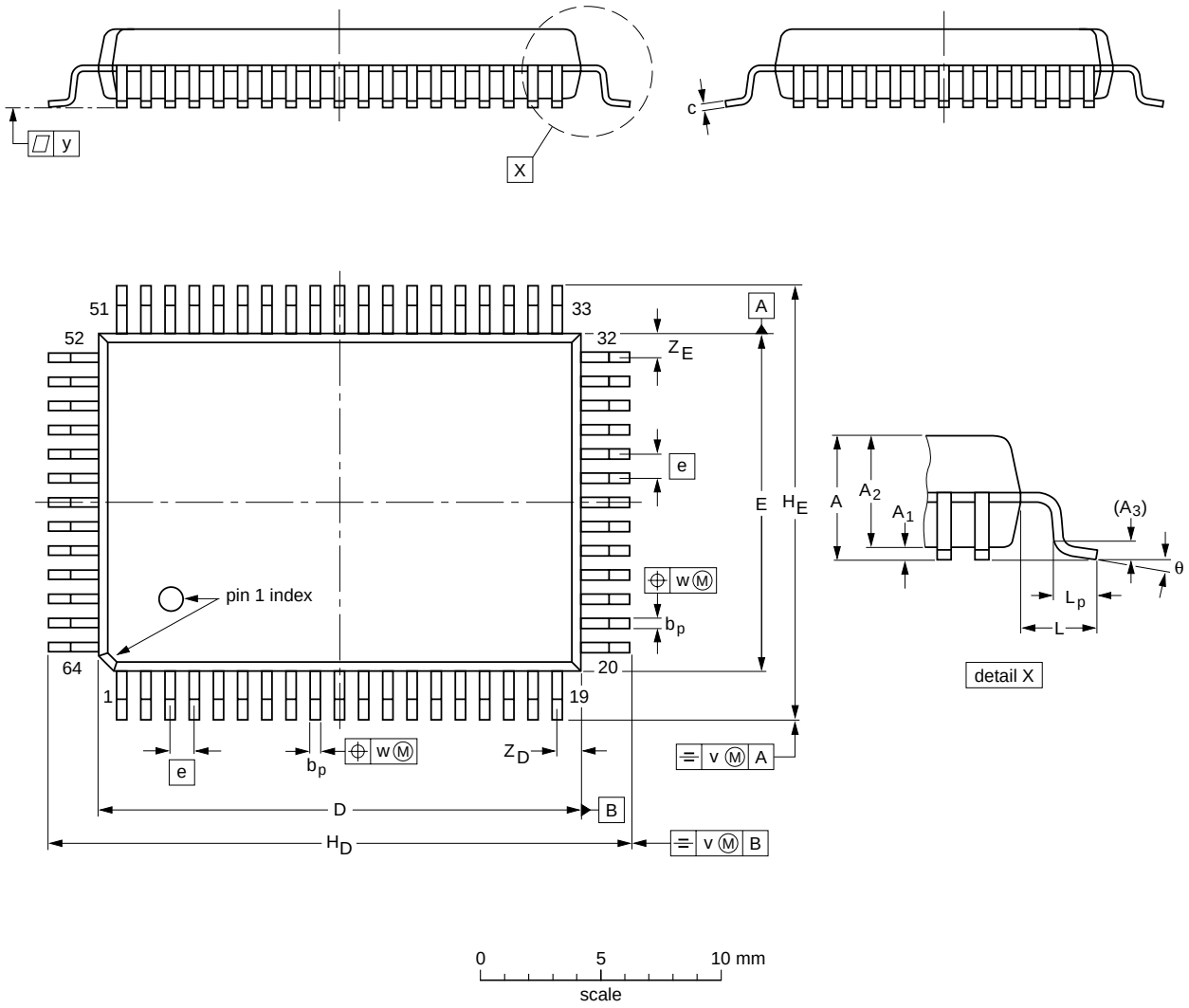
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	47.9 47.1	14.0 13.7	1.778	15.24	3.2 2.8	15.80 15.24	17.15 15.90	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT247-1						~~90-01-22~~ 95-03-11

QFP64: plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT319-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.50 0.35	0.25 0.14	20.1 19.9	14.1 13.9	1	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT319-2						~~95-02-04~~ 97-08-01

15 SOLDERING

15.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

15.2 SDIP

15.2.1 Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

15.2.2 Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

15.3 QFP

15.3.1 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary from 50 to 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheat for 45 minutes at 45 °C.

15.3.2 Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured. Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.3.3 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

16 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

17 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

18 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

NOTES

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