19-2813; Rev 0; 4/03

MAXIM

3V/5V, 6dB Video Buffer with Sync-Tip Clamp, Output Sag Correction, and 150nA Shutdown Current

MAX4090

General Description

The MAX4090 3V/5V, 6dB video buffer with sync-tip clamp, output sag correction, and low-power shutdown mode is available in tiny SOT23 and SC70 packages. The sag-corrected output of the MAX4090 is designed to drive AC-coupled, 150Ω back-terminated video loads in portable video applications such as digital still cams, portable DVD players, digital camcorders, PDAs, video-enabled cell phones, portable game systems, and notebook computers. The sag correction feature introduces low-frequency compensation that reduces the value of the normally bulky and expensive 330µF AC-coupling capacitor to two small, less expensive 22µF capacitors. The input clamp positions the video waveform at the output and allows the MAX4090 to be used as either an AC- or DC-coupled output driver.

The MAX4090 operates from a single 2.7V to 5.5V supply and consumes only 6.5mA of supply current. The low-power shutdown mode reduces the supply current to 150nA, making the MAX4090 ideal for low-voltage, battery-powered video applications.

The MAX4090 is available in tiny 6-pin SOT23 and SC70 packages and is specified over the extended -40°C to +85°C temperature range.

Applications

Portable Video/Game Systems/DVD Players

Digital Camcorders/Televisions/Still Cameras

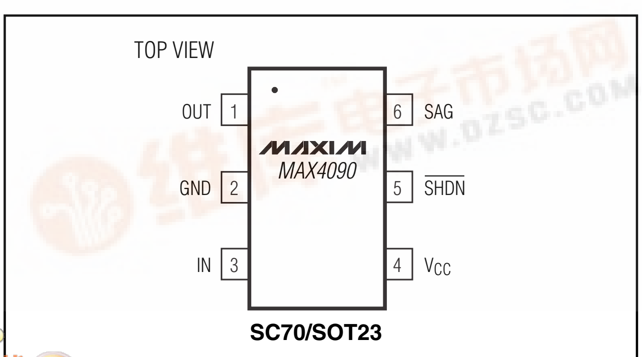
PDAs

Video-Enabled Cell Phones

Notebook Computers

Portable/Flat-Panel Displays

Pin Configuration



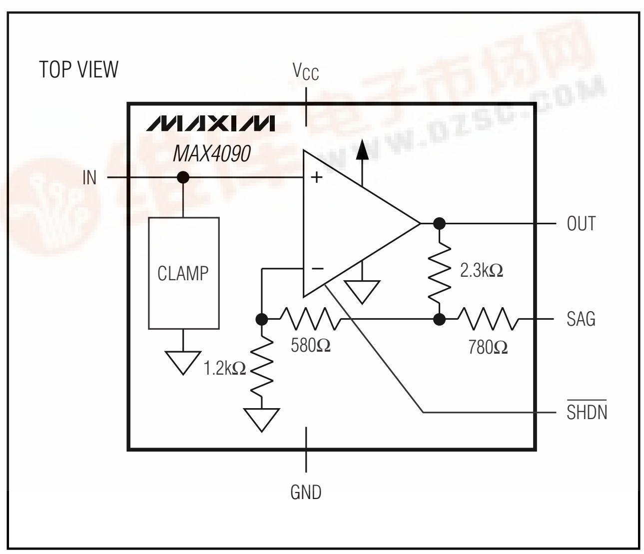
Features

- ♦ **Single-Supply Operation from 2.7V to 5.5V**
- ♦ **Input Sync-Tip Clamp**
- ♦ **AC- or DC-Coupled Output**
- ♦ **Low-Power Shutdown Mode Reduces Supply Current to 150nA**
- ♦ **SAG Correction Reduces Output-Coupling Capacitors from 330µF to 22µF**
- ♦ **Available in Space-Saving SOT23 and SC70 Packages**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4090EXT-T	-40°C to +85°C	6 SC70-6	ABM
MAX4090EUT-T	-40°C to +85°C	6 SOT23-6	ABOX

Block Diagram



3V/5V, 6dB Video Buffer with Sync-Tip Clamp, Output Sag Correction, and 150nA Shutdown Current

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .... -0.3V to +6V
OUT, SAG, $\overline{SHDN}$ to GND .... -0.3V to (V_{CC} + 0.3V)
IN to GND (Note 1) .... V_{CLP} to (V_{CC} + 0.3V)
IN Short-Circuit Duration from -0.3V to V_{CLP} 1min
Output Short-Circuit Duration to V_{CC} or GND .... Continuous
Continuous Power Dissipation (T_A = +70°C)
6-Pin SOT23 (derate 8.7mW/°C above +70°C) 695mW
6-Pin SC70 (derate 3.1mW/°C above +70°C) 245mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Note 1: V_{CLP} is the input clamp voltage as defined in the *DC Electrical Characteristics* table.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V, GND = 0V, C_{IN} = 0.1µF from IN to GND, R_L = infinity to GND, SAG shorted to OUT, $\overline{SHDN}$ = 3.0V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	Guaranteed by PSRR		2.7		5.5	V
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CLP}	V_{CC} = 3V		6.5	10	mA
			V_{CC} = 5V		6.5	10	
Shutdown Supply Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = 0V			0.15	1	µA
Input Clamp Voltage	V_{CLP}	Input referred		0.27	0.38	0.47	V
Input Voltage Range	V_{IN}	Inferred from voltage gain (Note 3)		V_{CLP}		1.45	V
Input Bias Current	I_{BIAS}	V_{IN} = 1.45V			22.5	35	µA
Input Resistance		V_{CLP} + 0.5V < V_{IN} < V_{CLP} + 1V			3		MΩ
Voltage Gain	A_V	R_L = 150Ω, 0.5V < V_{IN} < 1.45V (Note 4)		1.9	2	2.1	V/V
Power-Supply Rejection Ratio	PSRR	2.7V < V_{CC} < 5.5V		60	80		dB
Output Voltage High Swing	V_{OH}	R_L = 150Ω	V_{CC} = 3V	2.55	2.7		V
			V_{CC} = 5V	4.3	4.6		
Output Voltage Low Swing	V_{OL}	R_L = 150Ω			V_{CLP}	0.47	V
Output Current	I_{OUT}	Sourcing, R_L = 20Ω to GND		45	85		mA
		Sinking, R_L = 20Ω to V_{CC}		40	85		
Output Short-Circuit Current	I_{SC}	OUT shorted to V_{CC} or GND			110		mA
$\overline{SHDN}$ Logic-Low Threshold	V_{IL}					V_{CC} x 0.3	V
$\overline{SHDN}$ Logic-High Threshold	V_{IH}			V_{CC} x 0.7			V
$\overline{SHDN}$ Input Current	I_{IH}				0.003	1	µA
Shutdown Output Impedance	R_{OUT} (Disabled)	$\overline{SHDN}$ = 0V	At DC		4		kΩ
			At 3.58MHz or 4.43MHz		2		

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V, GND = 0V, C_{OUT} = C_{SAG} = 22µF, C_{IN} = 0.1µF, R_{IN} = 75Ω to GND, R_L = 150Ω to GND, $\overline{SHDN}$ = V_{CC}, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth	BW_{SS}	V_{OUT} = 100mV_{P-P}			55		MHz
Large-Signal -3dB Bandwidth	BW_{LS}	V_{OUT} = 2V_{P-P}			45		MHz
Small-Signal 0.1dB Gain Flatness	$BW_{0.1dBSS}$	V_{OUT} = 100mV_{P-P}			25		MHz
Large-Signal 0.1dB Gain Flatness	$BW_{0.1dBLS}$	V_{OUT} = 2V_{P-P}			17		MHz
Slew Rate	SR	V_{OUT} = 2V step			275		V/µs
Settling Time to 0.1%	t_S	V_{OUT} = 2V step			25		ns
Power-Supply Rejection Ratio	PSRR	f = 100kHz			50		dB
Output Impedance	Z_{OUT}	f = 5MHz			2.5		Ω
Differential Gain	DG	NTSC	V_{CC} = 3V		1		%
			V_{CC} = 5V		0.5		
Differential Phase	DP	NTSC	V_{CC} = 3V		0.8		Degrees
			V_{CC} = 5V		0.5		
Group Delay	D/dT	f = 3.58MHz or 4.43MHz			20		ns
Peak Signal to RMS Noise	SNR	V_{IN} = 1V_{P-P}, 10MHz BW			65		dB
Droop		C_{IN} = 0.1µF (Note 4)			2	3	%
$\overline{SHDN}$ Enable Time	t_{ON}	V_{IN} = V_{CLP} + 1V, $\overline{SHDN}$ = 3V, V_{OUT} settled to within 1% of the final voltage			250		ns
$\overline{SHDN}$ Disable Time	t_{OFF}	V_{IN} = V_{CLP} + 1V, $\overline{SHDN}$ = 0V, V_{OUT} settled to below 1% of the output voltage			50		ns

Note 2: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.

Note 3: Voltage gain (A_V) is referenced to the clamp voltage, i.e., an input voltage of V_{IN} = V_{CLP} + VI would produce an output voltage of V_{OUT} = V_{CLP} + A_V x VI.

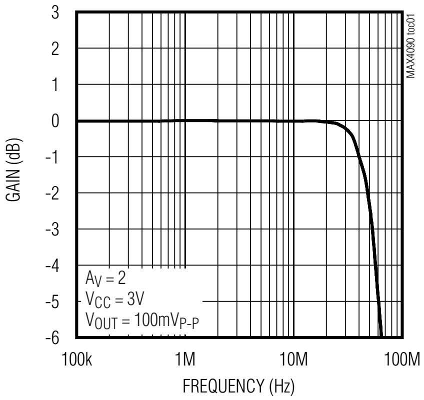
Note 4: Droop is guaranteed by the Input Bias Current specification.

3V/5V, 6dB Video Buffer with Sync-Tip Clamp, Output Sag Correction, and 150nA Shutdown Current

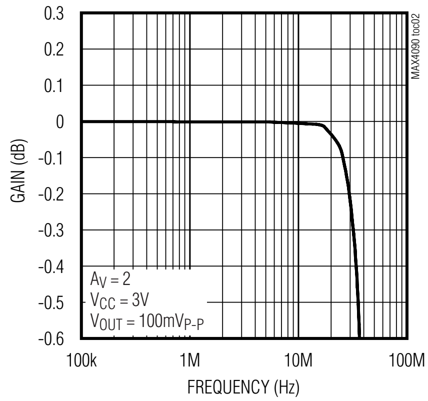
Typical Operating Characteristics

(V_{CC} = 3.0V, GND = 0V, C_{OUT} = C_{SAG} = 22µF, C_{IN} = 0.1µF, R_{IN} = 75Ω to GND, R_L = 150Ω to GND, $\overline{SHDN}$ = V_{CC}, T_A = +25°C, unless otherwise noted.)

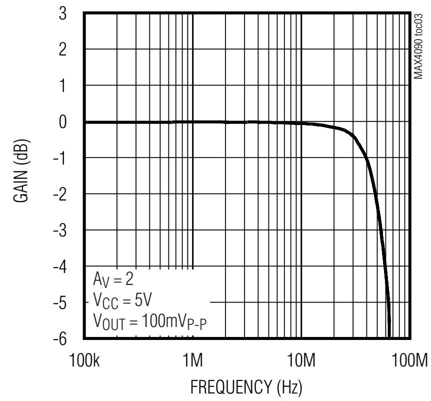
SMALL-SIGNAL GAIN vs. FREQUENCY



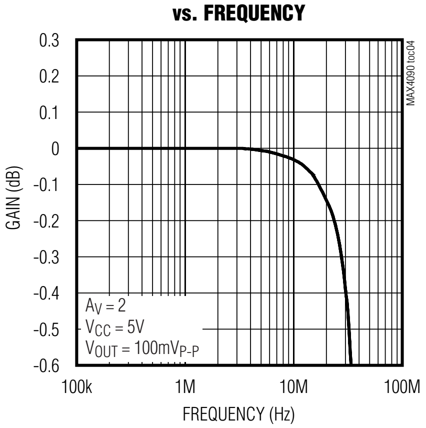
SMALL-SIGNAL GAIN FLATNESS vs. FREQUENCY



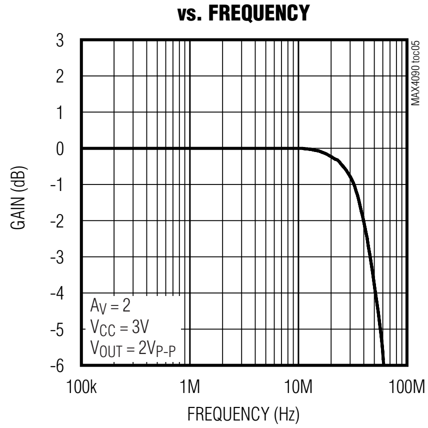
SMALL-SIGNAL GAIN vs. FREQUENCY



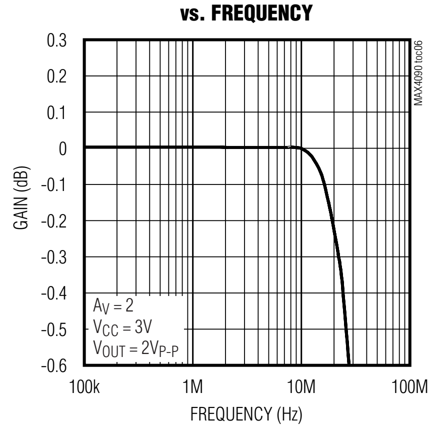
SMALL-SIGNAL GAIN FLATNESS vs. FREQUENCY



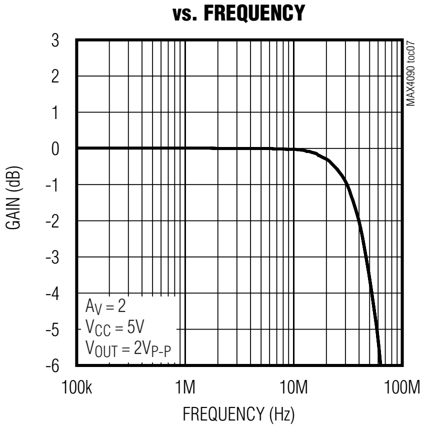
LARGE-SIGNAL GAIN vs. FREQUENCY



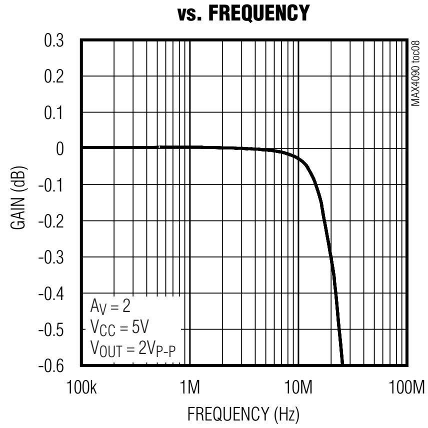
LARGE-SIGNAL GAIN FLATNESS vs. FREQUENCY



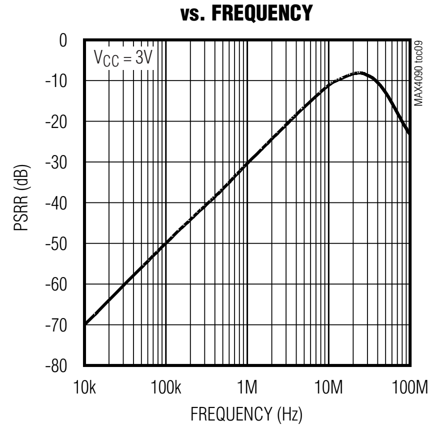
LARGE-SIGNAL GAIN vs. FREQUENCY



LARGE-SIGNAL GAIN FLATNESS vs. FREQUENCY



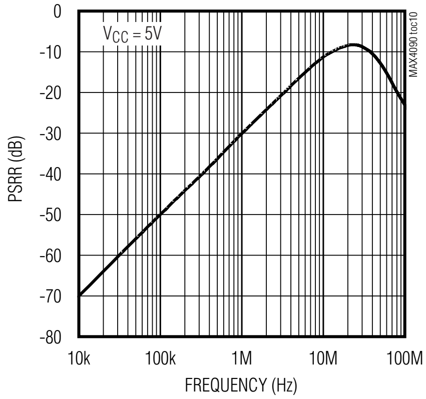
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



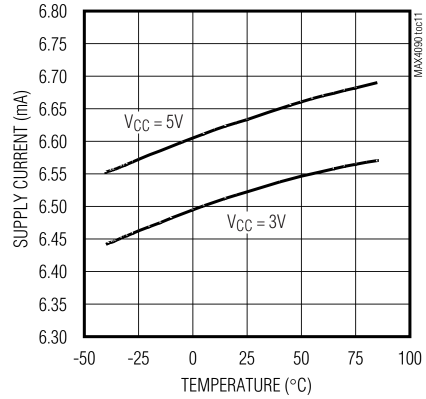
Typical Operating Characteristics (continued)

(V_{CC} = 3.0V, GND = 0V, C_{OUT} = C_{SAG} = 22µF, C_{IN} = 0.1µF, R_{IN} = 75Ω to GND, R_L = 150Ω to GND, $\overline{SHDN}$ = V_{CC}, T_A = +25°C, unless otherwise noted.)

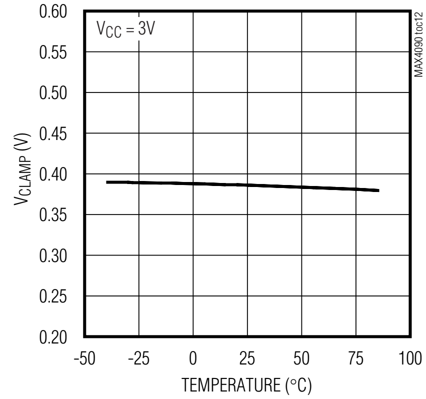
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



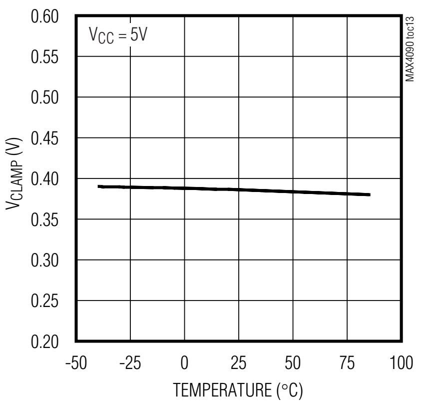
QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



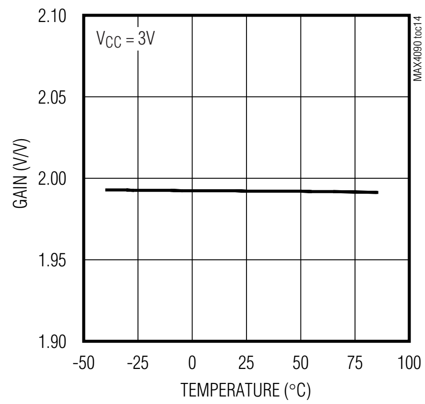
CLAMP VOLTAGE vs. TEMPERATURE



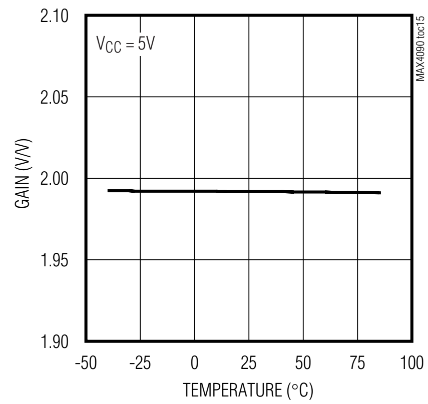
CLAMP VOLTAGE vs. TEMPERATURE



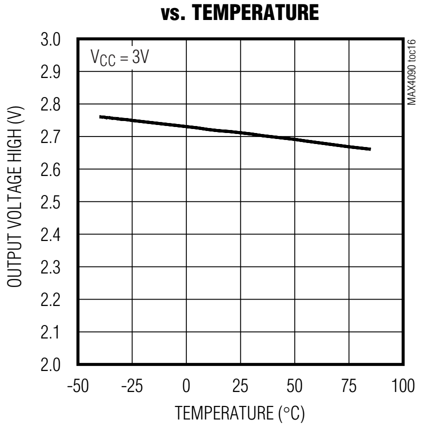
VOLTAGE GAIN vs. TEMPERATURE



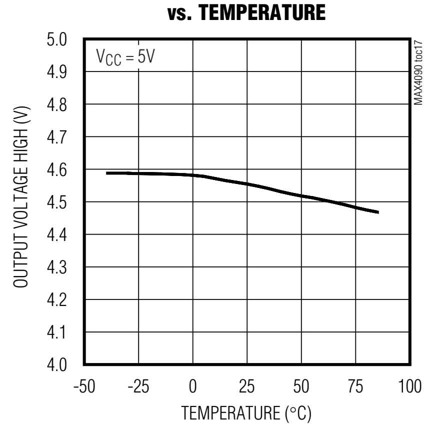
VOLTAGE GAIN vs. TEMPERATURE



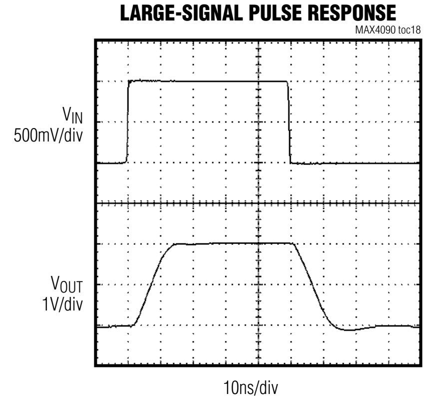
OUTPUT VOLTAGE HIGH SWING vs. TEMPERATURE



OUTPUT VOLTAGE HIGH SWING vs. TEMPERATURE



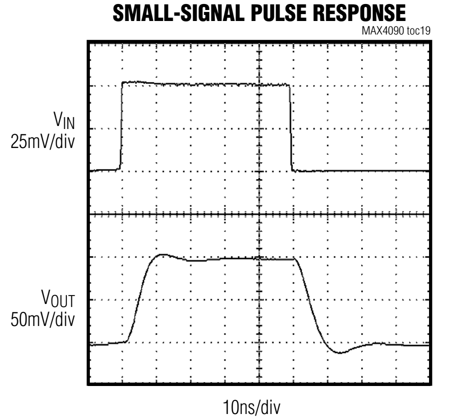
LARGE-SIGNAL PULSE RESPONSE

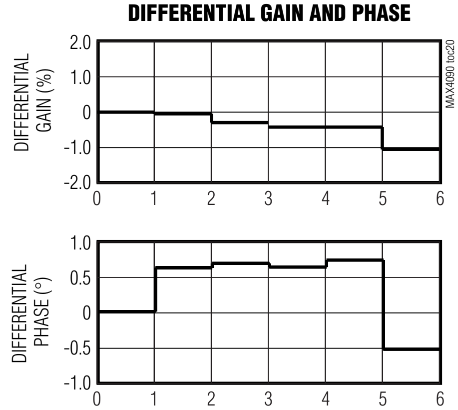


3V/5V, 6dB Video Buffer with Sync-Tip Clamp, Output Sag Correction, and 150nA Shutdown Current

Typical Operating Characteristics (continued)

(V_{CC} = 3.0V, GND = 0V, C_{OUT} = C_{SAG} = 22µF, C_{IN} = 0.1µF, R_{IN} = 75Ω to GND, R_L = 150Ω to GND, $\overline{SHDN}$ = V_{CC}, T_A = +25°C, unless otherwise noted.)

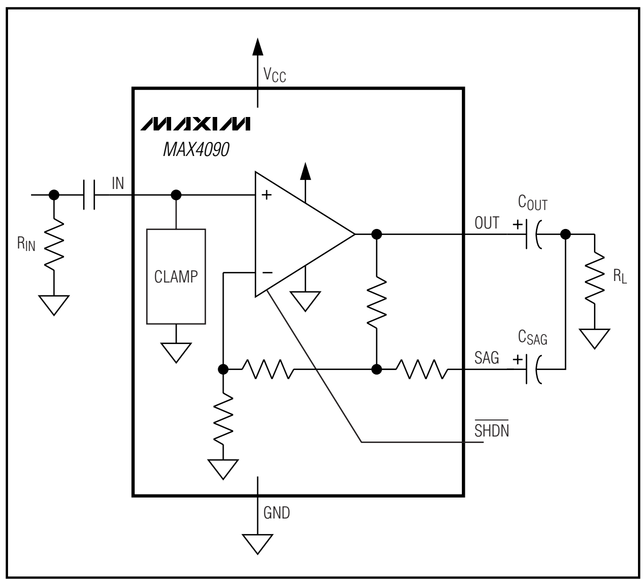




Pin Description

PIN	NAME	FUNCTION
1	OUT	Video Output
2	GND	Ground
3	IN	Video Input
4	V_{CC}	Power-Supply Voltage. Bypass with a 0.1µF capacitor to ground as close to pin as possible.
5	$\overline{SHDN}$	Shutdown. Pull $\overline{SHDN}$ low to place the MAX4090 in low-power shutdown mode.
6	SAG	Sag Correction

Typical Application Circuit



Detailed Description

The MAX4090 3V/5V, 6dB video buffer with sync-tip clamp, output sag correction, and low-power shutdown mode is available in tiny SOT23 and SC70 packages. The sag-corrected output of the MAX4090 is designed to drive AC-coupled, 150Ω back-terminated video loads in portable video applications such as digital still cams, portable DVD players, digital camcorders, PDAs, video-enabled cell phones, portable game systems, and notebook computers. The sag correction feature introduces low-frequency compensation that reduces the value of the normally bulky and expensive 330µF AC-coupling capacitor to two small, less expensive 22µF capacitors. The input clamp positions the video waveform at the output and allows the MAX4090 to be used as either an AC- or DC-coupled output driver.

The MAX4090 operates from a single 2.7V to 5.5V supply and consumes only 6.5mA of supply current. The low-power shutdown mode reduces the supply current to 150nA, making the MAX4090 ideal for low-voltage, battery-powered video applications.

The input signal to the MAX4090 is AC-coupled through a capacitor into an active sync-tip clamp circuit, which places the minimum of the video signal at approximately 0.38V. The output buffer amplifies the video signal while still maintaining the 0.38V clamp voltage at the output. For example, if V_{IN} = 0.38V, then V_{OUT} = 0.38V. If V_{IN} = (0.38V + 1V) = 1.38V, then V_{OUT} = (0.38V + 2 X (1V)) = 2.38V when SAG is shorted OUT. The net result is that a 2V video output signal swings within the usable output voltage range of the output buffer when V_{CC} = 3V.

There are two common output connections for the MAX4090:

1) SAG is shorted to OUT and 150Ω is directly connected from OUT to ground (see Figure 2).
2) Two capacitors and 150Ω are connected between OUT, SAG, and ground (see Figure 3).

Sag Correction

Sag correction refers to the low-frequency compensation of the highpass filter formed by the 150Ω load of a back-terminated coax and the output-coupling capacitor. This break point must be low enough in frequency to pass the Vertical Sync Interval *(<25Hz for PAL and <30Hz for NTSC)* to avoid Field Tilt. Traditionally, the break point is made <3~5Hz, and the coupling capacitor must be very large, typically >330µF. The MAX4090 reduces the value of this coupling capacitor, replacing it with a pair of 22µF capacitors. This is done by putting a resistor network in series with the feedback, raising the gain, and creating a high-impedance node at the SAG output. This node is AC-coupled to the load in parallel with the normal output, as shown in Figure 3. This allows the use of two smaller capacitors (C_{OUT} and C_{SAG}), typically 22µF, substantially reducing the size of the interface caps and their cost while retaining the low-frequency response.

The minimum value of the output-coupling capacitor is a function of the acceptable Field Tilt. In Figure 1, the Field Tilt is given for several values of capacitance from 10µF to 47µF for comparison. Although values lower than 22µF may have acceptable Field Tilt, they are not recommended, since tolerance, aging, and voltage and temperature coefficients reduce the capacitance in actual applications. Increasing the output-coupling capacitors beyond 47µF does not improve performance.

Shutdown Mode

The MAX4090 features a low-power shutdown mode ($I_{\overline{SHDN}}$ = 150nA) for battery-powered/portable applications. Pulling the $\overline{SHDN}$ pin high enables the output. Connecting the $\overline{SHDN}$ pin to ground (GND) disables the output and places the MAX4090 into a low-power shutdown mode.

Applications Information

Input Coupling the MAX4090

The MAX4090 input must be AC-coupled because the input capacitor stores the clamp voltage. The MAX4090 requires a typical value of 0.1µF for the input clamp to meet the Line Droop specification. A minimum of a ceramic capacitor with an X7R temperature coefficient is recommended to avoid temperature-related prob-

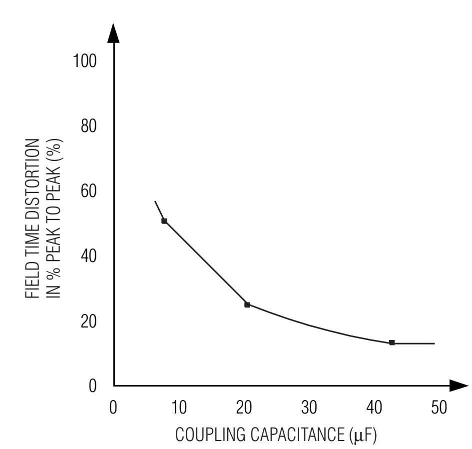


Figure 1. Field Tilt vs. Output-Coupling Capacitance

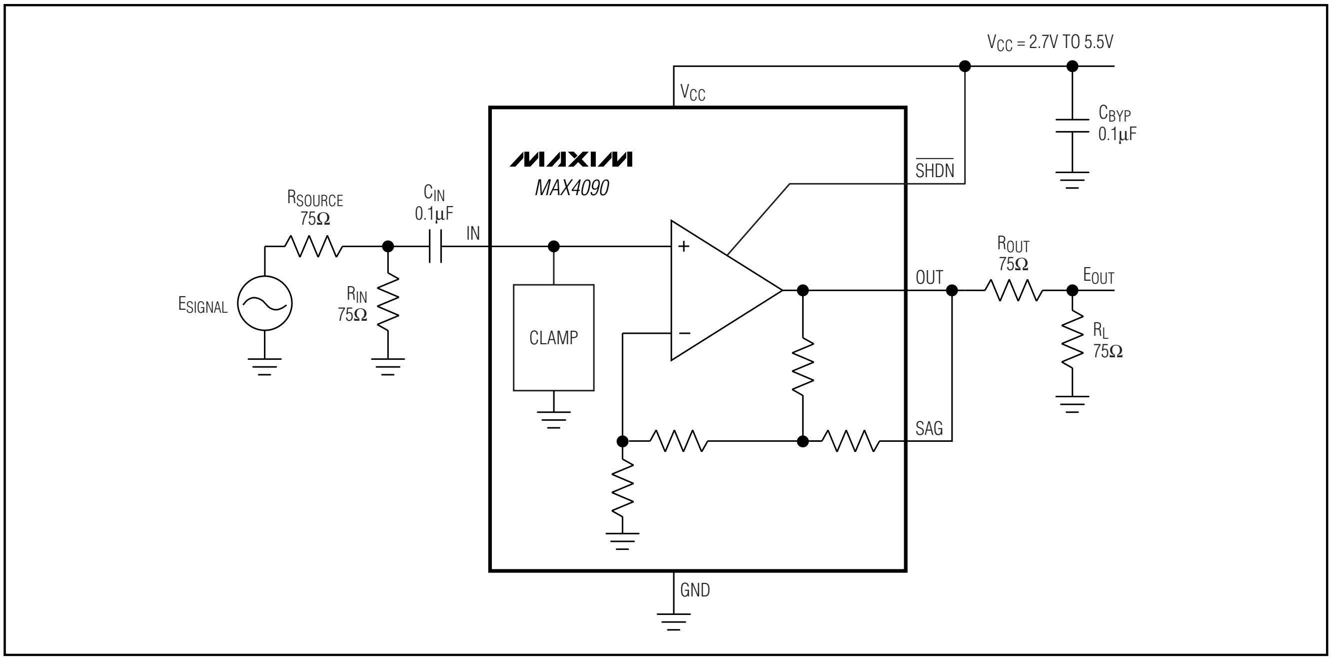


Figure 2. DC-Coupling the MAX4090

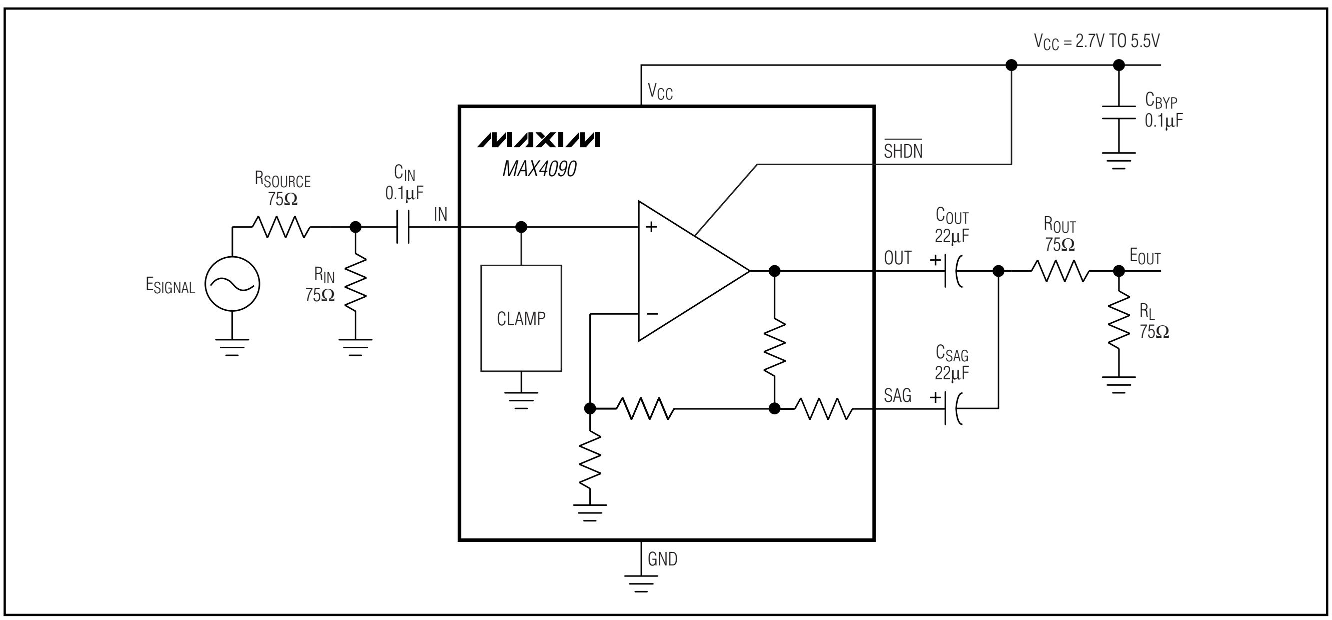


Figure 3. AC-Coupling the MAX4090

lems with Line Droop. For extended temperature operation, such as outdoor applications, or where the impressed voltage is close to the rated voltage of the capacitor, a film dielectric is recommended. Increasing the capacitor value slows the clamp capture time. Values above 0.5µF should be avoided since they do not improve the clamp's performance.

The active sync-tip clamp also requires that the input impedance seen by the input capacitor be less than 100Ω typically to function properly. This is easily met by the 75Ω input resistor prior to the input-coupling capacitor and the back termination from a prior stage. Insufficient input resistance to ground causes the MAX4090 to appear to oscillate. Never operate the MAX4090 in this mode.

Output Coupling the MAX4090

The output of the MAX4090 can be AC- or DC-coupled to the load. In the DC-coupled mode, the MAX4090 provides accurate sync-tip clamping for single-supply operation and still can drive a 150Ω, back-terminated load. In the AC-coupled mode, the MAX4090 allows the use of minimal size capacitors to drive a back-terminated video load of 150Ω.

DC-Coupling the Output

By shorting SAG to OUT, the device becomes an amplifier with DC restore, optimally placing the video within the dynamic range of the output. In this mode, the MAX4090 can be used as the input conditioner for a video signal, providing gain and biasing in single-supply applications. DC-coupling also improves the MAX4090's performance in terms of differential gain and phase. This reflects the improvement in the low-frequency response due to DC-coupling.

AC-Coupling the Output

The MAX4090's output is configured to support AC-coupling with minimal capacitance. This is called "sag correction." It refers to the improved bandwidth achieved by using two smaller capacitors to replace a single large capacitor shown in Figure 3.

Layout and Power-Supply Bypassing

The MAX4090 operates from single 2.7V to 5.5V supply. Bypass the supply with a 0.1µF capacitor as close to the pin as possible. Maxim recommends using microstrip and stripline techniques to obtain full bandwidth. To ensure that the PC board does not degrade the device's performance, design it for a frequency greater than 1GHz. Pay careful attention to inputs and outputs to avoid large parasitic capacitance. Whether or not you use a constant-impedance board, observe the following design guidelines:

- Do not use wire-wrap boards; they are too inductive.
- Do not use IC sockets; they increase parasitic capacitance and inductance.
- Use surface-mount instead of through-hole components for better, high-frequency performance.
- Use a PC board with at least two layers; it should be as free from voids as possible.
- Keep signal lines as short and as straight as possible. Do not make 90° turns; round all corners.

Chip Information

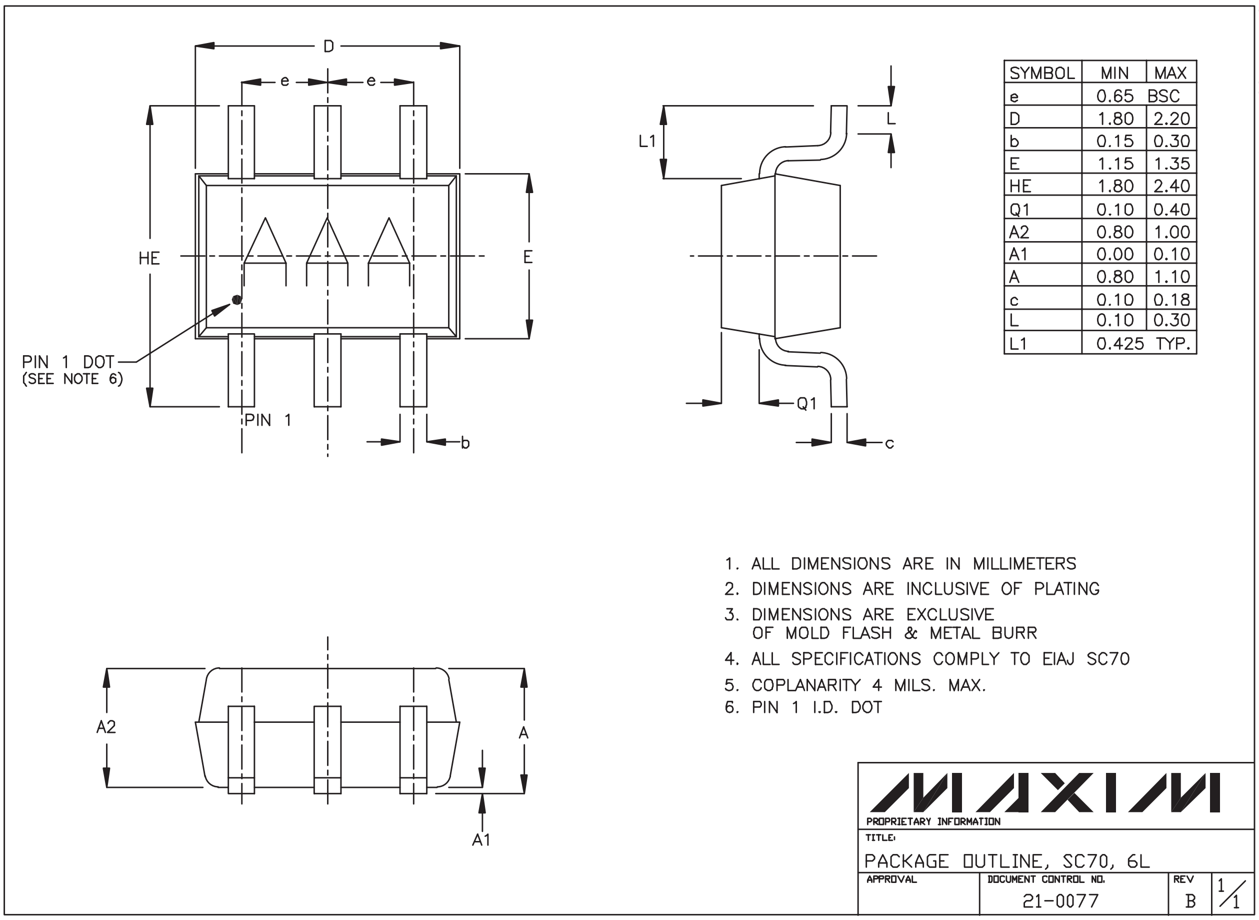
TRANSISTOR COUNT: 755

PROCESS: BiCMOS

3V/5V, 6dB Video Buffer with Sync-Tip Clamp, Output Sag Correction, and 150nA Shutdown Current

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



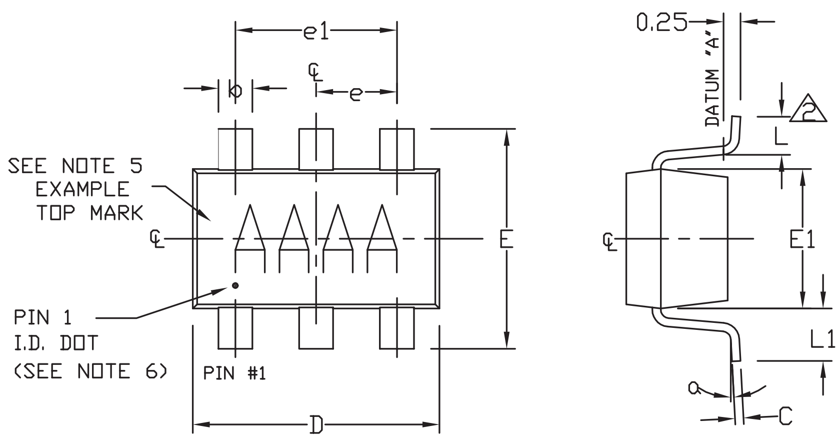
SYMBOL	MIN	MAX
e	0.65	BSC
D	1.80	2.20
b	0.15	0.30
E	1.15	1.35
HE	1.80	2.40
Q1	0.10	0.40
A2	0.80	1.00
A1	0.00	0.10
A	0.80	1.10
c	0.10	0.18
L	0.10	0.30
L1	0.425	TYP.

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS ARE INCLUSIVE OF PLATING
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR
4. ALL SPECIFICATIONS COMPLY TO EIAJ SC70
5. COPLANARITY 4 MILS. MAX.
6. PIN 1 I.D. DOT

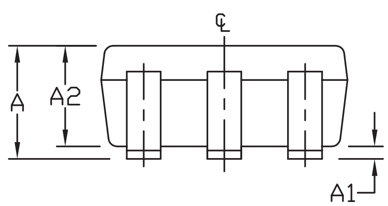
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

6LSOT.EPS



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.60
L1	0.60 REF.	
e1	1.90 BSC.	
e	0.95 BSC.	
α	0°	10°



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25 MM.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
6. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.
7. MEETS JEDEC MO178, VARIATION AB.
8. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEADTIP.
9. LEAD TO BE COPLANAR WITHIN 0.1 MM.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, SOT-23, 6L
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