DALLAS SEMICONDUCTOR MAXIM

DS1830/A
Reset Sequence Pushbutton

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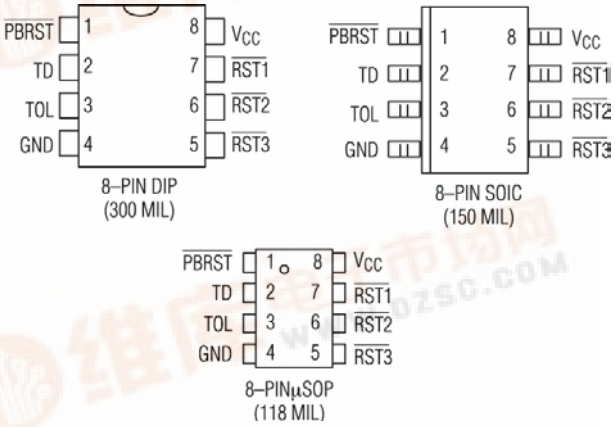
FEATURES

- 5V (DS1830) or 3.3V (DS1830A) power-on reset
- Excellent for systems that need power-on resets in a consistent sequence
- Asserts resets during power transients
- Pushbutton reset input for system override
- Selectable reset timing
- Reduces need for discrete components
- Precision temperature-compensated voltage reference
- 8-pin DIP, 8-pin SO, or space saving 8-pin µSOP
- Operating temperature of -40°C to +85°C
- Open-drain, active-low inputs

PIN ASSIGNMENT



PIN DESCRIPTION

1	$\overline{\text{PBRST}}$	- Pushbutton Reset Input
2	TD	- Time Delay Select Input
3	TOL	- V_{CC} Tolerance Select Input
4	GND	- Ground
8	V_{CC}	- Power Supply
7	$\overline{\text{RST1}}$	- Reset 1 Output
6	$\overline{\text{RST2}}$	- Reset 2 Output
5	$\overline{\text{RST3}}$	- Reset 3 Output

DESCRIPTION

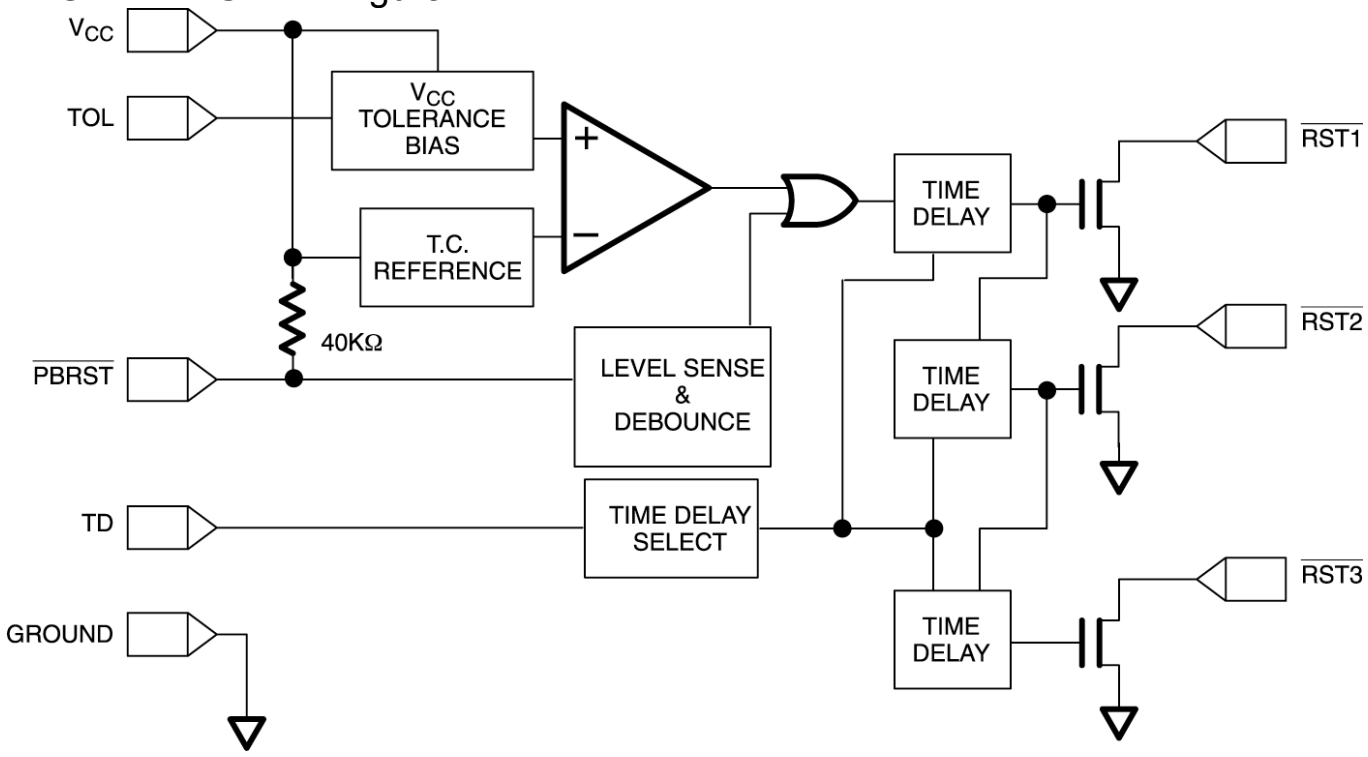
The DS1830 Reset Sequencer monitors the power supply for an in-tolerance condition and the pushbutton reset input for a manual reset. First a precision temperature-compensated reference and comparator circuit monitors the status of the power supply and when an out-of-tolerance condition is detected, an internal power fail signal is generated that forces the reset lines to go to an active state. If the power supply returns to an in-tolerance condition, $\overline{\text{RST1}}$ will release followed by $\overline{\text{RST2}}$ and finally $\overline{\text{RST3}}$. Sequencing of resets allows for systems to power-up in an orderly manner providing superior reliability.

Note: Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: http://dbserv.maxim-ic.com/errata.cfm.

OPERATION — POWER MONITOR

The DS1830 provides the functions of detecting out-of-tolerance conditions on a power supply and warning a processor based system of impending power failure. When V_{CC} is detected as out-of-tolerance all reset outputs will be forced active. When V_{CC} returns to a valid state, $\overline{RST1}$ will remain active for period of time based on the condition of the TD input. Reset outputs $\overline{RST2}$ and $\overline{RST3}$ follow $\overline{RST1}$, each one at the proper delays for the condition of the TD input. All resets will remain in the inactive state (high) until the next V_{CC} out-of-tolerance condition or pushbutton reset. On power-up all resets are kept active for an appropriate period determined by the status of the TD input after the power supply inputs have reached the selected tolerance. This allows the power supply and system power to stabilize before the reset sequences are released.

BLOCK DIAGRAM Figure 1



OPERATION — TOLERANCE SELECT

The DS1830/A provides a TOL input for individual customization of the DS1830x to specific application requirements (see Table 1). For the tolerance selection, see Table 1 below. The TOL input is only sampled while V_{CC} is below the lowest potential trip value and can not be changed after the V_{CC} voltage exceeds the lowest potential trip value.

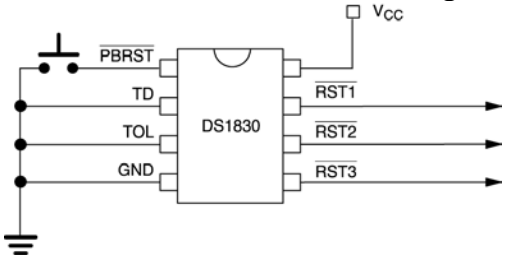
TOL — TOLERANCE SELECT Table 1

TOL	5V (DS1830)	3.3V (DS1830A)
V_{CC}	5%	5%
GND	10%	10%
OPEN (N.C.)	15%	20%

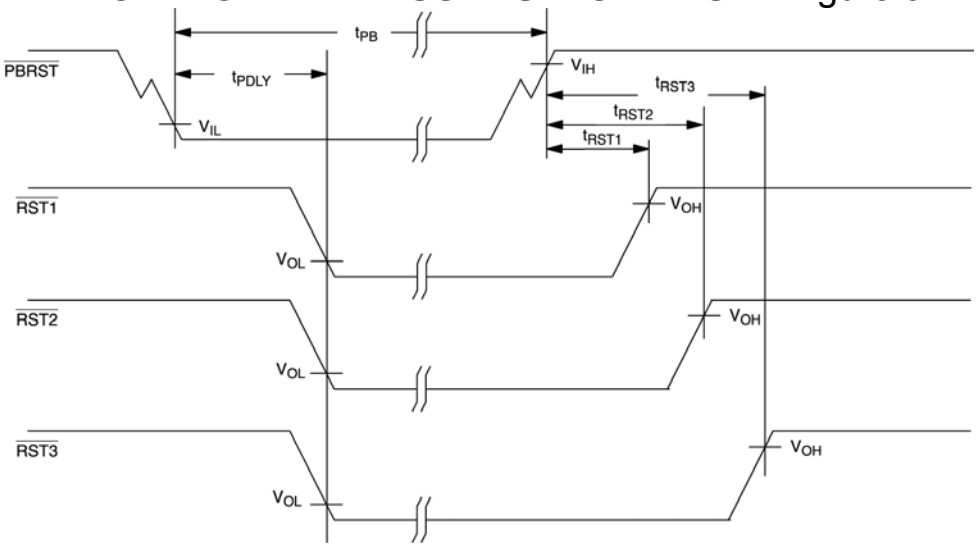
OPERATION — PUSHBUTTON RESET

The DS1830 provides a pushbutton switch for manual reset control. When any of the DS1830/A resets are not active (low) a reset cycle can be initiated by a pushbutton reset. The pushbutton reset is generated by pulling the PBRST pin low for at least 1ms. When the push- button is held low all resets are forced active. The reset will remain active until the pushbutton input is released and then will start a sequenced time-out based on the condition of the TD input. The Pushbutton input is pulled high through an internal 40kΩ pull-up resistor and debounced via internal circuitry. See Figure 2 for an application example and Figure 3 for the timing diagram.

PUSHBUTTON RESET Figure 2



TIMING DIAGRAM — PUSHBUTTON RESET Figure 3



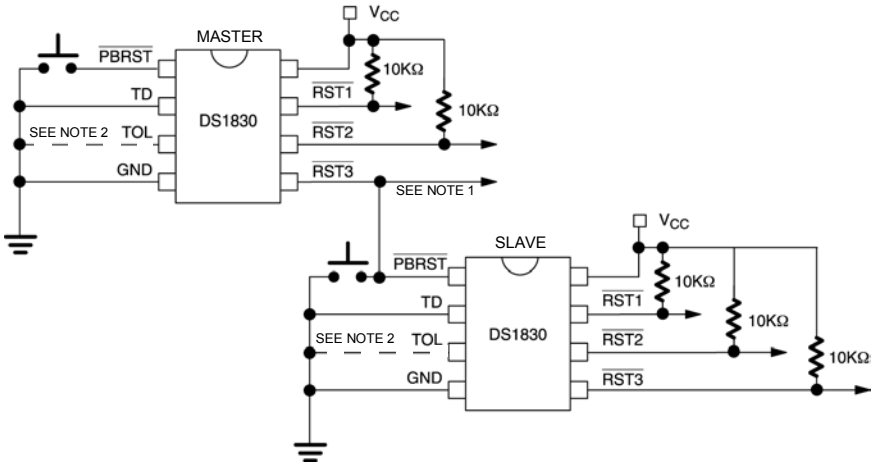
OPERATION — TIME DELAY SELECT

The DS1830 provides an input to select three time delay characteristics for the reset outputs. The TD input has 3 states high (V_{CC}), low (ground) and no connect (N.C.). Table 2 details the minimum timing based on the state of the TD input. If the TD input is connected to ground; $\overline{RST1}$ will have a minimum time delay of 10 ms after V_{CC} is in tolerance. If the TD input is floated; $\overline{RST1}$ will have a minimum time delay of 20 ms after V_{CC} is in tolerance. If the TD input is connected to V_{CC}, $\overline{RST1}$ will have a minimum time delay of 50 ms after V_{CC} is in tolerance. An oscillator and clock chain generate the reset timing with each time delay based on the same device oscillator. The time delay for $\overline{RST2}$ will be 5 times as long as $\overline{RST1}$ and $\overline{RST3}$ will be 10 times the duration of $\overline{RST1}$.

TD CONTROL MINIMUM RESET TIMING Table 2

TD	T_{RST1}	T_{RST2}	T_{RST3}
TD = GND	10ms	50ms	100ms
TD = N.C.	20ms	100ms	200ms
TD = V_{CC}	50ms	250ms	500ms

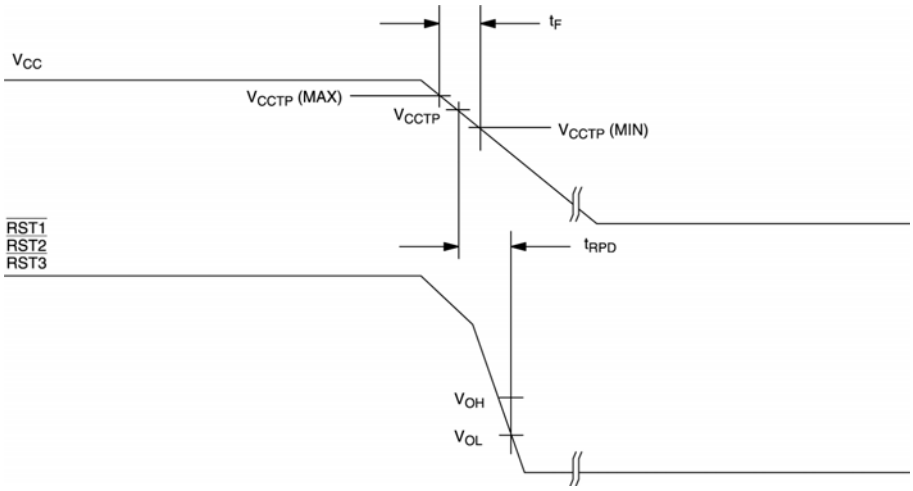
APPLICATION DIAGRAM — CASCADE DELAY CONFIGURATIONS Figure 4



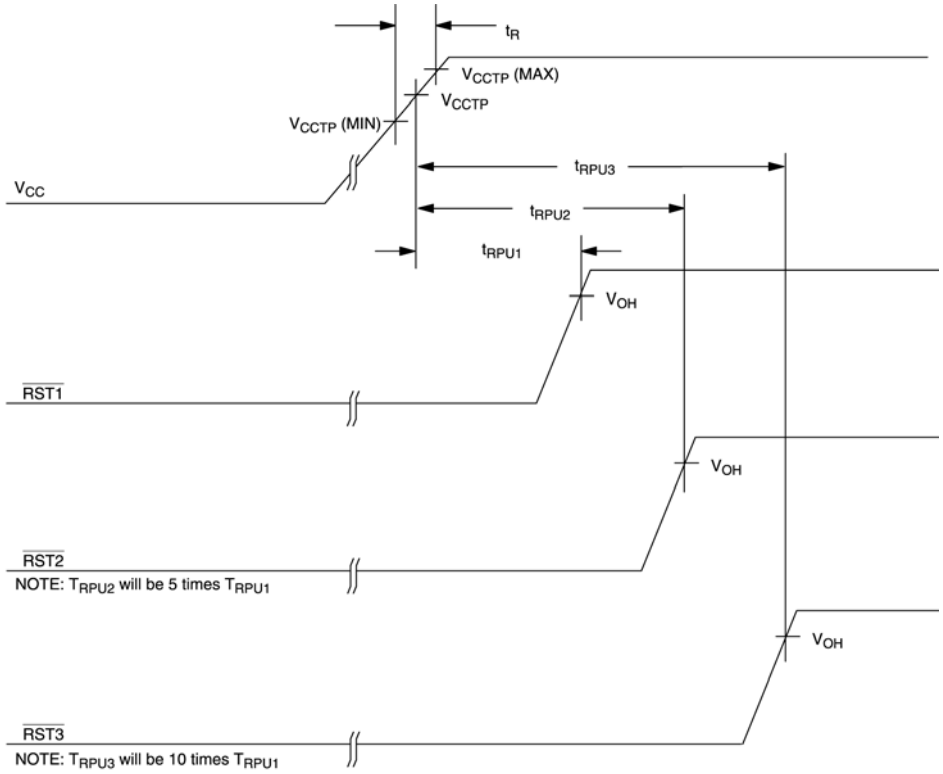
Note 1: The $\overline{RST3}$ output tied to the pushbutton reset would be pulled to V_{CC} through the 40kΩ resistor in the pushbutton input. If a stronger pull-up is required an additional pull-up resistor could be added.

Note 2: When using the cascade configuration, it is important that the TOL pins of the master and the slave are configured so that the master's V_{CCTP} is greater than the slave's V_{CCTP}. This will ensure that when the master's higher V_{CCTP} is crossed, the resets will ripple through to the slave.

TIMING DIAGRAM — POWER-DOWN Figure 5



TIMING DIAGRAM — POWER-UP Figure 6



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +6.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	See IPC/JEDEC J-STD-020A

** This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.*

RECOMMENDED DC OPERATING CONDITIONS (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	1.0		5.5	V	1
$\overline{\text{PBRST}}$ Input High Level	V_{IH}	2.0		V_{CC} + 0.3	V	
$\overline{\text{PBRST}}$ Input Low Level	V_{IL}	-0.3		+0.5	V	

DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{CC} = 1.0V to 5.5V)

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
V_{CC} Trip Point (TOL= V_{CC}) DS1830	V_{CCTP}		4.50	4.62	4.74	V	
V_{CC} Trip Point (TOL=GND) DS1830	V_{CCTP}		4.25	4.37	4.49	V	
V_{CC} Trip Point (TOL=Open) DS1830	V_{CCTP}		4.00	4.13	4.24	V	
V_{CC} Trip Point (TOL= V_{CC}) DS1830A	V_{CCTP}		2.98	3.06	3.15	V	
V_{CC} Trip Point (TOL=GND) DS1830A	V_{CCTP}		2.80	2.88	2.97	V	
V_{CC} Trip Point (TOL=Open) DS1830A	V_{CCTP}		2.47	2.55	2.64	V	
Input Leakage	I_{IL}		-1.0		+1.0	µA	2
Output Current @ 0.4V	I_{OL}		20			mA	3
Operating Current (Standby)	I_{CC}	DS1830		18	35	µA	4
		DS1830A		10	25		

AC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{CC} = 1.0V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PBRST} = V_{IL}$	t_{PB}	t_{PDLY}			ms	
RESET Active Time ($\overline{RST1}$ /TD =GND)	t_{RST1}	10	15	20	ms	
RESET Active Time ($\overline{RST1}$ /TD =Float)	t_{RST1}	20	30	40	ms	
RESET Active Time ($\overline{RST1}$ /TD = V_{CC})	t_{RST1}	50	75	100	ms	
RESET Active Time ($\overline{RST2}$)	t_{RST2}		5x $t_{RST}1$		ms	
RESET Active Time ($\overline{RST3}$)	t_{RST3}		10x $t_{RST}1$		ms	
V_{CC} Detect to RST	t_{RPD}		5	8	µs	5
V_{CC} Slew Rate	t_F	20			µs	6
V_{CC} Detect to RST	t_{RPU}	See RESET Active Times			ms	7
V_{CC} Slew Rate	t_R	0			ns	
$\overline{PBRST}$ Stable Low to RST	t_{PDLY}	1.0	1.5	2.0	ms	

CAPACITANCE (TA = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

NOTES:

1. All voltages are referenced to ground.
2. $\overline{\text{PBRST}}$ is internally pulled up to V_{CC} with an internal impedance of 40kΩ typical.
3. Measured with $\overline{\text{PBRST}} = V_{CC}$ and $\overline{\text{RST1}}$, $\overline{\text{RST2}}$, and $\overline{\text{RST3}}$ open.
4. Measured with outputs open and all inputs at V_{CC} or Ground (except TD and TOL can be floating).
5. Noise Immunity - Pulses < 2ms at V_{CC} TP minimum will not cause a reset.
6. The t_F value is for reference in defining values for t_{RPD} and should not be considered a requirement for proper operation or use of the device.
7. See t_{RST1}, t_{RST2}, and t_{RST3} for specific t_{RPU} AC timing parameters.

ORDERING INFORMATION

PART #	PIN PACKAGE	TEMP	TYPE
DS1830	8-DIP 300-MIL	-40°C to +85°C	5V Reset Sequencer
DS1830S	8-SO 150-MIL	-40°C to +85°C	5V Reset Sequencer
DS1830U	8-µSOP 118-MIL	-40°C to +85°C	5V Reset Sequencer
DS1830A	8-DIP 300-MIL	-40°C to +85°C	3.3V Reset Sequencer
DS1830AS	8-SO 150-MIL	-40°C to +85°C	3.3V Reset Sequencer
DS1830AU	8-µSOP 118-MIL	-40°C to +85°C	3.3V Reset Sequencer