LT1466L/LT1467L

Micropower Dual/Quad Precision Rail-to-Rail Input and Output Op Amps

FEATURES

- **Rail-to-Rail Input and Output**
- **Low Supply Current: 75μA Max**
- **390μV $V_{OS(MAX)}$ for $V_{CM} = V^-$ to V^+**
- **High Common Mode Rejection Ratio: 83dB Min**
- High A_{VOL}: 400V/mV Min
- Wide Supply Range: 2V to ±5V
- Low Input Bias Current: 6nA Typ
- 120kHz Gain Bandwidth Product

APPLICATIONS

- Supply Current Sensing
- Driving A/D Converters
- Test Equipment Amplifiers

DESCRIPTION

The LT®1466L/LT1467L are dual/quad bipolar op amps that combine rail-to-rail input and output operation with precision specifications. Using a patented technique, both input stages of the LT1466L/LT1467L are trimmed: one at the negative supply and the other at the positive supply. The resulting common mode rejection of 83dB minimum is much better than other rail-to-rail input op amps. A minimum open-loop gain of 400V/mV into a 10k load virtually eliminates all gain error. Operation is specified for 3V, 5V and ±5V supplies.
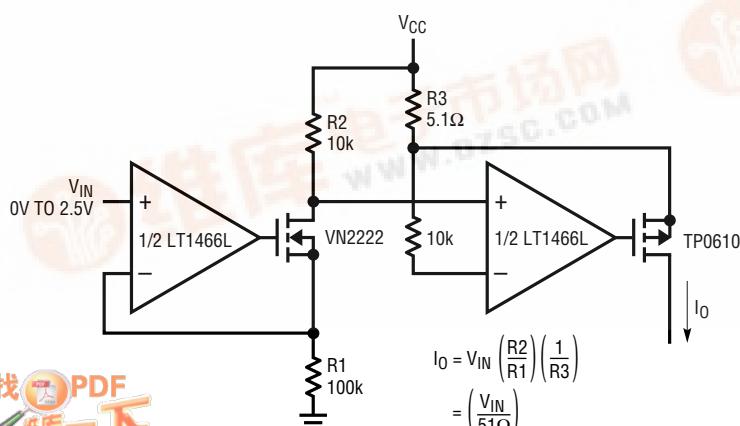
Unlike other rail-to-rail amplifiers, the input offset voltage of 390μV maximum is guaranteed across the entire rail-to-rail input range, not just at half supply. The graph below contrasts the V_{OS} specifications of the LT1466L/LT1467L to a competitive part that is specified only at half supply. As can be seen, the LT1466L/LT1467L's limits are much tighter for inputs near either supply.

The LT1466L is available in 8-lead PDIP and SO-8 packages with the standard dual pinout. The LT1467L features the standard quad pinout and is available in a 16-lead narrow SO package.
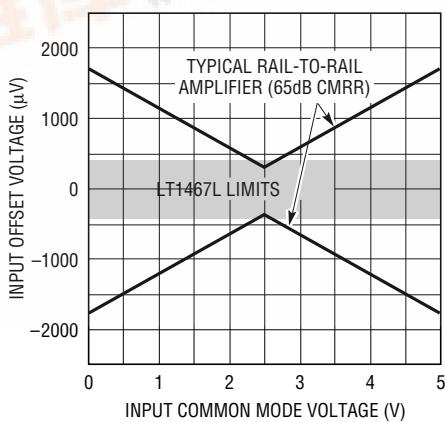
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TYPICAL APPLICATION

Variable Current Source

$$I_O = V_{IN} \left(\frac{R2}{R1} \right) \left(\frac{1}{R3} \right)$$

$$= \left(\frac{V_{IN}}{51\Omega} \right)$$

1466L/67L TA01

Worst-Case V_{OS} vs Input Common Mode Voltage

1466L/67L TA02
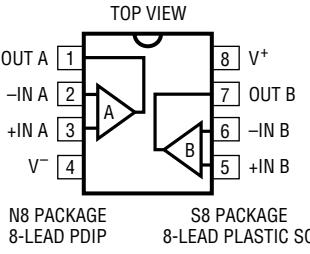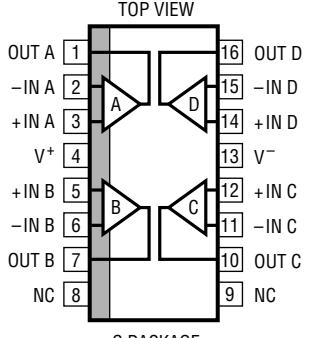
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ....±8V
Input Current ....±15mA
Output Short-Circuit Duration (Note 1) ....Continuous
Specified Temperature Range ....0°C to 70°C

Junction Temperature..150°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ....300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
TOP VIEW OUT A [1] ... [8] V$^+$ −IN A [2] ... [7] OUT B +IN A [3] A ... B [6] −IN B V$^-$ [4] ... [5] +IN B N8 PACKAGE 8-LEAD PDIP · S8 PACKAGE 8-LEAD PLASTIC SO T$_{JMAX}$ = 150°C, θ$_{JA}$ = 130°C/W (N) T$_{JMAX}$ = 150°C, θ$_{JA}$ = 190°C/W (S)	LT1466LCN8 LT1466LCS8
	S8 PART MARKING 1466L

	ORDER PART NUMBER
TOP VIEW OUT A [1] ... [16] OUT D −IN A [2] A ... D [15] −IN D +IN A [3] ... [14] +IN D V$^+$ [4] ... [13] V$^-$ +IN B [5] ... [12] +IN C −IN B [6] B ... C [11] −IN C OUT B [7] ... [10] OUT C NC [8] ... [9] NC S PACKAGE 16-LEAD PLASTIC SO T$_{JMAX}$ = 150°C, θ$_{JA}$ = 150°C/W	LT1467LCS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T$_A$ = 25°C, V$_S$ = 5V, 0V; V$_S$ = 3V, 0V; V$_{CM}$ = V$_O$ = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V$_{OS}$	Input Offset Voltage	V$_{CM}$ = V$^+$			110	390	μV
		V$_{CM}$ = V$^-$			110	390	μV
ΔV$_{OS}$	Input Offset Voltage Shift	V$_{CM}$ = V$^-$ to V$^+$			75	345	μV
	Input Offset Voltage Match (Channel-to-Channel)	V$_{CM}$ = V$^-$, V$^+$ (Notes 3, 4)			150	550	μV
I$_B$	Input Bias Current	V$_{CM}$ = V$^+$			3	14	nA
		V$_{CM}$ = V$^-$		−14	−6		nA
ΔI$_B$	Input Bias Current Shift	V$_{CM}$ = V$^-$ to V$^+$			9	28	nA
I$_{OS}$	Input Offset Current	V$_{CM}$ = V$^+$			0.6	3.6	nA
		V$_{CM}$ = V$^-$			0.4	3.6	nA
ΔI$_{OS}$	Input Offset Current Shift	V$_{CM}$ = V$^-$ to V$^+$			0.9	5.1	nA
	Input Bias Current Match (Channel-to-Channel)	V$_{CM}$ = V$^+$ (Note 4)			0.6	5.1	nA
		V$_{CM}$ = V$^-$ (Note 4)			0.6	5.1	nA
e$_n$	Input Noise Voltage Density	f = 1kHz			45		nV/√Hz
i$_n$	Input Noise Current Density	f = 1kHz			0.05		pA/√Hz
A$_{VOL}$	Large-Signal Voltage Gain	V$_S$ = 5V, V$_O$ = 0.5V to 4.4V, R$_L$ = 10k		400	1500		V/mV
		V$_S$ = 3V, V$_O$ = 0.5V to 2.4V, R$_L$ = 10k		250	1000		V/mV

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = 5V$, $0V$; $V_S = 3V$, $0V$; $V_{CM} = V_O$ = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^-$ to V^+, $V_S = 5V$		83	96		dB
	CMRR Match (Channel-to-Channel)	$V_{CM} = V^-$ to V^+, $V_S = 5V$ (Note 4)		80	93		dB
PSRR	Power Supply Rejection Ratio	$V_S = 2.3V$ to $12V$, $V_{CM} = V_O = 0.5V$		90	105		dB
	PSRR Match (Channel-to-Channel)	$V_S = 2.3V$ to $12V$, $V_{CM} = V_O = 0.5V$ (Note 4)		84	105		dB
V_{OL}	Output Voltage Swing LOW	No Load			32	60	mV
		$I_{SINK} = 0.5mA$			135	270	mV
		$I_{SINK} = 2.5mA$			235	470	mV
V_{OH}	Output Voltage Swing HIGH	No Load		$V^+ - 0.052$	$V^+ - 0.026$		V
		$I_{SOURCE} = 0.5mA$		$V^+ - 0.270$	$V^+ - 0.135$		V
		$I_{SOURCE} = 2.5mA$		$V^+ - 0.570$	$V^+ - 0.265$		V
I_{SC}	Short-Circuit Current			10	17		mA
I_S	Supply Current per Amplifier				60	75	µA

$0°C \leq T_A \leq 70°C$, $V_S = 5V$, $0V$; $V_S = 3V$, $0V$; $V_{CM} = V_O$ = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$	●		140	585	µV
		$V_{CM} = V^-$	●		140	585	µV
V_{OS} TC	Input Offset Voltage Drift (Note 2)		●		2	7	µV/°C
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^-$ to V^+	●		80	500	µV
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^-$, V^+ (Notes 3, 4)	●		170	825	µV
I_B	Input Bias Current	$V_{CM} = V^+$	●		8	16	nA
		$V_{CM} = V^-$	●	−16	−8		nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^-$ to V^+	●		16	32	nA
I_{OS}	Input Offset Current	$V_{CM} = V^+$	●		0.7	5.3	nA
		$V_{CM} = V^-$	●		0.5	5.3	nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^-$ to V^+	●		0.8	7.5	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+$ (Note 4)	●		0.7	7.5	nA
		$V_{CM} = V^-$ (Note 4)	●		0.6	7.5	nA
A_{VOL}	Large-Signal Voltage Gain	$V_S = 5V$, $V_O = 0.5V$ to $4.4V$, $R_L = 10k$	●	100	500		V/mV
		$V_S = 3V$, $V_O = 0.5V$ to $2.4V$, $R_L = 10k$	●	70	400		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^-$ to V^+, $V_S = 5V$	●	80	96		dB
	CMRR Match (Channel-to-Channel)	$V_{CM} = V^-$ to V^+, $V_S = 5V$ (Note 4)	●	75	93		dB
PSRR	Power Supply Rejection Ratio	$V_S = 2.3V$ to $12V$, $V_{CM} = V_O = 0.5V$	●	80	105		dB
	PSRR Match (Channel-to-Channel)	$V_S = 2.3V$ to $12V$, $V_{CM} = V_O = 0.5V$ (Note 4)	●	80	105		dB
V_{OL}	Output Voltage Swing LOW	No Load	●		42	80	mV
		$I_{SINK} = 0.5mA$	●		150	300	mV
		$I_{SINK} = 2.5mA$	●		270	540	mV
V_{OH}	Output Voltage Swing HIGH	No Load	●	$V^+ - 0.065$	$V^+ - 0.033$		V
		$I_{SOURCE} = 0.5mA$	●	$V^+ - 0.305$	$V^+ - 0.155$		V
		$I_{SOURCE} = 2.5mA$	●	$V^+ - 0.620$	$V^+ - 0.310$		V
I_{SC}	Short-Circuit Current		●	7	16		mA
I_S	Supply Current per Amplifier		●		70	85	µA

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = ±5V$, $V_{CM} = V_O = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$			120	475	μV
		$V_{CM} = V^-$			120	475	μV
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^-$ to V^+			80	390	μV
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^-$, V^+ (Notes 3, 4)			150	685	μV
I_B	Input Bias Current	$V_{CM} = V^+$			3	14	nA
		$V_{CM} = V^-$		−14	−6		nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^-$ to V^+			9	28	nA
I_{OS}	Input Offset Current	$V_{CM} = V^+$			0.6	3.6	nA
		$V_{CM} = V^-$			0.4	3.6	nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^-$ to V^+			0.9	5.1	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+$ (Note 4)			0.6	5.1	nA
		$V_{CM} = V^-$ (Note 4)			0.6	5.1	nA
A_{VOL}	Large-Signal Voltage Gain	$V_O = ±4.25V$, $R_L = 10k$		250	450		V/mV
	Channel Separation	$V_O = ±4.25V$, $R_L = 10k$		120	130		dB
SR	Slew Rate	$A_V = −1$, $R_L = ∞$		0.018	0.04		V/μs
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^-$ to V^+		88	102		dB
	CMRR Match (Channel-to-Channel)	$V_{CM} = V^-$ to V^+ (Note 4)		82	99		dB
V_{OL}	Output Voltage Swing LOW	No Load			$V^- + 0.032$	$V^- + 0.060$	V
		$I_{SINK} = 0.5mA$			$V^- + 0.135$	$V^- + 0.270$	V
		$I_{SINK} = 2.5mA$			$V^- + 0.235$	$V^- + 0.470$	V
V_{OH}	Output Voltage Swing HIGH	No Load		$V^+ - 0.052$	$V^+ - 0.026$		V
		$I_{SOURCE} = 0.5mA$		$V^+ - 0.270$	$V^+ - 0.135$		V
		$I_{SOURCE} = 2.5mA$		$V^+ - 0.570$	$V^+ - 0.265$		V
I_{SC}	Short-Circuit Current			10	18		mA
I_S	Supply Current per Amplifier				70	80	μA
GBW	Gain Bandwidth Product	f = 1kHz			120		kHz

$0°C \le T_A \le 70°C$, $V_S = ±5V$, $V_{CM} = V_O = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$	●		150	660	μV
		$V_{CM} = V^-$	●		150	660	μV
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^-$ to V^+	●		90	500	μV
	Input Offset Voltage Match (Channel-to-Channel)	$V_{CM} = V^-$, V^+ (Notes 3, 4)	●		180	900	μV
I_B	Input Bias Current	$V_{CM} = V^+$	●		8	16	nA
		$V_{CM} = V^-$	●	−16	−8		nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^-$ to V^+	●		16	32	nA
I_{OS}	Input Offset Current	$V_{CM} = V^+$	●		0.8	5.3	nA
		$V_{CM} = V^-$	●		0.6	5.3	nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^-$ to V^+	●		0.9	7.5	nA
	Input Bias Current Match (Channel-to-Channel)	$V_{CM} = V^+$ (Note 4)	●		0.7	7.5	nA
		$V_{CM} = V^-$ (Note 4)	●		0.6	7.5	nA
A_{VOL}	Large-Signal Voltage Gain	$V_O = ±4.25V$, $R_L = 10k$	●	100	250		V/mV
	Channel Separation	$V_O = ±4.25V$, $R_L = 10k$	●	120	130		dB
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^-$ to V^+	●	86	101		dB
	CMRR Match (Channel-to-Channel)	$V_{CM} = V^-$ to V^+ (Note 4)	●	80	98		dB

ELECTRICAL CHARACTERISTICS

$0°C \leq T_A \leq 70°C$, $V_S = \pm 5V$, $V_{CM} = V_O = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	Output Voltage Swing LOW	No Load	●		$V^- + 0.042$	$V^- + 0.080$	V
		$I_{SINK} = 0.5mA$	●		$V^- + 0.150$	$V^- + 0.300$	V
		$I_{SINK} = 2.5mA$	●		$V^- + 0.270$	$V^- + 0.540$	V
V_{OH}	Output Voltage Swing HIGH	No Load	●	$V^+ - 0.065$	$V^+ - 0.033$		V
		$I_{SOURCE} = 0.5mA$	●	$V^+ - 0.305$	$V^+ - 0.155$		V
		$I_{SOURCE} = 2.5mA$	●	$V^+ - 0.620$	$V^+ - 0.310$		V
I_{SC}	Short-Circuit Current		●	7	18		mA
I_S	Supply Current per Amplifier		●		70	90	µA

The ● denotes specifications which apply over the full operating temperature range.
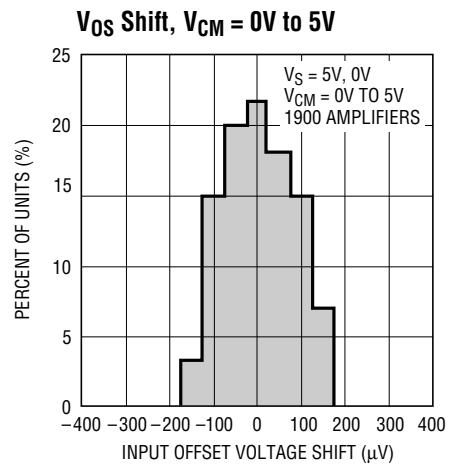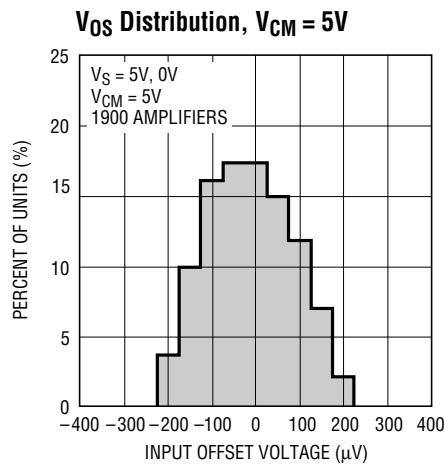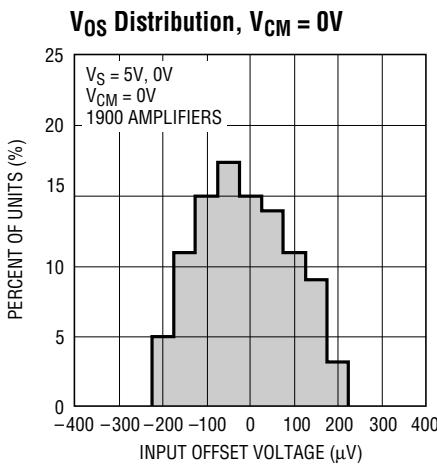
Note 1: A heat sink may be required to keep the junction temperature below the Absolute Maximum Rating when the output is shorted indefinitely.

Note 2: This parameter is not 100% tested.

Note 3: Input offset match is the difference in offset voltage between amplifiers measured at both $V_{CM} = V^-$ and $V_{CM} = V^+$.

Note 4: Matching parameters are the difference between amplifiers A and D and between B and C.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{OS} Distribution, V_{CM} = 0V

V_{OS} Distribution, V_{CM} = 5V

V_{OS} Shift, V_{CM} = 0V to 5V
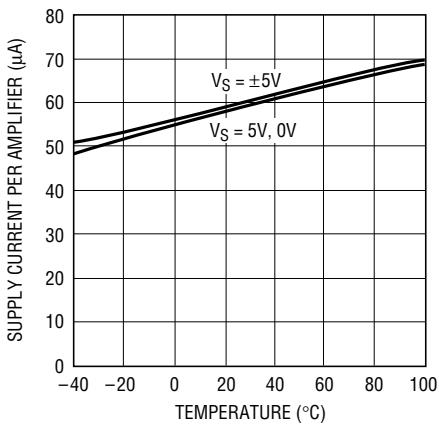
LT1466L/LT1467L
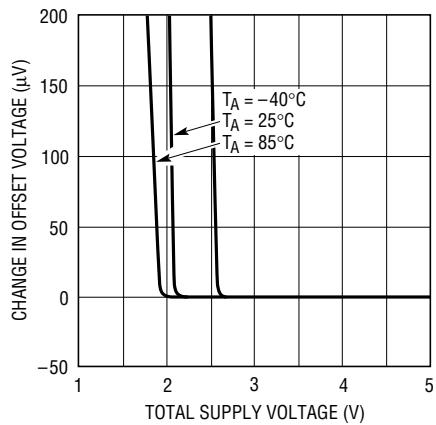
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Temperature

$V_S = \pm 5V$

$V_S = 5V, 0V$
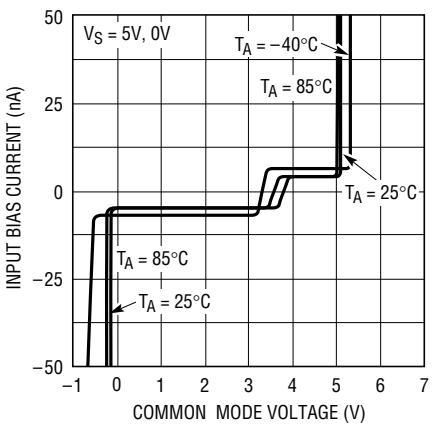
1466L/67L G04

Minimum Supply Voltage

$T_A = -40°C$
$T_A = 25°C$
$T_A = 85°C$
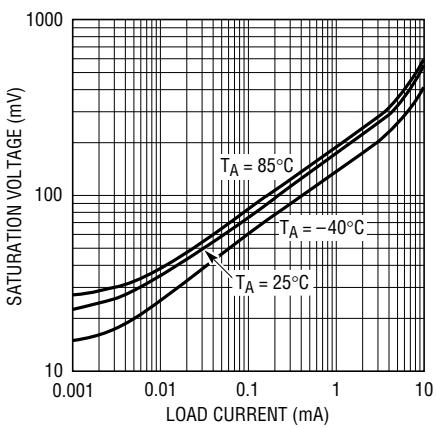
1466L/67L G05

**Input Bias Current
vs Common Mode Voltage**

$V_S = 5V, 0V$
$T_A = -40°C$
$T_A = 85°C$
$T_A = 25°C$
$T_A = 85°C$
$T_A = 25°C$
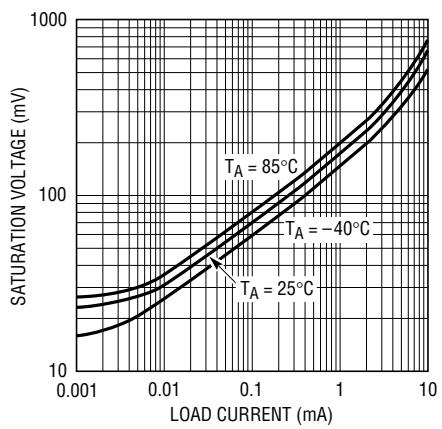
1466L/67L G06

**Output Saturation Voltage
vs Load Current (Output Low)**

$T_A = 85°C$
$T_A = -40°C$
$T_A = 25°C$
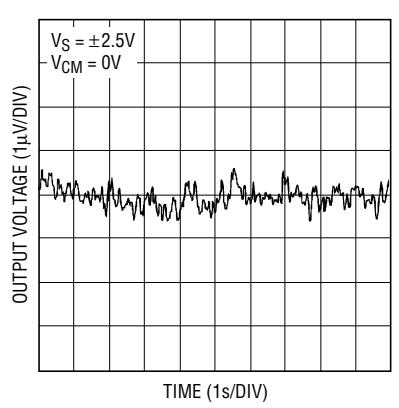
1466L/67L G07

**Output Saturation Voltage
vs Load Current (Output High)**

$T_A = 85°C$
$T_A = -40°C$
$T_A = 25°C$
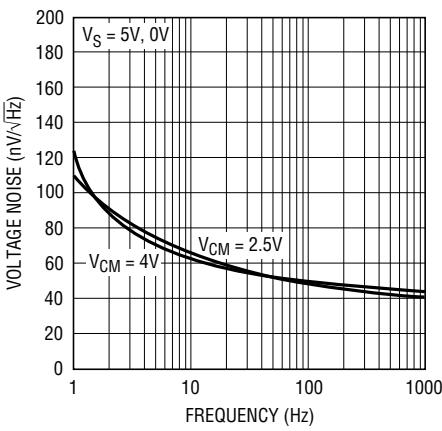
1466L/67L G08

**0.1Hz to 10Hz
Output Voltage Noise**

$V_S = \pm 2.5V$
$V_{CM} = 0V$
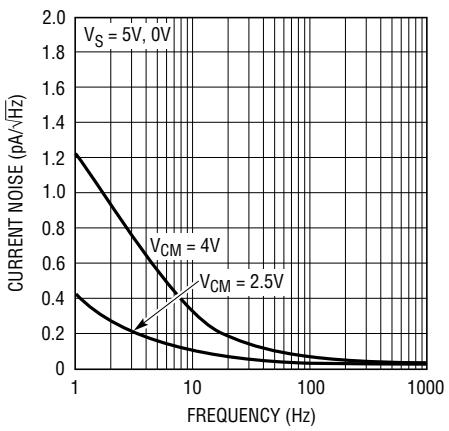
1466L/67L G09

Voltage Noise Spectrum

$V_S = 5V, 0V$
$V_{CM} = 2.5V$
$V_{CM} = 4V$
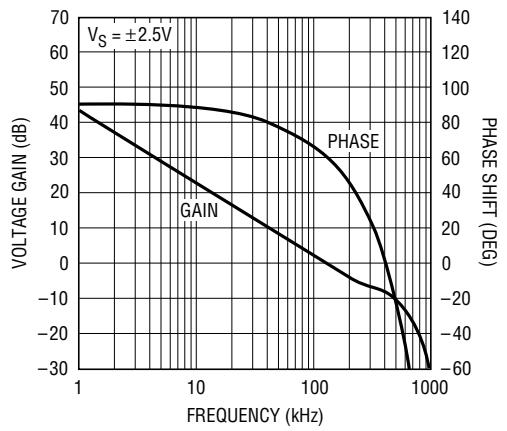
1466L/67L G10

Current Noise Spectrum

$V_S = 5V, 0V$
$V_{CM} = 4V$
$V_{CM} = 2.5V$

1466L/67L G11

Gain and Phase Shift vs Frequency

$V_S = \pm 2.5V$
PHASE
GAIN
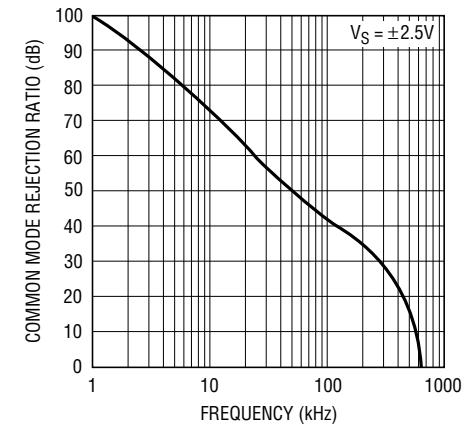
1466L/67L G12

TYPICAL PERFORMANCE CHARACTERISTICS

Gain Bandwidth and Phase Margin vs Supply Voltage

Common Mode Rejection Ratio vs Frequency
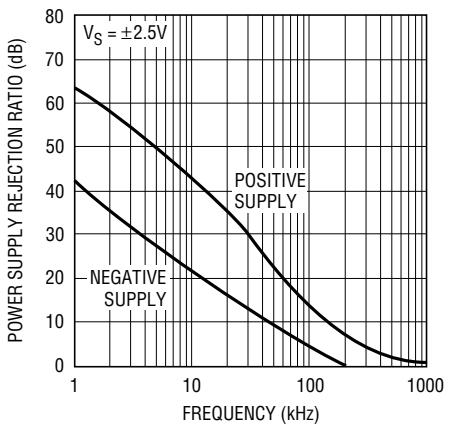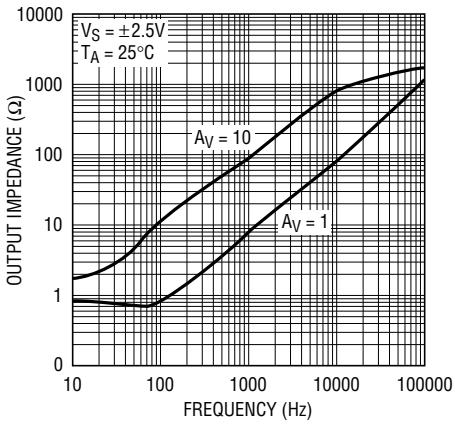
Power Supply Rejection Ratio vs Frequency

1466L/67L G13
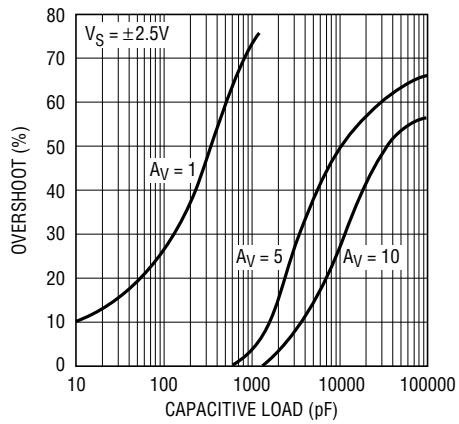
1466L/67L G14

1466L/67L G15

Closed-Loop Output Impedance vs Frequency
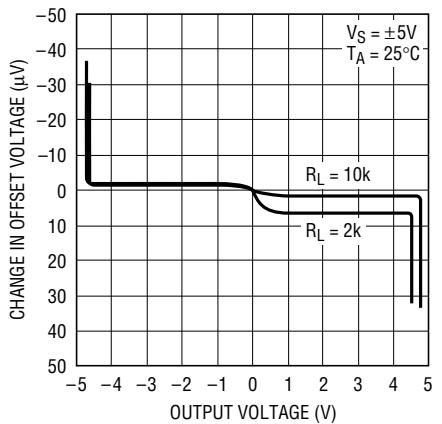
Capacitive Load Handling
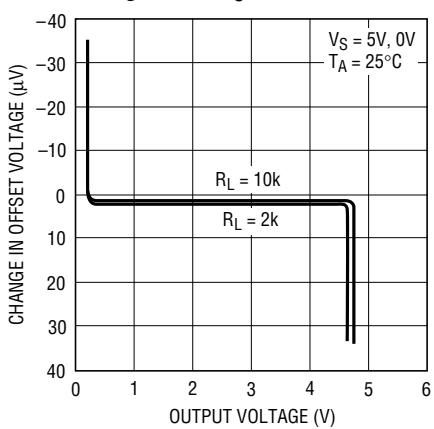
Voltage Gain, $V_S = \pm 5V$

1466L/67 G16
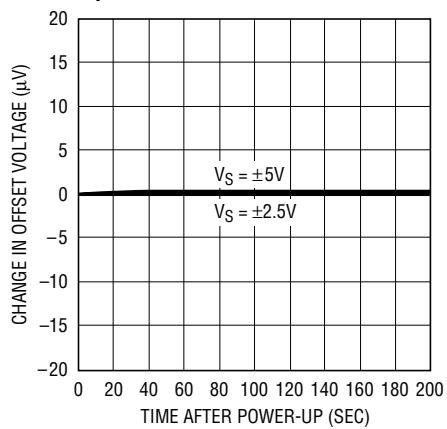
1466L/67L G17

1466L/67L G18

Voltage Gain, $V_S = 5V, 0V$
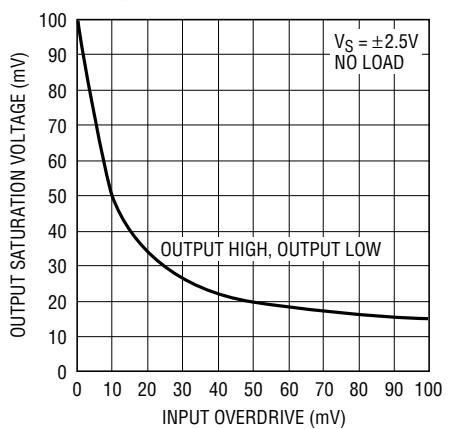
Input Offset Drift vs Time
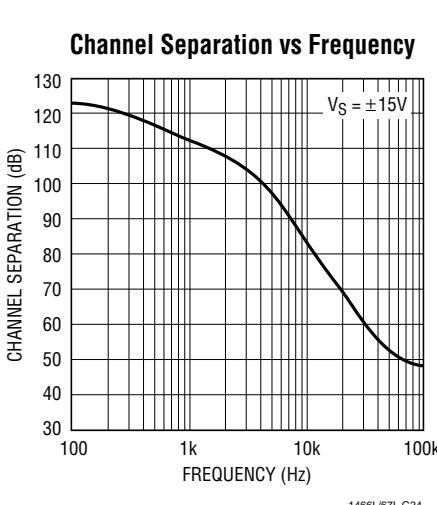
Output Saturation Voltage vs Input Overdrive

1466L/67L G19

1466L/67L G20

1466L/67/ G21

TYPICAL PERFORMANCE CHARACTERISTICS

Channel Separation vs Frequency

1466L/67L G24
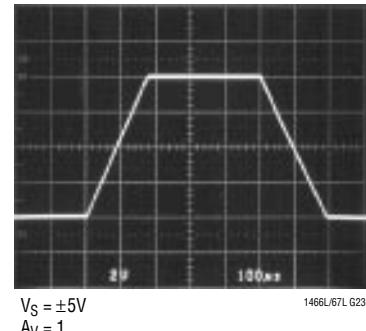
Small-Signal Response
$V_S = \pm 2.5V$

$V_S = \pm 2.5V$
$A_V = 1$

1466L/67L G22

Large-Signal Response
$V_S = \pm 5V$

$V_S = \pm 5V$
$A_V = 1$

1466L/67L G23

APPLICATIONS INFORMATION

Rail-to-Rail Operation

The LT1466L/LT1467L differ from conventional op amps in the design of both the input and output stages. Figure 1 shows a simplified schematic. The input stage consists of two differential amplifiers, a PNP stage Q1-Q2 and an NPN stage Q3-Q4, that are active over different portions of the input common mode range. Each input stage is trimmed for offset voltage. A complementary output configuration (Q12-Q13) is employed to create an output stage with rail-to-rail swing. The devices are fabricated on Linear Technology's proprietary complementary bipolar process, which ensures very similar DC and AC characteristics for the output devices Q12 and Q13.

First, looking at the input stage, Q5 switches the current from current source I_1 between the two input stages. When the input common mode voltage V_{CM} is near the negative supply, Q5 is reverse biased, so the current from I_1 becomes the tail current for the PNP differential pair Q1-Q2. At the other extreme, when V_{CM} is near the positive supply, the PNPs Q1-Q2 are biased off. The current from


1466L/67L F01
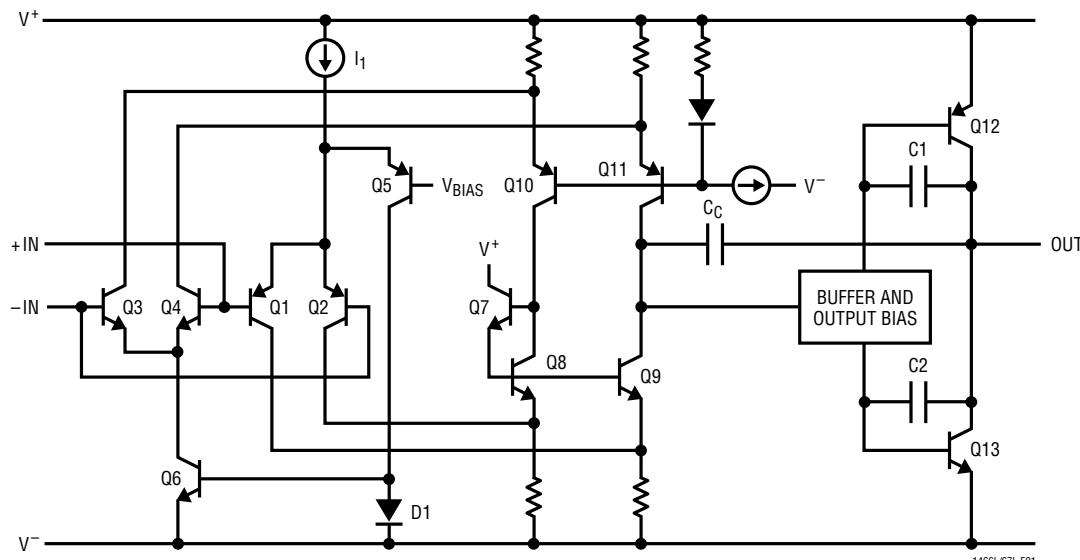
Figure 1. Simplified Schematic

APPLICATIONS INFORMATION

I_1 then flows through Q5 to the current mirror D3-Q6, furnishing the tail current for the NPN differential pair Q3-Q4. The switchover point between stages occurs when V_{CM} is equal to the base voltage of Q5, which is biased approximately 1.3V below the positive supply.

The collector currents of the two input pairs are combined in the second stage, consisting of Q7-Q11. Most of the voltage gain in the amplifier is contained in this stage. The output of the second stage is buffered and applied to the output devices Q12 and Q13. Capacitors C1 and C2 form local feedback loops around the output devices, lowering the output impedance at high frequencies. Capacitor C_C sets the amplifier bandwidth.

Input Offset Voltage

Since the amplifier has two input stages, the input offset voltage changes depending upon which stage is active. When the amplifier switches between stages, the offset voltage may go up, down or remain flat. Both stages of the LT1466L/LT1467L are trimmed; one at the negative sup-ply and the other at the positive supply. The resulting common mode rejection ratio of 83dB minimum is much better than typical rail-to-rail amplifiers.

Overdrive Protection

The LT1466L/LT1467L contain circuits that prevent the output from reversing polarity when the input voltage exceeds either supply. For these circuits to work properly, the input current should be limited to –10mA when the input is below the negative supply, and 0.5mA when the input is above the positive supply. If the amplifier is to be severely overdriven, an external resistor should be used to limit the current.
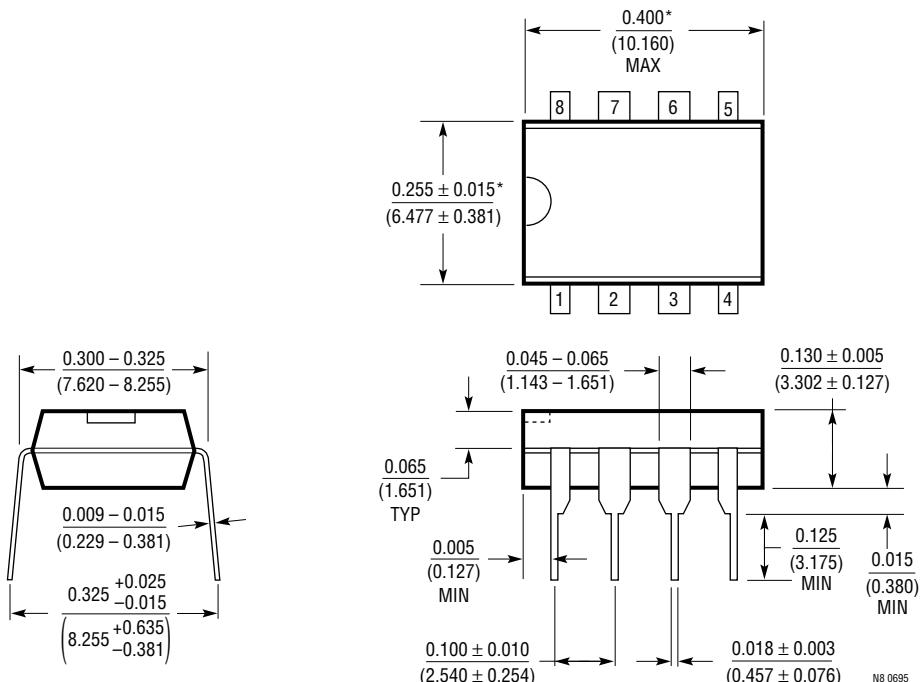
Output

The output voltage swing and current sinking capability of the LT1466L/LT1467L are affected by input overdrive as shown in the Typical Performance Characteristics. When monitoring voltages within 100mV of either rail, gain should be taken to keep the output from clipping.
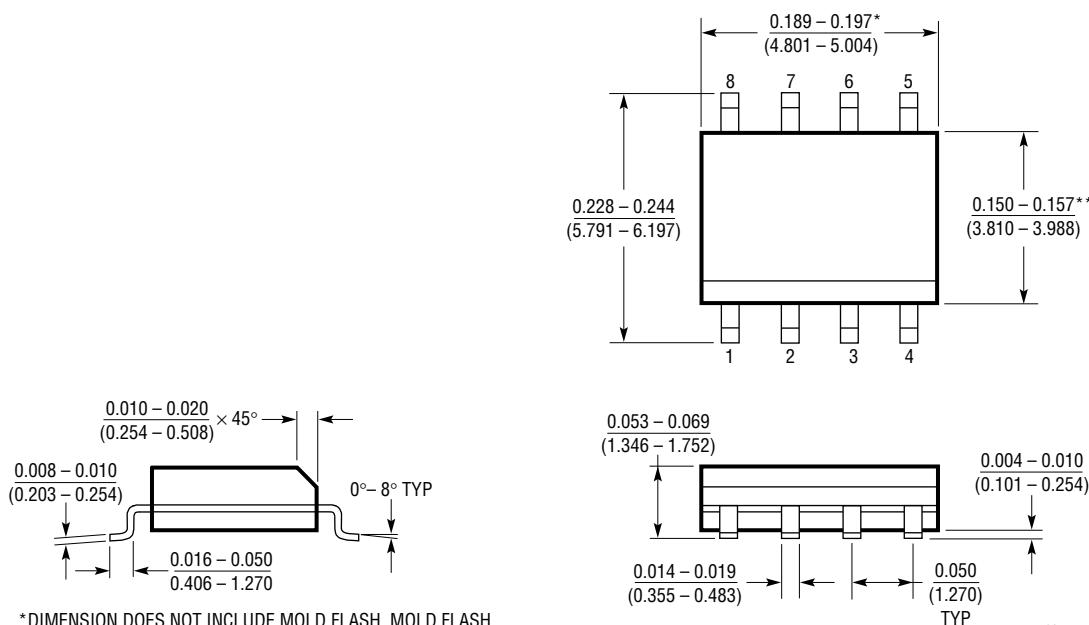
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

**N8 Package**
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

0.400*
(10.160)
MAX

8 7 6 5

0.255 ± 0.015*
(6.477 ± 0.381)

1 2 3 4

0.300 – 0.325
(7.620 – 8.255)

0.009 – 0.015
(0.229 – 0.381)

$0.325 {+0.025 \atop -0.015}$

$\left(8.255 {+0.635 \atop -0.381}\right)$

0.045 – 0.065
(1.143 – 1.651)

0.130 ± 0.005
(3.302 ± 0.127)

0.065
(1.651)
TYP

0.005
(0.127)
MIN

0.125
(3.175)
MIN

0.015
(0.380)
MIN

0.100 ± 0.010
(2.540 ± 0.254)

0.018 ± 0.003
(0.457 ± 0.076)

N8 0695

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)
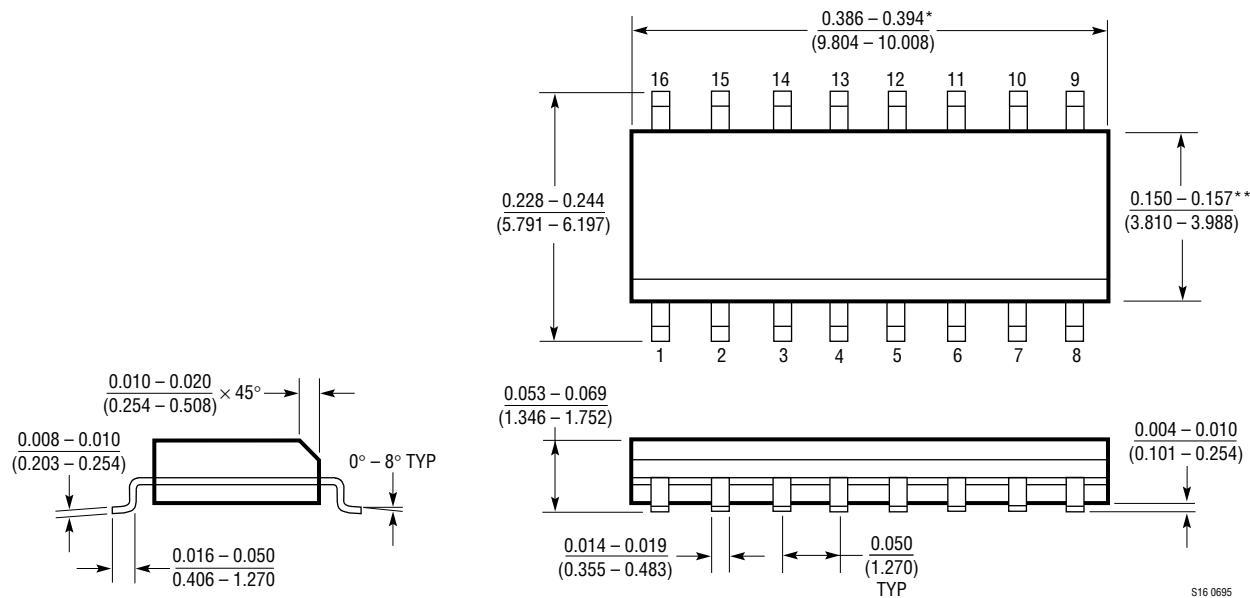
0.189 – 0.197*
(4.801 – 5.004)

8 7 6 5

0.228 – 0.244
(5.791 – 6.197)

0.150 – 0.157**
(3.810 – 3.988)

1 2 3 4

0.010 – 0.020
(0.254 – 0.508) × 45°

0.008 – 0.010
(0.203 – 0.254)

0° – 8° TYP

0.016 – 0.050
0.406 – 1.270

0.053 – 0.069
(1.346 – 1.752)

0.004 – 0.010
(0.101 – 0.254)

0.014 – 0.019
(0.355 – 0.483)

0.050
(1.270)
TYP

SO8 0996

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH
SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD
FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)
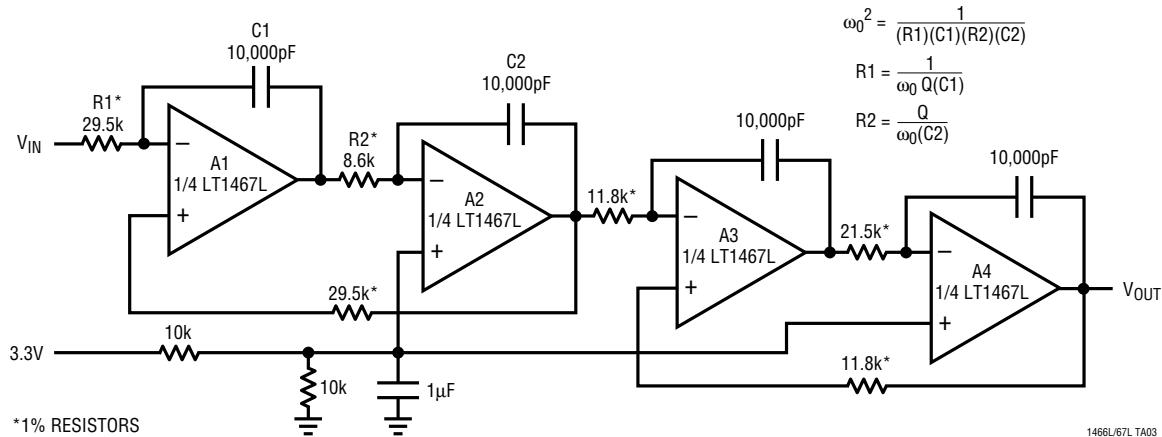
0.386 – 0.394*
(9.804 – 10.008)

16 15 14 13 12 11 10 9

0.228 – 0.244
(5.791 – 6.197)

0.150 – 0.157**
(3.810 – 3.988)

1   2   3   4   5   6   7   8

$\dfrac{0.010 - 0.020}{(0.254 - 0.508)} \times 45°$

0.008 – 0.010
(0.203 – 0.254)

0° – 8° TYP

$\dfrac{0.016 - 0.050}{0.406 - 1.270}$

0.053 – 0.069
(1.346 – 1.752)

0.004 – 0.010
(0.101 – 0.254)

0.014 – 0.019
(0.355 – 0.483)

$\dfrac{0.050}{(1.270)}$
TYP

S16 0695

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH
SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD
FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE
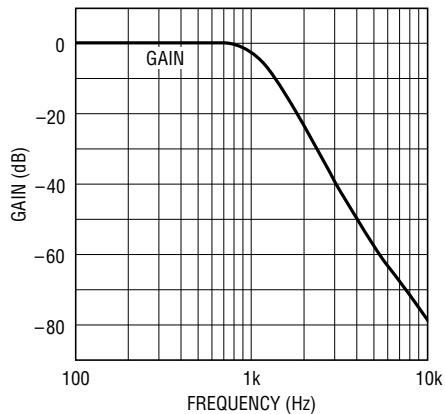
TYPICAL APPLICATIONS

4-Pole,1kHz, 3.3V Single Supply State Variable Filter Using the LT1467L

$$\omega_0{}^2 = \frac{1}{(R1)(C1)(R2)(C2)}$$

$$R1 = \frac{1}{\omega_0 \, Q(C1)}$$

$$R2 = \frac{Q}{\omega_0(C2)}$$

1466L/67L TA03

C1 10,000pF

R1* 29.5k

V_IN

A1 1/4 LT1467L

R2* 8.6k

C2 10,000pF

A2 1/4 LT1467L

11.8k*

10,000pF

A3 1/4 LT1467L

21.5k*

10,000pF

A4 1/4 LT1467L

V_OUT

29.5k*

3.3V

10k

10k

1µF

11.8k*

*1% RESISTORS

Frequency Response of 4th Order Butterworth Filter

1466L/67L TA04

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC®1152	Rail-to-Rail Input and Output, Zero-Drift Op Amp	High DC Accuracy, 10µV V_OS(MAX), 100nV/°C Drift, 0.7MHz GBW, 0.5V/µs Slew Rate, Maximum Supply Current 3mA
LT1366/LT1367	Dual/Quad Precision, Rail-to-Rail Input and Output Op Amps	475µV V_OS(MAX), 400kHz GBW, 0.13V/µs Slew Rate, Maximum Supply Current 520µA per Op Amp
LT1498 /LT1499	Dual/Quad, 10MHz Rail-to-Rail Input and Output Op Amps	High Speed, 5V/µs Slew Rate, 475µV V_OS(MAX) from V⁺ to V⁻, Max Supply Current 2.2mA per Op Amp