ANALOG DEVICES

SHARC® Processor

Preliminary Technical Data

ADSP-21365

SUMMARY

High performance 32-bit/40-bit floating point processor optimized for high performance automotive audio processing

Audio decoder and post processor-algorithm support with 32-bit floating-point implementations

Non-volatile memory may be configured to support audio decoders and post processor-algorithms like PCM, Dolby Digital EX, Dolby Prologic IIx, DTS 96/24, Neo:6, DTS ES, MPEG2 AAC, MPEG2 2channel, MP3, and functionalism like Bass management, Delay, Speaker equalization, Graphic equalization, and more. Decoder/post-processor algorithm combination support will vary depending upon the chip version & the system configurations. Please visit www.analog.com/SHARC

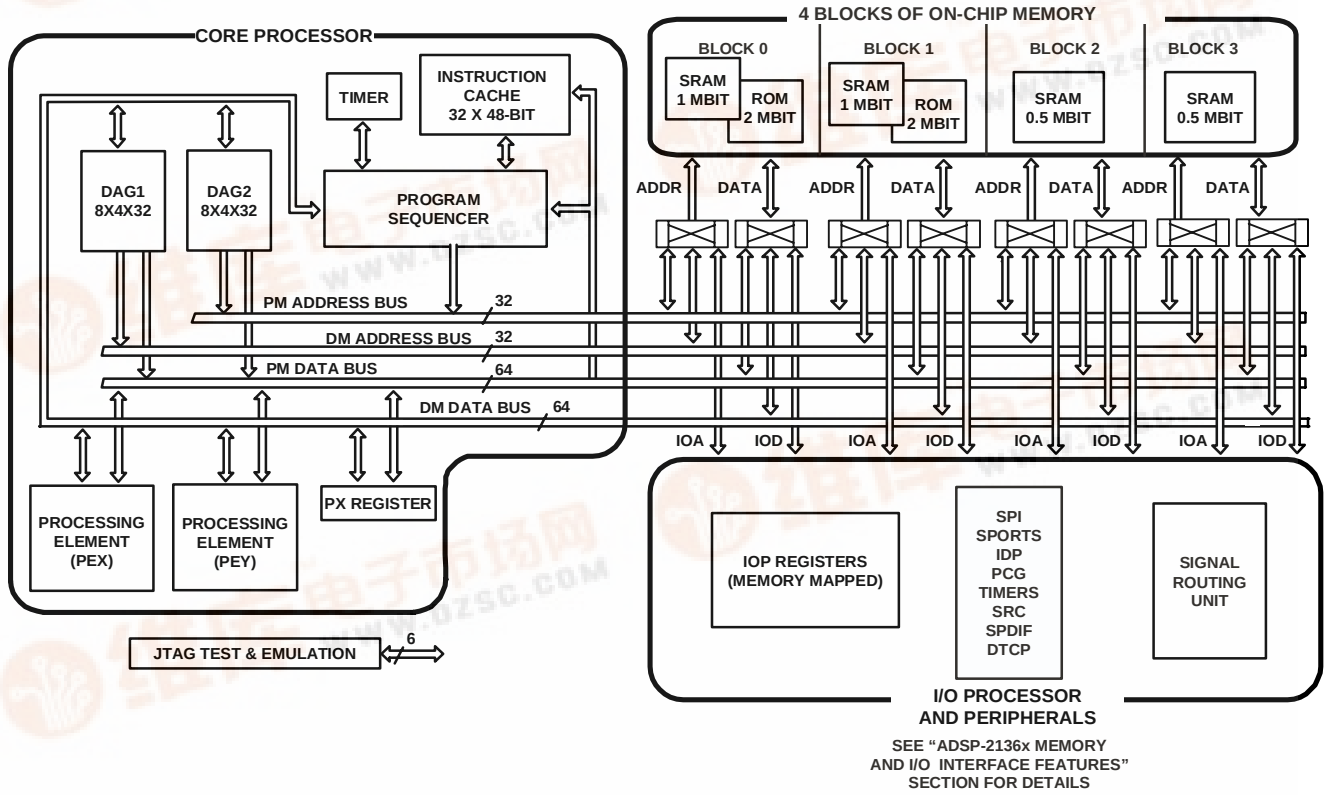
Single-Instruction Multiple-Data (SIMD) computational architecture

On-chip memory—3 Mbits of on-chip SRAM and a dedicated 4 Mbits of on-chip mask-programmable ROM

Code compatible with all other members of the SHARC family

The ADSP-21365 is available in a 300 MHz core instruction rate with unique audio centric peripherals such as the Digital Audio Interface, S/PDIF transceiver, serial ports, DTCP, 8-channel asynchronous sample rate converter, precision clock generators and more. For complete ordering information, see Ordering Guide on page 45

Figure 1. Functional Block Diagram – Processor Core



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KEY FEATURES – PROCESSOR CORE

At 300 MHz (3.33 ns) core instruction rate, the ADSP-21365 performs 1800 MFLOPS/600 MMACS

3 Mbits on-chip dual-ported SRAM (1M Bit block 0, and 1, 0.50M Bit blocks 2 and 3) for simultaneous access by core processor and DMA

4 Mbits on-chip dual-ported mask-programmable ROM (2 Mbits in block 0 and 2 Mbits in block 1)

Dual Data Address Generators (DAGs) with modulo and bit-reverse addressing

Zero-overhead looping with single-cycle loop setup, providing efficient program sequencing

Single Instruction Multiple Data (SIMD) architecture provides:

- Two computational processing elements
- Concurrent execution
- Code compatibility with other SHARC family members at the assembly level
- Parallelism in busses and computational units allows: Single cycle executions (with or without SIMD) of a multiply operation, an ALU operation, a dual memory read or write, and an instruction fetch

Transfers between memory and core at a sustained 4.8 Gbytes/s bandwidth at 300 MHz core instruction rate

ADSP-21365 I/O FEATURES

DMA Controller supports:

25 zero-overhead DMA channels for transfers between ADSP-21365 internal memory a variety of peripherals

32-bit DMA transfers at core clock speed, in parallel with full-speed processor execution

Asynchronous parallel port provides access to asynchronous external memory

16 multiplexed address/data lines support 24-bit address external address range with 8-bit data or 16-bit address external address range with 16-bit data

- 50 Mbyte per sec transfer rate

256 word page boundaries

External memory access in a dedicated DMA channel

8- to 32- bit and 16- to 32-bit word packing options

Programmable wait state options: 2 to 31 CCLK

Digital Audio Interface (DAI) includes 6 serial ports, two Precision Clock Generators, an Input Data Port, three timers, an S/PDIF transceiver, DTCP cipher, 8-channel asynchronous sample rate converter, an PI port, and a Signal Routing Unit

Six dual data line serial ports that operate at up to 50 Mbits/s on each data line — each has a clock, frame sync and two data lines that can be configured as either a receiver or transmitter pair

Left-justified Sample Pair and I^2S Support, programmable direction for up to 24 simultaneous receive or transmit channels using two I^2S compatible stereo devices per serial port

TDM support for telecommunications interfaces including 128 TDM channel support for newer telephony interfaces such as H.100/H.110

Up to 12 TDM stream support, each with 128 channels per frame

Companding selection on a per channel basis in TDM mode

Input Data Port provides an additional input path to the DSP core, configurable as 8 channels of serial data or 7 channels of serial data and a single channel of up to a 20-bit wide parallel data

Signal Routing Unit provides configurable and flexible connections between all DAI components–six serial ports, one SPI port, eight channels of asynchronous sample rate converters, an S/PDIF receiver/transmitter, three timers, an SPI port,10 interrupts, six flag inputs, six flag outputs, and 20 SRU I/O pins (DAI_Px)

Two Serial Peripheral Interfaces (SPI): primary on dedicated pins, secondary on DAI pins

- Master or slave serial boot through primary SPI
- Full-duplex operation
- Master-Slave mode multi-master support

Open drain outputs

Programmable baud rates, clock polarities and phases

3 Muxed Flag/IRQ lines

1 Muxed Flag/Timer expired line

DEDICATED AUDIO COMPONENTS

S/PDIF Compatible Digital Audio receiver/transmitter supports:

- EIAJ CP-340 (CP-1201), IEC-958, AES/EBU standards
- Left justified, I^2S or right justified serial data input with 16, 18, 20 or 24 bit word widths (transmitter)
- Two channel mode and Single Channel Double Frequency (SCDF) mode

Sample Rate Converter (SRC) Contains a Serial Input Port, De-emphasis Filter, Sample Rate Converter (SRC) and Serial Output Port providing up to -128db SNR performance

- Supports Left Justified, I^2S, TDM and Right Justified 24, 20, 18 and 16 bit serial formats (input)

Digital Transmission Content Protection (DTCP)—a cryptographic protocol for protecting audio content from unauthorized copying, intercepting, and tampering.

Pulse Width Modulation provides:

- 16 PWM outputs configured as four groups of four outputs
- Supports center-aligned or edge-aligned PWM waveforms
- Can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode

ROM Based Security features include:

- JTAG access to memory permitted with a 64-bit key
- Protected memory regions that can be assigned to limit access under program control to sensitive code

PLL has a wide variety of software and hardware multiplier/divider ratios

Dual voltage: 3.3 V I/O, 1.2 V core

Available in 136-ball BGA Package

GENERAL DESCRIPTION

The ADSP-21365 SHARC DSP is a member of the SIMD SHARC family of DSPs that feature Analog Devices' Super Harvard Architecture. The ADSP-21365 is source code compatible with the ADSP-2126x, and ADSP-2116x, DSPs as well as with first generation ADSP-2106x SHARC processors in SISD (Single-Instruction, Single-Data) mode. The ADSP-21365 is a 32-bit/40-bit floating point processor optimized for high performance automotive audio applications with its large on-chip SRAM and mask-programmable ROM, multiple internal buses to eliminate I/O bottlenecks, and an innovative Digital Audio Interface (DAI).

As shown in the functional block diagram on page 1, the ADSP-21365 uses two computational units to deliver a significant performance increase over the previous SHARC processors on a range of DSP algorithms. Fabricated in a state-of-the-art, high speed, CMOS process, the ADSP-21365 DSP achieves an instruction cycle time of 3.33 ns at 300 MHz. With its SIMD computational hardware, the ADSP-21365 can perform 1800 MFLOPS running at 300 MHz.

Table 1 shows performance benchmarks for the ADSP-21365.

Table 1. ADSP-21365 Benchmarks (at 300 MHz)

Benchmark Algorithm	Speed (at 300 MHz)
1024 Point Complex FFT (Radix 4, with reversal)	31 µs
FIR Filter (per tap)[1]	1.67 ns
IIR Filter (per biquad)[1]	6.66 ns
Matrix Multiply (pipelined)	
[3x3] × [3x1]	15 ns
[4x4] × [4x1]	26.60 ns
Divide (y/x)	11.66 ns
Inverse Square Root	18.15 ns

[1] Assumes two files in multichannel SIMD mode

The ADSP-21365 continues SHARC's industry leading standards of integration for DSPs, combining a high performance 32-bit DSP core with integrated, on-chip system features. These features include 3 Mbits on-chip SRAM memory, 4 Mbits ROM, an I/O processor that supports 25 DMA channels, six serial ports, an SPI interface, external parallel bus, and Digital Audio Interface (DAI).

The block diagram of the ADSP-21365 on page 1, illustrates the following architectural features:

- Two processing elements, each of which comprises an ALU, Multiplier, Shifter and Data Register File
- Data Address Generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core at every core processor cycle
- Three Programmable Interval Timers with PWM Generation, PWM Capture/Pulse width Measurement, and External Event Counter Capabilities
- On-Chip SRAM (3 Mbits)
- On-Chip mask-programmable ROM (4 Mbits)
- 8- or 16-bit Parallel port that supports interfaces to off-chip memory peripherals
- JTAG test access port

The block diagram of the ADSP-21365 on page 5, illustrates the following architectural features:

- DMA controller
- Six full duplex serial ports
- SPI-compatible interface
- Digital Audio Interface that includes a two precision clock generators (PCG), an input data port (IDP), an S/PDIF receiver/transmitter, eight channels asynchronous sample rate converters, DTCP cipher, six serial ports, eight serial interfaces, a 20-bit parallel input port, 10 interrupts, six flag outputs, six flag inputs, three timers, and a flexible signal routing unit (SRU)

Figure 2 on page 4 shows one sample configuration of a SPORT using the precision clock generators to interface with an I^2S ADC and an I^2S DAC with a much lower jitter clock than the serial port would generate itself. Many other SRU configurations are possible.

ADSP-21365 FAMILY CORE ARCHITECTURE

The ADSP-21365 is code compatible at the assembly level with the ADSP-2126x, ADSP-21160 and ADSP-21161, and with the first generation ADSP-2106x SHARC DSPs. The ADSP-21365 shares architectural features with the ADSP-2126x and ADSP-2116x SIMD SHARC family of DSPs, as detailed in the following sections.

SIMD Computational Engine

The ADSP-21365 contains two computational processing elements that operate as a Single-Instruction Multiple-Data (SIMD) engine. The processing elements are referred to as PEX and PEY and each contains an ALU, multiplier, shifter and register file. PEX is always active, and PEY may be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the band-

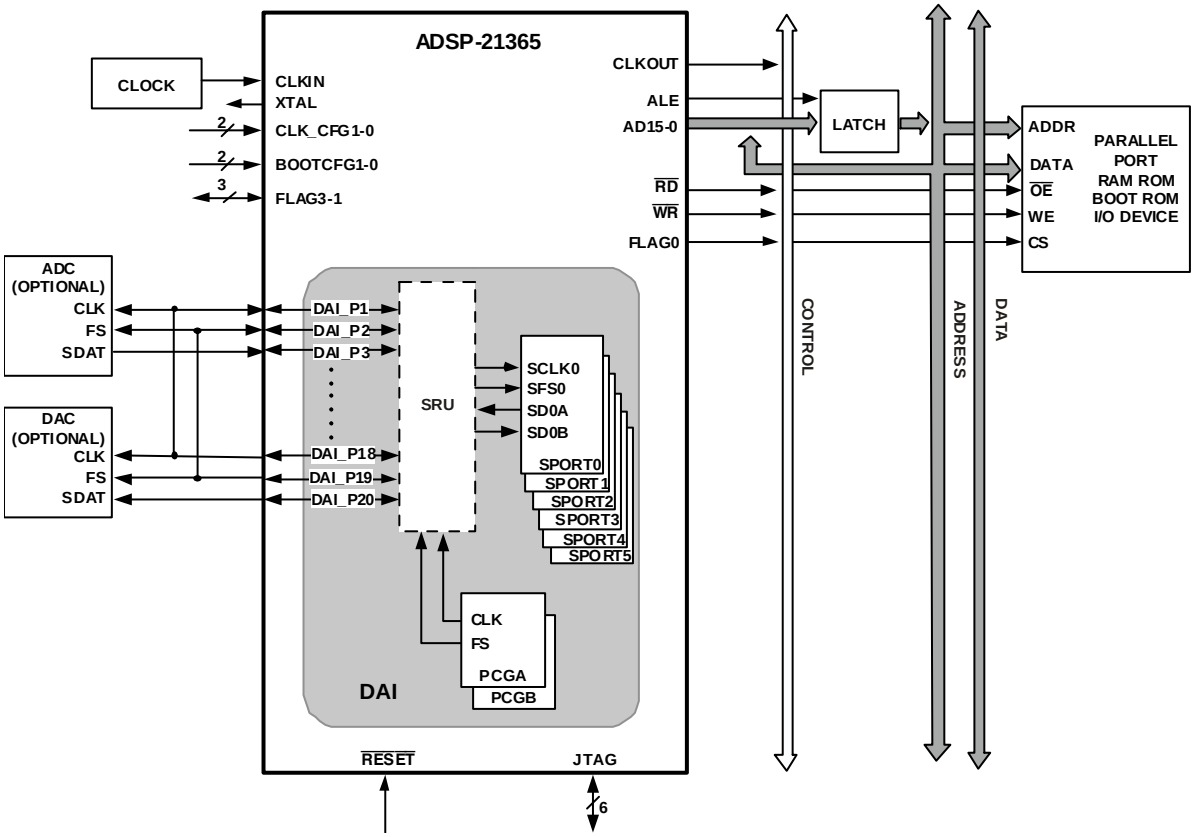


Figure 2. ADSP-21365 System Sample Configuration

width between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier and shifter. These units perform all operations in a single cycle. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multi-function instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

Data Register File

A general purpose data register file is contained in each processing element. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the ADSP-2136x enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0-R15 and in PEY as S0-S15.

Single-Cycle Fetch of Instruction and Four Operands

The ADSP-21365 features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 1 on page 1). With the ADSP-21365's separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

Instruction Cache

The ADSP-21365 includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective — only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full-speed execution of core, looped operations such as digital filter multiply-accumulates and FFT butterfly processing.

Data Address Generators With Zero-Overhead Hardware Circular Buffer Support

The ADSP-21365's two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital

signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the ADSP-21365 contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wrap-around, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-21365 can conditionally execute a multiply, an add, and a subtract in both processing elements while branching, and fetching up to four 32-bit values from memory—all in a single instruction.

ADSP-21365 MEMORY AND I/O INTERFACE FEATURES

The ADSP-21365 adds the following architectural features to the SIMD SHARC family core:

On-Chip Memory

The ADSP-21365 contains three megabits of internal SRAM and four megabits of internal mask-programmable ROM. Each block can be configured for different combinations of code and data storage (see Figure 4 on page 6). Each memory block supports single-cycle, independent accesses by the core processor and I/O processor. The ADSP-21365 memory architecture, in combination with its separate on-chip buses, allow two data transfers from the core and one from the I/O processor, in a single cycle.

The ADSP-21365's, SRAM can be configured as a maximum of 96K words of 32-bit data, 192K words of 16-bit data, 64K words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to three megabits. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one dedicated to each memory block assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

DMA Controller

The ADSP-21365's on-chip DMA controller allows data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the ADSP-21365's internal memory and its serial ports, the SPI-compatible (Serial Peripheral Interface) ports, the

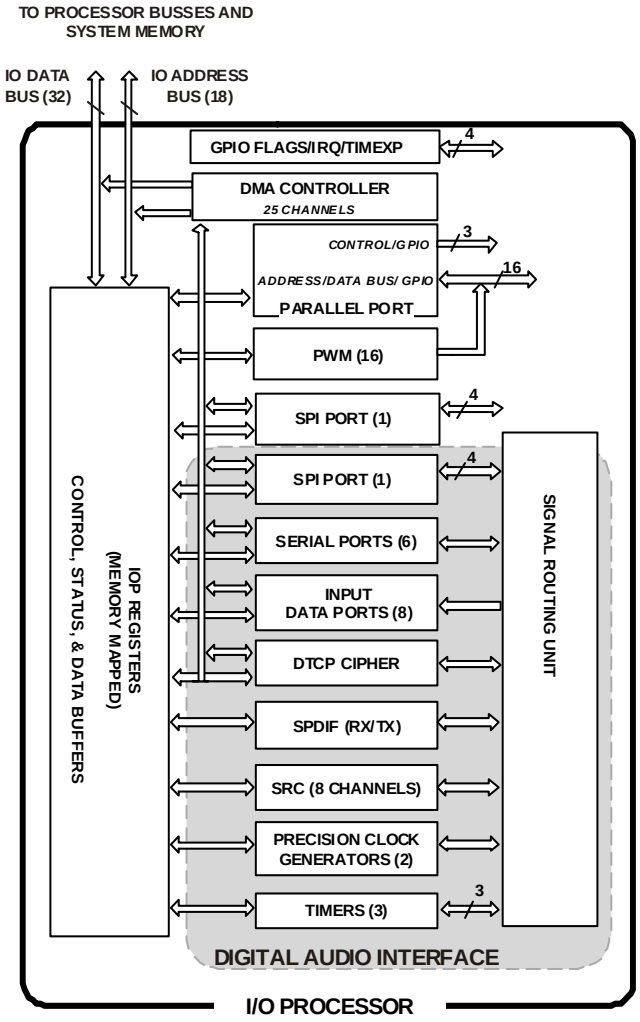


Figure 3. ADSP-21365 I/O Processor and Peripherals Block Diagram

IDP (Input Data Port), the parallel data acquisition port or the parallel port. Twenty-five channels of DMA are available on the ADSP-21365 — two for the SPI interface, twelve via the serial ports, eight via the Input Data Port two for DTCP and one via the processor's parallel port. Programs can be downloaded to the ADSP-21365 using DMA transfers. Other DMA features include interrupt generation upon completion of DMA transfers, and DMA chaining for automatic linked DMA transfers.

Digital Audio Interface (DAI)

The Digital Audio Interface (DAI) provides the ability to connect various peripherals to any of the DSPs DAI pins (DAI_P[20:1]).

Programs make these connections using the Signal Routing Unit (SRU, shown in Figure 3).

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI

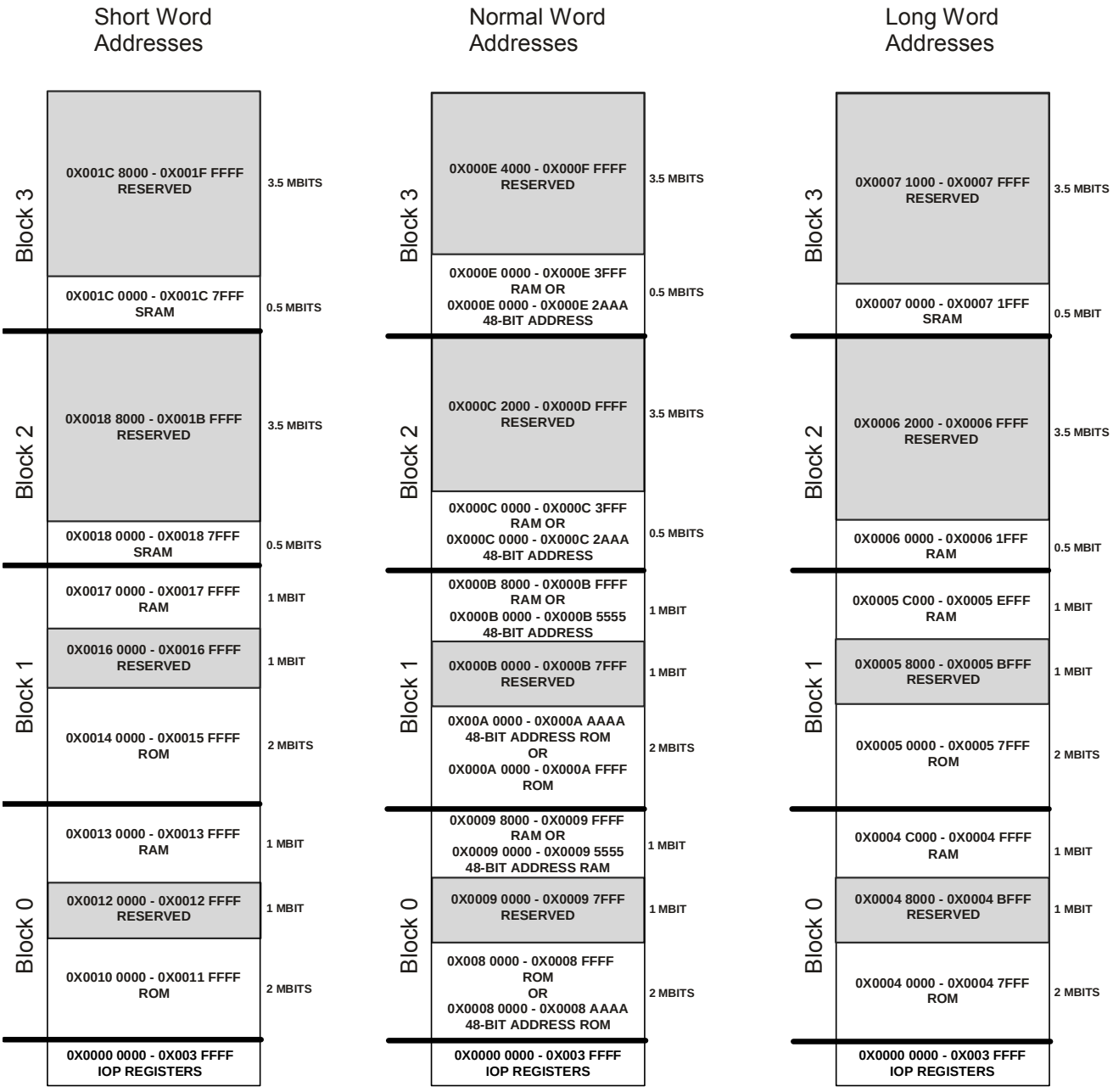


Figure 4. ADSP-21365 Memory Map

associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with non-configurable signal paths.

The DAI also includes six serial ports, a DTCP cipher, an S/PDIF receiver/transmitter, a precision clock generator (PCG), eight channels of asynchronous sample rate converters, an input data port (IDP), an SPI port, six flag outputs and six flag inputs, and 3 timers. The IDP provides an additional input path to the ADSP-21365 core, configurable as either eight channels of I^2S serial data or as 7 channels plus a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the ADSP-21365's serial ports.

For complete information on using the DAI, see the *ADSP-2136x SHARC DSP Core Reference*.

Serial Ports

The ADSP-21365 features six synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog devices AD183x

family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial ports are enabled via 12 programmable and simultaneous receive or transmit pins that support up to 24 transmit or 24 receive channels of audio data when all six SPORTS are enabled, or six full duplex TDM streams of 128 channels per frame.

The serial ports operate at a maximum data rate of 50 Mbits/s. Serial port data can be automatically transferred to and from on-chip memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in four modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I^2S mode
- Left-justified sample pair mode

Left-justified Sample Pair Mode is a mode in which each Frame Sync cycle two samples of data are transmitted/received — one sample on the high segment of the frame sync, the other on the low segment of the frame sync. The user has control over various attributes of this mode.

Each of the serial ports supports the Left-justified Sample Pair and I^2S protocols (I^2S is an industry standard interface commonly used by audio codecs, ADCs and DACs such as the Analog Devices AD183x family), with two data pins, allowing four Left-justified Sample Pair or I^2S channels (using two stereo devices) per serial port, with a maximum of up to 24 I^2S channels. The serial ports permit little-endian or big-endian transmission formats and word lengths selectable from 3 bits to 32 bits. For the Left-justified Sample Pair and I^2S modes, data-word lengths are selectable between 8 bits and 32 bits. Serial ports offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding selection on a per channel basis. Serial port clocks and frame syncs can be internally or externally generated.

Parallel Port

The Parallel Port provides interfaces to SRAM and peripheral devices. The multiplexed address and data pins (AD15-0) can access 8-bit devices with up to 24 bits of address, or 16-bit devices with up to 16 bits of address. In either mode, 8- or 16-bit, the maximum data transfer rate is 50 Mbytes/sec.

DMA transfers are used to move data to and from internal memory. Access to the core is also facilitated through the parallel port register read/write functions. The $\overline{RD}$, $\overline{WR}$, and ALE (Address Latch Enable) pins are the control pins for the parallel port.

Serial Peripheral (Compatible) Interface

The ADSP-21365 SHARC processor contains two Serial Peripheral Interface ports (SPI). The SPI is an industry standard synchronous serial link, enabling the ADSP-21365 SPI-compatible port to communicate with other SPI-compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multi-master environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The ADSP-21365 SPI-compatible peripheral implementation also features programmable baud rate and clock phase and polarities. The ADSP-21365 SPI-compatible port uses open drain drivers to support a multi-master configuration and to avoid data contention.

S/PDIF Compatible Digital Audio Receiver/Transmitter and Synchronous/Asynchronous Sample Rate Converter

The S/PDIF transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a Biphase encoded signal. The serial data input to the transmitter can be formatted as left justified, I^2S or right justified with word widths of 16, 18, 20 or 24 bits.

The serial data, clock and frame sync inputs to the S/PDIF transmitter are routed through the Signal Routing Unit (SRU). They can come from a variety of sources such as the SPORTs, external pins, the precision clock generators (PCG) or the sample rate converters (SRC) and are controlled by SRU control registers.

The sample rate converter (SRC) contains four SRC blocks and is the same core as that used in the AD1896 192 kHz Stereo Asynchronous Sample Rate Converter providing up to 128dB SNR. The SRC block is used to perform synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multi-channel audio data without phase mismatches. Finally, the SRC is used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

Digital Transmission Content Protection

The DTCP specification defines a cryptographic protocol for protecting audio entertainment content from illegal copying, intercepting and tampering as it traverses high performance digital buses, such as the IEEE 1394 standard. Only legitimate entertainment content delivered to a source device via another approved copy protection system (such as the DVD Content Scrambling System) will be protected by this copy protection system.

Pulse Width Modulation

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor control, electronic valve control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate comple-

mentary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has four groups of four PWM outputs each. Therefore this module generates 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM output.

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single update mode or double update mode. In single update mode the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the mid-point of the PWM period. In double update mode, a second updating of the PWM registers is implemented at the mid-point of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in three-phase PWM inverters.

Timers

The ADSP-21365 has a total of four timers: a core timer able to generate periodic interrupts and three general purpose timers that can that can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse Waveform Generation mode
- Pulse Width Count /Capture mode
- External Event Watchdog mode

The core timer can be configured to use FLAG3 as a Timer Expired signal, and each general purpose timer has one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables all three general purpose timers independently.

ROM Based Security

The ADSP-21365 has a ROM security feature that provides hardware support for securing user software code by preventing unauthorized reading from the internal code when enabled. When using this feature, the DSP does not boot-load any external code, executing exclusively from internal SRAM/ROM. Additionally, the DSP is not freely accessible via the JTAG port. Instead, a unique 64-bit key, which must be scanned in through the JTAG or Test Access Port will be assigned to each customer. The device will ignore a wrong key. Emulation features and external boot modes are only available after the correct key is scanned.

Program Booting

The internal memory of the ADSP-21365 boots at system power-up from an 8-bit EPROM via the parallel port, an SPI master, an SPI slave or an internal boot. Booting is determined by the Boot Configuration (BOOTCFG1-0) pins. Selection of the boot source is controlled via SPI as either a master or slave device, or it can immediately begin executing from ROM.

Phased Locked Loop

The ADSP-21365 uses an on-chip Phase Locked Loop (PLL) to generate the internal clock for the core. On power up, the CLKCFG1-0 pins are used to select ratios of 32:1, 16:1, and 6:1. After booting, numerous other ratios can be selected via software control.

The ratios are made up of software configurable numerator values from 1 to 64 and software configurable divisor values of 1, 2, 4, and 8.

Power Supplies

The ADSP-21365 has separate power supply connections for the internal (V_{DDINT}), external (V_{DDEXT}), and analog (A_{VDD}/A_{VSS}) power supplies. The internal and analog supplies must meet the 1.2V requirement. The external supply must meet the 3.3V requirement. All external supply pins must be connected to the same power supply.

Note that the analog supply (A_{VDD}) powers the ADSP-21365's clock generator PLL. To produce a stable clock, you should provide an external circuit to filter the power input to the A_{VDD} pin. Place the filter as close as possible to the pin. For an example circuit, see Figure 5. To prevent noise coupling, use a wide trace for the analog ground (A_{VSS}) signal and install a decoupling capacitor as close as possible to the pin. Note that the A_{VSS} and A_{VDD} pins specified in Figure 5 are inputs to the DSP and not the analog ground plane on the board.

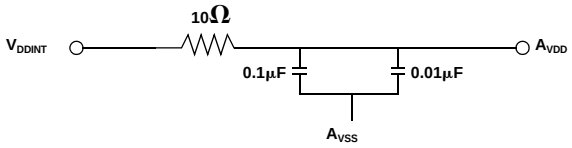


Figure 5. Analog Power (A_{VDD}) Filter Circuit

Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-21365 processor to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, see the appropriate "Emulator Hardware User's Guide".

DEVELOPMENT TOOLS

The ADSP-21365 is supported by a complete automotive reference design and development board as well as by a complete home audio reference design board available from Analog Devices. These boards implement complete audio decoding and post processing algorithms that are factory programmed into

the ROM of the ADSP-21365. SIMD optimized libraries consume less processing resources, which results in more available processing power for custom proprietary features.

The non-volatile memory of the ADSP-21365 can be configured to contain a combination of PCM 96KHz, Dolby Digital, Dolby Prologic, Dolby Prologic II, Dolby Prologic IIx, DTS 96/24, Neo:6, ES, EX, MPEG2 AAC, MPEG2 2channel, MP3, and other functions including bass management, delay, speaker equalization, graphic equalization, and spatialization.

Multiple SPDIF and analog I/Os are provided to maximize the overall system flexibility.

The ADSP-21365 is supported with a complete set of CROSSCORE™ software and hardware development tools, including Analog Devices emulators and VisualDSP++™ development environment. The same emulator hardware that supports other SHARC processors also fully emulates the ADSP-21365.

The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy to use assembler (which is based on an algebraic syntax), an archiver (librarian/library builder), a linker, a loader, a cycle-accurate instruction-level simulator, a C/C++ compiler, and a C/C++ runtime library that includes DSP and mathematical functions. A key point for these tools is C/C++ code efficiency. The compiler has been developed for efficient translation of C/C++ code to DSP assembly. The SHARC has architectural features that improve the efficiency of compiled C/C++ code.

The VisualDSP++ debugger has a number of important features. Data visualization is enhanced by a plotting package that offers a significant level of flexibility. This graphical representation of user data enables the programmer to quickly determine the performance of an algorithm. As algorithms grow in complexity, this capability can have increasing significance on the designer's development schedule, increasing productivity. Statistical profiling enables the programmer to non intrusively poll the processor as it is running the program. This feature, unique to VisualDSP++, enables the software developer to passively gather important code execution metrics without interrupting the real-time characteristics of the program. Essentially, the developer can identify bottlenecks in software quickly and efficiently. By using the profiler, the programmer can focus on those areas in the program that impact performance and take corrective action.

Debugging both C/C++ and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C/C++ and assembly code (interleaved source and object information)
- Insert breakpoints
- Set conditional breakpoints on registers, memory, and stacks
- Trace instruction execution
- Perform linear or statistical profiling of program execution
- Fill, dump, and graphically plot the contents of memory
- Perform source level debugging
- Create custom debugger windows

The VisualDSP++ IDDE lets programmers define and manage DSP software development. Its dialog boxes and property pages let programmers configure and manage all of the SHARC development tools, including the color syntax highlighting in the VisualDSP++ editor. This capability permits programmers to:

- Control how the development tools process inputs and generate outputs
- Maintain a one-to-one correspondence with the tool's command line switches

The VisualDSP++ Kernel (VDK) incorporates scheduling and resource management tailored specifically to address the memory and timing constraints of DSP programming. These capabilities enable engineers to develop code more effectively, eliminating the need to start from the very beginning, when developing new application code. The VDK features include Threads, Critical and Unscheduled regions, Semaphores, Events, and Device flags. The VDK also supports Priority-based, Preemptive, Cooperative, and Time-Sliced scheduling approaches. In addition, the VDK was designed to be scalable. If the application does not use a specific feature, the support code for that feature is excluded from the target system.

Because the VDK is a library, a developer can decide whether to use it or not. The VDK is integrated into the VisualDSP++ development environment, but can also be used via standard command line tools. When the VDK is used, the development environment assists the developer with many error-prone tasks and assists in managing system resources, automating the generation of various VDK based objects, and visualizing the system state, when debugging an application that uses the VDK.

VisualDSP++ Component Software Engineering (VCSE) is Analog Devices technology for creating, using, and reusing software components (independent modules of substantial functionality) to quickly and reliably assemble software applications. Download components from the Web and drop them into the application. Publish component archives from within VisualDSP++. VCSE supports component implementation in C/C++ or assembly language.

Use the Expert Linker to visually manipulate the placement of code and data on the embedded system. View memory utilization in a color-coded graphical form, easily move code and data to different areas of the DSP or external memory with the drag of the mouse, examine run time stack and heap usage. The Expert Linker is fully compatible with existing Linker Definition File (LDF), allowing the developer to move between the graphical and textual environments.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the SHARC processor family. Hardware tools include SHARC processor PC plug-in cards. Third party software tools include DSP libraries, real-time operating systems, and block diagram design tools.

DESIGNING AN EMULATOR-COMPATIBLE DSP BOARD (TARGET)

The Analog Devices family of emulators are tools that every DSP developer needs to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG Test Access Port (TAP) on each JTAG DSP. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing. The emulator uses the TAP to access the internal features of the DSP, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The DSP must be halted to send data and commands, but once an operation has been completed by the emulator, the DSP system is set running at full speed with no impact on system timing.

To use these emulators, the target board must include a header that connects the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, multiprocessor scan chains, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21365 architecture and functionality. For detailed information on the ADSP-2136x Family core architecture and instruction set, refer to the ADSP-2136x DSP Hardware Reference and the ADSP-21160 SHARC DSP Instruction Set Reference.

PIN FUNCTION DESCRIPTIONS

ADSP-21365 pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$). Tie or pull unused inputs to V_{DDEXT} or GND, except for the following:

- DAI_Px, SPICLK, MISO, MOSI, $\overline{\text{EMU}}$, TMS,$\overline{\text{TRST}}$, TDI and AD15-0 (NOTE: These pins have pull-up resistors.)

The following symbols appear in the Type column of Table 2: A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open Drain, and T = Three-State.

Table 2. Pin Descriptions

Pin	Type	State During & After Reset	Function
AD15-0	I/O/T	Three-state with pull-up enabled	**Parallel Port Address/Data.** The ADSP-21365 parallel port and its corresponding DMA unit output addresses and data for peripherals on these multiplexed pins. The multiplex state is determined by the ALE pin. The parallel port can operate in either 8-bit or 16-bit mode. Each AD pin has a 22.5 kΩ internal pull-up resistor. See Address Data Modes on page 14 for details of the AD pin operation: For 8-bit mode: ALE is automatically asserted whenever a change occurs in the upper 16 external address bits, A23-8; ALE is used in conjunction with an external latch to retain the values of the A23-8. For 16-bit mode: ALE is automatically asserted whenever a change occurs in the address bits, A15-0; ALE is used in conjunction with an external latch to retain the values of the A15-0. To use these pins as flags (FLAGS15-0) or PWMs (PWM15-0): 1) set (=1) bit 20 of the SYSCTL register to disable the parallel port, 2) set (=1) bits 22-25 of the SYSCTL register to enable FLAGS in groups of four (bit 22 for FLAGS3-0, bit 23 for FLAGS7-4 etc.) or, set (=1) bits 26-29 of the SYSCTL register to enable PWMs in groups of four (bit 26 for PWM0-3, bit 27 for PWM4-7, and so on). When used as an input, the IDP Channel0 can use these pins for parallel input data.
$\overline{\text{RD}}$	O	Output only, driven high[1]	**Parallel Port Read Enable.** $\overline{\text{RD}}$ is asserted low whenever the DSP reads 8-bit or 16-bit data from an external memory device. When AD15-0 are flags, this pin remains deasserted.
$\overline{\text{WR}}$	O	Output only, driven high[1]	**Parallel Port Write Enable.** $\overline{\text{WR}}$ is asserted low whenever the DSP writes 8-bit or 16-bit data to an external memory device. When AD15-0 are flags, this pin remains deasserted.
ALE	O	Output only, driven low[1]	**Parallel Port Address Latch enable.** ALE is asserted whenever the DSP drives a new address on the parallel port address pins. On reset, ALE is active high. However, it can be reconfigured using software to be active low. When AD15-0 are flags, this pin remains deasserted.
FLAG3-0	I/O/A	Three-state	**Flag Pins.** Each flag pin is configured via control bits as either an input or output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals. These pins can be used as an SPI interface slave select output during SPI mastering. These pins are also multiplexed with the $\overline{\text{IRQx}}$ and the TIMEXP signals. In SPI master boot mode, FLAG0 is the slave select pin that must be connected to an SPI EPROM. FLAG0 is configured as a slave select during SPI master boot. When bit 16 is set (=1) in the SYSCTL register, FLAG0 is configured as $\overline{\text{IRQ0}}$. When bit 17 is set (=1) in the SYSCTL register, FLAG1 is configured as $\overline{\text{IRQ1}}$. When bit 18 is set (=1) in the SYSCTL register, FLAG2 is configured as $\overline{\text{IRQ2}}$. When bit 19 is set (=1) in the SYSCTL register, FLAG3 is configured as TIMEXP which indicates that the system timer has expired.

Table 2. Pin Descriptions (Continued)

Pin	Type	State During & After Reset	Function
DAI_P20-1	I/O/T	Three-state with programmable pull-up	**Digital Audio Interface Pins**. These pins provide the physical interface to the SRU. The SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the SRU may be routed to any of these pins. The SRU provides the connection from the Serial ports, Input data port, precision clock generators and timers, DTCP cipher, S/PDIF transceiver, sample rate converters and SPI to the DAI_P20-1 pins These pins have internal 22.5 kΩ pull-up resistors which are enabled on reset. These pull-ups can be disabled in the DAI_PIN_PULLUP register.
SPICLK	I/O	Three-state with pull-up enabled	**Serial Peripheral Interface Clock Signal**. Driven by the master, this signal controls the rate at which data is transferred. The master may transmit data at a variety of baud rates. SPICLK cycles once for each bit transmitted. SPICLK is a gated clock that is active during data transfers, only for the length of the transferred word. Slave devices ignore the serial clock if the slave select input is driven inactive (HIGH). SPICLK is used to shift out and shift in the data driven on the MISO and MOSI lines. The data is always shifted out on one clock edge and sampled on the opposite edge of the clock. Clock polarity and clock phase relative to data are programmable into the SPICTL control register and define the transfer format. SPICLK has a 22.5 kΩ internal pull-up resistor.
$\overline{\text{SPIDS}}$	I	Input only	**Serial Peripheral Interface Slave Device Select**. An active low signal used to select the DSP as an SPI slave device. This input signal behaves like a chip select, and is provided by the master device for the slave devices. In multi-master mode the DSPs $\overline{\text{SPIDS}}$ signal can be driven by a slave device to signal to the DSP (as SPI master) that an error has occurred, as some other device is also trying to be the master device. If asserted low when the device is in master mode, it is considered a multi-master error. For a single-master, multiple-slave configuration where flag pins are used, this pin must be tied or pulled high to V_{DDEXT} on the master device. For ADSP-21365 to ADSP-21365 SPI interaction, any of the master ADSP-21365's flag pins can be used to drive the $\overline{\text{SPIDS}}$ signal on the ADSP-21365 SPI slave device.
MOSI	I/O (O/D)	Three-state with pull-up enabled	**SPI Master Out Slave In**. If the ADSP-21365 is configured as a master, the MOSI pin becomes a data transmit (output) pin, transmitting output data. If the ADSP-21365 is configured as a slave, the MOSI pin becomes a data receive (input) pin, receiving input data. In an ADSP-21365 SPI interconnection, the data is shifted out from the MOSI output pin of the master and shifted into the MOSI input(s) of the slave(s). MOSI has a 22.5 kΩ internal pull-up resistor.
MISO	I/O (O/D)	Three-state with pull-up enabled	**SPI Master In Slave Out**. If the ADSP-21365 is configured as a master, the MISO pin becomes a data receive (input) pin, receiving input data. If the ADSP-21365 is configured as a slave, the MISO pin becomes a data transmit (output) pin, transmitting output data. In an ADSP-21365 SPI interconnection, the data is shifted out from the MISO output pin of the slave and shifted into the MISO input pin of the master. MISO has a 22.5 kΩ internal pull-up resistor. MISO can be configured as O/D by setting the OPD bit in the SPICTL register. **Note:** *Only one slave is allowed to transmit data at any given time.* To enable broadcast transmission to multiple SPI-slaves, the DSP's MISO pin may be disabled by setting (=1) bit 5 (DMISO) of the SPICTL register.
BOOTCFG1-0	I	Input only	**Boot Configuration Select**. This pin is used to select the boot mode for the DSP. The BOOTCFG pins must be valid before reset is asserted. See Table 3 for a description of the boot modes.

Table 2. Pin Descriptions (Continued)

Pin	Type	State During & After Reset	Function
CLKIN	I	Input only	**Local Clock In**. Used in conjunction with XTAL. CLKIN is the ADSP-21365 clock input. It configures the ADSP-21365 to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the ADSP-21365 to use the external clock source such as an external clock oscillator. The core is clocked either by the PLL output or this clock input depending on the CLKCFG1-0 pin settings. CLKIN may not be halted, changed, or operated below the specified frequency.
XTAL	O	Output only[2]	**Crystal Oscillator Terminal**. Used in conjunction with CLKIN to drive an external crystal.
CLKCFG1-0	I	Input only	**Core/CLKIN Ratio Control**. These pins set the start up clock frequency. See Table 4 for a description of the clock configuration modes. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset.
CLKOUT	O	Output only	**Local Clock Out/ Reset Out**. Drives out the core reset signal to an external device. CLKOUT can also be configured as a reset out pin.The functionality can be switched between the PLL output clock and reset out by setting bit 12 of the PMCTREG register. The default is reset out.
$\overline{\text{RESET}}$	I/A	Input only	**Processor Reset**. Resets the ADSP-21365 to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
TCK	I	Input only[3]	**Test Clock (JTAG)**. Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21365.
TMS	I/S	Three-state with pull-up enabled	**Test Mode Select (JTAG)**. Used to control the test state machine. TMS has a 22.5 kΩ internal pull-up resistor.
TDI	I/S	Three-state with pull-up enabled	**Test Data Input (JTAG)**. Provides serial data for the boundary scan logic. TDI has a 22.5 kΩ internal pull-up resistor.
TDO	O	Three-state[4]	**Test Data Output (JTAG)**. Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	Three-state with pull-up enabled	**Test Reset (JTAG)**. Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21365. $\overline{\text{TRST}}$ has a 22.5 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$	O (O/D)	Three-state with pull-up enabled	**Emulation Status**. Must be connected to the ADSP-21365 Analog Devices DSP Tools product line of JTAG emulators target board connector only. $\overline{\text{EMU}}$ has a 22.5 kΩ internal pullup resistor.
V_{DDINT}	P		**Core Power Supply**. Nominally +1.2 V dc and supplies the DSP's core processor (13 pins on the BGA package, 32 pins on the LQFP package).
V_{DDEXT}	P		**I/O Power Supply**. Nominally +3.3 V dc. (6 pins on the BGA package, 10 pins on the LQFP package).
A_{VDD}	P		**Analog Power Supply**. Nominally +1.2 V dc and supplies the DSP's internal PLL (clock generator). This pin has the same specifications as V_{DDINT}, except that added filtering circuitry is required. For more information, see Power Supplies on page 8.
A_{VSS}	G		**Analog Power Supply Return**.
GND	G		**Power Supply Return**. (54 pins on the BGA package, 39 pins on the LQFP package).

[1] $\overline{\text{RD}}$, $\overline{\text{WR}}$, and ALE are continuously driven by the DSP and won't be three-stated.
[2] Output only is a three-state driver with its output path always enabled.
[3] Input only is three-state driver with both output path.
[4] Three-state is three-state driver.

BOOT MODES

Table 3. Boot Mode Selection

BOOTCFG1-0	Booting Mode
00	SPI Slave Boot
01	SPI Master Boot
10	Parallel Port boot via EPROM
11	Internal Boot Mode (ROM code only)

CORE INSTRUCTION RATE TO CLKIN RATIO MODES

Table 4. Core Instruction Rate/ CLKIN Ratio Selection

CLKCFG1-0	Core to CLKIN Ratio
00	6:1
01	32:1
10	16:1

ADDRESS DATA MODES

The following table shows the functionality of the AD pins for 8-bit and 16-bit transfers to the parallel port. For 8-bit data transfers, ALE latches address bits A23-A8 when asserted, followed by address bits A7-A0 and data bits D7-D0 when deasserted. For 16-bit data transfers, ALE latches address bits A15-A0 when asserted, followed by data bits D15-D0 when deasserted.

Table 5. Address/ Data Mode Selection

EP Data Mode	ALE	AD7-0 Function	AD15-8 Function
8-bit	Asserted	A15-8	A23-16
8-bit	Deasserted	D7-0	A7-0
16-bit	Asserted	A7-0	A15-8
16-bit	Deasserted	D7-0	D15-8

ADSP-21365 SPECIFICATIONS

Timing is measured on signals when they cross the 1.5 V level as described in Figure 31 on page 39. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

RECOMMENDED OPERATING CONDITIONS

Parameter[1]		K Grade		
		Min	Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage	1.14	1.26	V
A_{VDD}	Analog (PLL) Supply Voltage	1.14	1.26	V
V_{DDEXT}	External (I/O) Supply Voltage	3.13	3.47	V
V_{IH}	High Level Input Voltage[2], @ V_{DDEXT} = max	2.0	V_{DDEXT}+0.5	V
V_{IL}	Low Level Input Voltage[2] @ V_{DDEXT} = min	-0.5	0.8	V
C_{LOAD}	Load Capacitance on Output Pins		30	pf
T_{AMB}	Ambient Operating Temperature[3]	0	+70	°C

[1] Specifications subject to change without notice.
[2] Applies to input and bidirectional pins: AD15-0, FLAG3-0, DAI_Px, SPICLK, MOSI, MISO, $\overline{SPIDS}$, BOOTCFGx, CLKIN, CLKCFGx, $\overline{RESET}$, TCK, TMS, TDI, $\overline{TRST}$.
[3] See Thermal Characteristics on page 40 for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Parameter[1]		Test Conditions	Min	Max	Unit
V_{OH}	High Level Output Voltage [2]	@ V_{DDEXT} = min, I_{OH} = -1.0 mA[3]	2.4		V
V_{OL}	Low Level Output Voltage[2]	@ V_{DDEXT} = min, I_{OL} = 1.0 mA[3]		0.4	V
I_{IH}	High Level Input Current[4,5]	@ V_{DDEXT} = max, V_{IN} = V_{DDEXT} max		10	µA
I_{IL}	Low Level Input Current[4]	@ V_{DDEXT} = max, V_{IN} = 0 V		10	µA
I_{ILPU}	Low Level Input Current Pull-Up[5]	@ V_{DDEXT} = max, V_{IN} = 0 V		200	µA
I_{OZH}	Three-State Leakage Current [6,7]	@ V_{DDEXT}= max, V_{IN} = V_{DDEXT} max		10	µA
I_{OZL}	Three-State Leakage Current[6]	@ V_{DDEXT} = max, V_{IN} = 0 V		10	µA
I_{OZLPU}	Three-State Leakage Current Pull-Up1[7]	@ V_{DDEXT} = max, V_{IN} = 0 V		200	µA
$I_{DD-INTYP}$	Supply Current (Internal)[8,9]	t_{CCLK} = 5.0 ns, V_{DDINT} = 1.2		500	mA
AI_{DD}	Supply Current (Analog)[10]	A_{VDD} = max		10	mA
C_{IN}	Input Capacitance[11, 12]	f_{IN}=1 MHz, T_{CASE}=25°C, V_{IN}=1.2V		4.7	pF

[1] Specifications subject to change without notice.
[2] Applies to output and bidirectional pins: AD15-0, $\overline{RD}$, $\overline{WR}$, ALE, FLAG3-0, DAI_Px, SPICLK, MOSI, MISO, $\overline{EMU}$, TDO, CLKOUT, XTAL.
[3] See Output Drive Currents on page 39 for typical drive current capabilities.
[4] Applies to input pins: $\overline{SPIDS}$, BOOTCFGx, CLKCFGx, TCK, $\overline{RESET}$, CLKIN.
[5] Applies to input pins with 22.5 kΩ internal pull-ups: $\overline{TRST}$, TMS, TDI.
[6] Applies to three-statable pins: FLAG3-0.
[7] Applies to three-statable pins with 22.5 kΩ pull-ups: AD15-0, DAI_Px, $\overline{SPICLK}$, $\overline{EMU}$, $\overline{MISO}$, $\overline{MOSI}$.
[8] Typical internal current data reflects nominal operating conditions.
[9] See Engineering-to-Engineering Note (No. TBD) for further information.
[10] Characterized, but not tested.
[11] Applies to all signal pins.
[12] Guaranteed, but not tested.

ABSOLUTE MAXIMUM RATINGS

Internal (Core) Supply Voltage (V_{DDINT})[1]	0.3 V to +1.5 V
Analog (PLL) Supply Voltage (A_{VDD})[1]	-0.3 V to +1.5 V
External (I/O) Supply Voltage (V_{DDEXT})[1]	-0.3 V to +4.6 V
Input Voltage	-0.5 V to V_{DDEXT}[1] + 0.5 V
Output Voltage Swing	-0.5 V to V_{DDEXT}[1] + 0.5 V
Load Capacitance[1]	200 pF
Storage Temperature Range[1]	-65°C to +150°C

[1] Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-21365 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

The ADSP-21365's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, serial ports, and parallel port (as required for read/write strobes in asynchronous access mode). During reset, program the ratio between the DSP's internal clock frequency and external (CLKIN) clock frequency with the CLKCFG1-0 pins. To determine switching frequencies for the serial ports, divide down the internal clock, using the programmable divider control of each port (DIVx for the serial ports).

The ADSP-21365's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the DSP uses an internal phase-locked loop (PLL). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the DSP's internal clock (the clock source for the parallel port logic and I/O pads).

Note the definitions of various clock periods that are a function of CLKIN and the appropriate ratio control (Table 6).

Table 6. ADSP-21365 CLKOUT and CCLK Clock Generation Operation

Timing Requirements	Description	Calculation
CLKIN	Input Clock	$1/t_{CK}$
CCLK	Core Clock	$1/t_{CCLK}$

Timing Requirements	Description[1]
t_{CK}	CLKIN Clock Period
t_{CCLK}	(Processor) Core Clock Period
t_{PCLK}	(Peripheral) Clock Period = $2 \times t_{CCLK}$
t_{SCLK}	Serial Port Clock Period = $(t_{PCLK}) \times SR$
t_{SPICLK}	SPI Clock Period = $(t_{PCLK}) \times SPIR$

[1] where:
SR = serial port-to-core clock ratio (wide range, determined by SPORT CLKDIV)
SPIR = SPI-to-Core Clock Ratio (wide range, determined by SPIBAUD register)
DAI_Px = Serial Port Clock
SPICLK = SPI Clock

Figure 6 shows Core to CLKIN ratios of 6:1, 16:1 and 32:1 with external oscillator or crystal.

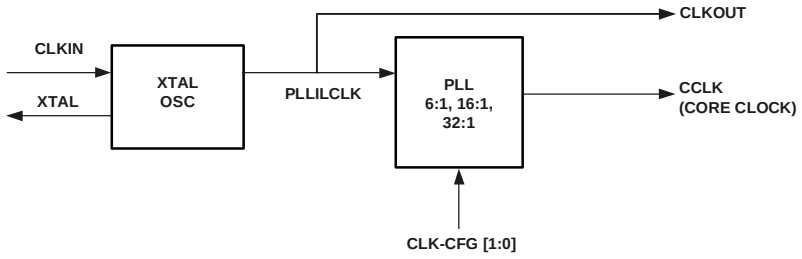


Figure 6. Core Clock and System Clock Relationship to CLKIN

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times.

See Figure 31 on page 39 under Test Conditions for voltage reference levels.

Switching Characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

The ADSP-21365's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, serial ports, and parallel port (as required for read/write strobes in asynchronous access mode). During reset, program the ratio between the DSP's internal clock frequency and external (CLKIN) clock frequency with the CLKCFG1-0 pins. To determine switching frequencies for the serial ports, divide down the internal clock, using the programmable divider control of each port (DIVx for the serial ports).

The ADSP-21365's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the DSP uses an internal phase-locked loop (PLL). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the DSP's internal clock (the clock source for the parallel port logic and I/O pads).

Note the following definitions of various clock periods that are a function of CLKIN and the appropriate ratio control.

Power up Sequencing

The timing requirements for DSP startup are given in Table 7.

Table 7. Power Up Sequencing Timing Requirements (DSP Startup)

Name	Parameter	Min	Max	Units
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ low before V_{DDINT}/V_{DDEXT} on	0		ns
$t_{IVDDEVDD}$	V_{DDINT} on before V_{DDEXT}	-50	200	ms
t_{CLKVDD}	CLKIN valid after V_{DDINT}/V_{DDEXT} valid[1]	0	200	ms
t_{CLKRST}	CLKIN valid before $\overline{\text{RESET}}$ deasserted	10[2]		µs
t_{PLLRST}	PLL control setup before $\overline{\text{RESET}}$ deasserted	20[3]		µs
t_{WRST}	Subsequent $\overline{\text{RESET}}$ low pulse width[4]	$4t_{CK}$		ns
Switching Characteristics				
$t_{CORERST}$	DSP core reset deasserted after $\overline{\text{RESET}}$ deasserted	$4096t_{CK} + 2\ t_{CCLK}$ [4, 5]		

[1] Valid V_{DDINT}/V_{DDEXT} assumes that the supplies are fully ramped to their 1.2 and 3.3 volt rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case startup timing of crystal oscillators. Refer to your crystal oscillator manufacturer's datasheet for startup time. Assume a 25 ms maximum oscillator startup time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Based on CLKIN cycles

[4] Applies after the power-up sequence is complete. Subsequent resets require a minimum of 4 CLKIN cycles for $\overline{\text{RESET}}$ to be held low in order to properly initialize and propagate default states at all I/O pins.

[5] The 4096 cycle count depends on t_{SRST} specification in Table 9. If setup time is not met, 1 additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

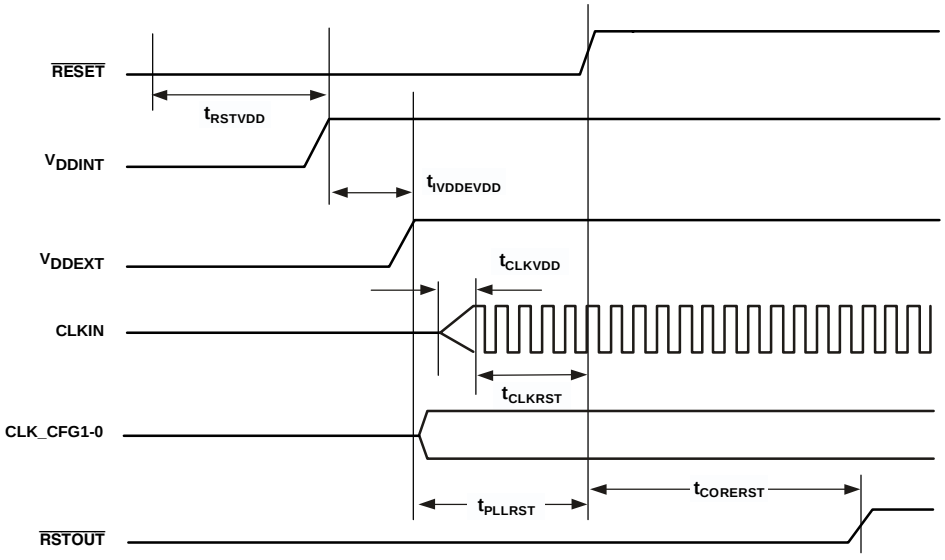


Figure 7. Power Up Sequencing

Clock Input

Table 8. Clock Input

Parameter		300 MHz		Units
		Min	Max	
Timing Requirements				
t_{CK}	CLKIN Period	19.8[1]	TBD[2]	ns
t_{CKL}	CLKIN Width Low	8[1]	TBD[2]	ns
t_{CKH}	CLKIN Width High	8[1]	TBD[2]	ns
t_{CKRF}	CLKIN Rise/Fall (0.4V-2.0V)		TBD	ns
t_{CCLK}	CCLK Period[3]	3.3[1]	TBD	ns

[1] Applies only for CLKCFG1-0 = 00 and default values for PLL control bits in PMCTL.
[2] Applies only for CLKCFG1-0 = 01 and default values for PLL control bits in PMCTL.
[3] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.

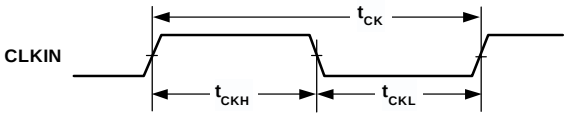
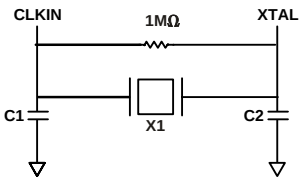


Figure 8. Clock Input

Clock Signals

The ADSP-21365 can use an external clock or a crystal. See CLKIN pin description. The programmer can configure the ADSP-21365 to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 9 shows the component connections used for a crystal operating in fundamental mode.



NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. CRYSTAL SELECTION MUST COMPLY WITH CLKCFG1-0 = 10 OR = 01.

Figure 9. 300 MHz Operation (Fundamental Mode Crystal)

Reset

Table 9. Reset

Parameter		Min	Max	Units
Timing Requirements				
t_{WRST}	$\overline{\text{RESET}}$ Pulse Width Low[1]	$4t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN Low	8		ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable VDD and CLKIN (not including start-up time of external clock oscillator).

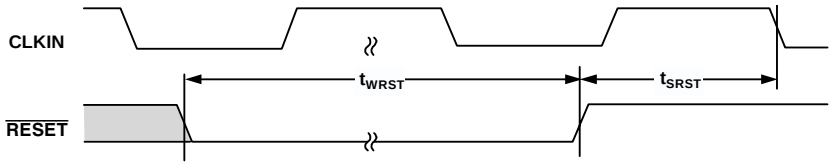


Figure 10. Reset

Interrupts

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts.

Table 10. Interrupts

Parameter		Min	Max	Units
Timing Requirements				
t_{IPW}	$\overline{\text{IRQx}}$ Pulse Width	$2 \times t_{PCLK} + 2$		ns

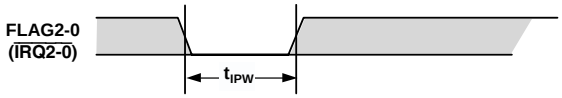


Figure 11. Interrupts

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (CTIMER).

Table 11. Core Timer

Parameter		Min	Max	Units
Switching Characteristic				
t_{WCTIM}	CTIMER Pulse width	$4 \times t_{PCLK} - 1$		ns

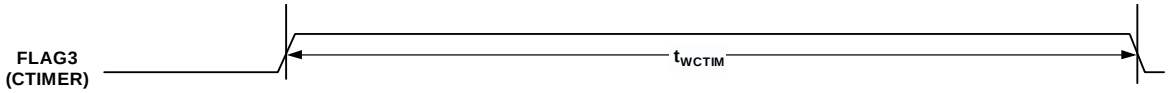


Figure 12. Core Timer

Timer PWM_OUT Cycle Timing

The following timing specification applies to Timer[2:0] in PWM_OUT (pulse width modulation) mode. Timer signals are routed to the DAI_P[20:1] pins through the SRU. Therefore, the timing specifications provided below are valid at the DAI_P[20:1] pins.

Table 12. Timer[2:0] PWM_OUT Timing

Parameter		Min	Max	Units
Switching Characteristic				
t_{PWMO}	Timer[2:0] Pulse width Output	$2 t_{PCLK} - 1$	$2(2^{31} - 1) t_{PCLK}$	ns

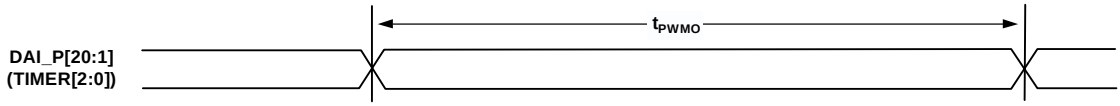


Figure 13. Timer[2:0] PWM_OUT Timing

Timer WDTH_CAP Timing

The following timing specification applies to Timer[2:0] in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DAI_P[20:1] pins through the SRU. Therefore, the timing specifications provided below are valid at the DAI_P[20:1] pins.

Table 13. Timer[2:0] Width Capture Timing

Parameter		Min	Max	Units
Timing Requirement				
t_{PWI}	Timer[2:0] Pulse width	2 t_{PCLK}	$2(2^{31}-1)$ t_{PCLK}	ns

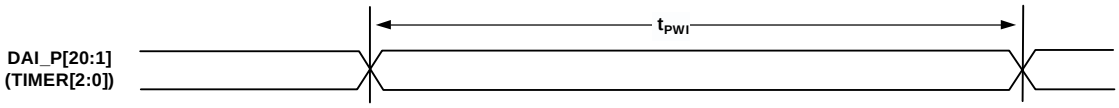


Figure 14. Timer[2:0] Width Capture Timing

DAI Pin to Pin Direct Routing

For direct pin connections only (for example DAI_PB01_I to DAI_PB02_O).

Table 14. DAI Pin to Pin Routing

Parameter		Min	Max	Units
Timing Requirement				
t_{DPIO}	Delay DAI Pin Input Valid to DAI Output Valid	1.5	10	ns

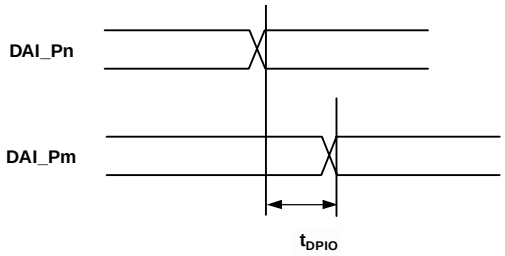


Figure 15. DAI Pin to PIN Direct Routing

Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the Precision Clock Generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers) there is not timing data available. All Timing Parameters and Switching Characteristics apply to external DAI pins (DAI_P07 – DAI_P20).

Table 15. Precision Clock Generator (Direct Pin Routing)

Parameter		Min	Max	Units
Timing Requirement				
t_{PCGIW}	Input Clock Period	20		
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	2		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	2		ns
Switching Characteristics				
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	10	ns
t_{DTRIG}	PCG Output Clock and Frame Sync Delay After PCG Trigger	$2.5 + 2.5 \times t_{PCGOW}$	$10 + 2.5 \times t_{PCGOW}$	ns
t_{PCGOW}	Output Clock Period	40		

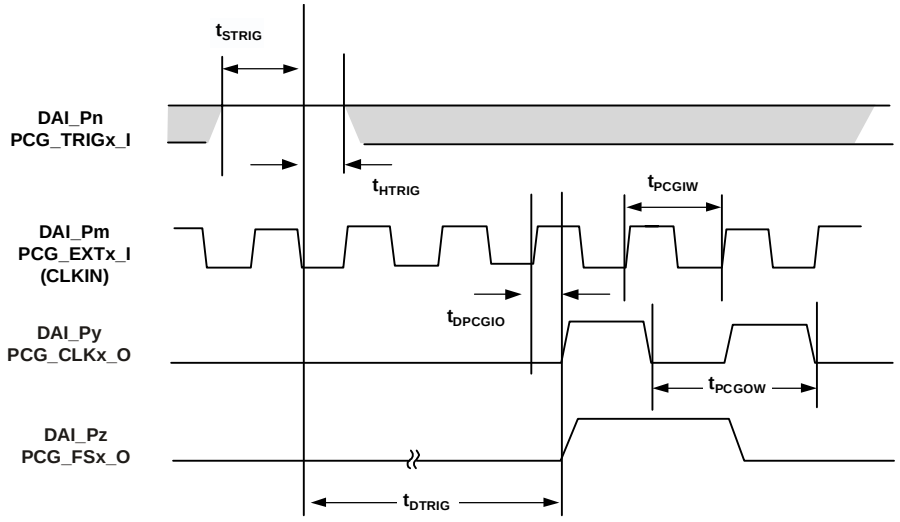


Figure 16. Precision Clock Generator (Direct Pin Routing)

Flags

The timing specifications provided below apply to the FLAG[3:0] and DAI_P[20:1] pins, the parallel port and the serial peripheral interface (SPI). See Table 2, "Pin Descriptions," on page 11 for more information on flag use.

Table 16. Flags

Parameter		Min	Max	Units
Timing Requirement				
t_{FIPW}	FLAG[3:0] IN Pulse Width	$2 \times t_{PCLK}+3$		ns
Switching Characteristic				
t_{FOPW}	FLAG[3:0] OUT Pulse Width	$2 \times t_{PCLK} - 1$		ns

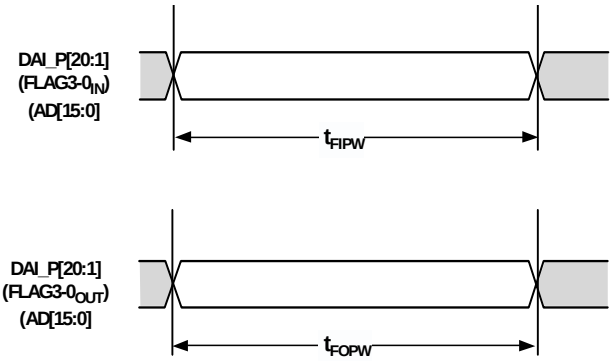


Figure 17. Flags

Memory Read–Parallel Port

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) when the ADSP-21365 is accessing external memory space.

Table 17. 8-Bit Memory Read Cycle

Parameter		Min	Max	Units
Timing Requirements				
t_{DRS}	Address/data [7:0] setup before $\overline{RD}$ high	3.3		ns
t_{DRH}	Address/data [7:0] hold after $\overline{RD}$ high	0		ns
t_{DAD}	Address [15:8] to data valid		D + t_{PCLK} – 3.5	ns
Switching Characteristics				
t_{ALEW}	ALE pulse width	2 × t_{PCLK} – 2.0		ns
t_{ADAS}	Address/data [15:0] setup before ALE deasserted[1]	2 × t_{PCLK} - 1.0		ns
t_{ADAH}	Address/data [15:0] hold after ALE deasserted[1]	t_{PCLK} – 0.8		
t_{ALEHZ}	ALE deasserted[1] to Address/Data[7:0] in high Z	t_{PCLK} – 0.8	t_{PCLK}	ns
t_{RW}	$\overline{RD}$ pulse width	D – 2		ns
t_{ADRH}	Address/data [15:8] hold after $\overline{RD}$ high	H		ns

D = (Data Cycle Duration) × t_{PCLK}

H= t_{PCLK} (if a hold cycle is specified, else H = 0)

[1] On reset, ALE is an active high cycle. However, it can be configured by software to be active low

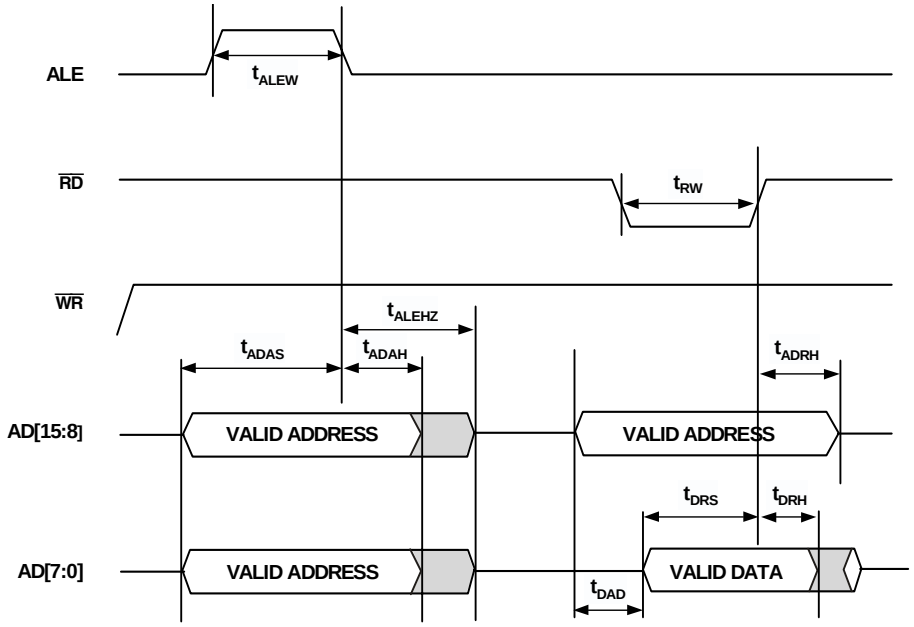


Figure 18. Read Cycle For 8-bit Memory Timing

Table 18. 16-bit Memory Read Cycle

Parameter		Min	Max	Units
Timing Requirements				
t_{DRS}	Address/data [15:0] setup before $\overline{RD}$ high	3.3		ns
t_{DRH}	Address/data [15:0] hold after $\overline{RD}$ high	0		ns
Switching Characteristics				ns
t_{ALEW}	ALE pulse width	$2 \times t_{PCLK} - 2$		ns
t_{ADAS}	Address/data [15:0] setup before ALE deasserted[1]	$2 \times t_{PCLK} - 1.0$		ns
t_{ADAH}	Address/data [15:0] hold after ALE deasserted[1]	$t_{PCLK} - 0.8$		ns
t_{ALEHZ}	ALE deasserted[1] to Address/Data[15:0] in high Z	$t_{PCLK} - 0.8$		ns
t_{RW}	$\overline{RD}$ pulse width	D – 2		ns

D = (Data Cycle Duration) × t_{PCLK}
H = t_{PCLK} (if a hold cycle is specified, else H = 0)

[1] On reset, ALE is an active high cycle. However, it can be configured by software to be active low.

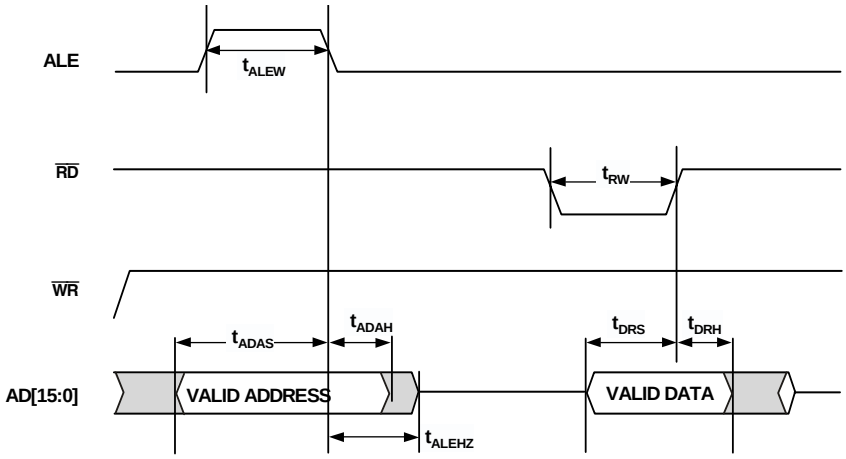


Figure 19. Read Cycle For 16-bit Memory Timing

Memory Write—Parallel Port

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) when the ADSP-21365 is accessing external memory space.

Table 19. 8-bit Memory Write Cycle

Parameter		Min	Max	Units
Switching Characteristics:				
t_{ALEW}	ALE pulse width	$2 \times t_{PCLK} - 2$		ns
t_{ADAS}	Address/data [15:0] setup before ALE deasserted[1]	$2 \times t_{PCLK} - 1.0$		ns
t_{ALERW}	ALE Deasserted to Read/Write Asserted	$1 \times t_{CCLK} - 1$		ns
t_{ADAH}	Address/data [15:0] hold after ALE deasserted [1]	$t_{PCLK} - 0.5$		ns
t_{WW}	$\overline{WR}$ pulse width	D – 2		ns
t_{ADWL}	Address/data [15:8] to $\overline{WR}$ low	$t_{PCLK} - 1.5$		ns
t_{ADWH}	Address/data [15:8] hold after $\overline{WR}$ high	H		ns
t_{ALEHZ}	ALE deasserted[1] to Address/Data[15:0] in high Z	$t_{PCLK} - 1.5$		ns
t_{DWS}	Address/data [7:0] setup before $\overline{WR}$ high	D		ns
t_{DWH}	Address/data [7:0] hold after $\overline{WR}$ high	H		ns
t_{DAWH}	Address/data to $\overline{WR}$ high	D		ns

D = (Data Cycle Duration) × t_{PCLK}

H = t_{PCLK} (if a hold cycle is specified, else H = 0)

[1] On reset, ALE is an active high cycle. However, it can be configured by software to be active low

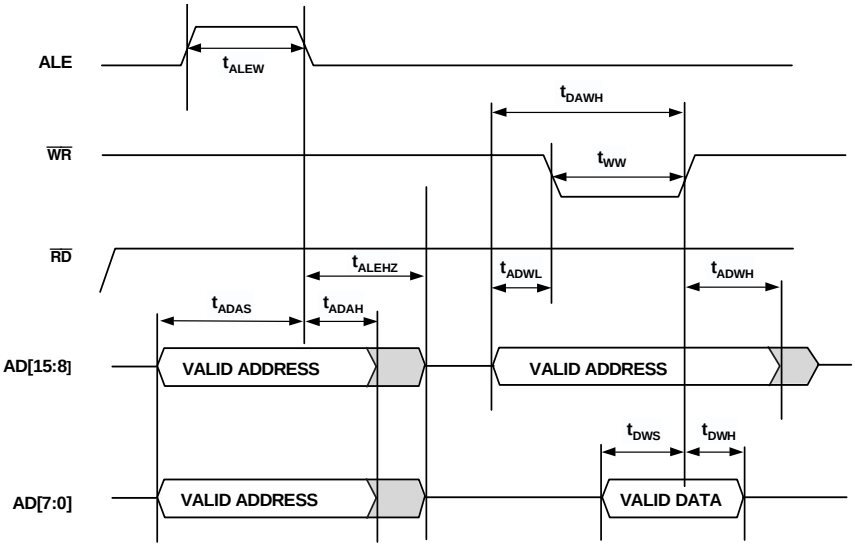


Figure 20. Write Cycle For 8-bit Memory Timing

Table 20. 16-bit Memory Write Cycle

Parameter		Min	Max	Units
Switching Characteristics				
t_{ALEW}	ALE pulse width	$2 \times t_{PCLK} - 2$		ns
t_{ADAS}	Address/data [15:0] setup before ALE deasserted[1]	$2 \times t_{PCLK} - 1.0$		ns
t_{ADAH}	Address/data [15:0] hold after ALE deasserted[1]	$t_{PCLK} - 0.5$		ns
t_{WW}	$\overline{WR}$ pulse width	D – 2		ns
t_{ALEHZ}	ALE deasserted[1] to Address/Data[15:0] in high Z	$t_{PCLK} - 1.5$		ns
t_{DWS}	Address/data [15:0] setup before $\overline{WR}$ high	D		ns
t_{DWH}	Address/data [15:0] hold after $\overline{WR}$ high	H		ns

D = (Data Cycle Duration) × t_{PCLK}
H = t_{PCLK} (if a hold cycle is specified, else H = 0)

[1] On reset, ALE is an active high cycle. However, it can be configured by software to be active low.

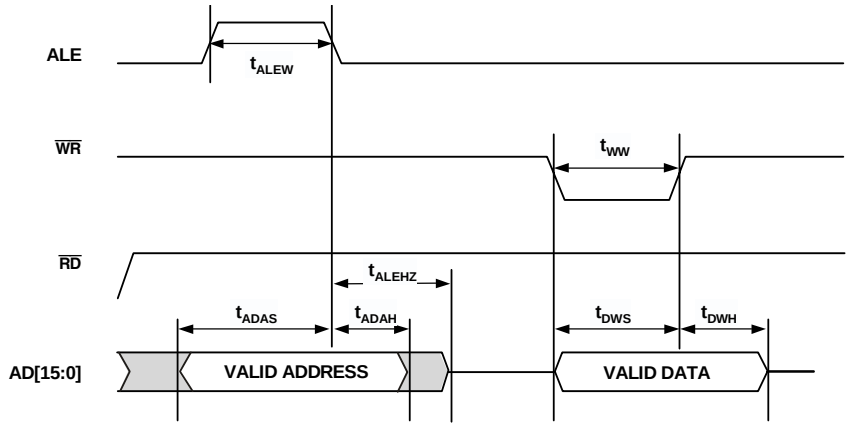


Figure 21. Write Cycle For 16-bit Memory Timing

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Serial port signals (SCLK, FS, DxA,/DxB) are routed to the DAI_P[20:1] pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P[20:1] pins.

Table 21. Serial Ports—External Clock

Parameter		Min	Max	Units
Timing Requirements				
t_{SFSE}	FS Setup Before SCLK (Externally Generated FS in either Transmit or Receive Mode)[1]	4		ns
t_{HFSE}	FS Hold After SCLK (Externally Generated FS in either Transmit or Receive Mode)[1]	5.5		ns
t_{SDRE}	Receive Data Setup Before Receive SCLK[1]	4		ns
t_{HDRE}	Receive Data Hold After SCLK[1]	5.5		ns
t_{SCLKW}	SCLK Width	20		ns
t_{SCLK}	SCLK Period	40		ns
Switching Characteristics				
t_{DFSE}	FS Delay After SCLK (Internally Generated FS in either Transmit or Receive Mode) [2]		7	ns
t_{HOFSE}	FS Hold After SCLK (Internally Generated FS in either Transmit or Receive Mode)1	2		ns
t_{DDTE}	Transmit Data Delay After Transmit SCLK[1]		7	ns
t_{HDTE}	Transmit Data Hold After Transmit SCLK[1]	2		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 22. Serial Ports—Internal Clock

Parameter		Min	Max	Units
Timing Requirements				
t_{SFSI}	FS Setup Before SCLK (Externally Generated FS in either Transmit or Receive Mode)[1]	7		ns
t_{HFSI}	FS Hold After SCLK (Externally Generated FS in either Transmit or Receive Mode)[1]	–4		ns
t_{SDRI}	Receive Data Setup Before SCLK[1]	7		ns
t_{HDRI}	Receive Data Hold After SCLK[1]	2.5		ns
Switching Characteristics				
t_{DFSI}	FS Delay After SCLK (Internally Generated FS in Transmit Mode)[2]		3	ns
t_{HOFSI}	FS Hold After SCLK (Internally Generated FS in Transmit Mode)[1]	–1.5		ns
t_{DFSI}	FS Delay After SCLK (Internally Generated FS in Receive or Mode)		3	ns
t_{HOFSI}	FS Hold After SCLK (Internally Generated FS in Receive Mode)	–4		ns
t_{DDTI}	Transmit Data Delay After SCLK[1]		3	ns
t_{HDTI}	Transmit Data Hold After SCLK[1]	–1.5		ns
t_{SCLKIW}	Transmit or Receive SCLK Width	$0.5t_{SCLK}$–2	$0.5t_{SCLK}$+2	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.

Table 23. Serial Ports—Enable and Three-State

Parameter		Min	Max	Units
Switching Characteristics				
t_{DDTEN}	Data Enable from External Transmit SCLK[1]	2		ns
t_{DDTTE}	Data Disable from External Transmit SCLK[1]		7	ns
t_{DDTIN}	Data Enable from Internal Transmit SCLK[1]	0		ns

[1] Referenced to drive edge.

Table 24. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Units
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External Transmit FS or External Receive FS with MCE = 1, MFD = 0[1]		7	ns
$t_{DDTENFS}$	Data Enable for MCE = 1, MFD = 0[1]	0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to Left-justified Sample Pair as well as DSP serial mode, and MCE = 1, MFD = 0.

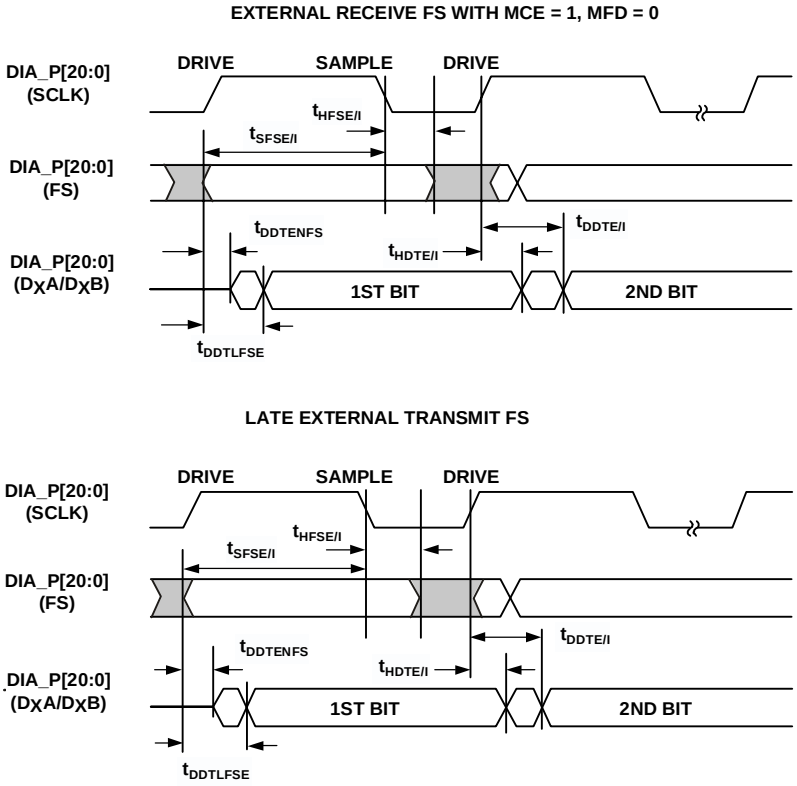
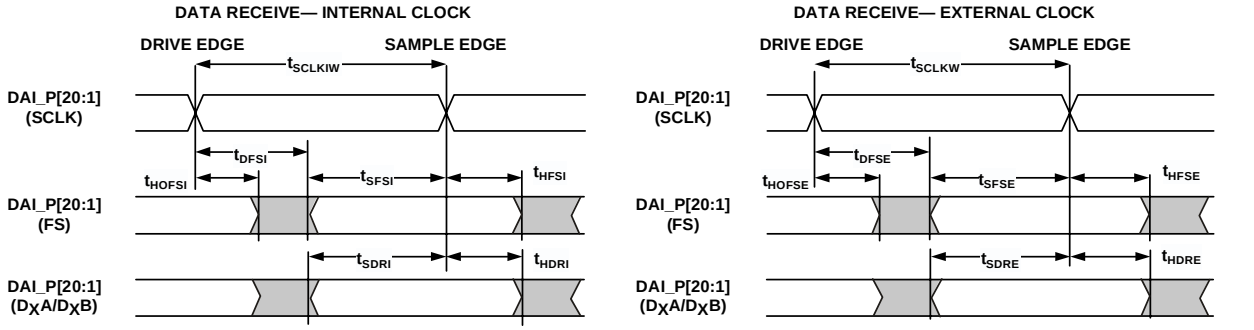
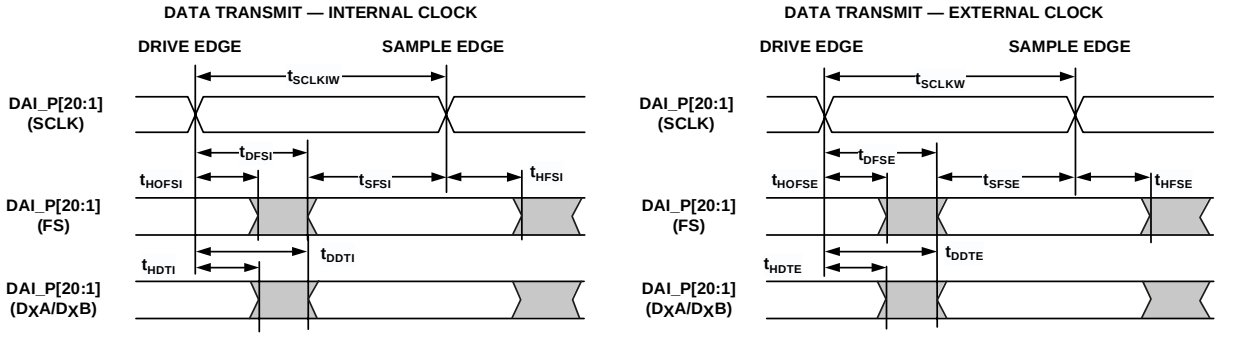


Figure 22. External Late Frame Sync[1]

[1] This figure reflects changes made to support Left-justified Sample Pair mode.



NOTE: EITHER THE RISING EDGE OR FALLING EDGE OF SCLK (EXTERNAL), SCLK (INTERNAL) CAN BE USED AS THE ACTIVE SAMPLING EDGE.



NOTE: EITHER THE RISING EDGE OR FALLING EDGE OF SCLK (EXTERNAL), SCLK (INTERNAL) CAN BE USED AS THE ACTIVE SAMPLING EDGE.

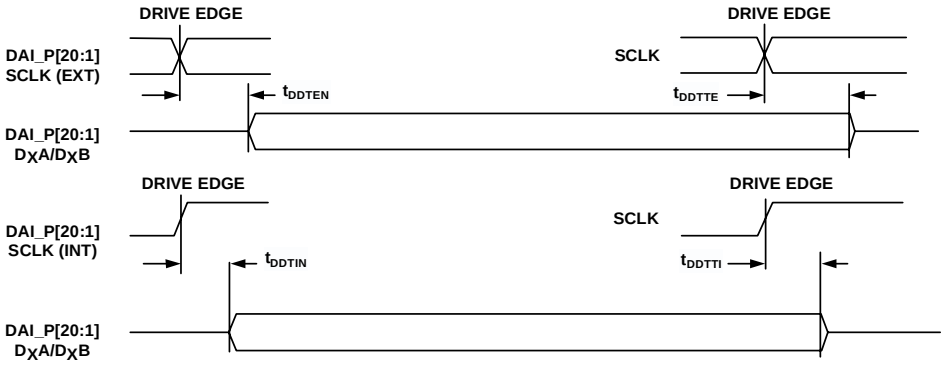


Figure 23. Serial Ports

Input Data Port

The timing requirements for the IDP are given in Table 25.IDP Signals (SCLK, FS, SDATA) are routed to the DAI_P[20:1] pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P[20:1] pins.

Table 25. IDP

Parameter		Min	Max	Units
Timing Requirements				
t_{SIFS}	FS Setup Before SCLK Rising Edge[1]	4		ns
t_{SIHFS}	FS Hold After SCLK Rising Edge[1]	5.5		ns
t_{SISD}	SData Setup Before SCLK Rising Edge[1]	4		ns
t_{SIHD}	SData Hold After SCLK Rising Edge[1]	5.5		ns
$t_{IDPCLKW}$	Clock Width	9		ns
t_{IDPCLK}	Clock Period	20		ns

[1] DATA, SCLK, FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

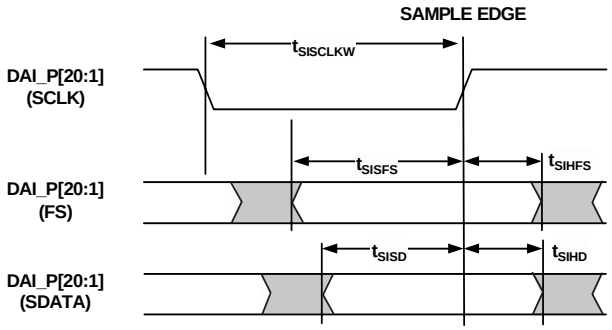


Figure 24. IDP Master Timing

Parallel Data Acquisition Port (PDAP)

The timing requirements for the PDAP are provided in Table 26. PDAP is the parallel mode operation of channel 0 of the IDP. For details on the operation of the IDP, see the IDP chapter of the *ADSP-2136x Peripherals Manual*. Note that the most significant 16 bits of external PDAP data can be provided through either the parallel port AD[15:0] or the DAI_P[20:5] pins. The remaining 4 bits can only be sourced through DAI_P[4:1]. The timing below is valid at the DAI_P[20:1] pins or at the AD[15:0] pins.

Table 26. Parallel Data Acquisition Port (PDAP)

Parameter		Min	Max	Units
Timing Requirements				
$t_{SPCLKEN}$	PDAP_CLKEN Setup Before PDAP_CLK Sample Edge[1]	4		ns
$t_{HPCLKEN}$	PDAP_CLKEN Hold After PDAP_CLK Sample Edge[1]	5.5		ns
t_{PDSD}	PDAP_DAT Setup Before SCLK PDAP_CLK Sample Edge[1]	4		ns
t_{PDHD}	PDAP_DAT Hold After SCLK PDAP_CLK Sample Edge[1]	5.5		ns
t_{PDCLKW}	Clock Width	9		ns
t_{PDCLK}	Clock Period	20		ns
t_{PDHLDD}	Delay of PDAP strobe after last PDAP_CLK capture edge for a word	$2 \times t_{PCLK}$		ns
t_{PDSTRB}	PDAP Strobe Pulse Width	$2 \times t_{PCLK}$		ns

[1] Source pins of DATA are ADDR[7:0], DATA[7:0], or DAI pins. Source pins for SCLK and FS are: 1) DAI pins, 2) CLKIN through PCG, or 3) DAI pins through PCG.

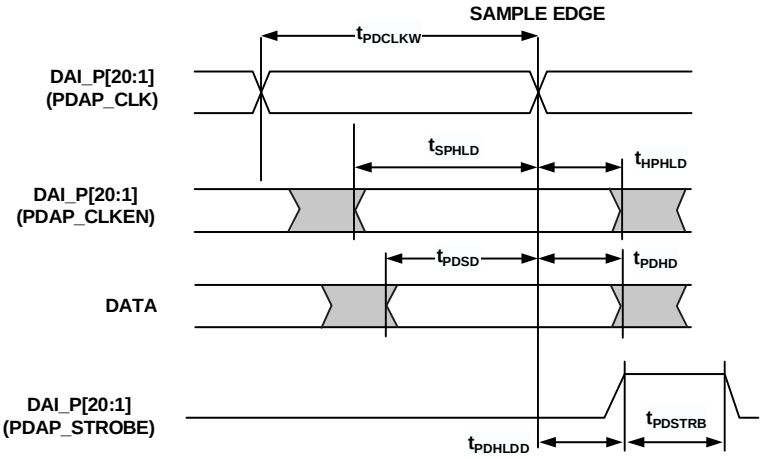


Figure 25. PDAP Timing

Sample Rate Converter

TBD

S/PDIF Compatible Transiever

TBD

SPI Interface—Master

Table 27. SPI Interface Protocol — Master Switching and Timing Specifications

Parameter		Min	Max	Units
Switching Characteristics				
$t_{SPICLKM}$	Serial clock cycle	$8 \times t_{PCLK}$		ns
t_{SPICHM}	Serial clock high period	$4 \times t_{PCLK}$		ns
t_{SPICLM}	Serial clock low period	$4 \times t_{PCLK} - 2$		ns
$t_{DDSPIDM}$	SPICLK edge to data out valid (data out delay time)		0	
$t_{HDSPIDM}$	SPICLK edge to data out not valid (data out hold time)	2		ns
t_{SDSCIM}	FLAG3-0IN (SPI device select) low to first SPICLK edge	$4 \times t_{PCLK} - 2$		ns
t_{HDSM}	Last SPICLK edge to FLAG3-0IN high	$4 \times t_{PCLK} - 1$		ns
t_{SPITDM}	Sequential transfer delay	$4 \times t_{PCLK} - 1$		ns
Timing Requirements				
t_{SSPIDM}	Data input valid to SPICLK edge (data input set-up time)	8		ns
t_{HSPIDM}	SPICLK last sampling edge to data input not valid	2		ns

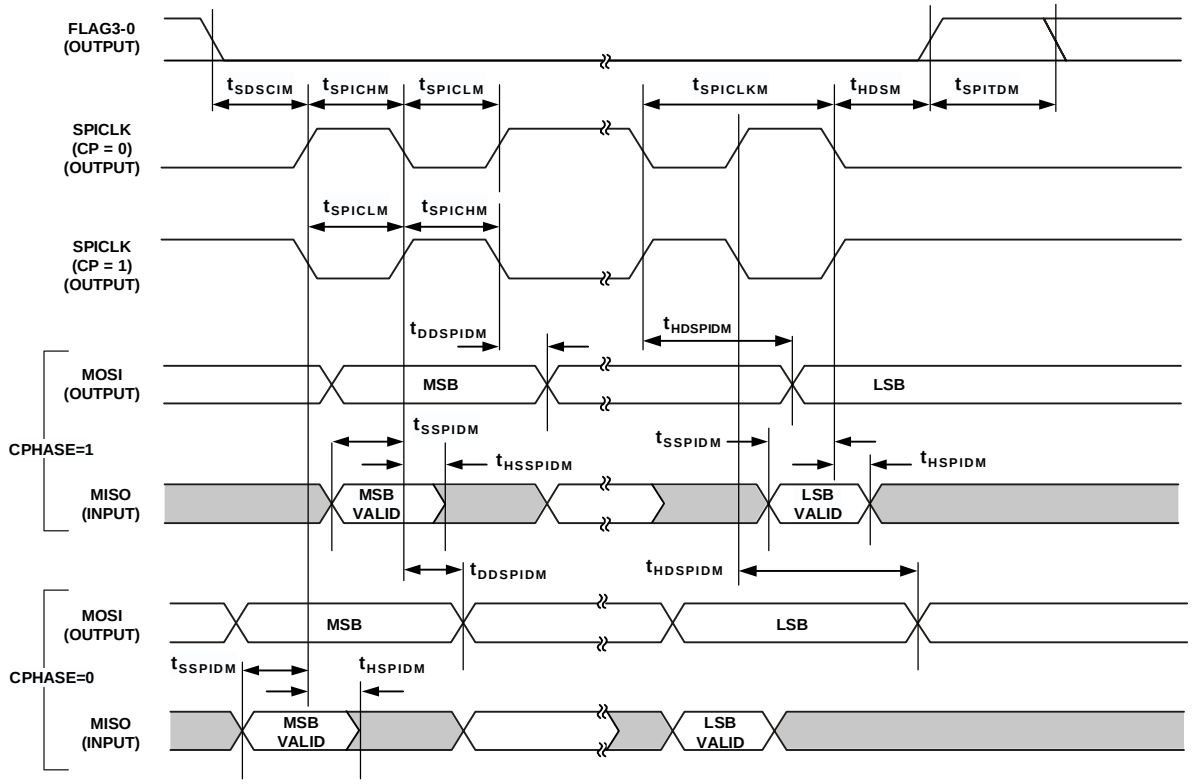


Figure 26. SPI Master Timing

SPI Interface—Slave

Table 28. SPI Interface Protocol —Slave Switching and Timing Specifications

Parameter		Min	Max	Units
Switching Characteristics				
t_{DSOE}	$\overline{SPIDS}$ assertion to data out active	0	4	ns
t_{DSDHI}	$\overline{SPIDS}$ deassertion to data high impedance	0	4	ns
$t_{DDSPIDS}$	SPICLK edge to data out valid (data out delay time)		9.4	ns
$t_{HDSPIDS}$	SPICLK edge to data out not valid (data out hold time)	$2 \times t_{PCLK}$		ns
t_{DSOV}	$\overline{SPIDS}$ assertion to data out valid (CPHASE=0)		$5 \times t_{PCLK}$	ns
Timing Requirements				
$t_{SPICLKS}$	Serial clock cycle	$4 \times t_{PCLK}$		ns
t_{SPICHS}	Serial clock high period	$2 \times t_{PCLK}$		ns
t_{SPICLS}	Serial clock low period	$2 \times t_{PCLK} - 2$		ns
t_{SDSCO}	$\overline{SPIDS}$ assertion to first SPICLK edge			ns
	CPHASE = 0	$2 \times t_{PCLK}$		
	CPHASE = 1	$2 \times t_{PCLK}$		
t_{HDS}	Last SPICLK edge to $\overline{SPIDS}$ not asserted	$2 \times t_{PCLK}$		
	CPHASE = 0			ns
t_{SSPIDS}	Data input valid to SPICLK edge			
	(data input set-up time)	2		ns
t_{HSPIDS}	SPICLK last sampling edge to data input not valid	2		ns
t_{SDPPW}	$\overline{SPIDS}$ deassertion pulse width (CPHASE=0)	$2 \times t_{PCLK}$		ns

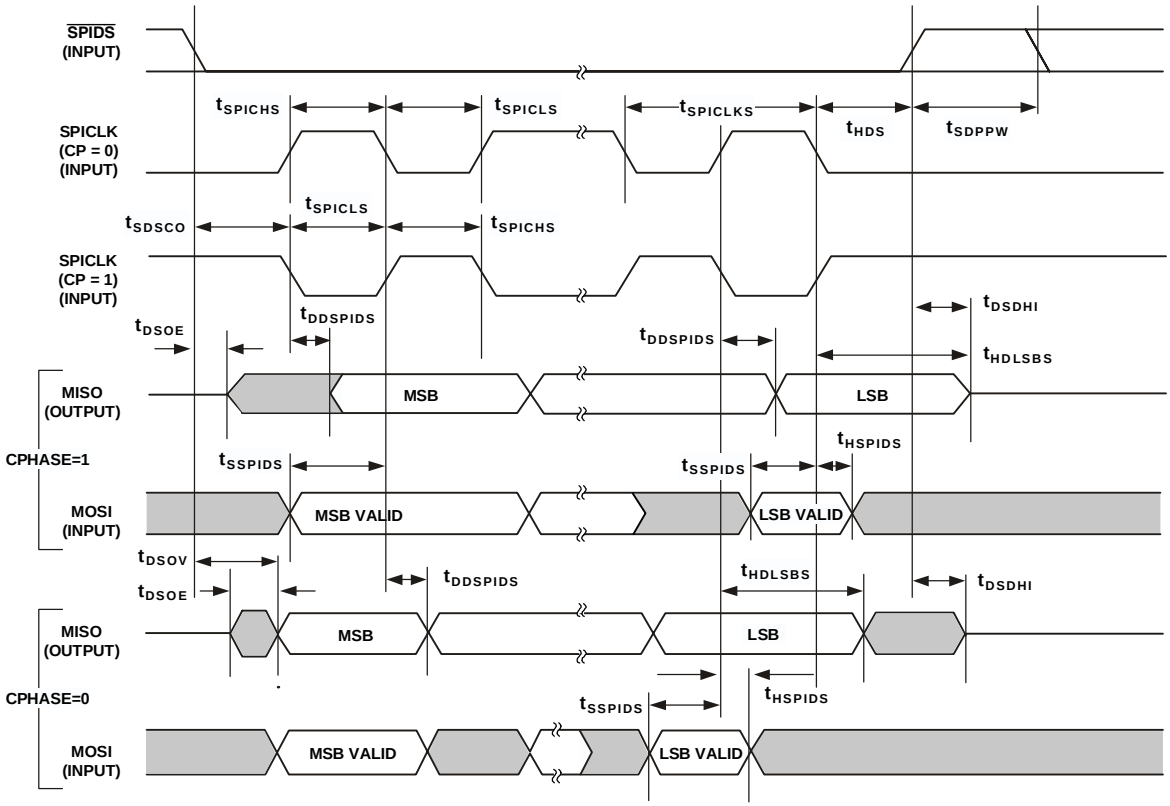


Figure 27. SPI Slave Timing

JTAG Test Access Port and Emulation

Table 29. JTAG Test Access Port and Emulation

Parameter		Min	Max	Units
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}	System Inputs Setup Before TCK Low[1]	7		ns
t_{HSYS}	System Inputs Hold After TCK Low[1]	18		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width	$4t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		13	ns
t_{DSYS}	System Outputs Delay After TCK Low[2]		30	ns

[1] System Inputs = AD15-0, $\overline{SPIDS}$, CLKCFG1-0, $\overline{RESET}$, BOOTCFG1-0, MISO, MOSI, SPICLK, DAI_Px, FLAG3-0.
[2] System Outputs = MISO, MOSI, SPICLK, DAI_Px, AD15-0, $\overline{RD}$, $\overline{WR}$, FLAG3-0, CLKOUT, $\overline{EMU}$, ALE.

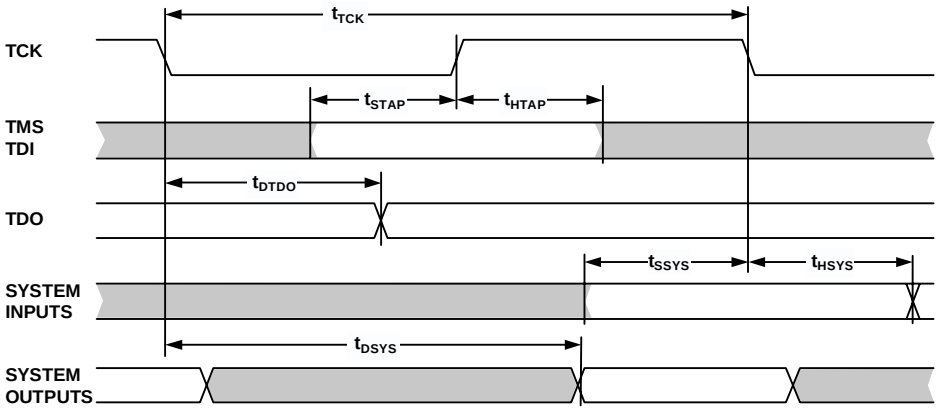


Figure 28. IEEE 11499.1 JTAG Test Access Port

OUTPUT DRIVE CURRENTS

Figure 29 shows typical I-V characteristics for the output drivers of the ADSP-21365. The curves represent the current drive capability of the output drivers as a function of output voltage.

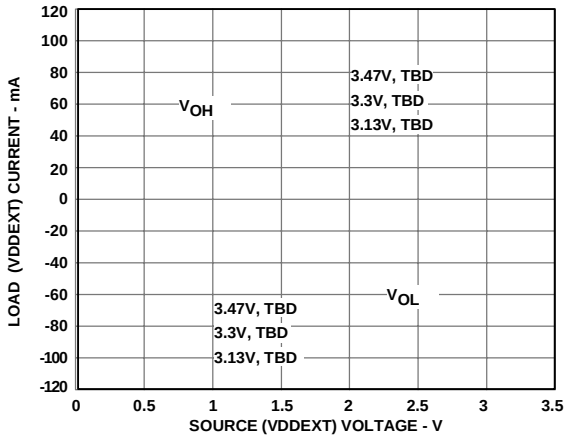


Figure 29. ADSP-21365 Typical Drive

TEST CONDITIONS

The ac signal specifications (timing parameters) appear Table 9 on page 20 through Table 29 on page 38. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 30.

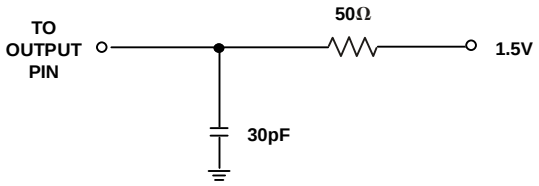


Figure 30. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

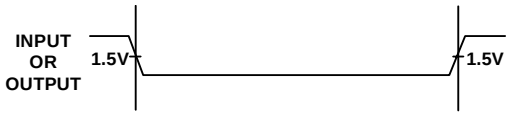


Figure 31. Voltage Reference Levels for AC Measurements

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 30). Figure 34 shows graphically how output delays and holds vary with load capacitance. The graphs of Figure 32, Figure 34 and Figure 33 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20%-80%, V=Min) vs. Load Capacitance.

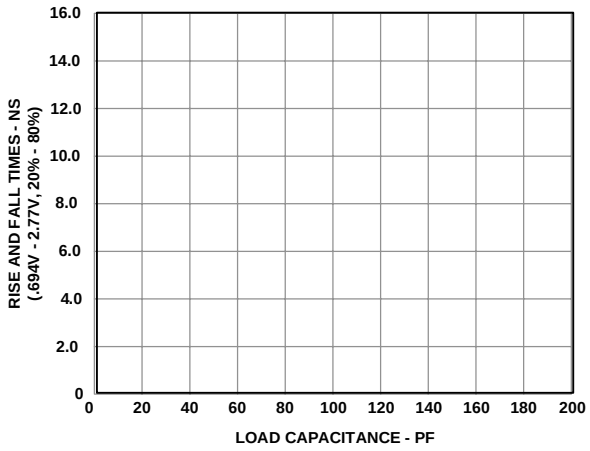


Figure 32. Typical Output Rise/Fall Time (20%-80%, V_{DDEXT} = Max)

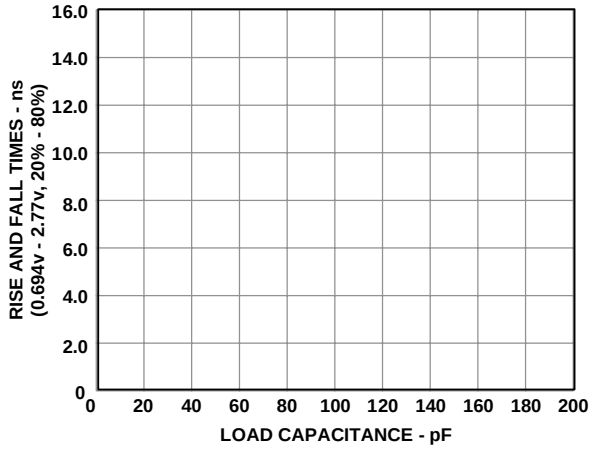


Figure 33. Typical Output Fall Time (20%-80%, V_{DDEXT} = Min)

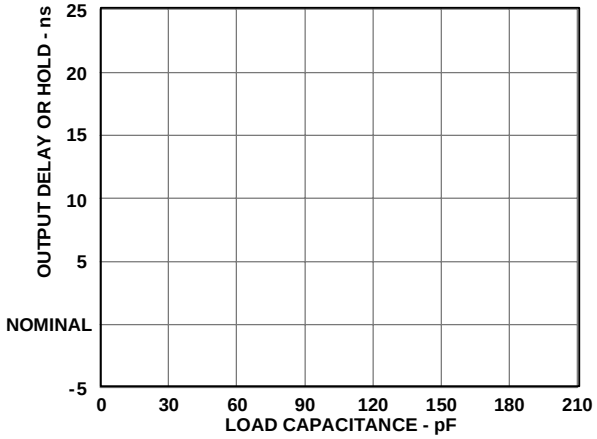


Figure 34. Typical Output Delay or Hold vs. Load Capacitance (at Ambient Temperature)

ENVIRONMENTAL CONDITIONS

The ADSP-21365 is available in 136-Ball Grid Array (BGA) package.

THERMAL CHARACTERISTICS

The ADSP-21365 processor is rated for performance over the commercial temperature range, T_{AMB} = 0°C to 70°C.

Table 30 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6 and the junction-to-board measurement complies with JESD51-8. The junction-to-case measurement complies with MIL- STD-883. All measurements use a 2S2P JEDEC test board.

To determine the Junction Temperature of the device while on the application PCB, use:

$$T_J = T_{CASE} + (\Psi_{JT} \times PD)$$

Where:

T_J= Junction temperature ^{0}C

T_{CASE}= Case temperature (^{0}C) measured at the top center of the package

Ψ_{JT}= Junction-to-Top (of package) characterization parameter = Typical value from the tables below

P_D= Power dissipation see EE Note #TBD

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a 1st order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times PD)$$

Where:

T_A = Ambient Temperature ^{0}C

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heatsink is required.

Values of θ_{JB} are provided for package comparison and PCB design considerations.

Table 30. Thermal Characteristics for 136 Ball BGA[1]

Parameter	Condition	Typical	Units
θ_{JA}	Airflow = 0 m/s	TBD	°C/W
θ_{JMA}	Airflow = 1 m/s	TBD	°C/W
θ_{JMA}	Airflow = 2 m/s	TBD	°C/W
θ_{JB}	–	TBD	°C/W
θ_{JC}	–	TBD	°C/W
Ψ_{JT}	Airflow = 0 m/s	TBD	°C/W
Ψ_{JMT}	Airflow = 1 m/s	TBD	°C/W
Ψ_{JMT}	Airflow = 2 m/s	TBD	°C/W

[1] The thermal characteristics values provided in this table are modeled values.

136-BALL BGA PIN CONFIGURATIONS

Table 31. 136-Ball BGA Pin Assignments

Pin Name	BGA Pin#	Pin Name	BGA Pin#	Pin Name	BGA Pin#	Pin Name	BGA Pin#
CLKCFG0	A01	CLKCFG1	B01	BOOTCFG1	C01	V_{DDINT}	D01
XTAL	A02	GND	B02	BOOTCFG0	C02	GND	D02
TMS	A03	V_{DDEXT}	B03	GND	C03	GND	D04
TCK	A04	CLKIN	B04	GND	C12	GND	D05
TDI	A05	TRST	B05	GND	C13	GND	D06
CLKOUT	A06	A_{VSS}	B06	V_{DDINT}	C14	GND	D09
TDO	A07	A_{VDD}	B07			GND	D10
$\overline{EMU}$	A08	V_{DDEXT}	B08			GND	D11
MOSI	A09	$\overline{SPICLK}$	B09			GND	D13
MISO	A10	$\overline{RESET}$	B10			V_{DDINT}	D14
$\overline{SPIDS}$	A11	V_{DDINT}	B11				
V_{DDINT}	A12	GND	B12				
GND	A13	GND	B13				
GND	A14	GND	B14				
V_{DDINT}	E01	FLAG1	F01	AD7	G01	AD6	H01
GND	E02	FLAG0	F02	V_{DDINT}	G02	V_{DDEXT}	H02
GND	E04	GND	F04	V_{DDEXT}	G13	DAI_P18 (SD5B)	H13
GND	E05	GND	F05	DAI_P19 (SCLK45)	G14	DAI_P17 (SD5A)	H14
GND	E06	GND	F06				
GND	E09	GND	F09				
GND	E10	GND	F10				
GND	E11	GND	F11				
GND	E13	FLAG2	F13				
FLAG3	E14	DAI_P20 (SFS45)	F14				

Table 31. 136-Ball BGA Pin Assignments (Continued)

Pin Name	BGA Pin#	Pin Name	BGA Pin#	Pin Name	BGA Pin#	Pin Name	BGA Pin#
AD5	J01	AD3	K01	AD2	L01	AD0	M01
AD4	J02	V_{DDINT}	K02	AD1	L02	$\overline{WR}$	M02
GND	J04	GND	K04	GND	L04	GND	M03
GND	J05	GND	K05	GND	L05	GND	M12
GND	J06	GND	K06	GND	L06	DAI_P12 (SD3B)	M13
GND	J09	GND	K09	GND	L09	DAI_P13 (SCLK23)	M14
GND	J10	GND	K10	GND	L10		
GND	J11	GND	K11	GND	L11		
V_{DDINT}	J13	GND	K13	GND	L13		
DAI_P16 (SD4B)	J14	DAI_P15 (SD4A)	K14	DAI_P14 (SFS23)	L14		
AD15	N01	AD14	P01				
ALE	N02	AD13	P02				
$\overline{RD}$	N03	AD12	P03				
V_{DDINT}	N04	AD11	P04				
V_{DDEXT}	N05	AD10	P05				
AD8	N06	AD9	P06				
V_{DDINT}	N07	DAI_P1 (SD0A)	P07				
DAI_P2 (SD0B)	N08	DAI_P3 (SCLK0)	P08				
V_{DDEXT}	N09	DAI_P5 (SD1A)	P09				
DAI_P4 (SFS0)	N10	DAI_P6 (SD1B)	P10				
V_{DDINT}	N11	DAI_P7 (SCLK1)	P11				
V_{DDINT}	N12	DAI_P8 (SFS1)	P12				
GND	N13	DAI_P9 (SD2A)	P13				
DAI_P10 (SD2B)	N14	DAI_P11 (SD3A)	P14				

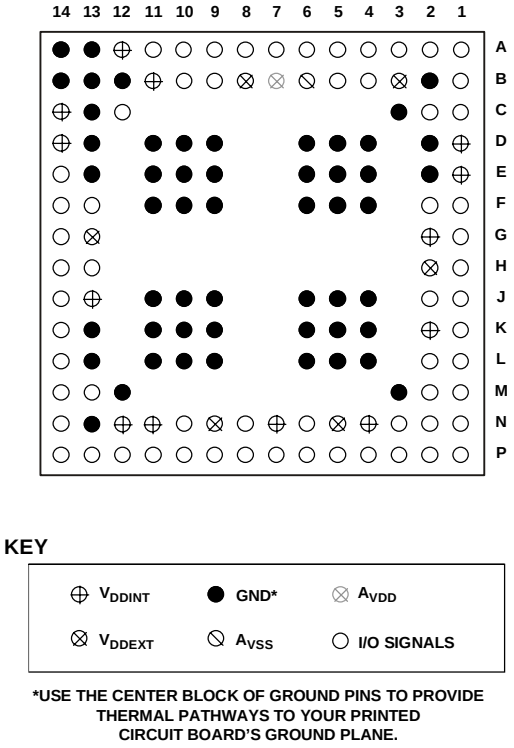
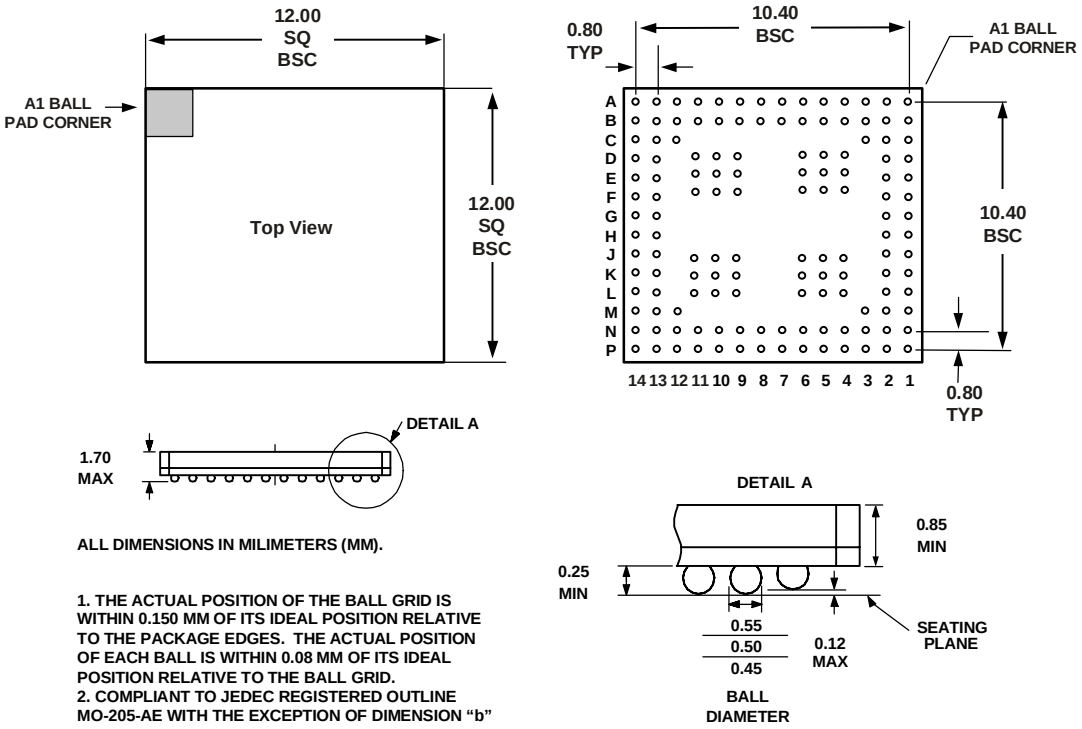


Figure 35. 136-Ball BGA Pin Assignments (Bottom View, Summary)

PACKAGE DIMENSIONS

The ADSP-21365 is available in a 136-ball BGA package. All dimensions are in millimeters (mm).

Figure 36. 136-ball BGA ()



ALL DIMENSIONS IN MILIMETERS (MM).

1. THE ACTUAL POSITION OF THE BALL GRID IS WITHIN 0.150 MM OF ITS IDEAL POSITION RELATIVE TO THE PACKAGE EDGES. THE ACTUAL POSITION OF EACH BALL IS WITHIN 0.08 MM OF ITS IDEAL POSITION RELATIVE TO THE BALL GRID.
2. COMPLIANT TO JEDEC REGISTERED OUTLINE MO-205-AE WITH THE EXCEPTION OF DIMENSION "b"

ORDERING GUIDE

Analog Devices offers a wide variety of audio algorithms and combinations to run on the ADSP-21365 DSP. These products are sold as part of a chip set, bundled with necessary application software under special part numbers. For a complete list, visit our web site at www.analog.com\SHARC.

These product also may contain 3rd party IPs that may require users to have authorization from the respective IP holders to receive them. Royalty for use of the 3rd party IPs may also be payable by users.

Part Number[1,2,3]	Ambient Temperature Range	Instruction Rate	On-Chip SRAM	ROM	Operating Voltage	Packages
ADSP-21365SKBCZENG	0°C to +70°C	300 MHz	3 Mbit	4 Mbit	1.2 INT/3.3 EXT V	136-Lead BGA
ADSP-21365SKBC-ENG	0°C to +70°C	300 MHz	3 Mbit	4 Mbit	1.2 INT/3.3 EXT V	136-Lead BGA pb free

[1] K indicates commercial grade temperature (0°C to +70°C).
[2] B indicates Ball Grid Array package.
[3] Z indicates Lead Free package. For more information about lead free package offerings, please visit www.analog.com.