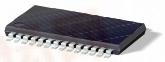
查询TPS54010供应商

捷多邦，专业PCB打样工厂，24小时加急出货



Typical Size
6,4 mm X 9,7 mm

2.2 – 4 -V, 14-A OUTPUT SYNCHRONOUS BUCK PWM SWITCHER WITH INTEGRATED FETs (SWIFT™)

FEATURES

- Separate Low-Voltage Power Bus
- 8-mΩ MOSFET Switches for High Efficiency at 14-A Continuous Output
- Adjustable Output Voltage Down to 0.9 V
- Externally Compensated With 1% Internal Reference Accuracy
- Fast Transient Response
- Wide PWM Frequency: Adjustable 280 kHz to 700 kHz
- Load Protected by Peak Current Limit and Thermal Shutdown
- Integrated Solution Reduces Board Area and Total Cost

APPLICATIONS

- Low-Voltage, High-Density Systems With Power Distributed at 2.5 V, 3.3 V Available
- Point of Load Regulation for High Performance DSPs, FPGAs, ASICs and Microprocessors
- Broadband, Networking and Optical Communications Infrastructure

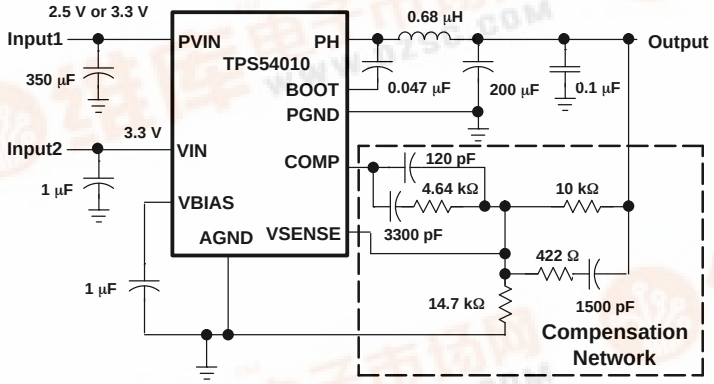
DESCRIPTION

As a member of the SWIFT™ family of dc/dc regulators, the TPS54010 low-input voltage high-output current synchronous buck PWM converter integrates all required active components. Included on the substrate with the listed features are a true, high performance, voltage error amplifier that enables maximum performance under transient conditions and flexibility in choosing the output filter L and C components; an under-voltage-lockout circuit to prevent start-up until the VIN input voltage reaches 3 V; an internally and externally set slow-start circuit to limit in-rush currents; and a power good output useful for processor/logic reset, fault signaling, and supply sequencing.

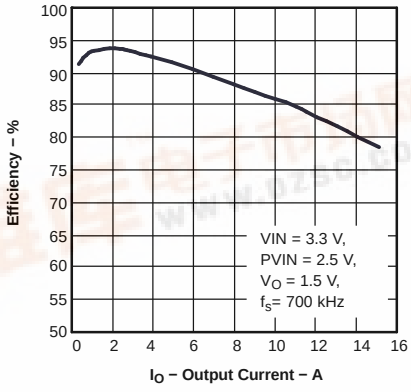
The TPS54010 is available in a thermally enhanced 28-pin TSSOP (PWP) PowerPAD™ package, which eliminates bulky heatsinks.

PRODUCT PREVIEW

SIMPLIFIED SCHEMATIC



EFFICIENCY VS OUTPUT CURRENT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SWIFT, PowerPAD are trademarks of Texas Instruments.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the

Copyright © 2004, Texas Instruments Incorporated

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	OUTPUT VOLTAGE	PACKAGE	PART NUMBER
-40°C to 85°C	Adjustible down to 0.9 V	Plastic HTSSOP (PWP)(1)	TPS54010PWP

(1) The PWP package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS54010PWPR). See the application section of the data sheet for PowerPAD drawing and layout information.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

			TPA6120A2
V_I	Input voltage range	SS/ENA, SYNC	-0.3 V to 7 V
		RT	-0.3 V to 6 V
		VSENSE	-0.3 V to 4 V
		PVIN, VIN	-0.3 V to 4.5 V
		BOOT	-0.3 V to 10 V
V_O	Output voltage range	VBIAS, COMP, PWRGD	-0.3 V to 7 V
		PH	-0.6 V to 6 V
V_O	Source current	PH	Internally limited
		COMP, VBIAS	6 mA
I_S	Sinlk current	PH	25 A
		COMP	6 mA
		SS/ENA, PWRGD	10 mA
	Voltage differential	AGND to PGND	±0.3 V
T_J	Operating junction temperature range		- 40°C to 125°C
T_{stg}	Storage temperature range		- 65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

PRODUCT PREVIEW

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_I	Input voltage, VIN	3		4	V
	Power Input voltage, PVIN	2.2	2.5	4	V
T_J	Operating junction temperature	-40		125	°C

DISSIPATION RATINGS(1)(2)

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT	T_A = 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
28-Pin PWP with solder	14.4°C/W	6.94 W(3)	3.81 W	2.77 W
28-Pin PWP without solder	27.9°C/W	3.58 W	1.97 W	1.43 W

(1) For more information on the PWP package, refer to TI technical brief, literature number SLMA002.
(2) Test board conditions:
  a. 3 inch x 3 inch, 4 layers, thickness: 0.062 inch
  b. 1.5 oz. copper traces located on the top of the PCB
  c. 1.5 oz. copper ground plane on the bottom of the PCB
  d. 0.5 oz. copper ground planes on the 2 internal layers
  e. 12 thermal vias (see Recommended Land Pattern in applications section of this data sheet)
(3) Maximum power dissipation may be limited by over current protection.

ELECTRICAL CHARACTERISTICS

T_J = -40°C to 125°C, VIN = 3 V to 4 V, PVIN = 2.2 V to 4 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE, VIN							
V_I	Imput voltage, VIN			3		4	V
	Supply voltage range, PVIN	Output = 1.8 V		2.2	2.5	4	V
I_Q	Quiescent current	f_s = 350 kHz, RT open, PH pin open, PVIN = 2.5 V, SYNC = 0 V	VIN		6.3	10	mA
		f_s = 550 kHz, RT open, PH pin open, SYNC ≥ 2.5 V, PVIN = 2.5 V	VIN		8.3	13	mA
		SHUTDOWN, SS/ENA = 0 V, PVIN = 2.5 V	VIN		1	1.4	mA
		f_s = 350 kHz, RT open, PH pin open, PVIN = 3.3 V, SYNC = 0 V	PVIN		6	8	mA
		f_s = 550 kHz, RT open, PH pin open, SYNC ≥ 2.5 V, PVIN = 2.5 V, VIN = 3.3 V	PVIN		6	9	mA
		SHUTDOWN, SS/ENA = 0 V, VIN = 3.3 V	PVIN		<140		µA
UNDERVOLTAGE LOCKOUT (VIN)							
	Start threshold voltage, UVLO				2.95	3	V
	Stop threshold voltage, UVLO			2.7	2.8		V
	Hysteresis voltage, UVLO				0.16		V
	Rising and falling edge deglitch, UVLO(1)				2.5		µs
BIAS VOLTAGE							
	Output voltage, VBIAS	$I_{(VBIAS)}$ = 0		2.7	2.8	2.9	V
	Output current, VBIAS(2)					100	µA
CUMULATIVE REFERENCE							
V_{ref}	Accuracy			0.882	0.891	0.900	V
REGULATION							
	Line regulation(1)(3)	I_L = 7 A, f_s = 350 kHz, T_J = 85°C			0.07		%/V
	Load regulation(1)(3)	I_L = 0 A to 14 A, f_s = 350 kHz, T_J = 85°C			0.03		%/A
OSCILLATOR							
	Internally set—free running frequency	RT open(1), SYNC ≤ 0.8 V		280	350	420	kHz
		RT open(1), SYNC ≥ 2.5 V		440	550	660	kHz
	Externally set—free running frequency range	RT = 180 kΩ (1% resistor to AGND)(1)		262	280	308	kHz
		RT = 100 kΩ (1% resistor to AGND)		460	500	540	kHz
		RT = 68 kΩ (1% resistor to AGND)(1)		663	700	762	kHz
	High-level threshold voltage, SYNC			2.5			V
	Low-level threshold voltage, SYNC					0.8	V
	Pulse duration, SYNC(1)			50			ns
	Frequency range, SYNC			300		700	kHz
	Ramp Valley(1)				0.75		V
	Ramp amplitude (peak-to-peak)(1)				1		V
	Minimum controllable on time(1)					200	ns
	Maximum duty cycle(1)			90%			

(1) Specified by design
(2) Static resistive loads only
(3) Specified by the circuit used in Figure 10

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

T_J = -40°C to 125°C, VIN = 3 V to 4 V, PVIN = 2.2 V to 4 V (unless otherwise noted)

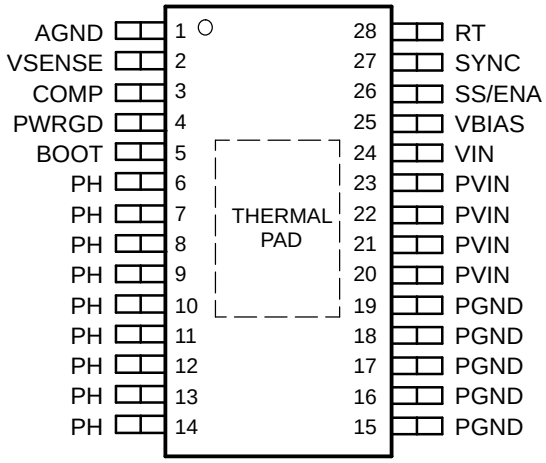
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER						
	Error amplifier open loop voltage gain	1 kΩ COMP to AGND(4)	90	110		dB
	Error amplifier unity gain bandwidth	Parallel 10 kΩ, 160 pF COMP to AGND(4)	3	5		MHz
	Error amplifier common mode input voltage range	Powered by internal LDO(4)	0		VBIAS	V
	Input bias current, VSENSE	VSENSE = V_{ref}		60	250	nA
	Output voltage slew rate (symmetric), COMP		1	1.4		V/µs
PWM COMPARATOR						
	PWM comparator propagation delay time, PWM comparator input to PH pin (excluding deadtime)	10-mV overdrive(4)		70	85	ns
SLOW-START/ENABLE						
	Enable threshold voltage, SS/ENA		0.82	1.2	1.4	V
	Enable hysteresis voltage, SS/ENA(4)			0.03		V
	Falling edge deglitch, SS/ENA(4)			2.5		µs
	Internal slow-start time		2.4	3.13	4.1	s
	Charge current, SS/ENA	SS/ENA = 0 V	2	5	8	µA
	Discharge current, SS/ENA	SS/ENA = 0.2 V, VIN = 2.7 V, PVIN = 2.5 V	1.3	2	4	mA
POWER GOOD						
	Power good threshold voltage	VSENSE falling		93		%V_{ref}
	Power good hysteresis voltage(4)			3		%V_{ref}
	Power good falling edge deglitch(4)			35		µs
	Output saturation voltage, PWRGD	$I_{(sink)}$ = 2.5 mA		0.18	0.3	V
	Leakage current, PWRGD	VIN = 3.3 V, PVIN = 2.5 V			1	µA
CURRENT LIMIT						
	Current limit	VIN = 3.3 V, PVIN = 2.5 V(1)(4), Output shorted	14.5	21		A
	Current limit leading edge blanking time(4)			100		ns
	Current limit total response time(4)			200		ns
THERMAL SHUTDOWN						
	Thermal shutdown trip point(4)		135	150	165	°C
	Thermal shutdown hysteresis(4)			10		°C
OUTPUT POWER MOSFETS						
$r_{DS(on)}$	Power MOSFET switches	VIN = 3 V, PVIN = 2.5 V		8	20	mΩ
		VIN = 3.6 V, PVIN = 2.5 V		8	20	

(4) Specified by design

PRODUCT PREVIEW

DEVICE INFORMATION

PWP PACKAGE
(TOP VIEW)



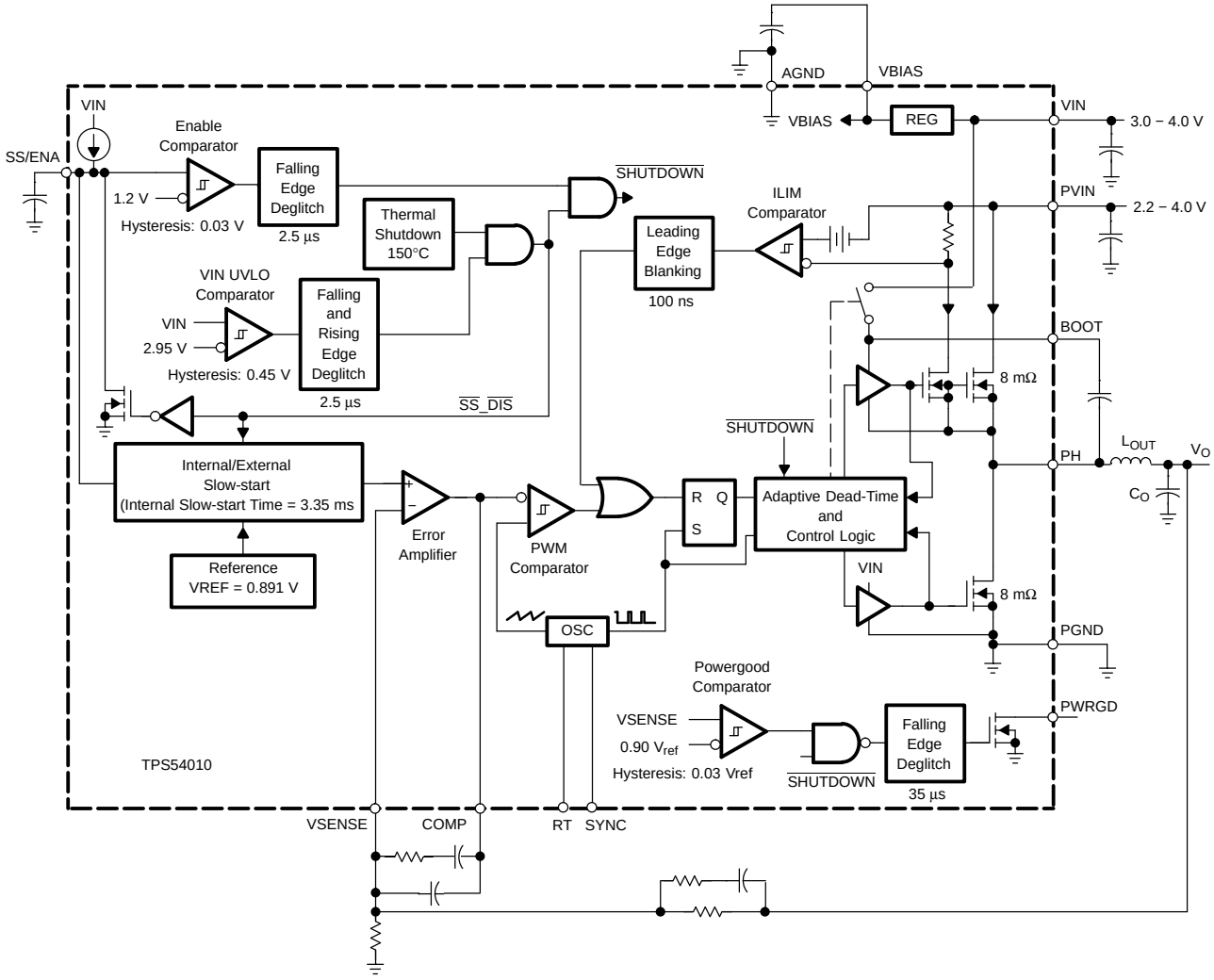
TERMINAL FUNCTIONS

PIN NAME	PIN NUMBER	DESCRIPTION
AGND	1	Analog ground. Return for compensation network/output divider, slow-start capacitor, VBIAS capacitor, and RT resistor. If using the PowerPAD, connect it to AGND. See the *Application Information* section for details.
BOOT	5	Bootstrap output. 0.022-µF to 0.1-µF low-ESR capacitor connected from BOOT to PH generates floating drive for the high-side FET driver.
COMP	3	Error amplifier output. Connect frequency compensation network from COMP to VSENSE
PGND	15, 16, 17, 18, 19	Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors. A single point connection to AGND is recommended.
PH	6-14	Phase output. Junction of the internal high-side and low-side power MOSFETs, and output inductor.
PVIN	20, 21, 22, 23	Input supply for the power MOSFET switches and internal bias regulator. Bypass the PVIN pins to the PGND pins close to device package with a high-quality, low-ESR 10-µF ceramic capacitor.
PWRGD	4	Power good open drain output. High when VSENSE . 90% V_{ref}, otherwise PWRGD is low. Note that output is low when SS/ENA is low or the internal shutdown signal is active.
RT	28	Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency, f_s.
SS/ENA	26	Slow-start/enable input/output. Dual function pin which provides logic input to enable/disable device operation and capacitor input to externally set the start-up time.
SYNC	27	Synchronization input. Dual function pin which provides logic input to synchronize to an external oscillator or pin select between two internally set switching frequencies. When used to synchronize to an external signal, a resistor must be connected to the RT pin.
VBIAS	25	Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high-quality, low-ESR 0.1-µF to 1.0-µF ceramic capacitor.
VIN	24	Input supply for the internal control circuits. Bypass the VIN pin to the PGND pins close to device package with a high-quality, low-ESR 1-µF ceramic capacitor.
VSENSE	2	Error amplifier inverting input. Connect to output voltage compensation network/output divider.

PRODUCT PREVIEW

PRODUCT PREVIEW

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

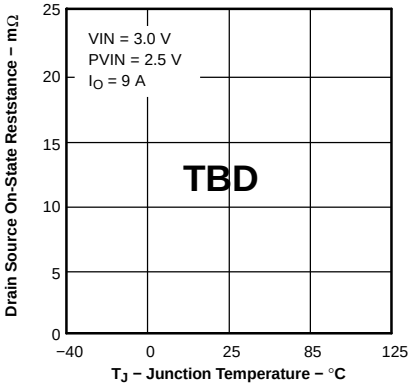


Figure 1.

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

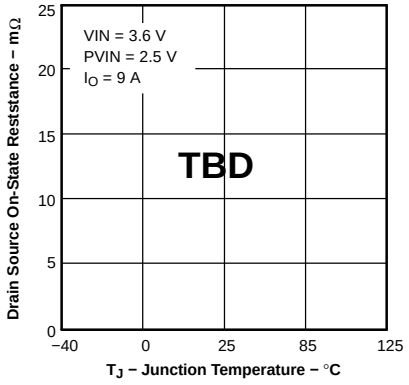


Figure 2.

INTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

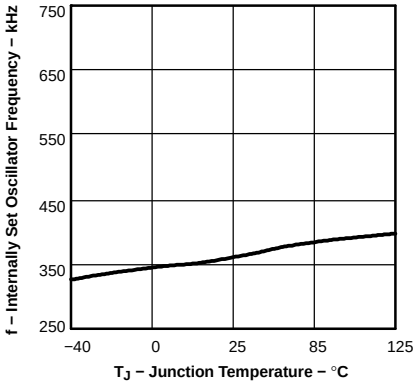


Figure 3.

EXTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

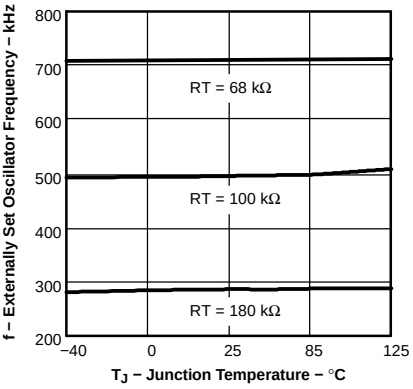


Figure 4.

VOLTAGE REFERENCE vs JUNCTION TEMPERATURE

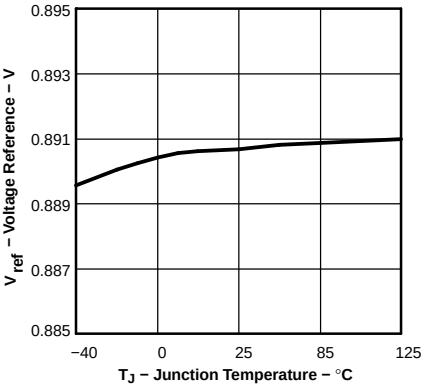


Figure 5.

DEVICE POWER LOSSES vs LOAD CURRENT

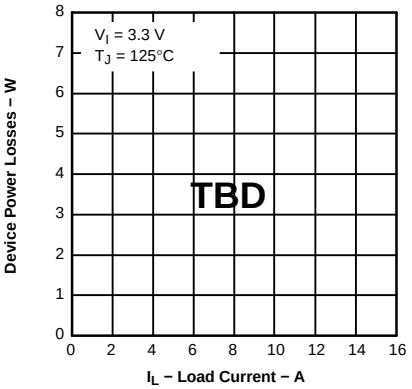


Figure 6.

REFERENCE VOLTAGE vs INPUT VOLTAGE

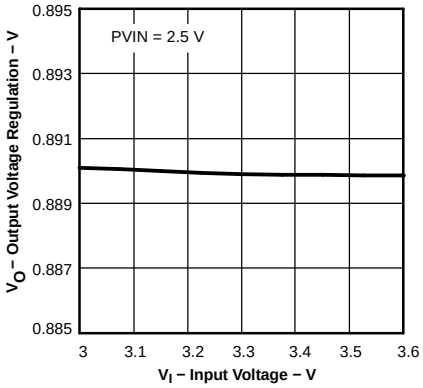


Figure 7.

ERROR AMPLIFIER OPEN LOOP RESPONSE

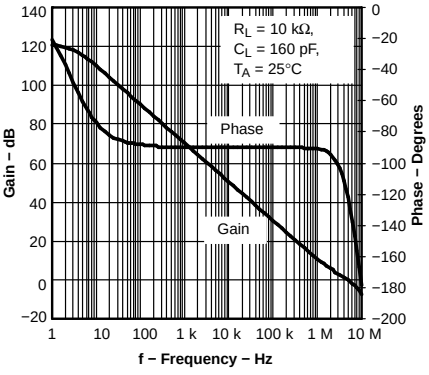


Figure 8.

INTERNAL SLOWS-START TIME vs JUNCTION TEMPERATURE

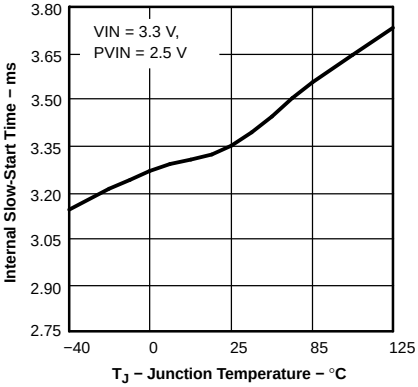


Figure 9.

PRODUCT PREVIEW

DETAILED DESCRIPTION

UNDERVOLTAGE LOCKOUT (UVLO)

The TPS54010 incorporates an under voltage lockout circuit to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until VIN exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start-up begins. The device operates until VIN falls below the nominal UVLO stop threshold of 2.8 V. Hysteresis in the UVLO comparator, and a 2.5-ms rising and falling edge deglitch circuit reduce the likelihood of shutting the device down due to noise on VIN. UVLO is with respect to VIN and not PVIN, see the *Application Information* section.

SLOW-START/ENABLE (SS/ENA)

The slow-start/enable pin provides two functions. First, the pin acts as an enable (shutdown) control by keeping the device turned off until the voltage exceeds the start threshold voltage of approximately 1.2 V. When SS/ENA exceeds the enable threshold, device start-up begins. The reference voltage fed to the error amplifier is linearly ramped up from 0 V to 0.891 V in 3.35 ms. Similarly, the converter output voltage reaches regulation in approximately 3.35 ms. Voltage hysteresis and a 2.5-ms falling edge deglitch circuit reduce the likelihood of triggering the enable due to noise.

The second function of the SS/ENA pin provides an external means of extending the slow-start time with a low-value capacitor connected between SS/ENA and AGND.

Adding a capacitor to the SS/ENA pin has two effects on start-up. First, a delay occurs between release of the SS/ENA pin and start-up of the output. The delay is proportional to the slow-start capacitor value and lasts until the SS/ENA pin reaches the enable threshold. The start-up delay is approximately:

$$t_d = C_{(SS)} \times \frac{1.2\ V}{5\ \mu A} \quad (1)$$

Second, as the output becomes active, a brief ramp-up at the internal slow-start rate may be observed before the externally set slow-start rate takes control and the output rises at a rate proportional to the slow-start capacitor. The slow-start time set by the capacitor is approximately:

$$t_{(SS)} = C_{(SS)} \times \frac{0.7\ V}{5\ \mu A} \quad (2)$$

The actual slow-start time is likely to be less than the above approximation due to the brief ramp-up at the internal rate.

VBIAS REGULATOR (VBIAS)

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R or X5R grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor must be placed close to the VBIAS pin and returned to AGND.

External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.70 V, and external loads on VBIAS with ac or digital switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits. VBIAS is derived from the VIN pin, see the functional block diagram of this data sheet.

VOLTAGE REFERENCE

The voltage reference system produces a precise Vref signal by scaling the output of a temperature stable bandgap circuit. During manufacture, the bandgap and scaling circuits are trimmed to produce 0.891 V at the output of the error amplifier, with the amplifier connected as a voltage follower. The trim procedure adds to the high precision regulation of the TPS54010, since it cancels offset errors in the scale and error amplifier circuits.

OSCILLATOR AND PWM RAMP

The oscillator frequency is set to an internally fixed value of 350 kHz. The oscillator frequency can be externally adjusted from 280 to 700 kHz by connecting a resistor between the RT pin to ground. The switching frequency is approximated by the following equation, where R is the resistance from RT to AGND:

$$\text{Switching Frequency} = \frac{100\ k\Omega}{R} \times 500\ [kHz] \quad (3)$$

ERROR AMPLIFIER

The high performance, wide bandwidth, voltage error amplifier sets the TPS54010 apart from most dc/dc converters. The user is given the flexibility to use a wide range of output L and C filter components to suit the particular application needs. Type-2 or Type-3 compensation can be employed using external compensation components.

PRODUCT PREVIEW

PWM CONTROL

Signals from the error amplifier output, oscillator, and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead-time and control-logic block. During steady-state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch. Once the PWM latch is set, the low-side FET remains on for a minimum duration set by the oscillator pulse width. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp. During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset, and the high-side FET remains on until the oscillator pulse signals the control logic to turn the high-side FET off and the low-side FET on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as VREF. If the error amplifier output is low, the PWM latch is continually reset and the high-side FET does not turn on. The low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS54010 is capable of sinking current continuously until the output reaches the regulation set-point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high-side FET turns off and low-side FET turns on to decrease the energy in the output inductor and consequently the output current. This process is repeated each cycle in which the current limit comparator is tripped.

DEAD-TIME CONTROL AMD MOSFET DRIVERS

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs during the switching transitions by actively controlling the turn-on times of the MOSFET drivers. The high-side driver does not turn on until the voltage at the gate of the low-side FET is below 2 V. While the low-side driver does not turn on until the voltage at the gate of the high-side MOSFET is below 2 V.

The high-side and low-side drivers are designed with 300-mA source and sink capability to quickly drive the power MOSFETs gates. The low-side driver is supplied from VIN, while the high-side drive is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and an internal 2.5-Ω bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external component count.

OVERCURRENT PROTECTION

The cycle-by-cycle current limiting is achieved by sensing the current flowing through the high-side MOSFET and comparing this signal to a preset overcurrent threshold. The high side MOSFET is turned off within 200 ns of reaching the current limit threshold. A 100-ns leading edge blanking circuit prevents current limit false tripping. Current limit detection occurs only when current flows from VIN to PH when sourcing current to the output filter. Load protection during current sink operation is provided by thermal shutdown.

THERMAL SHUTDOWN

The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown automatically when the junction temperature decreases to 10°C below the thermal shutdown trip point, and starts up under control of the slow-start circuit.

Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. With a persistent fault condition, the device cycles continuously; starting up by control of the slow-start circuit, heating up due to the fault condition, and then shutting down upon reaching the thermal shutdown trip point. This sequence repeats until the fault condition is removed.

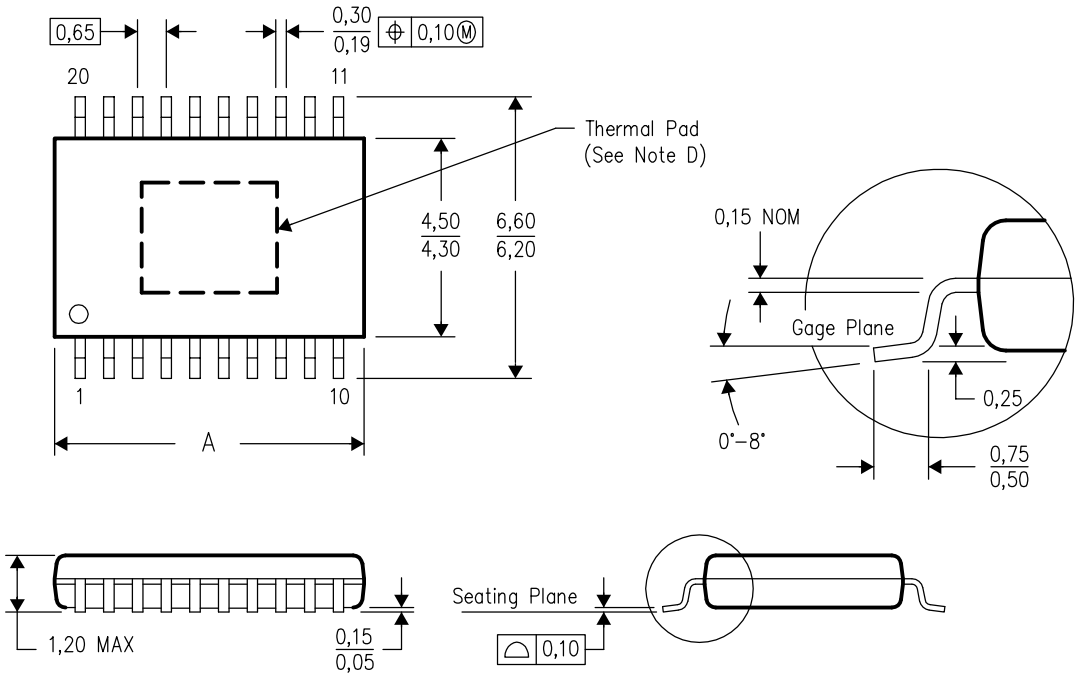
POWER-GOOD (PWRGD)

The power good circuit monitors for under voltage conditions on VSENSE. If the voltage on VSENSE is 10% below the reference voltage, the open-drain PWRGD output is pulled low. PWRGD is also pulled low if VIN is less than the UVLO threshold or SS/ENA is low. When VIN . UVLO threshold, SS/ENA . enable threshold, and VSENSE > 90% of Vref, the open drain output of the PWRGD pin is high. A hysteresis voltage equal to 3% of V_{ref} and a 35-µs falling edge deglitch circuit prevent tripping of the power good comparator due to high frequency noise.

PRODUCT PREVIEW

PWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/G 08/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2004, Texas Instruments Incorporated