June 2002

8 - Bit Micro-controller

with 64KB flash & 4KB RAM embedded

Product List

SM79164V16J/Q,16MHz 64KB internal flash MCU
SM79164L20P, 20MHz 64KB internal flash MCU
SM79164L25J/Q, 25MHz 64KB internal flash MCU
SM79164C25P, 25MHz 64KB internal flash MCU
SM79164C35J/Q, 35MHz 64KB internal flash MCU

Description

The SM79164 series product is an 8 - bit single chip micro controller with 64KB on-chip flash and 4K byte RAM embedded. It is a derivative of the 8052 micro controller family. It has 8-channel PWM build-in. User can access on-chip expanded RAM with easier and faster way by its 'bank mapping direct addressing mode' scheme. With its hardware features and powerful instruction set, it's straight forward to make it a versatile and cost effective controller for those applications which demand up to 32 I/O pins for PDIP package or up to 36 I/O pins for PLCC/QFP package, or applications which need up to 64K byte flash memory for program data.
To program the on-chip flash memory, a commercial writer is available to do it in parallel programming method.

Ordering Information

yywwv
SM79164ihhk

yy: year, ww:week
v: version identifier {, A, B,...}
i:process identifier {V=2.4V~3.0V, L=3.0V ~ 3.6V, C=4.5V ~ 5.5V}
hh: working clock in MHz {20, 25, 35}
k: package type postfix {as below table}

Postfix	Package	Pin/Pad Configuration	Dimension
P	40L PDIP	page 2	page 21
J	44L PLCC	page 2	page 22
Q	44L QFP	page 2	page 23

Features

- Working voltage: 2.4V ~ 3.0V For V Version, 3.0V ~ 3.6V For L Version, 4.5V ~ 5.5V For C Version
- General 8052 family compatible
- 12 clocks per machine cycle
- 64K byte on chip program flash
- 4096 byte on-chip data RAM
- Three 16 bit Timers/Counters
- One Watch Dog Timer
- Four 8-bit I/O ports for PDIP package
- Four 8-bit I/O ports + one 4-bit I/O ports for PLCC or QFP package
- Full duplex serial channel
- Bit operation instruction
- Industrial Level
- 8-bit Unsigned Division
- 8-bit Unsigned Multiply
- BCD arithmetic
- Direct Addressing
- Indirect Addressing
- Nested Interrupt
- Two priority level interrupt
- A serial I/O port
- Power save modes: Idle mode and Power down mode
- Code protection function
- Low EMI (inhibit ALE)
- Bank mapping direct addressing mode for access on-chip RAM
- 8 channel PWM function with P1.0 ~ P1.7

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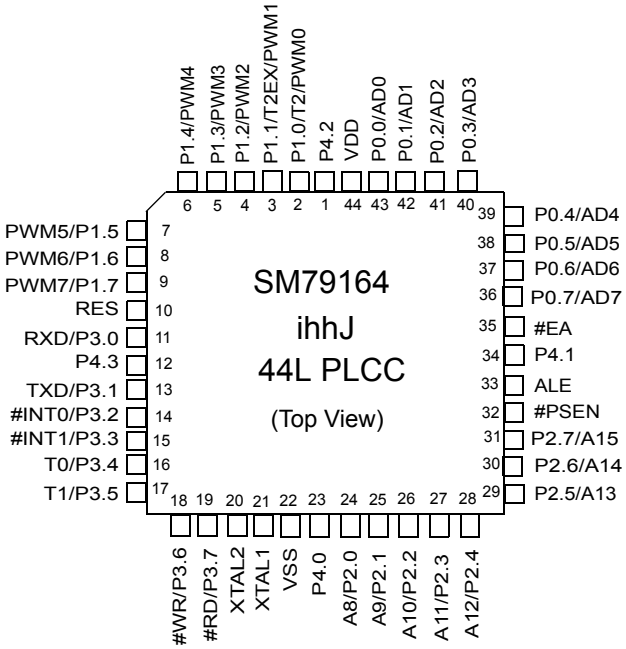
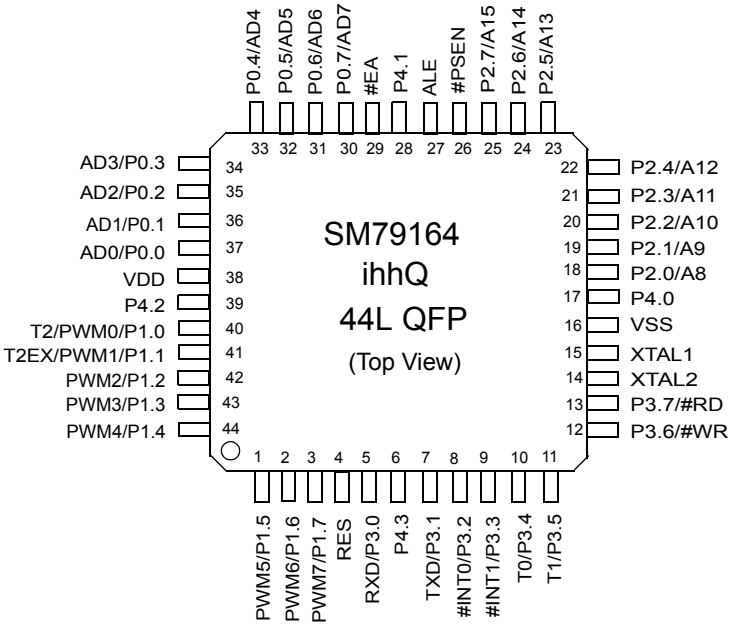
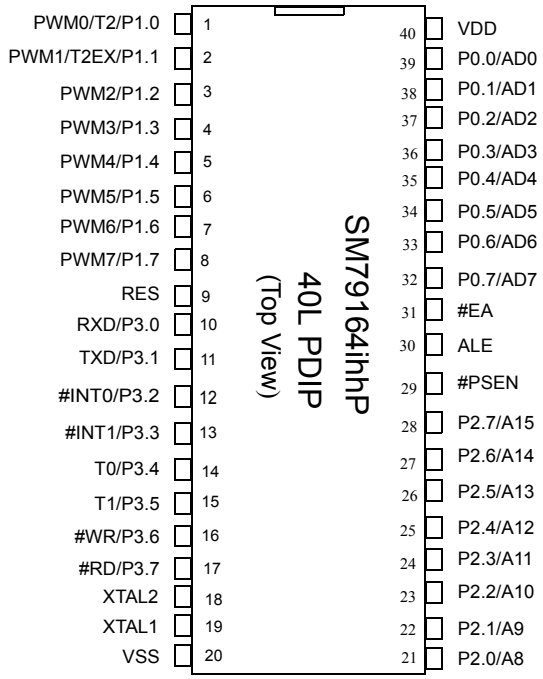
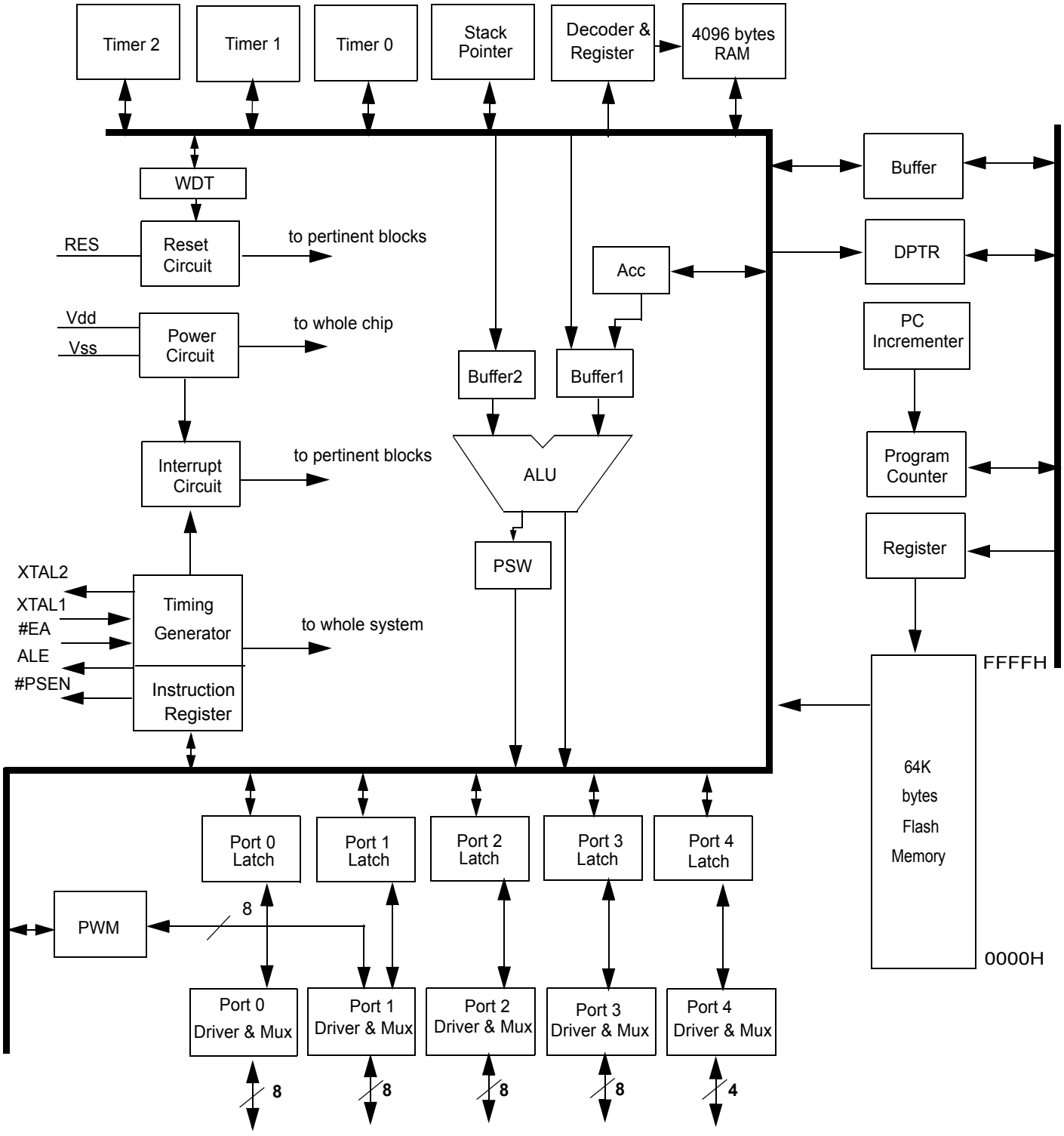
Pin Configurations







Block Diagram



Pin Descriptions

40L PDIP Pin#	44L QFP Pin#	44L PLCC Pin#	Symbol	Active	I/O	Names
1	40	2	P1.0/T2/PWM0		i/o	bit 0 of port 1 & timer 2 clock out , PWM channel 0
2	41	3	P1.1/T2EX/PWM1		i/o	bit 1 of port 1 & timer 2 control , PWM channel 1
3	42	4	P1.2/PWM2		i/o	bit 2 of port 1 & PWM channel 2
4	43	5	P1.3/PWM3		i/o	bit 3 of port 1 & PWM channel 3
5	44	6	P1.4/PWM4		i/o	bit 4 of port 1 & PWM channel 4
6	1	7	P1.5/PWM5		i/o	bit 5 of port 1 & PWM channel 5
7	2	8	P1.6/PWM6		i/o	bit 6 of port 1 & PWM channel 6
8	3	9	P1.7/PWM7		i/o	bit 7 of port 1 & PWM channel 7
9	4	10	RES	H	i	Reset
10	5	11	P3.0/RXD		i/o	bit 0 of port 3 & Receive data
11	7	13	P3.1/TXD		i/o	bit 1 of port 3 & Transmit data
12	8	14	P3.2/#INT0	L/ -	i/o	bit 2 of port 3 & low true interrupt 0
13	9	15	P3.3/#INT1	L/ -	i/o	bit 3 of port 3 & low true interrupt 1
14	10	16	P3.4/T0		i/o	bit 4 of port 3 & Timer 0
15	11	17	P3.5/T1		i/o	bit 5 of port 3 & Timer 1
16	12	18	P3.6/#WR		i/o	bit 6 of port 3 & ext. memory write
17	13	19	P3.7/#RD		i/o	bit 7 of port 3 & ext. mem. read
18	14	20	XTAL2		o	Crystal out
19	15	21	XTAL1		i	Crystal in
20	16	22	VSS			Sink Voltage, Ground
21	18	24	P2.0/A8		i/o	bit 0 of port 2 & bit 8 of ext. memory address
22	19	25	P2.1/A9		i/o	bit 1 of port 2 & bit 9 of ext. memory address
23	20	26	P2.2/A10		i/o	bit 2 of port 2 & bit 10 of ext. memory address
24	21	27	P2.3/A11		i/o	bit 3 of port 2 & bit 11 of ext. memory address
25	22	28	P2.4/A12		i/o	bit 4 of port 2 & bit 12 of ext. memory address
26	23	29	P2.5/A13		i/o	bit 5 of port 2 & bit 13 of ext. memory address
27	24	30	P2.6/A14		i/o	bit 6 of port 2 & bit 14 of ext. memory address
28	25	31	P2.7/A15		i/o	bit 7 of port 2 & bit 15 of ext. memory address
29	26	32	#PSEN		o	program storage enable
30	27	33	ALE		o	address latch enable
31	29	35	#EA	L	i	external access
32	30	36	P0.7/AD7		i/o	bit 7 of port 0 & data/address bit 7 of ext. memory
33	31	37	P0.6/AD6		i/o	bit 6 of port 0 & data/address bit 6 of ext. memory
34	32	38	P0.5/AD5		i/o	bit 5 of port 0 & data/address bit 5 of ext. memory
35	33	39	P0.4/AD4		i/o	bit 4 of port 0 & data/address bit 4 of ext. memory
36	34	40	P0.3/AD3		i/o	bit 3 of port 0 & data/address bit 3 of ext. memory
37	35	41	P0.2/AD2		i/o	bit 2 of port 0 & data/address bit 2 of ext. memory
38	36	42	P0.1/AD1		i/o	bit 1 of port 0 & data/address bit 1 of ext. memory
39	37	43	P0.0/AD0		i/o	bit 0 of port 0 & data/address bit 0 of ext. memory
40	38	44	VDD			Drive Voltage, +5 Vcc
	17	23	P4.0		i/o	bit 0 of Port 4
	28	34	P4.1		i/o	bit 1 of Port 4
	39	1	P4.2		i/o	bit 2 of Port 4
	6	12	P4.3		i/o	bit 3 of Port 4

Special Function Register (SFR)

The address $80 to $FF can be accessed by direct addressing mode only.
Address $80 to $FF is SFR area.
The following table lists the SFRs which are identical to general 8052, as well as SM79164 Extension SFRs.

Special Function Register (SFR) Memory Map

$F8									$FF
$F0	B								$F7
$E8									$EF
$E0	ACC								$E7
$D8	**P4**			**PWMC4**	**PWMC5**	**PWMC6**	**PWMC7**		$DF
$D0	PSW			**PWMC0**	**PWMC1**	**PWMC2**	**PWMC3**		$D7
$C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2			$CF
$C0									$C7
$B8	IP			**PWMD4**	**PWMD5**	**PWMD6**	**PWMD7**	**SCONF**	$BF
$B0	P3			**PWMD0**	**PWMD1**	**PWMD2**	**PWMD3**		$B7
$A8	IE								$AF
$A0	P2								$A7
$98	SCON	SBUF		**P1CON**				**WDTC**	$9F
$90	P1							**WDTKET**	$97
$88	TCON	TMOD	TL0	TL1	TH0	TH1			$8F
$80	P0	SP	DPL	DPH	(Reserved)	**RCON**	**DBANK**	PCON	$87

Note: The text of SFRs with bold type characters are Extension Special Function Registers for SM79164

Addr	SFR	Reset	7	6	5	4	3	2	1	0
85H	**RCON**	00H					RAMS3	RAMS2	RAMS1	RAMS0
86H	**DBANK**	0*000001	BSE		BS5	BS4	BS3	BS2	BS1	BS0
97H	**WDTKEY**	00H	WDTKEY7	WDTKEY6	WDTKEY5	WDTKEY4	WDTKEY3	WDTKEY2	WDTKEY1	WDTKEY0
9BH	**P1CON**	00H	PWME7	PWME6	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
9FH	**WDTC**	0*0**000	WDTE	Reserve	CLEAR			PS2	PS1	PS0
B3H	**PWMD0**	00H	PWMD07	PWMD06	PWMD05	PWMD04	PWMD03	PWMD02	PWMD01	PWMD00
B4H	**PWMD1**	00H	PWMD17	PWMD16	PWMD15	PWMD14	PWMD13	PWMD12	PWMD11	PWMD10
B5H	**PWMD2**	00H	PWMD27	PWMD26	PWMD25	PWMD24	PWMD23	PWMD22	PWMD21	PWMD20
B6H	**PWMD3**	00H	PWMD37	PWMD36	PWMD35	PWMD34	PWMD33	PWMD32	PWMD31	PWMD30
BBH	**PWMD4**	00H	PWMD47	PWMD46	PWMD45	PWMD44	PWMD43	PWMD42	PWMD41	PWMD40
BCH	**PWMD5**	00H	PWMD57	PWMD56	PWMD55	PWMD54	PWMD53	PWMD52	PWMD51	PWMD50
BDH	**PWMD6**	00H	PWMD67	PWMD66	PWMD65	PWMD64	PWMD63	PWMD62	PWMD61	PWMD60
BEH	**PWMD7**	00H	PWMD77	PWMD76	PWMD75	PWMD74	PWMD73	PWMD72	PWMD71	PWMD70

Addr	SFR	Reset	7	6	5	4	3	2	1	0
BFH	**SCONF**	0*****00	WDR						OME	ALEI
C8H	**T2CON**	00H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
C9H	**T2MOD**	******00							T2OE	DCEN
D3H	**PWMC0**	*****000						PBS0	PFS01	PFS00
D4H	**PWMC1**	*****000						PBS1	PFS11	PFS10
D5H	**PWMC2**	*****000						PBS2	PFS21	PFS20
D6H	**PWMC3**	*****000						PBS3	PFS31	PSF30
DBH	**PWMC4**	*****000						PBS4	PFS41	PFS40
DCH	**PWMC5**	*****000						PBS5	PFS51	PFS50
DDH	**PWMC6**	*****000						PBS6	PFS61	PFS60
DEH	**PWMC7**	*****000						PBS7	PFS71	PSF70
D8H	**P4**	****1111					P4.3	P4.2	P4.1	P4.0

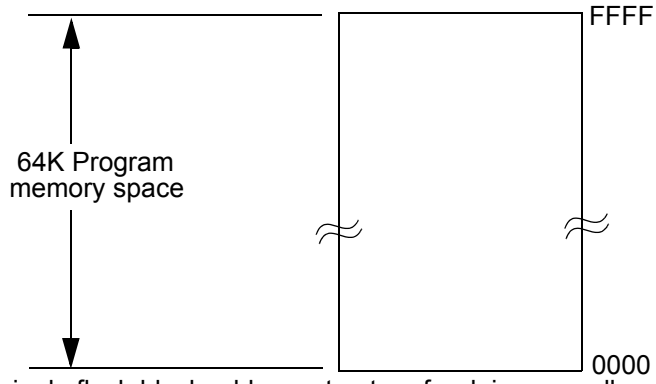
Extension Function Description

1. Memory Structure

The SM79164 is the general 8052 hardware core as a single chip micro controller. Its memory structure follows general 8052 structure.

1.1 Program Memory

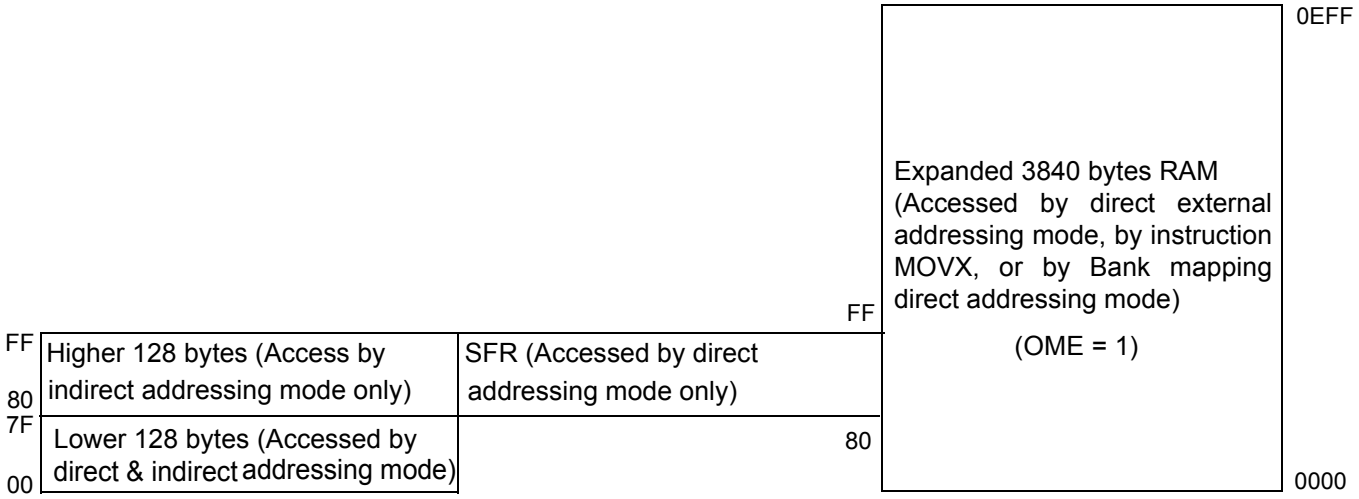
The SM79164 has 64K byte on-chip flash memory which used as general program memory. The address range for the 64K byte is $0000 to $FFFF.



Note: The single flash block address structure for doing as well as program ROM flash.

1.2 Data Memory

The SM79164 has 4K bytes on-chip RAM, 256 bytes of it are the same as general 8052 internal memory structure while the expanded 3840 bytes on-chip RAM can be accessed by external memory addressing method (by instruction MOVX), or by 'Bank mapping direct addressing mode' as described in page 8.



On-chip expanded RAM address structure.

1.2.1 Data Memory - Lower 128 byte ($00 to $7F, Bank 0 & Bank 1)

Data Memory $00 to $FF is the same as 8052.

The address $00 to $7F can be accessed by direct and indirect addressing modes.

Address $00 to $1F is register area.

Address $20 to $2F is memory bit area.

Address $30 to $7F is for general memory area.

1.2.2 Data Memory - Higher 128 byte ($80 to $FF, Bank 2 & Bank 3)

The address $80 to $FF can be accessed by indirect addressing mode or by bank mapping direct addressing mode.

Address $80 to $FF is data area.

1.2.3 Data Memory - Expanded 3840 bytes ($0000 to $0EFF, Bank 4 ~ Bank 63)

From external address $0000 to $0EFF is the on-chip expanded RAM area, total 3840 bytes. This area can be accessed by external direct addressing mode (by instruction MOVX) or by bank mapping direct addressing mode as described below:

1.3 Bank mapping direct addressing mode:

We provide RAM bank address '40H~7FH' as mapping window which allow user access all the 4KB on-chip RAM through this RAM bank address.

That means using direct addressing mode can access all the 4KB on-chip RAM. Please see next page for the mapping mode table.

BS5	BS4	BS3	BS2	BS1	BS0	040h ~ 07fh mapping address	Note
0	0	0	0	0	0	000h ~ 03fh	lower 128 byte RAM
0	0	0	0	0	1	040h ~ 07fh	lower 128 byte RAM
0	0	0	0	1	0	080h ~ 0bfh	higher 128 byte RAM
0	0	0	0	1	1	0c0h ~ 0ffh	higher 128 byte RAM
0	0	0	1	0	0	0000h ~ 003fh	on-chip expanded 3840 byte RAM
0	0	0	1	0	1	0040h ~ 007fh	“
0	0	0	1	1	0	0080h ~ 00bfh	“
0	0	0	1	1	1	00c0h ~ 00ffh	“
0	0	1	0	0	0	0100h ~ 013fh	“
0	0	1	0	0	1	0140h ~ 017fh	“
0	0	1	0	1	0	0180h ~ 01bfh	“
0	0	1	0	1	1	01c0h ~ 01ffh	“
0	0	1	1	0	0	0200h ~ 023fh	“
0	0	1	1	0	1	0240h ~ 027fh	“
0	0	1	1	1	0	0280h ~ 02bfh	“
0	0	1	1	1	1	02c0h ~ 02ffh	“
0	1	0	0	0	0	0300h ~ 033fh	“
0	1	0	0	0	1	0340h ~ 037fh	“
0	1	0	0	1	0	0380h ~ 03bfh	“
0	1	0	0	1	1	03c0h ~ 03ffh	“
0	1	0	1	0	0	0400h ~ 043fh	“
0	1	0	1	0	1	0440h ~ 047fh	“
0	1	0	1	1	0	0480h ~ 04bfh	“
0	1	0	1	1	1	04c0h~04ffh	“
≈	≈	≈	≈	≈	≈	≈	≈ ≈
1	1	1	0	0	1	0d40h ~ 0d7fh	“
1	1	1	0	1	0	0d80h ~ 0dbfh	“
1	1	1	0	1	1	0dc0h ~ 0dffh	“
1	1	1	1	0	0	0e00h ~ 0e3fh	“
1	1	1	1	0	1	0e40h ~ 0e7fh	“
1	1	1	1	1	0	0e80h ~ 0ebfh	“
1	1	1	1	1	1	0ec0h ~ 0effh	“

With this bank mapping scheme, user can access entire 4k byte on-chip RAM with direct addressing method. That means using the window area ($040~$07F), user can access any bank (64 byte) data of 4k byte on-chip RAM space which is selected by BS[5:0] of data bank control register (DBANK, $86).

For example, user write #30h to $101 address:

```
MOV   DBANK, #88H        ; set bank mapping $040~$07f to $0100~$013f
MOV   A, #30H            ; store #30H to A
MOV   41H, A             ; write #30H to $0101 address
```

Data Bank Control Register (DBANK, $86)

	bit-7							bit-0
	BSE	Unused	BS5	BS4	BS3	BS2	BS1	BS0
Read / Write:	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	*	0	0	0	0	0	1

Data bank select enable bit BSE = 1 enables the data bank select function

Data bank select enable bit BSE = 0 disables the data bank select function

BS[5:0] setting will map $040~$07F RAM space to entire 4k byte on-chip RAM space.

Internal RAM Control Register (RCON, $85)

	bit-7							bit-0
	Unused	Unused	Unused	Unused	RAMS3	RAMS2	RAMS1	RAMS0
Read / Write:	-	-	-	-	R/W	R/W	R/W	R/W
Reset value:	*	*	*	*	0	0	0	0

SM79164 has 3840 byte on-chip RAM which can be accessed by external memory addressing method only. (By instruction MOVX). The address space of instruction MOVX @Rn is determined by bit 3, bit2, bit1, bit 0 (RAMS3, RAMS2, RAMS1, RAMS0) of RCON. The default setting of RAMS3, RAMS2, RAMS1, RAMS0 bits is 0000 (page0).

RAMS3	RAMS2	RAMS1	RAMS0	MOVX @Ri i=0,1 mapping to expended RAM address
0	0	0	0	$0000 ~ $00FF
0	0	0	1	$0100 ~ $01FF
0	0	1	0	$0200 ~ $02FF
0	0	1	1	$0300 ~ $03FF
0	1	0	0	$0400 ~ $04FF
0	1	0	1	$0500 ~ $05FF
0	1	1	0	$0600 ~ $06FF
0	1	1	1	$0700 ~ $07FF
1	0	0	0	$0800 ~ $08FF
1	0	0	1	$0900 ~ $09FF
1	0	1	0	$0A00 ~ $0AFF
1	0	1	1	$0B00 ~ $0BFF
1	1	0	0	$0C00 ~ $0CFF
1	1	0	1	$0D00 ~ $0DFF
1	1	1	0	$0E00 ~ $0EFF

The port 0, port2, port3.6 and port3.7 can be used as general purpose I/O pin while port0 is open-drain structure.

System Control Register (SCONF, $BF)

	bit-7							bit-0
	WDR	Unused	Unused	Unused	Unused	Unused	OME	ALEI
Read / Write:	R/W	-	-	-	-	-	R/W	R/W
Reset value:	0	*	*	*	*	*	0	0

WDR : Watch Dog Timer Reset.
OME : 3840 bytes on-chip RAM enable bit
ALEI : ALE output inhibit bit, to reduce EMI

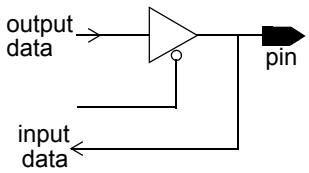
Setting bit 0 (ALEI) of SCONF can inhibit the clock signal in Fosc/6Hz output to the ALE pin.

The bit 1 (OME) of SCONF can enable or disable the on-chip expanded 3840 byte RAM. The default setting of OME bit is 0 (disable).

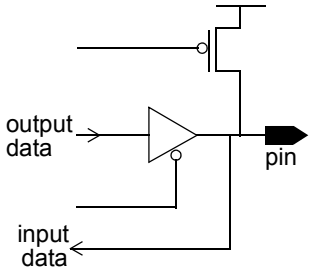
The bit 7 (WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever un-predicted reset happened.

1.4 I/O Pin Configuration

The ports 1, 2 and 3 of standard 8051 have internal pull-up resistor, and port 0 has open-drain outputs. Each I/O pin can be used independently as an input or an output. For I/O ports to be used as an input pin, the port bit latch must contain a '1' which turns off the output driver FET. Then for port 1, 2 and 3 port pin is pulled high by a weak internal pull-up, and can be pulled low by an external source. The port 0 has open-drain outputs which means its pull-ups are not active during normal port operation. Writing '1' to the port 0 bit latch will causing bit floating so that it can be used as a high-impedance input.
The port 4 used as GPIO will has the same function as port 1, 2 and 3.



port 0
standard 8051



port 1, 2 and 3
standard 8051

2. Port 4 for PLCC or QFP package:

The bit addressable port 4 is available with PLCC or QFP package. The port 4 has only 4 pins and its port address is located at 0D8H. The function of port 4 is the same as the function of port 1, port 2 and port 3.

Port4 (P4, $D8)

	bit-7							bit-0
	Unused	Unused	Unused	Unused	P4.3	P4.2	P4.1	P4.0
Read / Write:	-	-	-	-	R/W	R/W	R/W	R/W
Reset value:	*	*	*	*	1	1	1	1

The bit 3, bit 2, bit 1, bit 0 output the setting to pin P4.3, P4.2, P4.1, P4.0 respectively.

3. Watch Dog Timer

The Watch Dog Timer (WDT) is a 16-bit free-running counter that generate reset signal if the counter overflows. The WDT is useful for systems which are susceptible to noise, power glitches, or electronics discharge which causing software dead loop or runaway. The WDT function can help user software recover from abnormal software condition. The WDT is different from Timer0, Timer1 and Timer2 of general 8052. To prevent a WDT reset can be done by software periodically clearing the WDT counter. User should check WDR bit of SCONF register whenever un-predicted reset happened.
The purpose of the secure procedure is to prevent the WDTC value from being changed when system runaway.
There is a 250KHz RC oscillator embedded in chip. Set WDTE = "1" will enable the RC oscillator and the frequency is independent to the system frequency.
To enable the WDT is done by setting 1 to the bit 7 (WDTE) of WDTC. After WDTE set to 1, the 16-bit counter starts to count with the RC oscillator. It will generate a reset signal when overflows. The WDTE bit will be cleared to 0 automatically when SM79164 been reset, either hardware reset or WDT reset.
To reset the WDT is done by setting 1 to the CLEAR bit of WDTC before the counter overflow. This will clear the content of the 16-bit counter and let the counter re-start to count from the beginning.

3.1 Watch Dog Timer Registers:

Watch Dog Timer Registers - WDT Control Register (WDTC, $9F)

	bit-7							bit-0
	WDTE	Reserve	CLEAR	Unused	Unused	PS2	PS1	PS0
Read / Write:	R/W	-	R/W	-	-	R/W	R/W	R/W
Reset value:	0	*	0	*	*	0	0	0

WDTE : Watch Dog Timer enable bit
CLEAR : Watch Dog Timer reset bit
PS[2:0] : Overflow period select bits

PS [2:0]	Overflow Period (ms)
000	2.048
001	4.096
010	8.192
011	16.384
100	32.768
101	65.536
110	131.072
111	262.144

Watch Dog Key Register - (WDTKEY, $97H)

	bit-7							bit-0
	WDT KEY7	WDT KEY6	WDT KEY5	WDT KEY4	WDT KEY3	WDT KEY2	WDT KEY1	WDT KEY0
Read / Write:	W	W	W	W	W	W	W	W
Reset value:	0	0	0	0	0	0	0	0

By default, the WDTC is read only. User need to write values 1EH, E1H sequentially to the WDTKEY($97H) register to enable the WDTC write attribute, That is

```
MOV WDTKEY, # 1EH
MOV WDTKEY, # E1H
```

When WDTC is set, user need to write another values E1H, 1EH sequentially to the WDTKEY($97H) register to disable the WDTC write attribute, That is

```
MOV WDTKEY, # E1H
MOV WDTKEY, # 1EH
```

Watch Dog Timer Register - System Control Register (SCONF, $BF)

	bit-7							bit-0
	WDR	Unused	Unused	Unused	Unused	Unused	OME	ALEI
Read / Write:	R/W	-	-	-	-	-	R/W	R/W
Reset value:	0	*	*	*	*	*	0	0

The bit 7 (WDR) of SCONF is Watch Dog TImer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever un-predicted reset happened

4. Reduce EMI Function

The SM79164 allows user to reduce the EMI emission by setting 1 to the bit 0 (ALEI) of SCONF register. This function will inhibit the clock signal in Fosc/6Hz output to the ALE pin.

5. Pulse Width Modulation (PWM)

The Pulse Width Modulation (PWM) module contains 1 kind of PWM sub module: PWM. PWM also has four 8-bit channels.

5.1 PWM Function Description:

Each PWM channel contains a 8-bit wide PWM data register (PWMDR) to decide number of continuous pulses within a PWM frame cycle. The value programmed in the register will determine the pulse length of the output. The PWM channel can be configured as 5-bit or 8-bit resolution. If a channel is configured as 5-bit resolution, only LSB 5 bits are available. The value of each PWM Data Register (PWMDR) is continuously compared with the content of an internal counter to determine the state of each PWM channel output pin.

5.2 PWM Registers - P1CON[7:0], PWMC[7:0], PWMD[7:0]

PWM Registers - Port1 Configuration Register (P1CON, $9B)

	PWME7	PWME6	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
Read / Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	0	0	0	0	0	0	0

PWM[7:0]E: When the bit set to one, the corresponding PWM pin is active as PWM function. When the bit reset to zero, the corresponding PWM pin is active as I/O pin. Five bits are cleared upon reset.

PWM Registers - PWM Control Register (PWMC[7:0], $DE ~ $DB, $D6 ~ $D3)

	bit-7							bit-0
	Unused	Unused	Unused	Unused	Unused	PBS[7:0]	PFS[7:0]1	PFS[7:0]0
Read / Write:	-	-	-	-	-	R/W	R/W	R/W
Reset value:	*	*	*	*	*	0	0	0

PFS[7:0][1:0] : These two bits is 2's power parameter to form a frequency divider for input clock.

PBS[7:0] : This bit decides channel bit resolution. If PBS[7:0] is set, the channel is 5-bit resolution.

PFS[7:0]1	PFS[7:0]0	Divider	PWM clock, Fosc=12MHz	PWM clock, Fosc=24MHz
0	0	0.5	24MHz (note)	48MHz (note)
0	1	1	12MHz	24MHz
1	0	2	6MHz	12MHz
1	1	4	3KHz	6MHz

note : If X'tal > 24MHz, can not select PFS[1:0] = 00

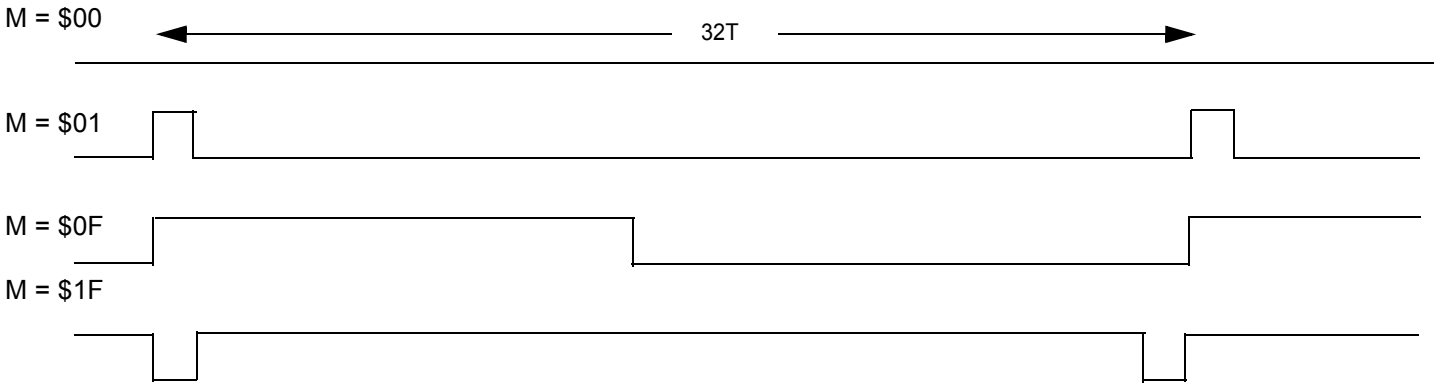
PWM Registers - PWM Data Register (PWMD[7:0], $BE ~ $BB, $B6 ~ $B3)

	bit-7							bit-0
	PWMD [7:0]7	PWMD [7:0]6	PWMD [7:0]5	PWMD [7:0]4	PWMD [7:0]3	PWMD [7:0]2	PWMD [7:0]1	PWMD [7:0]0
Read / Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	0	0	0	0	0	0	0

PWM[7:0][7:0] : content of PWM Data Register. If PBS[7:0] is set, only PWM[7:0][4:0] are available.]

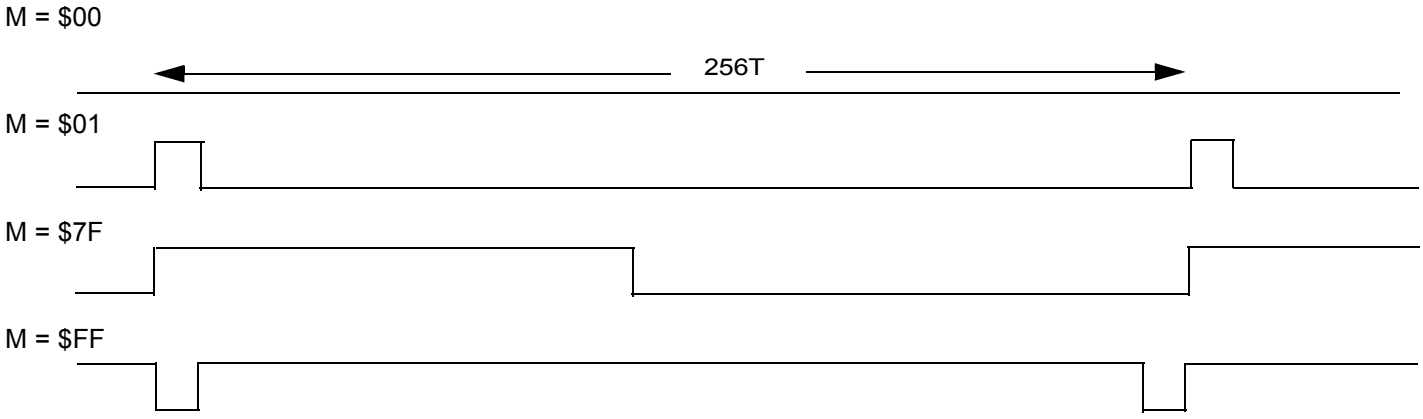
Example of PWM timing diagram:

For 5-bit resolution channel, M = content of PWMD[7:0]:



PWM Clock Frequency = 1/T = Fosc / Divider
The PWM output cycle frame frequency = PWM Clock frequency / 32

For 8-bit resolution channel:



PWM Clock Frequency = 1/T = Fosc / Divider
The PWM output cycle frame frequency = PWM Clock frequency / 256

Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Operating temperature	-40	25	85	°C	Ambient temperature under bias
TS	Storage temperature	-55	25	155	°C	
VCC	Supply voltage	2.4	-	5.5	V	Note1
Fosc35	Oscillator Frequency	3.0	-	35	MHz	Note2

Note1:Operating Voltage {V=2.4V ~ 3.0V, L=3.0V ~ 3.6V, C=4.5V ~ 5.5V}
Note2:Working Frequency {V=16MHZ for J/Q package,L=20MHZ for P package,L=25MHZ for J/Q package,C=25MHZ for P package,C=35MHZ for J/Q package}

DC Characteristics

(TA = -40 degree C to 85 degree C, Vcc = 2.4V to 5.5V)

Symbol	Parameter	Valid	Min.	Max.	Unit	Test Conditions
VIL1	Input Low Voltage	port 0,1,2,3,4,#EA	-0.5	0.8	V	
VIL2	Input Low Voltage	RES, XTAL1	0	0.8	V	
VIH1	Input High Voltage	port 0,1,2,3,4,#EA	2.0	Vcc+0.5	V	
VIH2	Input High Voltage	RES, XTAL1	70%Vcc	Vcc+0.5	V	
VOL1	Output Low Voltage	port 0, ALE, #PSEN		0.45	V	IOL=3.2mA
VOL2	Output Low Voltage	port 1,2,3,4		0.45	V	IOL=1.6mA
VOH1	Output High Voltage	port 0	2.4		V	IOH=-800uA (only for VCC=5V)
			90%Vcc		V	IOH=-80uA
VOH2	Output High Voltage	port 1,2,3,4,ALE,#PSEN	2.4		V	IOH=-60uA (only for VCC=5V)
			90%Vcc		V	IOH=-10uA
IIL	Logical 0 Input Current	port 1,2,3,4		-75	uA	Vin=0.45V
ITL	Logical Transition Current	port 1,2,3,4		-650	uA	Vin=2.0V
ILI	Input Leakage Current	port 0, #EA		±10	uA	0.45V<Vin<Vcc
R RES	Reset Pulldown Resistance	RES	50	300	Kohm	
C IO	Pin Capacitance			10	pF	Freq=1MHz, Ta=25°C
I CC	Power Supply Current	Vdd		20	mA	Active mode, 16MHz
				6.5	mA	Idle mode, 16MHz
				50	uA	Power down mode

Note1: Under steady state (non-transient) conditions, IOL must be externally
Limited as follows: Maximum IOL per port pin : 10mA
Maximum IOL per 8-bit port : port 0 :26mA
port 1,2,3 :15mA
Maximum total IOL for all output pins : 71mA
If IOL exceeds the condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

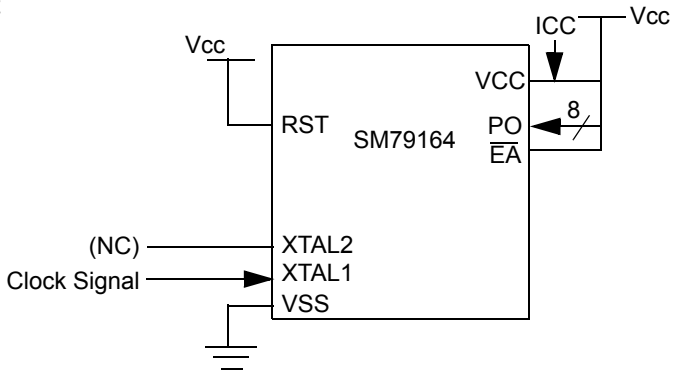
Note2 : Minimum VCC for Power-down is 2V.

AC Characteristics

(20/25MHz, operating conditions; CL for Port 0, ALE and PSEN Outputs=100pF; CL for all Other Output=80pF)

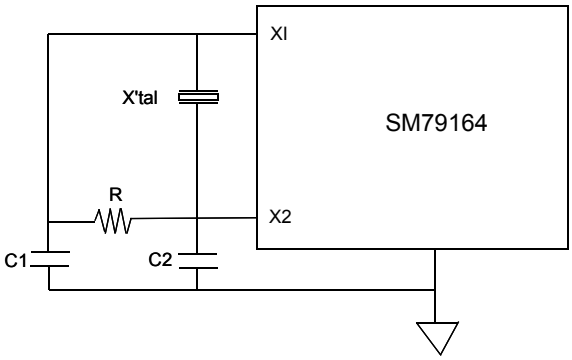
Symbol	Parameter	Valid Cycle	fosc=16MHz			Variable fosc			Unit	Remarks
			Min.	Typ.	Max	Min.	Typ.	Max		
T LHLL	ALE pulse width	RD/WRT	115			2xT - 10			nS	
T AVLL	Address Valid to ALE low	RD/WRT	43			T - 20			nS	
T LLAX	Address Hold after ALE low	RD/WRT	53			T - 10			nS	
T LLIV	ALE low to Valid Instruction In	RD			240			4xT - 10	nS	
T LLPL	ALE low to #PSEN low	RD	53			T - 10			nS	
T PLPH	#PSEN pulse width	RD	173			3xT - 15			nS	
T PLIV	#PSEN low to Valid Instruction In	RD			177			3xT - 10	nS	
T PXIX	Instruction Hold after #PSEN	RD	0			0			nS	
T PXIZ	Instruction Float after #PSEN	RD			87			T + 25	nS	
T AVIV	Address to Valid Instruction In	RD			292			5xT - 20	nS	
T PLAZ	#PSEN low to Address Float	RD			10			10	nS	
T RLRH	#RD pulse width	RD	365			6xT - 10			nS	
T WLWH	#WR pulse width	WRT	365			6xT - 10			nS	
T RLDV	#RD low to Valid Data In	RD			302			5xT - 10	nS	
T RHDX	Data Hold after #RD	RD	0			0			nS	
T RHDZ	Data Float after #RD	RD			145			2xT + 20	nS	
T LLDV	ALE low to Valid Data In	RD			590			8xT - 10	nS	
T AVDV	Address to Valid Data In	RD			542			9xT - 20	nS	
T LLYL	ALE low to #WR High or #RD low	RD/WRT	178		197	3xT - 10		3xT + 10	nS	
T AVYL	Address Valid to #WR or #RD low	RD/WRT	230			4xT - 20			nS	
T QVWH	Data Valid to #WR High	WRT	403			7xT - 35			nS	
T QVWX	Data Valid to #WR transition	WRT	38			T - 25			nS	
T WHQX	Data hold after #WR	WRT	73			T + 10			nS	
T RLAZ	#RD low to Address Float	RD						5	nS	
T YALH	#WR or #RD high to ALE high	RD/WRT	53		72	T -10		T + 10	nS	
T CHCL	clock fall time								nS	
T CLCX	clock low time								nS	
T CLCH	clock rise time								nS	
T CHCX	clock high time								nS	
T, TCLCL	clock period			63			1/fosc		nS	

ICC Active mode test circuit



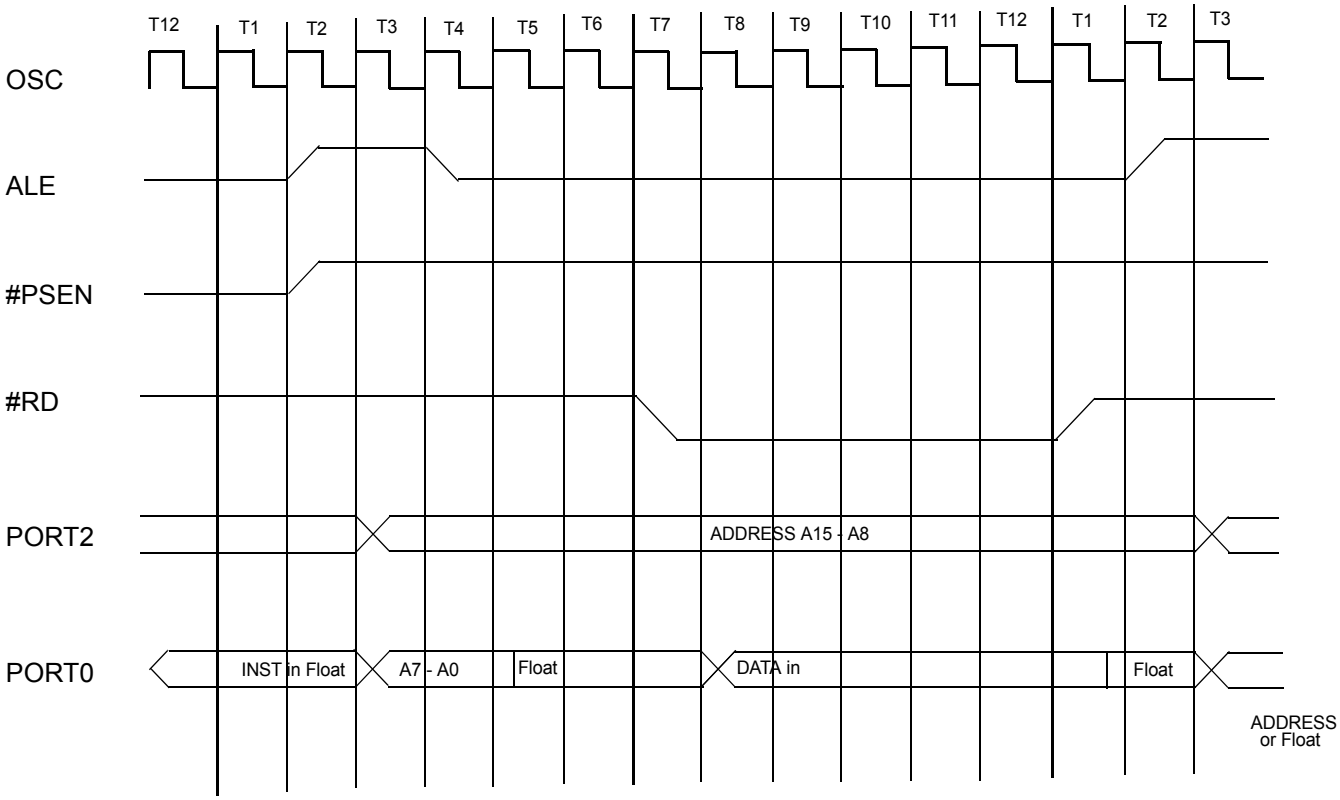
Application Reference

Valid for SM79164				
X'tal	3MHz	6MHz	9MHz	12MHz
C1	30 pF	30 pF	30 pF	30 pF
C2	30 pF	30 pF	30 pF	30 pF
R	open	open	open	open
X'tal	16MHz	25MHz	33MHz	
C1	30 pF	15 pF	5 pF	
C2	30 pF	15 pF	5 pF	
R	open	62KΩ	6.8KΩ	

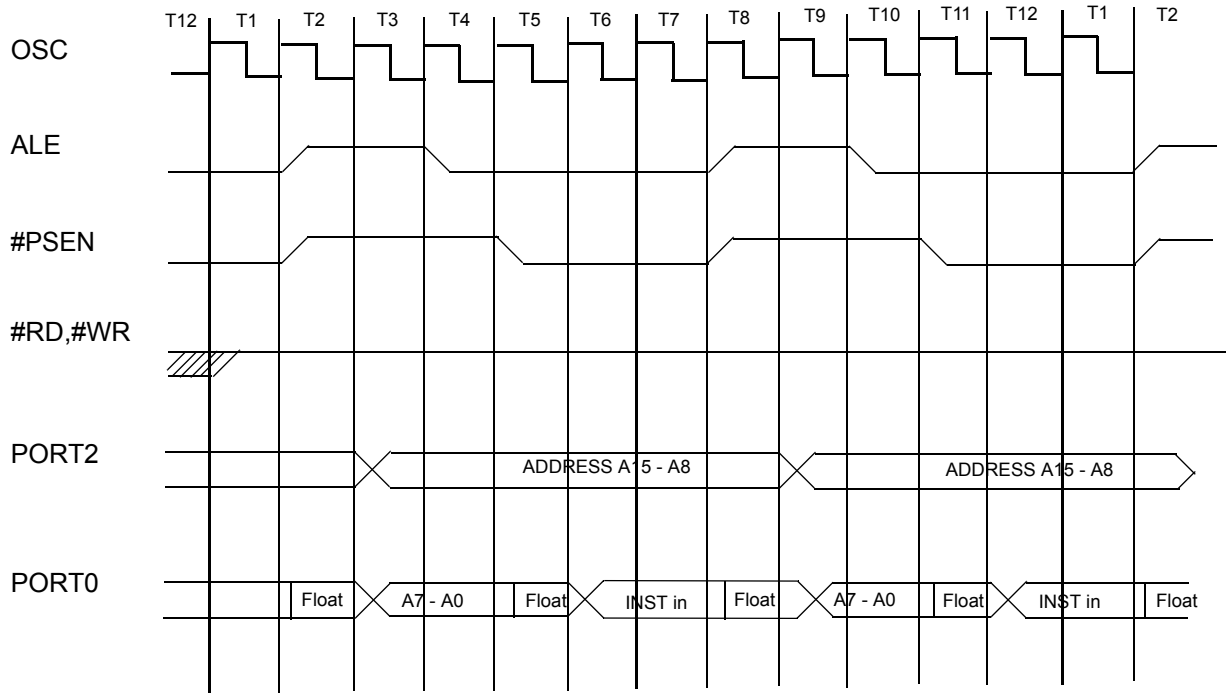


NOTE: Oscillation circuit may differs with different crystal or ceramic resonator in higher oscillation frequency which was due to each crystal or ceramic resonator has its own characteristics. User should check with the crystal or ceramic resonator manufacturer for appropriate value of external components.

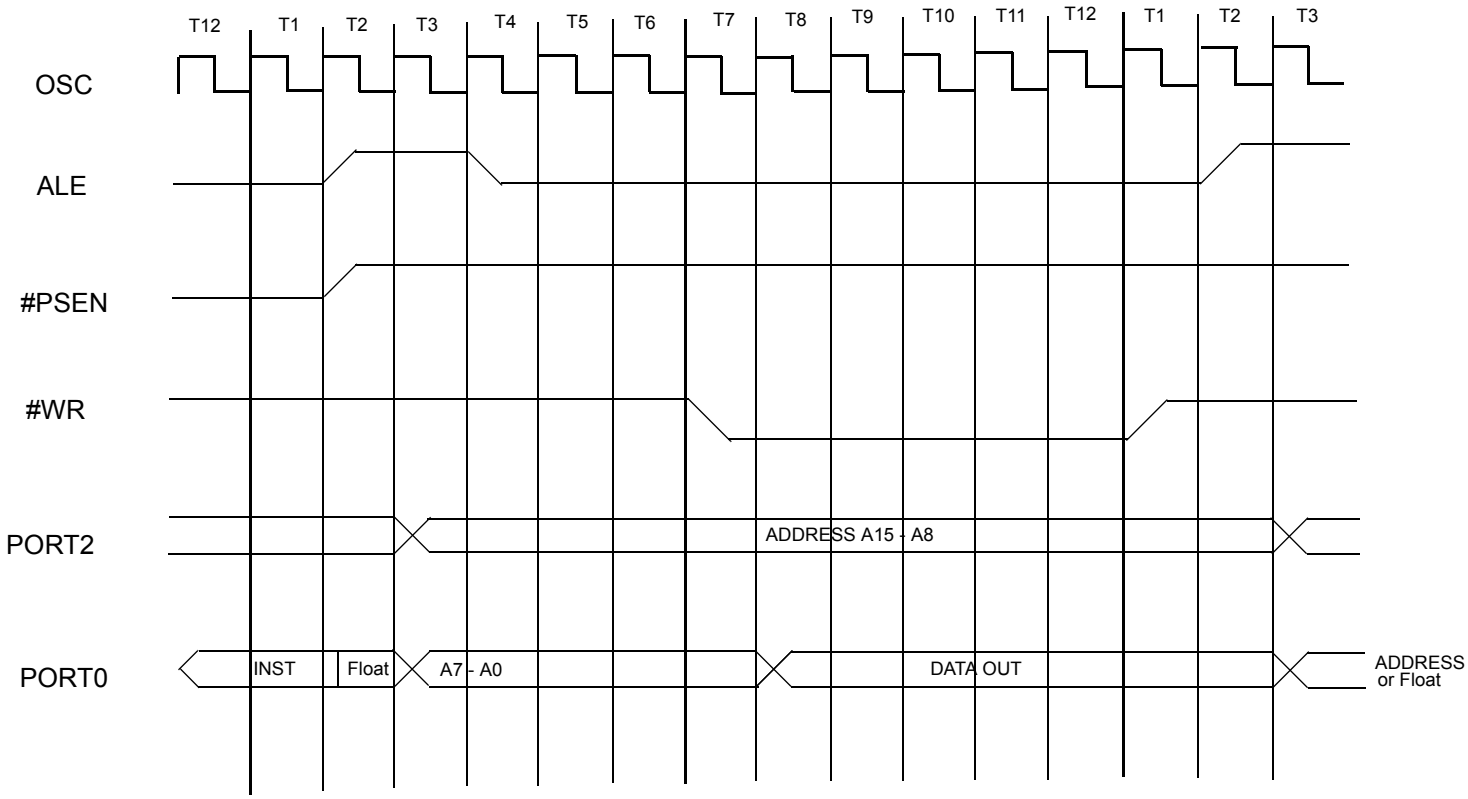
Data Memory Read Cycle Timing



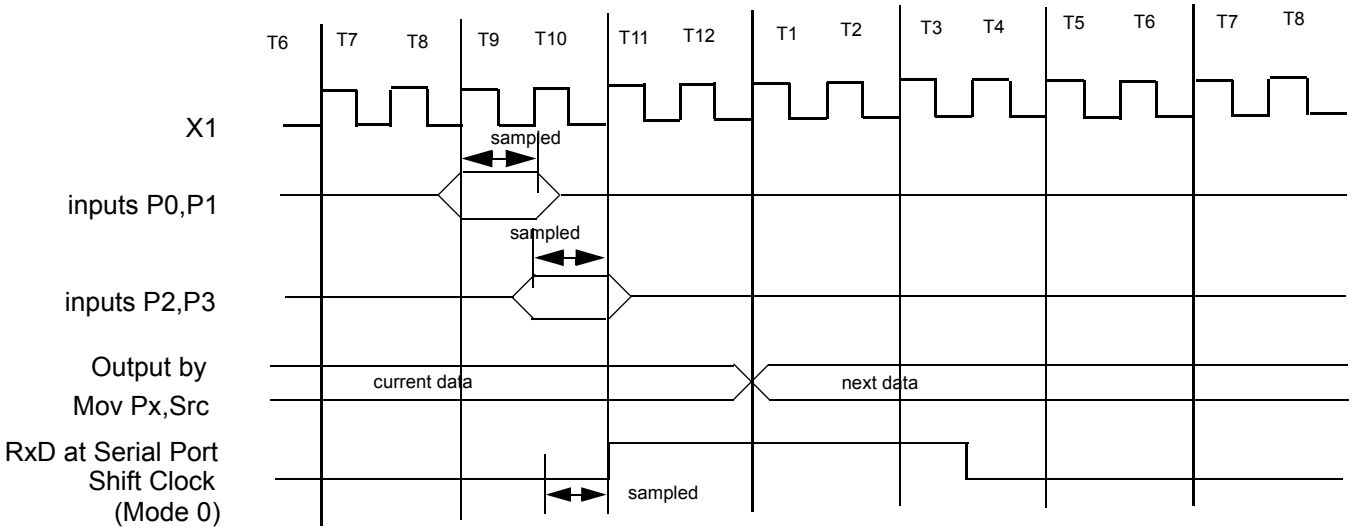
Program Memory Read Cycle Timing



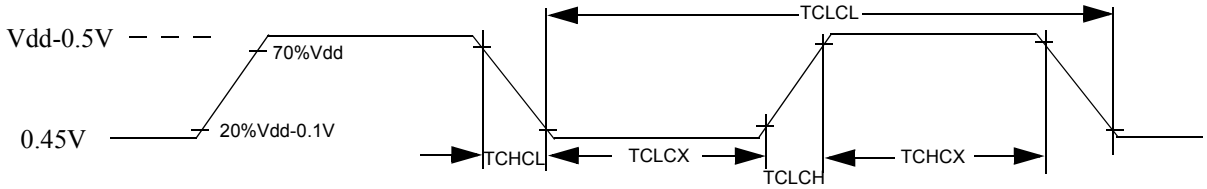
Data Memory Write Cycle Timing



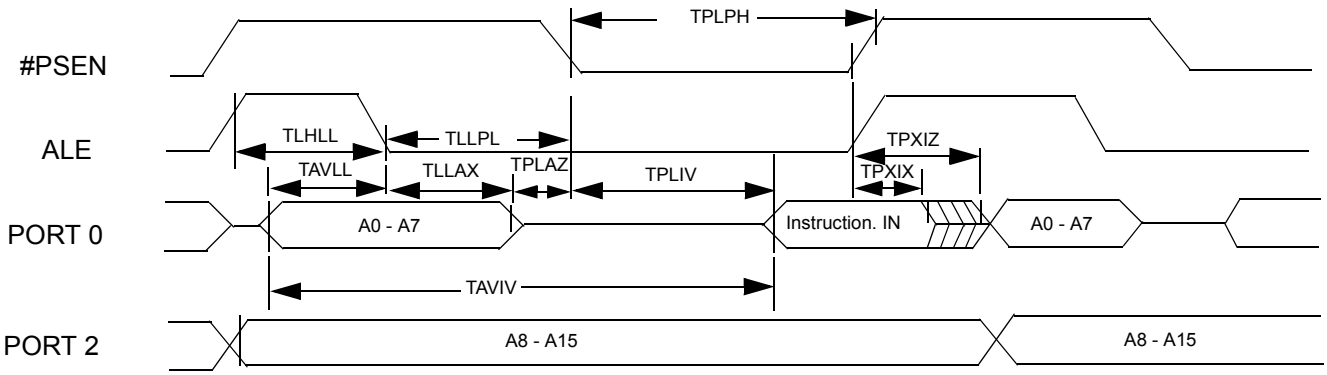
I/O Ports Timing



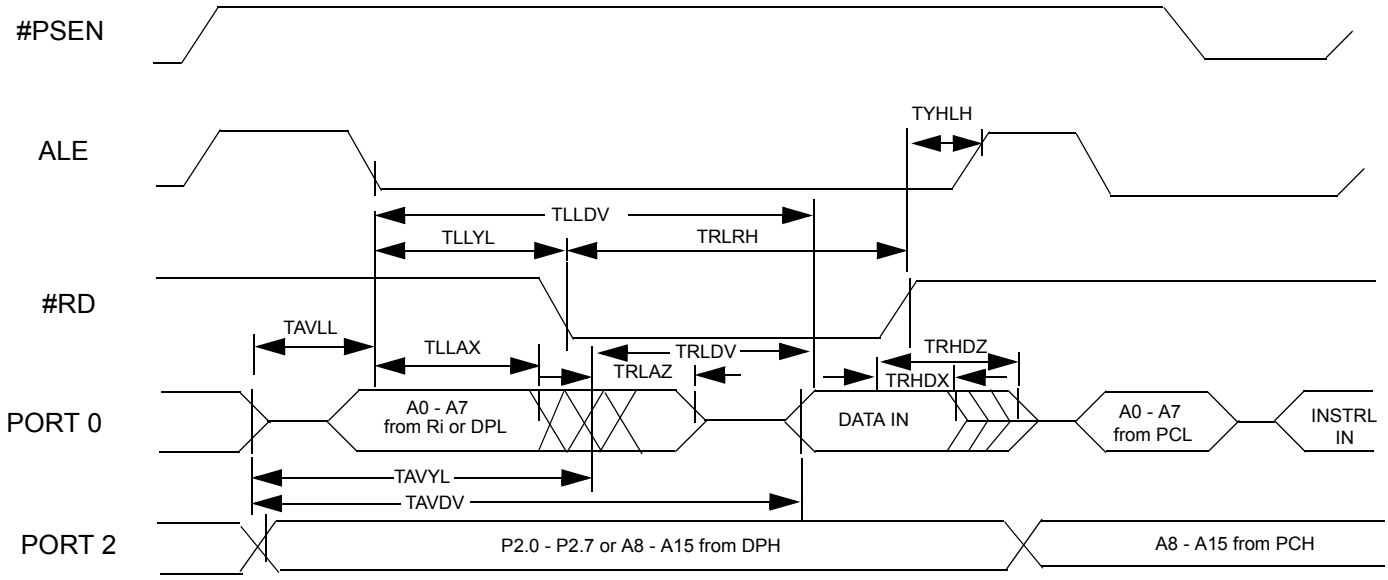
Timing Critical, Requirement of External Clock (Vss=0.0V is assumed)



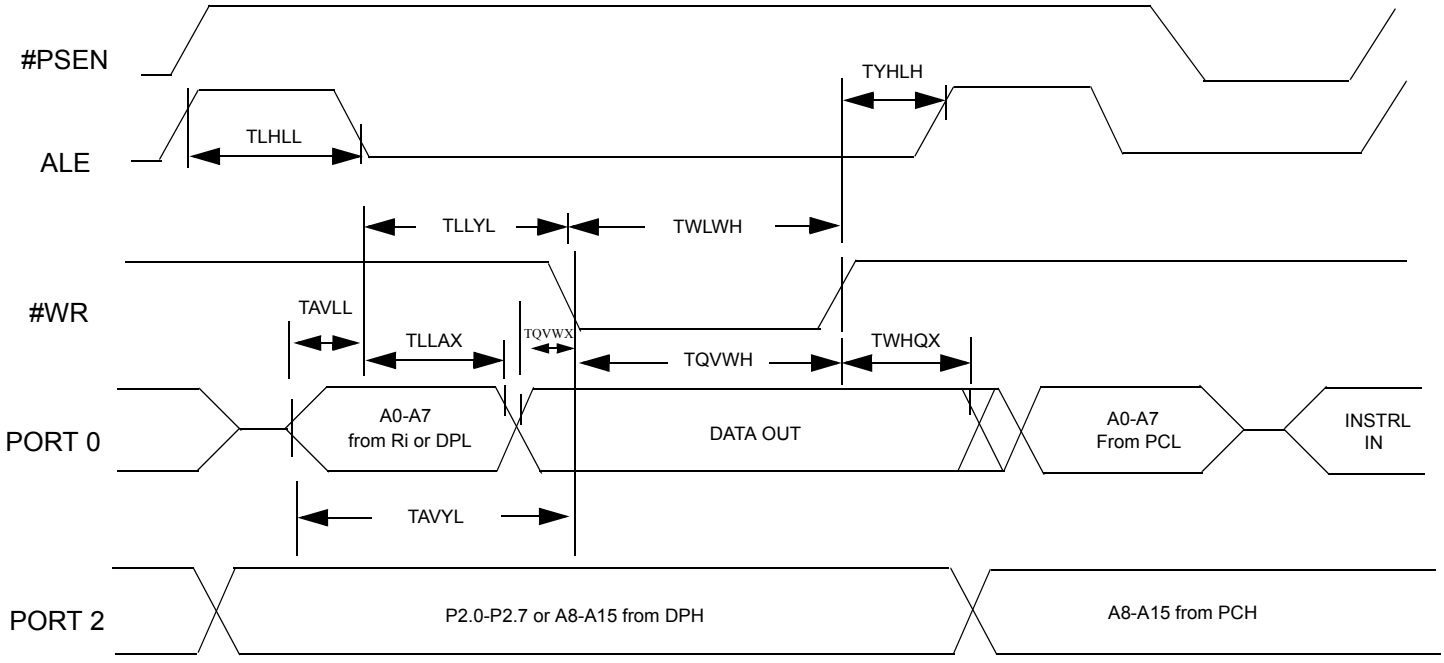
Tm.I External Program Memory Read Cycle



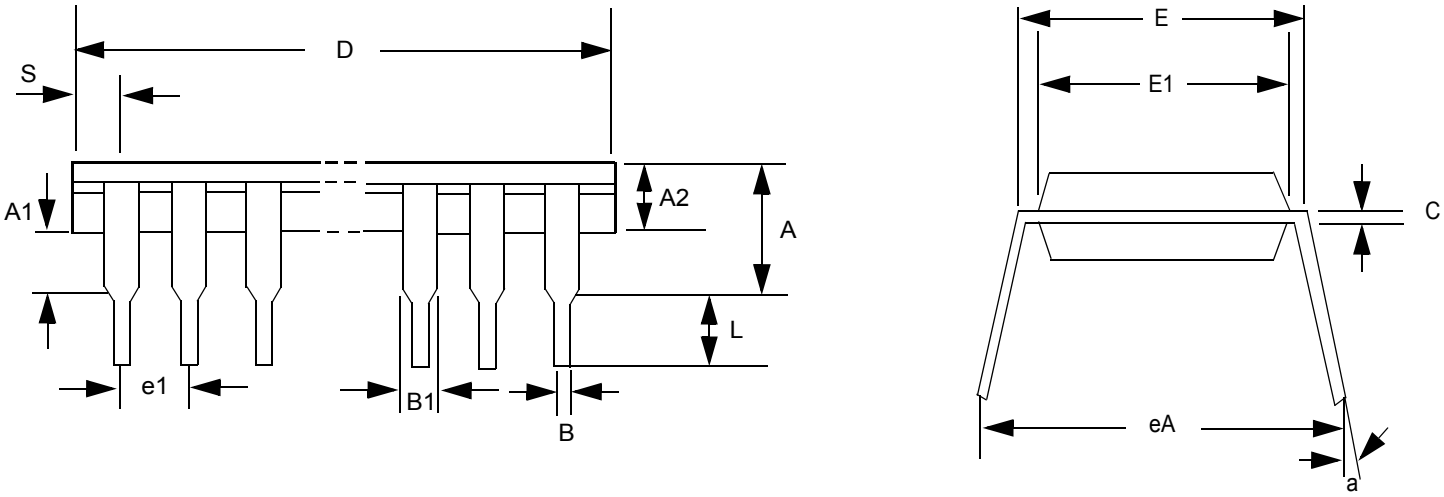
Tm.II External Data Memory Read Cycle



Tm.III External Data Memory Write Cycle



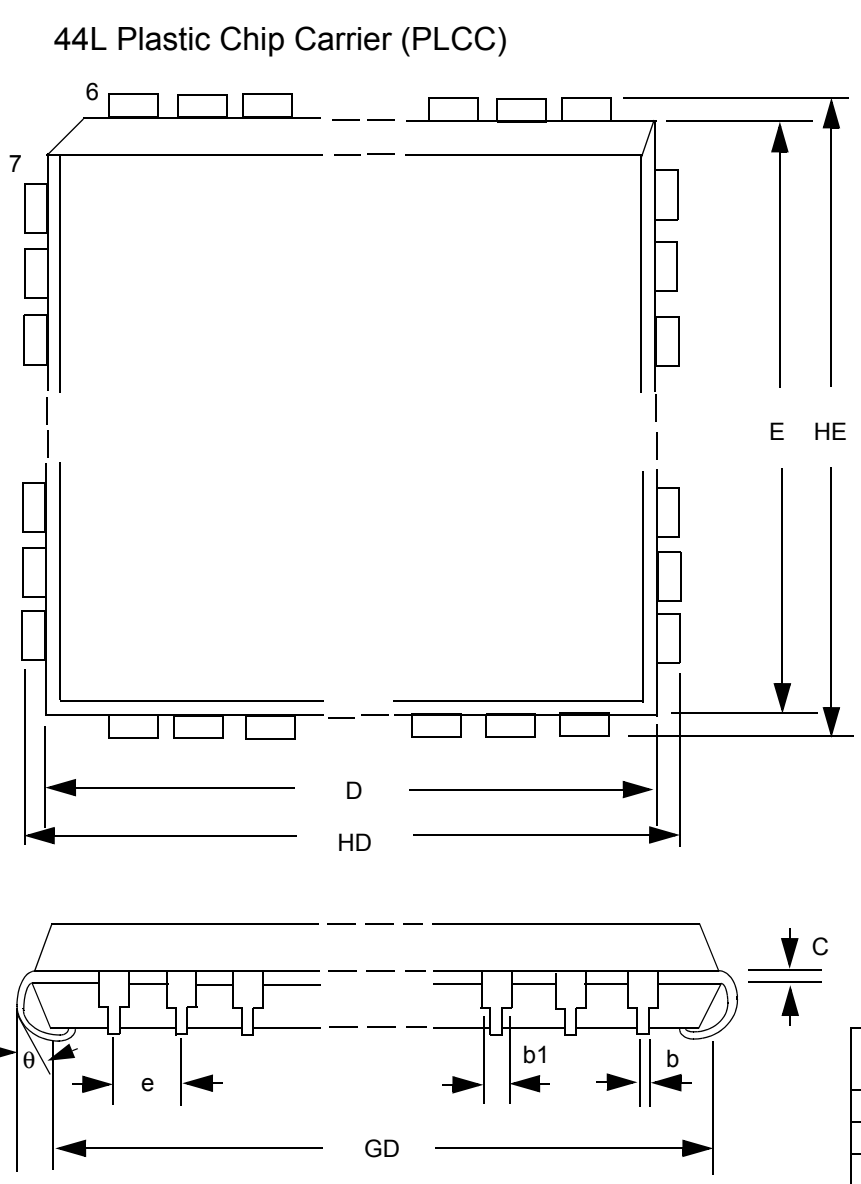
40L 600mil PDIP Information

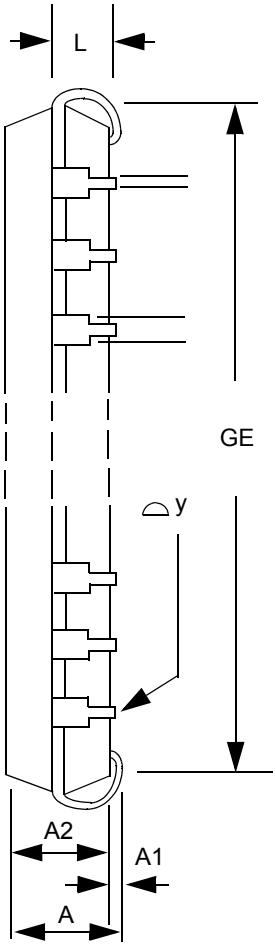


Note:
1. Dimension D Max & include mold flash or tie bar burrs.
2. Dimension E1 does not include inter lead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dampers protrusion/ infusion.
5. Controlling dimension is inch.
6. General appearance spec. should base on final visual inspection spec.

Symbol	Dimension in inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.210	- / 5.33
A1	0.010 / -	0.25 / -
A2	0.150 / 0.160	3.81 / 4.06
B	0.016 / 0.022	0.41 / 0.56
B1	0.048 / 0.054	1.22 / 1.37
C	0.008 / 0.014	0.20 / 0.36
D	- / 2.070	- / 52.58
E	0.590 / 0.610	14.99 / 15.49
E1	0.540 / 0.552	13.72 / 14.02
e1	0.090 / 0.110	2.29 / 2.79
L	0.120 / 0.140	3.05 / 3.56
a	0˚/ 15˚	0˚/ 15˚
eA	0.630 / 0.670	16.00 / 17.02
S	- / 0.090	- / 2.29

44L Plastic Chip Carrier (PLCC)

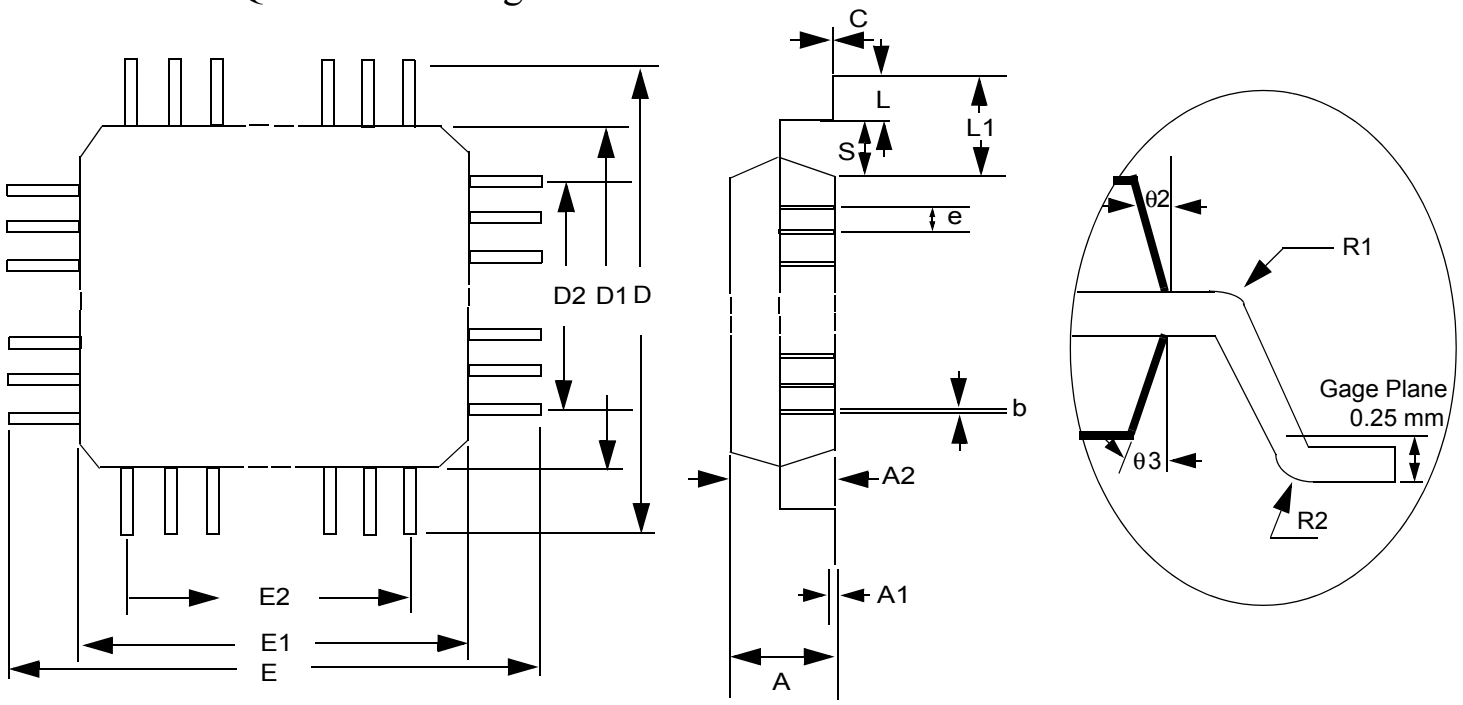


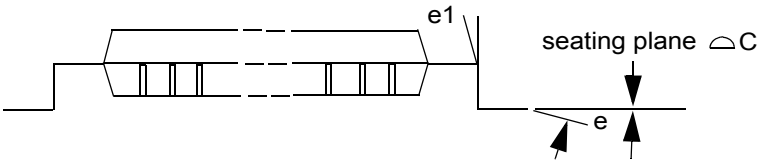


Symbol	Dimension in inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.185	- / 4.70
A1	0.020 / -	0.51 / -
A2	0.145 / 0.155	3.68 / 3.94
b1	0.026 / 0.032	0.66 / 0.81
b	0.016 / 0.022	0.41 / 0.56
C	0.008 / 0.014	0.20 / 0.36
D	0.648 / 0.658	16.46 / 16.71
E	0.648 / 0.658	16.46 / 16.71
e	0.050 BSC	1.27 BSC
GD	0.590 / 0.630	14.99 / 16.00
GE	0.590 / 0.630	14.99 / 16.00
HD	0.680 / 0.700	17.27 / 17.78
HE	0.680 / 0.700	17.27 / 17.78
L	0.090 / 0.110	2.29 / 2.79
θ	- / 0.004	- / 0.10
⌓ y	/	/

Note:
1. Dimension D & E does not include inter lead flash.
2. Dimension b1 does not include dam bar protrusion/ intrusion.
3. Controlling dimension: Inch
4. General appearance spec. should base on final visual inspection spec.

44L Plastic Quad Flat Package





Note:
Dimension D1 and E1 do not include mold protrusion.
Allowance protrusion is 0.25mm per side.
Dimension D1 and E1 do include mold mismatch
and are determined datum plane.
Dimension b does not include dam bar protrusion.
Allowance dam bar protrusion shall be 0.08 mm total
in excess of the b dimension at maximum material
condition. Dam bar cannot be located on the lower
radius or the lead foot.

Symbol	Dimension in Inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.100	- / 2.55
A1	0.006 / 0.014	0.15 / 0.35
A2	0.071 / 0.087	1.80 / 2.20
b	0.012 / 0.018	0.30 / 0.45
c	0.004 / 0.009	0.09 / 0.20
D	0.520 BSC	13.20 BSC
D1	0.394 BSC	10.00 BSC
D2	0.315	8.00
E	0.520 BSC	13.20 BSC
E1	0.394 BSC	10.00 BSC
E2	0.315	8.00
e	0.031 BSC	0.80 BSC
L	0.029 / 0.041	0.73 / 1.03
L1	0.063	1.60
R1	0.005 / -	0.13 / -
R2	0.005 / 0.012	0.13 / 0.30
S	0.008 / -	0.20 / -
θ	0°/ 7°	as left
θ1	0°/ -	as left
θ2	10°REF	as left
θ3	7°REF	as left
⌓C	0.004	0.10

eMCU writer list		
Company	Contact info	Programmer Model Number
Advantech 7F, No.98, Ming-Chung Rd., Shin-Tien City, Taipei, Taiwan, ROC Web site: http://www.aec.com.tw	Tel:02-22182325 Fax:02-22182435 E-mail: aecwebmaster@advantech.com.tw	LabTool - 48 (1 * 1) LabTool - 848 (1*8)
Caprilion P.O. Box 461 KaoHsiung, Taiwan, ROC Web site: http://www.market.net.tw/ ~ cap/	Tel:07-3865061 Fax:07-3865421 E-mail: cap@market.net.tw	UNIV2000
Hi-Lo 4F, No. 20, 22, LN, 76, Rui Guang Rd., Nei Hu, Taipei, Taiwan, ROC. Web site: http://www.hilosystems.com.tw	Tel:02-87923301 Fax:02-87923285 E-mail: support@hilosystems.com.tw	All - 11 (1*1) Gang - 08 (1*8)
Leap 6th F1-4, Lane 609, Chunghsin Rd., Sec. 5, Sanchung, Taipei Hsien, Taiwan, ROC Web site: http://www.leap.com.tw	Tel:02-29991860 Fax:02-29990015 E-mail: service@leap.com.tw	ChipStation (1*1) SU - 2000 (1*8)
Xeltek Electronic Co., Ltd 338 Hongwu Road, Nanjing, China 210002 Web site: http://www.xeltek-cn.com	Tel:+86-25-4408399, 4543153-206 E-mail: xelclw@jlonline.com, xelgbw@jlonline.com	Superpro/2000 (1*1) Superpro/680 (1*1) Superpro/280 (1*1) Superpro/L+(1*1)

June 2002

Feedback / Inquiry:

To :SyncMOS Technologies, Inc. Attn :MKT / Customer Service Dept. Fax :886-3-579-2960 :886-3-578-0493 Tel :886-3-579-2987 :886-3-578-3344 # 2667	From : _____ Company : _____ Dept, Section : _____ Position Title : _____ Inquiry Date : _____ Ref No : _____

Description: