W99682BCD Data Sheet

Winbond Electronics Corp.

DIGITAL IMAGE PROCESSOR

Table of Contents-

1. GENERAL DESCRIPTION

The W99682BCD is a high performance and highly-integrated DSC (Digital Still Camera) processor that it can preview, capture, compress, store, and display the digital still images or a short period of live video. In addition to processing still images, if connected to the PC through the USB, the W99682BCD based DSC can act as a PC camera, which captures real-time video (30 fps) to the PC.

An on-chip USB controller is deployed for data transfer between the W99682BCD based DSC and the PC. The compressed pictures on flash memory (or SDRAM) can be up-loaded to the PC through the USB, and also the compressed pictures on the PC can be downloaded to the DSC through the USB. In addition to transfer image data, the W99682BCD allows to download the programs of micro controller through the USB to update the external flash program ROM, which allows for end users with firmware upgrades through the Internet.

W99682BCD supports CCD and CMOS image sensors with high performance DSP functions including missing color interpolation, AE (Auto Exposure), AWB (Auto White Balance), Gamma Correction, edge enhancement, contrast stretching, hue and saturation adjusting etc.

W99682BCD has built-in the baseline JPEG codec for image compression and decompression, which corresponds to the ISO/IEC international standard 10918-1, with YCbCr4:2:2 or YCbCr4:2:0 components in interleaved scan. W99682BCD also supports the Exchangeable Image File format (EXIF) to ensure data compatibility and exchangeability.

W99682BCD implements full-speed USB controller complying with USB Spec. Rev. 1.1. It includes six endpoints in which one Control transfer for control data, two isochronous transfer for video and audio data, two programmable bulk transfer for compressed image data and one interrupt transfer for status or event.

W99682BCD includes an 8032 compatible CPU core, a 6K-byte SRAM and two 16-bit programmable timers. The internal 8032 can be optional to disable and connects with external microcontroller for software development.

W99682BCD supports a flexible flash memory interface and can directly connect to CompactFlash and NAND type flash. It also supports the DMA data transfer between SDRAM, USB and flash memory.

W99682BCD integrates a TV encoder to support both NTSC and PAL output.

2. FEATURES

❑ Host Interface

- Support UART / USB Bus Host Interface.
- Easy for host to develop Camera function through UART or USB Command set protocol.

❑ Sensor Interface

- Direct connect to CMOS and CCD image sensor:
- CMOS Image Sensor: AGILENT, HYUNDAI, IC MEDIA, MOTOROLA, OMNIVITION, PHOTOBIT, PIXART and TOSHIBA
- Supports real-time video resolutions up to 640X480 and still image resolutions up to 2048X2048
- High performance sensor DSP functions (includes black level compensation, color Interpolation, false color suppression, edge enhancement, color correction, gamma correction, AEC, AWB, contrast stretching, hue and saturation adjusting)

- Supports universal serial interface to program CMOS or CCD image sensor.

❑ **Audio Interface**

- Support I2S and AC-97 audio codec interface for audio record or playback.

❑ **Frame Memory Interface**

- Supports 16Mb and 64Mb SDRAM with Self Refresh mode
- 16-bit DRAM data bus in 2 Mbytes (1-1Mx16 SDRAM), 4 Mbytes (2-1Mx16 SDRAM), 8 Mbytes (1-4Mx16 SDRAM), or 16 Mbytes (2-4Mx16 SDRAM) configuration

❑ **Flash Memory Interface**

- Directly connect to CompactFlash (CF) and NAND type flash memory
- Supports DMA data transfer between SDRAM and flash memory

❑ **PC Interface**

- Compliant with USB Spec. Rev. 1.1 specification
- Supports six USB pipes including control pipe, isochronous-in pipe for video, isochronous-in pipe for audio, bulk-in pipe, bulk-out pipe, and interrupt pipe

❑ **User Interface**

- Built-in 8-bit 8032 compatible uC with internal 6K bytes data RAM
- Supports external 64K bytes program ROM or flash-ROM
- Supports external microcontroller mode to connect with In-Circuit-Emulator (ICE) for software development

❑ **JPEG CODEC for Image Compression and Decompression**

- Fully compliant with ISO/IEC 10918-1 international JPEG standard
- JPEG compression and decompression for still images
- Real-time motion JPEG (MJPEG) compression with advanced bit rate control for live video
- JPEG baseline sequential mode in interleaved scan YCbCr4:2:2 or YCbCr4:2:0 format
- Two programmable quantization tables for image/video quality control and bit-rate control.
- Support Exchangeable Image File format (EXIF).

❑ **Display Interface**

- Integrated TV encoder to support both NTSC and PAL output
- Support OSD function to display the user interface message on TV

❑ **Power Management**

- Advanced power management including Power-down, Stand-by, and Operating modes. Engines are only active when they are needed
- USB power management including Startup, Operating, and Suspend modes

❑ **Operation Modes**

- *Preview Mode:* Display the incoming video on TV
- *Record Mode:* Compressed images and audio are stored into the flash memory
- *Transfer Mode:* Transfer image/audio data between PC and W99682BCD through USB
- *Playback Mode:* Decode the compressed image to display on TV
- *PC Camera Mode:* Real-time video/audio to the PC through USB with snapshot

❑ **Built-in Two PLL (Phase-Locked Loops) Clock Synthesizers**

❑ **2.5V Core, 3.3V I/O, 5 V Input Tolerant**

❑ **W99682BCD is packaged in a 128 pins LQFP Package**

3. SYSTEM OVERVIEW

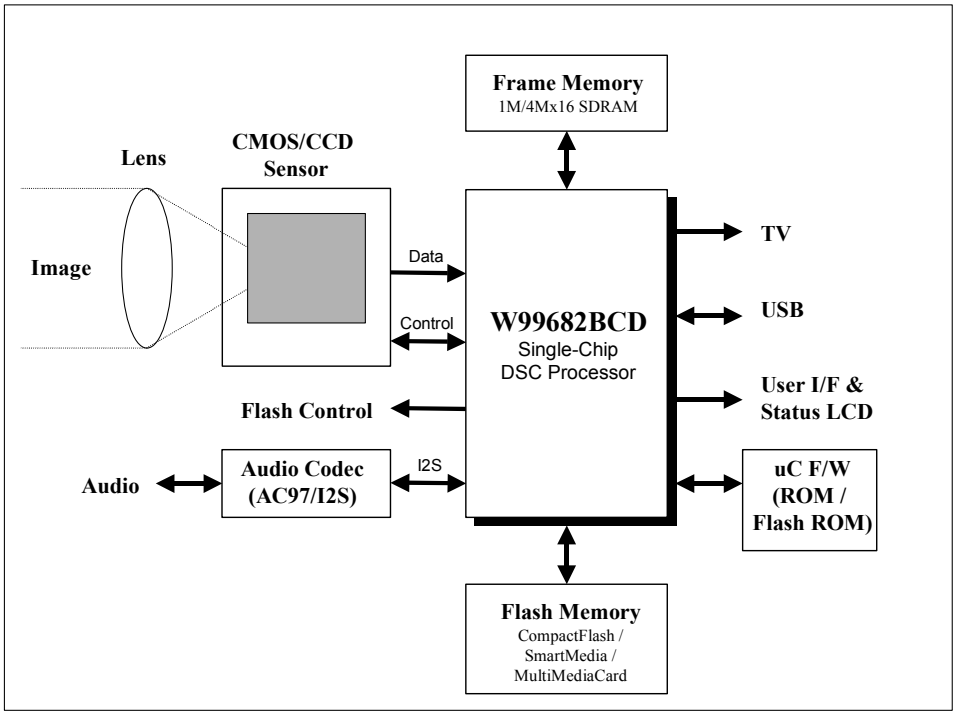


Figure 3.1 W99682BCD Based DSC System Diagram

3.1 Operation Modes

The W99682BCD provides seven operation modes:

- *Preview Mode*: Real-time capture and display the images (video) on TV.
- *Record Mode*: Capture/compress/store a still image (or video) on flash memory or SDRAM
- *Playback Mode*: Restore/decompress/display the stored images (single-image or thumbnails) on the TV
- *Transfer Mode*: Upload or download the flash memory or SDRAM to/from PC through the USB
- *Download Mode*: Download firmware from PC through the USB to external flash program ROM
- *PCCam Mode*: Real-time capture, compress, and transfer the video to PC through the USB
- *Power Down*: System enters power down mode to reduce the power consumption. It can be waked up from power down mode by reset or INT1_ event.

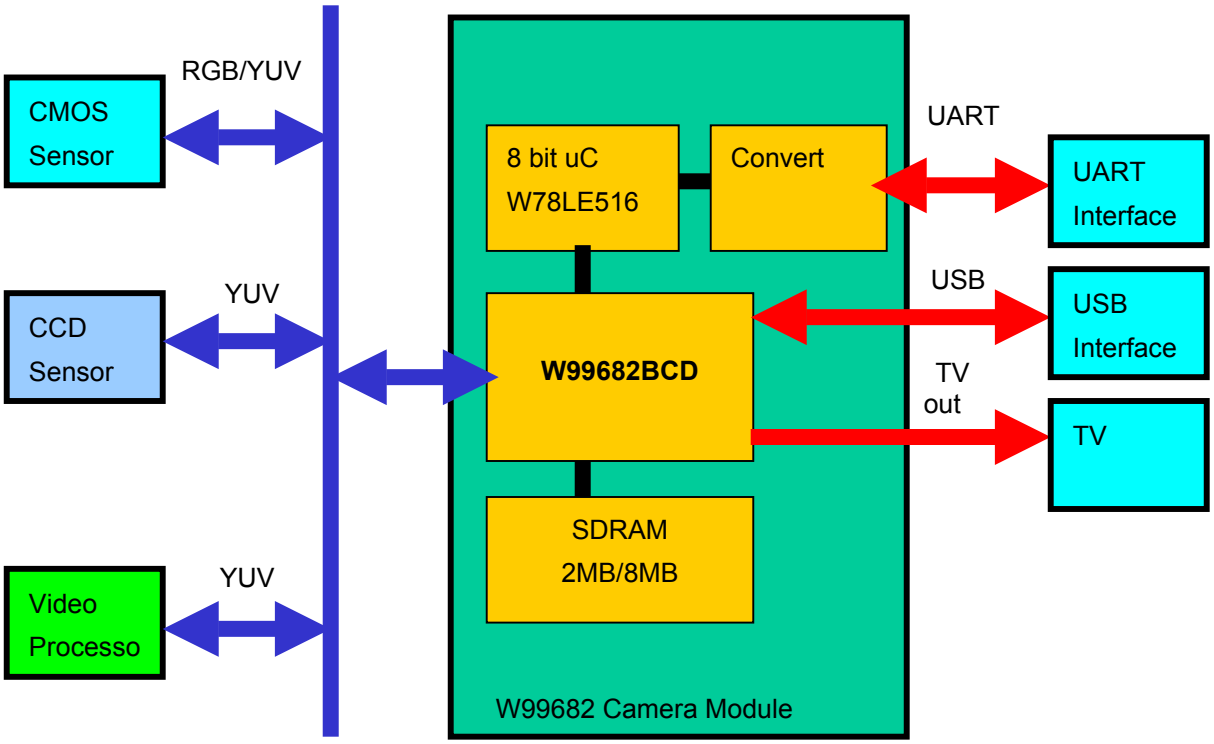
3.2 Address Mapping

µC ADDRESS	DESCRIPTION
0000H – 17FFH	6K Bytes Data RAM
1800H – F7FFH	Reserved (Not Used)
F800H -- FFFFH	Control and Status Registers

4. APPLICATION

4.1 System Camera Device

- **Host Interface**
  - **Support UART / USB Bus Host Interface.**
  - **Easy for host to develop Camera function through UART or USB Command set protocol.**
- Support RGB/YUV CMOS, Video Processor or CCD interface.
- Built-in TV encoder supports NTSC, PAL Composite Video Standards
- JPEG CODEC for Image Compression and Decompression.
- Support OSD function to display the user interface message on TV/LCD screen
- Audio record or playback interface I2S and AC-97
- Application for Modem Cam. , IP Cam. or Home security…etc.



5. PIN DESCRIPTION

The following signal types are used in these descriptions.

I	Input pin
IS	Input pin with Schmitt trigger
B	Bi-directional input/output pin
BR	Bi-directional input/output pin with repeater
BU	Bi-directional input/output pin with internal pull-up
O	Output pin
A	Analog input/output pin
P	Power supply pin
G	Ground pin
#	Active low

USB Interface (3 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
DM	46	A	Data Minus line of differential USB upstream port.
DP	45	A	Data Plus line of differential USB upstream port. Note: provide an external 1.5 KΩ pull-up resistor at DP so the device indicates to the host that it is a full-speed device.
VBUS	49	IS	USB Cable Power

SDRAM Interface (39 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
MD[15:0]	93, 91, 89, 86, 84, 82, 80, 77, 78, 81, 83, 85, 87, 90, 92, 94	BR	SDRAM Data Bus.
MA[11:0]	67, 64, 65, 62, 60, 57, 55, 53, 54, 56, 58, 61	O	SDRAM Address Bus. Note: for SDRAM, MA[10:0] are sampled during the ACTIVE command (row address MA[10:0]) and READ/WRITE command (column address MA[7:0], with MA10 defining AUTO PRECHARGE) to select one location out of the 521K available in the respective bank. MA10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (MA10 HIGH).

SDRAM Interface (39 pins), continued

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
BA1, BA0	66, 68	O	Bank Address: BA defines to which internal bank of SDRAM the ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA is also used to program the 12th and 13th bit of the Mode Register.
CS0#	69	O	Chip-0 Select: CS0# enables the command decoder for the external SDRAM BANK-0.
GPIO4 / CS1#	95	O	CR0007 Bit-7 = “1” => General Purpose I/O [4] CR0007 Bit-7 = “0” => CS1# for the external SDRAM BANK-1 chip select.
DQM	76	O	SDRAM Input/Output Mask. DQM are input mask signals for write accesses and output enable signals for read accesses.
CKE	71	O	SDRAM Clock Enable. CKE activates the SMCLK signal. The SDRAM enters precharge power-down to deactivate the input and output buffers, excluding CKE, for maximum power saving when CKE is LOW coincident with a NOP.
WE#	73	O	SDRAM Command Input. SRAS#, SCAS#, and WE# (along with CS#) define the command being entered.
RAS#	70	O	SDRAM Command Input. SRAS#, SCAS#, and WE# (along with CS#) define the command being entered.
CAS#	72	O	SDRAM Command Input. SRAS#, SCAS#, and WE# (along with CS#) define the command being entered.
MCLK	75	O	SDRAM Clock.

Sensor or Video Interface Interface (16 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
SPCLK	118	I	Clock for Sensor or Video Data Input
SVID[7:0]	117 -- 114, 111 -- 108	I	Sensor or Video Data Input.
SHS	121	B	Horizontal Sync Input. Programmable polarity.
SVS	120	B	Vertical Sync Input. Programmable polarity.
SCLK	123	O	Clock Output to Sensor
SBPF/ AEC	122	B	Black Pixel Flag / Auto Exposure Control
SCK	125	B	Serial Interface Clock
SDA/SDI	126	B	Serial Interface Data
SDO/SDE	127	B	Serial Interface Data Output / Serial Data Enable

Micro Controller Interface (34 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
AD[7:0] / P0[7:0] / FD[7:0]	20 -- 13	BU	Multiplexed low-order Address/Data Bus. Port – 0 Flash Memory Data Bus
A[15:8] / P2[7:0]	30 – 27, 24 -- 21	BU	High-order Address Bus. Port - 2
ALE	7	BU	Address Latch Enable. ALE is used to enable the address latch that separates the address from the data on AD bus.
PSEN#	8	BU	Program Strobe Enable. PSEN# forces the external ROM onto AD bus during fetch and MOVC operations.
INT1# / P3[3]	40	BU	External Interrupt – 1 Port-3 Bit-3
TXD / P3[1] / WR#	39	BU	Internal uC Enable (CR0000 Bit-2 = “1”) => Serial Transmit Data / Port-3 Bit-1 Internal uC Enable (CR0000 Bit-2 = “0”) => Data Write Strobe for access W99682BCD.
RXD / P3[0] / RD#	38	BU	Internal uC Enable (CR0000 Bit-2 = “1”) => Serial Receive Data / Port-3 Bit-0 Internal uC Enable (CR0000 Bit-2 = “0”) => Data Read Strobe for access W99682BCD.

Display Output (19 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
CVBS	100	A	TV Composite-0 Output
RSET	103	A	Full-scale adjust control pin. The full-scale current of DAC is controlled by connecting a resister (R_{SET}) between this pin and V_{SSA2}. The full-scale current I_{OUT} = 10.66 * V_{REF} / R_{SET} (mA).
COMP	104	A	Compensation pin. A 0.1 uF ceramic capacitor with lead length as short as possible must be used to decouple this pin to V_{DDA1}.
VREF	105	A	Voltage reference output. Typical value is 0.9V. A 0.1 μF ceramic capacitor with lead length as short as possible must be used to decouple this pin to V_{SSA2}.
DACVDDO	102	P	TV DAC Analog Power Supply for Output. +3.3 V ±0.3 V.
DACVSSO	101	G	TV DAC Analog Ground for Output
DACVDDI	106	P	TV DAC Analog Power Supply for Internal. +2.5 V ±0.25 V.
DACVSSI	107	G	TV DAC Analog Ground for Internal

Audio Codec Interface (6 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
ASCLK / GA0	32	O	Audio Interface Enable: Audio System Clock Audio Interface Enable: General Purpose I/O – A[0]
ABCLK / GA4	37	BR	Audio Interface Enable: Audio Bit Clock Audio Interface Enable: General Purpose I/O – A[4]
ADI / GA5	36	I	Audio Interface Enable: Audio Data Input Audio Interface Enable: General Purpose I/O – A[5]
ADO / GA1	33	O	Audio Interface Enable: Audio Data Output Audio Interface Enable: General Purpose I/O – A[1]
AWS / ASYNC / GA2	34	O	Audio Interface Enable: I2S => Audio Word Select AC97=> Audio Sample Sync Audio Interface Enable: General Purpose I/O – A[2]
ARST# / GA3	35	O	Audio Interface Enable: Audio Reset Audio Interface Enable: General Purpose I/O – A[3]

Flash Memory Interface (20 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
AD[7:0] / P0[7:0] / FD[7:0]	20 -- 13	BU	Multiplexed low-order Address/Data Bus. Port – 0 Flash Memory Data Bus
FWE# / FIOWR#	4	O	NAND: Write Enable CompactFlash: I/O Write Strobe
FRE# / FIORD#	2	O	NAND: Read Enable CompactFlash: I/O Read Strobe
FCS0# / FA0	1	O	NAND: Chip-0 Enable CompactFlash: Address-0
FCS1# / FA1	128	O	NAND: Chip-1 Enable CompactFlash: Address-1
FALE / FCE1#	6	O	NAND: Address Latch Enable CompactFlash: Chip Select Signal - 1
FCLE / FCE2#	5	O	NAND: Command Latch Enable CompactFlash: Chip Select Signal - 2
FRB#	3	I	NAND: Ready/Busy CompactFlash: Ready Signal

Miscellaneous (16pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
RESET	51	IS	Reset In. This pin is active high to reset chip.
XIN	10	I	Reference frequency input from a crystal or a clock source. It should be 48 MHz if PLL is off (PLLSEL = 0) or 12 Mhz if PLL is on (PLLSEL = 1) for full-speed device.
XOUT	11	O	Oscillator output to a crystal. This pin is left unconnected if an external clock source is employed.
GPIO[6:0]	48, 43, 95, 96, 97 -- 99	BR	General Purpose I/O [6:0]
GPIO[4] / CS1#	95	BR	General Purpose I/O [4] / SDRAM Bank-1 Chip Select
GPIO[3] / INT0#	96	BR	General Purpose I/O [3] / Interrupt Output to external μC
GPIO[2:0]	97 -- 99	BR	General Purpose I/O [2:0]
GB0/ PCLKA	26	BR	CR_0000 Bit-6 = "0: General Purpose I/O – B[0] CR_0000 Bit-6 = "0: Programmable Clock Output - A

Power and Ground (38 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
VDDB	12, 31, 47, 63, 79, 124	P	I/O Pad Buffer Power Supply. Provide isolated power to the I/O buffers for improved noise immunity. +3.3 V ±0.3 V.
VSSB	9, 25, 44, 59, 74, 88, 119	G	I/O Pad Buffer Ground.
VDDI	50, 113	P	Internal Core Logic Power Supply. +2.5 V ±0.25 V.
VSSI	52, 112	G	Internal Core Logic Ground.
AVDD	42	P	PLL Power Supply. . +2.5 V ±0.25 V.
AVSS	41	G	PLL Ground.

5.1 Power-on Reset Initialization

During power-on reset, the states of MD[15:0]] are latched into the W99682BCD's internal configuration registers (CR0000 and CR0001) as device configuration information. Since each pin of MD[15:0] has no internally pulled-up or pulled-down on its I/O buffer. It is required to properly pull-up or pull-down each pin of MD[15:0] bus to config the operation mode of W99682BCD.

POWER-on Reset Configuration Definitions

PINS	VALUE	DEFINITION	CONT'L REG
MD15	0 1	Normal Operation Macro Test Mode Enable (Only for Testing)	CR0001-7
MD14	0 1	UPLL Disable (Only for Debugging, UPLL Clock from Pin XIN) UPLL Enable	CR0001-6
MD13	0 1	VPLL Disable (Only for Debugging, VPLL Clock from Pin GB2) VPLL Enable	CR0001-5
MD12	0 1	Normal Operation, Internal Clock is Divided by 2. Fast Cycle, Internal Clock is same as the MC8051 Clock Input.	CR0001-4
MD11	0 1	Force D+ Signal to Low Normal Operation	CR0001-3
MD10	0 1	USB Self-Powered Device USB Bus-Powered Device	CR0001-2
MD9	0 1	USB Low Power Device USB High Power Device	CR0001-1
MD8	0 1	Internal RCV comes from SIE (Only for Debugging) Internal RCV comes from USB Transceiver	CR0001-0
MD7	0 1	Reserved Normal operation	CR0000_7
MD6	0 1	PCLKA Output Function General Purpose I/O B[1] Function	CR0000_6
MD5	0 1	Normal operation Reserved	CR0000_5
MD4	0 1	Normal operation Reserved	CR0000_4
MD3	0 1	Normal operation Reserved	CR0000_3
MD2	0 1	Internal uC Disable Internal uC Enable	CR0000_2
MD1	0 1	2 SDRAM Banks 1 SDRAM Bank	CR0000_1
MD0	0 1	4M x 16 SDRAM 1M x 16 SDRAM	CR0000_0

6. PIN CONFIGURATION

The W99682BCD is packed in a 128 pins LQFP.

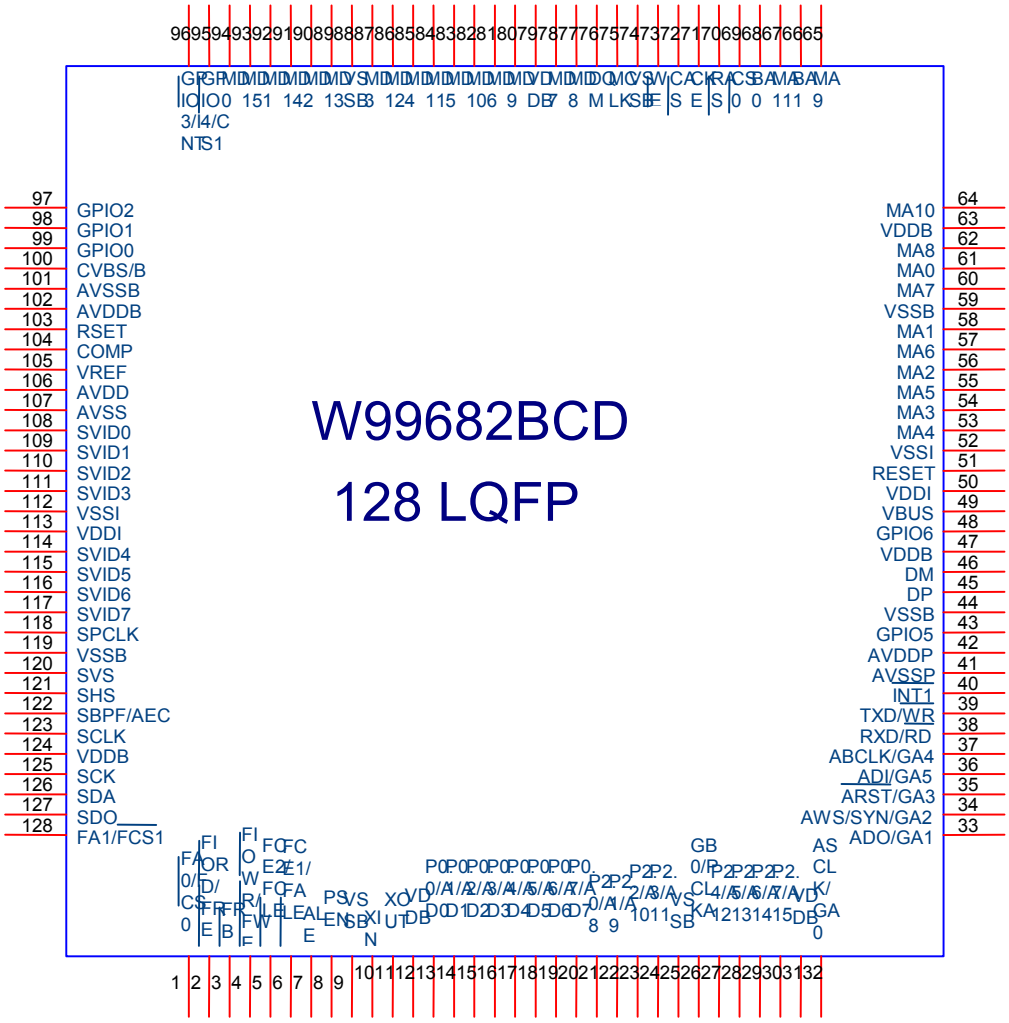


Figure 4.1

7. ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

PARAMETER	MIN.	MAX.	UNIT
Ambient temperature	0	70	°C
Storage temperature	-40	125	°C
DC supply voltage (2.5V)	0	3.5	V
DC supply voltage (3.3V)	0	4.6	V
I/O pin voltage with respect to Vss	– 0.3	5.25	V

Table 7-1

7.2 DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
VDDB	Power Supply for I/O Pads		3.0	3.6	V
DACVDDO	Power Supply for DAC Output		3.0	3.6	V
DACVDDI	Power Supply for DAC Internal Circuit		2.25	2.75	V
AVDD	Power Supply for PLL Analog		2.25	2.75	V
VDDI	Power Supply for Core		2.25	2.75	V
V_{IL}	Input Low Voltage		0	0.8	V
V_{IH}	Input High Voltage		2.0	5.25	V
V_{OL}	Output Low Voltage	I_{OUT} = 2 mA		Vss +0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -2 mA	2.4		V
I_{IL}	Input Low Leakage Current	V_{IN} = 0.4V		10	μA
I_{IH}	Input High Leakage Current	V_{IN} = 2.4V		-10	μA
I_{UP}	Pull-up Current	V_{IN} = 0V		-500	μA
I_{PD}	Power Down Current			TBD	μA
I_{DD}	Active Current			TBD	mA

Table 7-2

7.3 DAC DC Characteristics

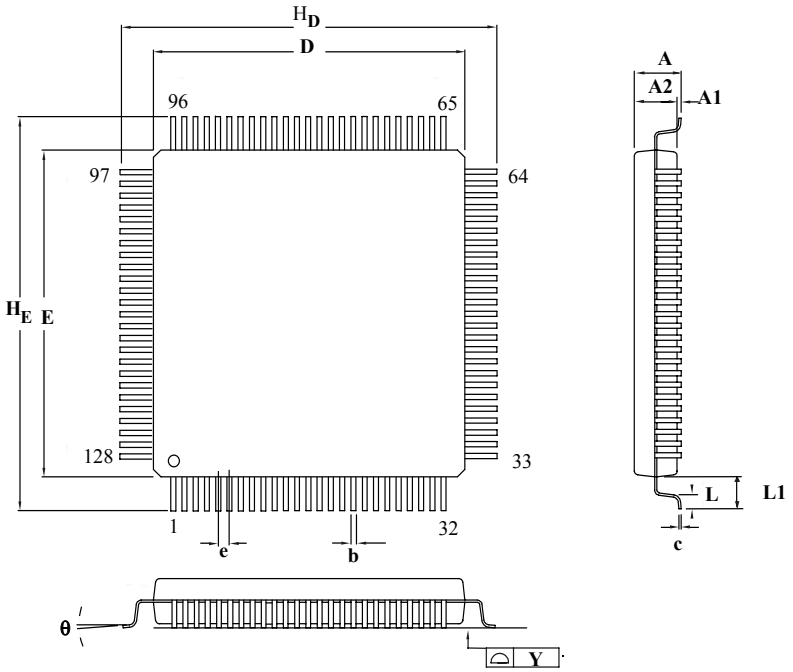
PARAMETER	MIN.	TYP.	MAX.	UNIT
TVDAC Resolution		10		Bits
Integral Linearity Error		0.5	±2	LSB
Differential Linearity Error		0.5	±1	LSB
Gray Scale Error			TBD	%Gray
LSB Size		33.28		μA
DAC-to-DAC Matching		2	5	%
Output Compliance	0	1.278		V
Gray Scale Current Range	2.0	34.08		mA
Output Impedance		TBD		Ω
Output Capacitance (f = 1 MHz; I_{OUT} = 0 mA)			TBD	pF
Monotonicity				Guaranteed
Internal V_{REF}	1.230	1.265	1.272	V
Power Supply Reject Ratio (f = 1 KHz)			TBD	%

Table 7-3

Note 1. Measured with VREF = 1.235 V, RSET = 386 Ω. RL = 37.5 Ω.

8. PACKAGING DIMENSION

128-pins LQFP



Controlling Dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	—	0.006	0.05	—	0.15
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.005	0.006	0.009	0.13	0.16	0.23
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.556	13.90	14.00	14.10
E	0.547	0.551	0.556	13.90	14.00	14.10
e	—	0.016	—	—	0.40	—
H_D	0.622	0.630	0.638	15.80	16.00	16.20
H_E	0.622	0.630	0.638	15.80	16.00	16.20
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

9. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Dec. 19, 2003	-	Initial Issue

Headquarters
No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5665577
http://www.winbond.com.tw/

Taipei Office
9F, No.480, Rueiguang Rd.,
Neihu District, Taipei, 114,
Taiwan, R.O.C.
TEL: 886-2-8177-7168
FAX: 886-2-8751-3579

Winbond Electronics Corporation America
2727 North First Street, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-5441798

Winbond Electronics Corporation Japan
7F Daini-ueno BLDG, 3-7-18
Shinyokohama Kohoku-ku,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

Winbond Electronics (Shanghai) Ltd.
27F, 2299 Yan An W. Rd. Shanghai,
200336 China
TEL: 86-21-62365999
FAX: 86-21-62365998

Winbond Electronics (H.K.) Ltd.
Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064