INITIAL RELEASE
Final Electrical Specifications

LTC1661

Micropower Dual 10-Bit DAC in MSOP

January 1999

FEATURES

- **Tiny: Two 10-Bit DACs in an 8-Lead MSOP—Half the Board Space of an SO-8**
- **Ultralow Power: 60µA per DAC Plus 1µA Sleep Mode for Extended Battery Life**
- Wide 2.7V to 5.5V Supply Range
- Double Buffered for Independent or Simultaneous DAC Updates
- **Rail-to-Rail Voltage Outputs Drive 1000pF**
- Reference Range Includes Supply for Ratiometric 0V-to-V_{CC} Output
- 3-Wire Serial Interface with Schmitt Trigger Inputs
- Differential Nonlinearity: ≤±0.75LSB Max

APPLICATIONS

- Mobile Communications
- Digitally Controlled Amplifiers and Attenuators
- Portable Battery-Powered Instruments
- Automatic Calibration for Manufacturing
- Remote Industrial Devices

DESCRIPTION

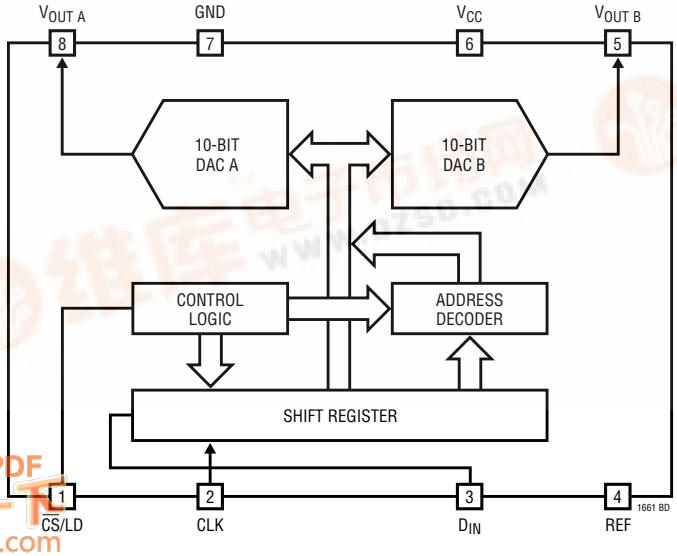
The LTC®1661 integrates two accurate, addressable, 10-bit digital-to-analog converters (DACs) in a single tiny MS8 package. Each buffered DAC consumes just 60µA total supply current, yet is capable of supplying DC output currents in excess of 5mA and reliably driving capacitive loads up to 1000pF. Sleep mode further reduces total supply current to a negligible 1µA.

Linear Technology's proprietary, inherently monotonic voltage interpolation architecture provides excellent linearity while allowing for an exceptionally small external form factor. The double-buffered input logic provides simultaneous update capability and can be used to write to either DAC without interrupting Sleep mode.

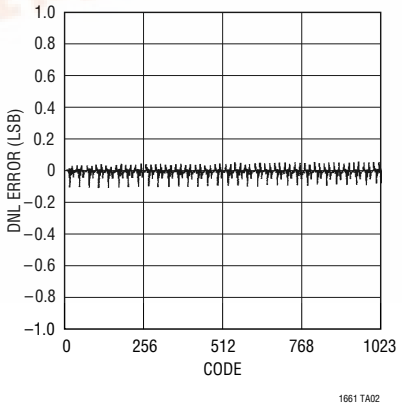
Ultralow supply current, power-saving Sleep mode and extremely compact size make the LTC1661 ideal for battery-powered applications, while its straightforward usability, high performance and wide supply range make it an excellent choice as a general purpose converter.

For additional outputs and even greater board density, please refer to the LTC1660 micropower octal 10-bit DAC.

BLOCK DIAGRAM



Differential Nonlinearity (DNL)



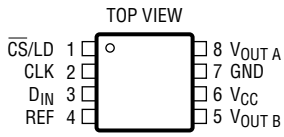
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} to GND ..... –0.5V to 7.5V
Logic Inputs to GND ..... –0.5V to 7.5V
$V_{OUT\ A}$, $V_{OUT\ B}$, REF to GND .....–0.2V to V_{CC} + 0.2V
Maximum Junction Temperature ..... 125°C
Storage Temperature Range ..... –65°C to 150°C

Operating Temperature Range
LTC1661C..... 0°C to 70°C
LTC1661I..... –40°C to 85°C
Lead Temperature (Soldering, 10 sec)..... 300°C

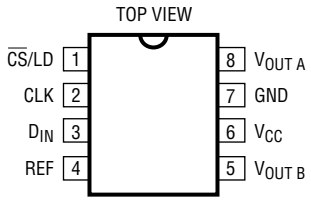
PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC1661CMS8 LTC1661IMS8
MS8 PART MARKING
LTDV LTDW



N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 125°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LTC1661CN8 LTC1661IN8

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 2.7V to 5.5V, $V_{REF} \leq V_{CC}$, V_{OUT} Unloaded, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Accuracy							
	Resolution		●	10			Bits
	Monotonicity	$V_{REF} \leq V_{CC}$ – 0.1V (Note 2)	●	10			Bits
DNL	Differential Nonlinearity	$V_{REF} \leq V_{CC}$ – 0.1V (Note 2)	●		±0.1	±0.75	LSB
INL	Integral Nonlinearity	$V_{REF} \leq V_{CC}$ – 0.1V (Note 2)	●		±0.4	±2	LSB
V_{OS}	Offset Error	Measured at Code 20	●		±5	±30	mV
	V_{OS} Temperature Coefficient				±15		µV/°C
FSE	Full-Scale Error	V_{CC} = 5V, V_{REF} = 4.096V	●		±1	±12	LSB
	Full-Scale Error Temperature Coefficient				±30		µV/°C
Reference Input							
	Input Voltage Range		●	0		V_{CC}	V
	Resistance	Not in Sleep Mode	●	140	260		kΩ
	Capacitance	(Note 6)	●		15		pF
I_{REF}	Reference Current	Sleep Mode	●		0.001	1	µA
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	2.7		5.5	V
I_{CC}	Supply Current	V_{CC} = 5V (Note 3) V_{CC} = 3V (Note 3) Sleep Mode (Note 3)	● ● ●		120 95 1	195 154 3	µA µA µA

ELECTRICAL CHARACTERISTICS

V_{CC} = 2.7V to 5.5V, $V_{REF} \leq V_{CC}$, V_{OUT} Unloaded, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Performance							
	Short-Circuit Current Low	V_{OUT} = 0V, $V_{CC} = V_{REF}$ = 5V, Code = 1023	●	10	25	100	mA
	Short-Circuit Current High	$V_{OUT} = V_{CC} = V_{REF}$ = 5V, Code = 0	●	7	19	120	mA
AC Performance							
	Voltage Output Slew Rate	Rising (Notes 4, 5) Falling (Notes 4, 5)			0.60 0.25		V/µs V/µs
	Voltage Output Settling Time	To ±0.5LSB (Notes 4, 5)			30		µs
Digital I/O							
V_{IH}	Digital Input High Voltage	V_{CC} = 2.7V to 5.5V V_{CC} = 2.7V to 3.6V	● ●	2.4 2.0			V V
V_{IL}	Digital Input Low Voltage	V_{CC} = 4.5V to 5.5V V_{CC} = 2.7V to 5.5V	● ●			0.8 0.6	V V
I_{LK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●			±10	µA
C_{IN}	Digital Input Capacitance	(Note 6)	●			10	pF

TIMING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} = 4.5V to 5.5V							
t_1	D_{IN} Valid to CLK Setup		●	40	15		ns
t_2	D_{IN} Valid to CLK Hold		●	0	–10		ns
t_3	CLK High Time	(Note 6)	●	30	14		ns
t_4	CLK Low Time	(Note 6)	●	30	14		ns
t_5	$\overline{CS}$/LD Pulse Width	(Note 6)	●	80	27		ns
t_6	LSB CLK High to $\overline{CS}$/LD High	(Note 6)	●	30	2		ns
t_7	$\overline{CS}$/LD Low to CLK High	(Note 6)	●	65	22		ns
t_9	CLK Low to $\overline{CS}$/LD Low	(Note 6)	●	0	–5		ns
t_{11}	$\overline{CS}$/LD High to CLK Positive Edge	(Note 6)	●	20	0		ns
V_{CC} = 2.7V to 5.5V							
t_1	D_{IN} Valid to CLK Setup	(Note 6)	●	60	20		ns
t_2	D_{IN} Valid to CLK Hold	(Note 6)	●	0	–10		ns
t_3	CLK High Time	(Note 6)	●	50	15		ns
t_4	CLK Low Time	(Note 6)	●	50	15		ns
t_5	$\overline{CS}$/LD Pulse Width	(Note 6)	●	100	30		ns
t_6	LSB CLK High to $\overline{CS}$/LD High	(Note 6)	●	50	3		ns
t_7	$\overline{CS}$/LD Low to CLK High	(Note 6)	●	80	23		ns
t_9	CLK Low to $\overline{CS}$/LD Low	(Note 6)	●	0	–5		ns
t_{11}	$\overline{CS}$/LD High to CLK Positive Edge	(Note 6)	●	30	0		ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: Nonlinearity and monotonicity are defined from the first code that is greater than or equal to the maximum offset specification to code 1023 (full scale). See Applications Information.

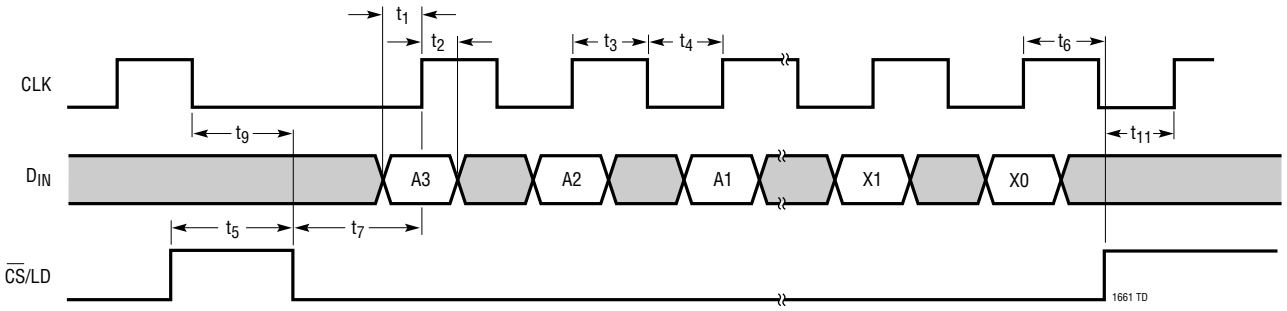
Note 3: Digital inputs at 0V or V_{CC}.

Note 4: Load is 10kΩ in parallel with 100pF.

Note 5: $V_{CC} = V_{REF}$ = 5V. DAC switched between $0.1V_{FS}$ and $0.9V_{FS}$, i.e., codes k = 102 and k = 922.

Note 6: Guaranteed by design and not subject to test.

TIMING DIAGRAM



PIN FUNCTIONS

$\overline{CS}$/LD (Pin 1): Serial Interface Chip Select/Load Input. When $\overline{CS}$/LD is low, CLK is enabled for shifting data on D_{IN} into the register. When $\overline{CS}$/LD is pulled high, CLK is disabled and data is loaded from the shift register into the specified DAC register(s), updating the analog output(s). CMOS and TTL compatible.

CLK (Pin 2): Serial Interface Clock Input. CMOS and TTL compatible.

D_{IN} (Pin 3): Serial Interface Data Input. Data on the D_{IN} pin is shifted into the 16-bit register on the rising edge of CLK. CMOS and TTL compatible.

REF (Pin 4): Reference Voltage Input. $0V \leq V_{REF} \leq V_{CC}$.

$V_{OUT\ A}$, $V_{OUT\ B}$ (Pins 8,5): DAC Analog Voltage Outputs. The output range is

$$0 \text{ to } V_{REF}\left(\frac{1023}{1024}\right)$$

V_{CC} (Pin 6): Supply Voltage Input. $2.7V \leq V_{CC} \leq 5.5V$.

GND (Pin 7): System Ground.

DEFINITIONS

Differential Nonlinearity (DNL): The difference between the measured change and the ideal 1LSB change for any two adjacent codes. The DNL error between any two codes is calculated as follows:

$$DNL = (\Delta V_{OUT} - LSB)/LSB$$

Where ΔV_{OUT} is the measured voltage difference between two adjacent codes.

Digital Feedthrough: The glitch that appears at the analog output caused by AC coupling from the digital inputs when they change state. The area of the glitch is specified in (nV)(sec).

Full-Scale Error (FSE): The deviation of the actual full-scale voltage from ideal. FSE includes the effects of offset and gain errors (see Applications Information).

Integral Nonlinearity (INL): The deviation from a straight line passing through the endpoints of the DAC transfer curve (Endpoint INL). Because the output cannot go below zero, the linearity is measured between full scale and the lowest code which guarantees the output will be greater than zero. The INL error at a given input code is calculated as follows:

$$INL = [V_{OUT} - V_{OS} - (V_{FS} - V_{OS})(code/1023)]/LSB$$

Where V_{OUT} is the output voltage of the DAC measured at the given input code.

DEFINITIONS

Least Significant Bit (LSB): The ideal voltage difference between two successive codes.

$LSB = V_{REF}/1024$

Resolution (n): Defines the number of DAC output states (2^n) that divide the full-scale range. Resolution does not imply linearity.

Voltage Offset Error (V_{OS}): Nominally, the voltage at the output when the DAC is loaded with all zeros. A single supply DAC can have a true negative offset, but the output cannot go below zero (see Applications Information).

For this reason, single supply DAC offset is measured at the lowest code that guarantees the output will be greater than zero.

OPERATION

Transfer Function

The transfer function for the LTC1661 is:

$$V_{OUT(IDEAL)} = \left(\frac{k}{1024}\right)V_{REF}$$

where k is the decimal equivalent of the binary DAC input code D9-D0 and V_{REF} is the voltage at REF (Pin 6).

Power-On Reset

The LTC1661 positively clears the outputs to zero scale when power is first applied, making system initialization consistent and repeatable.

Power Supply Sequencing

The voltage at REF (Pin 4) must not ever exceed the voltage at V_{CC} (Pin 6) by more than 0.2V. Particular care should be taken in the power supply turn-on and turn-off sequences to assure that this limit is observed. See Absolute Maximum Ratings.

Serial Interface

See Table 1. The 16-bit input word consists of the 4-bit DAC control code, the 10-bit input code and two don't care bits.

Table 1. LTC1661 Input Word

A3	A2	A1	A0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X1	X0
Control				Input Code										Don't Care	

The data path for the 10-bit input code is buffered by two latch registers. The first of these, the Input Register, is used for loading new input codes. The second buffer, the DAC Register, is used for updating the DAC outputs. Each DAC has its own 10-bit Input Register and 10-bit DAC Register.

By selecting the appropriate 4-bit DAC control code (see Table 2) it is possible to perform single operations, such as loading one DAC or changing Power-Down status (Sleep/Wake). In addition, some control codes perform two or more operations at the same time. For example, one such code loads DAC A, updates both outputs and Wakes the part. The DACs can be loaded separately or together, but the outputs are always updated together.

Register Loading Sequence

See Figure 1. With $\overline{CS}$/LD held low, data on the D_{IN} input is shifted into the 16-bit Shift Register on the positive edge of CLK. The 4-bit DAC control code, A3-A0, is loaded first, then the 10-bit input code, D9-D0, ordered MSB-to-LSB in each case. Two don't-care bits, X1 and X0, are loaded last. When the full 16-bit word has been shifted in, $\overline{CS}$/LD is pulled high, causing the system to respond according to Table 2. The clock is disabled internally when $\overline{CS}$/LD is high. Note: CLK must be low before $\overline{CS}$/LD is pulled low.

Sleep Mode

DAC control code 1110_b is reserved for the special Sleep instruction (see Table 2). In this mode, most internal bias currents are disabled while all digital circuitry stays fully active; static power consumption is thus virtually eliminated. The analog outputs are set in a high impedance state and all DAC settings are retained in memory so that when Sleep mode is exited, the outputs of DACs not updated by the Wake command are restored to their last active state.

OPERATION

Table 2. DAC Control Functions

CONTROL				INPUT REGISTER STATUS	DAC REGISTER STATUS	POWER-DOWN STATUS (SLEEP/WAKE)	COMMENTS
A3	A2	A1	A0				
0	0	0	0	No Change	No Update	No Change	No Operation. Power-Down Status Unchanged (Part Stays In Wake or Sleep Mode)
0	0	0	1	Load DAC A	No Update	No Change	Load Input Register A with Data. DAC Outputs Unchanged. Power-Down Status Unchanged
0	0	1	0	Load DAC B	No Update	No Change	Load Input Register B with Data. DAC Outputs Unchanged. Power-Down Status Unchanged
0	0	1	1	Reserved			
0	1	0	0	Reserved			
0	1	0	1	Reserved			
0	1	1	0	Reserved			
0	1	1	1	Reserved			
1	0	0	0	No Change	Update Outputs	Wake	Load Both DAC Regs with Existing Contents of Input Regs. Outputs Update. Part Wakes Up
1	0	0	1	Load DAC A	Update Outputs	Wake	Load Input Reg A. Load DAC Regs with New Contents of Input Reg A and Existing Contents of Reg B. Outputs Update. Part Wakes Up
1	0	1	0	Load DAC B	Update Outputs	Wake	Load Input Reg B. Load DAC Regs with Existing Contents of Input Reg A and New Contents of Reg B. Outputs Update. Part Wakes Up
1	0	1	1	Reserved			
1	1	0	0	Reserved			
1	1	0	1	No Change	No Update	Wake	Part Wakes Up. Input and DAC Regs Unchanged. DAC Outputs Reflect Existing Contents of DAC Regs
1	1	1	0	No Change	No Update	Sleep	Part Goes to Sleep. Input and DAC Regs Unchanged. DAC Outputs Set to High Impedance State
1	1	1	1	Load DACs A, B with Same 10-Bit Code	Update Outputs	Wake	Load Both Input Regs. Load Both DAC Regs with New Contents of Input Regs. Outputs Update. Part Wakes Up

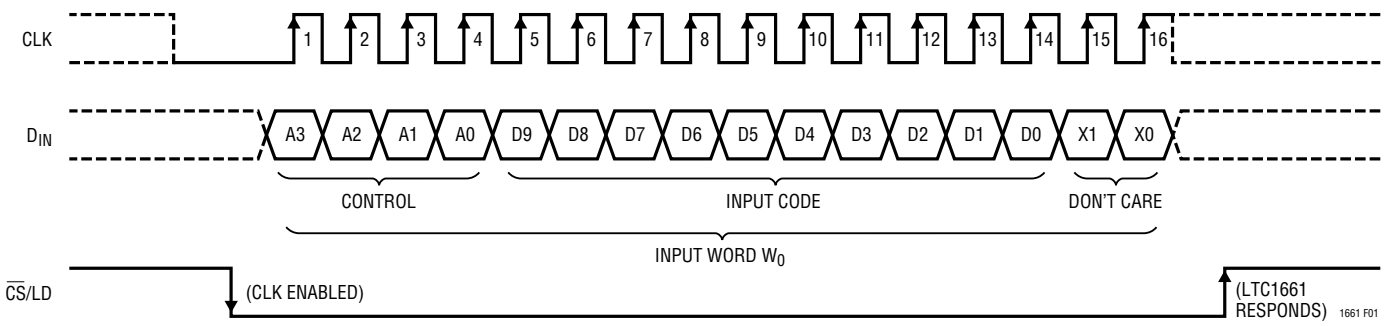


Figure 1. Register Loading Sequence

OPERATION

Sleep mode is initiated by performing a load sequence using control code 1110_b (the DAC input code D9-D0 is ignored). The input codes stored in the input register for each channel may be changed during Sleep by using control codes 0001_b and 0010_b.

Voltage Outputs

Each of the rail-to-rail output amplifiers contained in the LTC1661 can typically source or sink up to 5mA (V_{CC} = 5V). The outputs swing to within a few millivolts of either supply when unloaded and have an equivalent output resistance of 85Ω (typical) when driving a load to the rails. The output amplifiers are stable driving capacitive loads up to 1000pF.

A small resistor placed in series with the output can be used to achieve stability for any load capacitance. For example, a 0.1μF load can be successfully driven by inserting a 110Ω resistor. The phase margin of the resulting circuit is 45°, and increases monotonically from this point if larger values of resistance, capacitance or both are substituted for the values given.

APPLICATIONS INFORMATION

Rail-to-Rail Output Considerations

In any rail-to-rail DAC, the output swing is limited to voltages within the supply range.

If the DAC offset is negative, the output for the lowest codes limits at 0V as shown in Figure 2b.

Similarly, limiting can occur near full scale when the REF pin is tied to V_{CC}. If $V_{REF} = V_{CC}$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC} as shown in Figure 2c. No full-scale limiting can occur if V_{REF} is less than V_{CC} – FSE.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

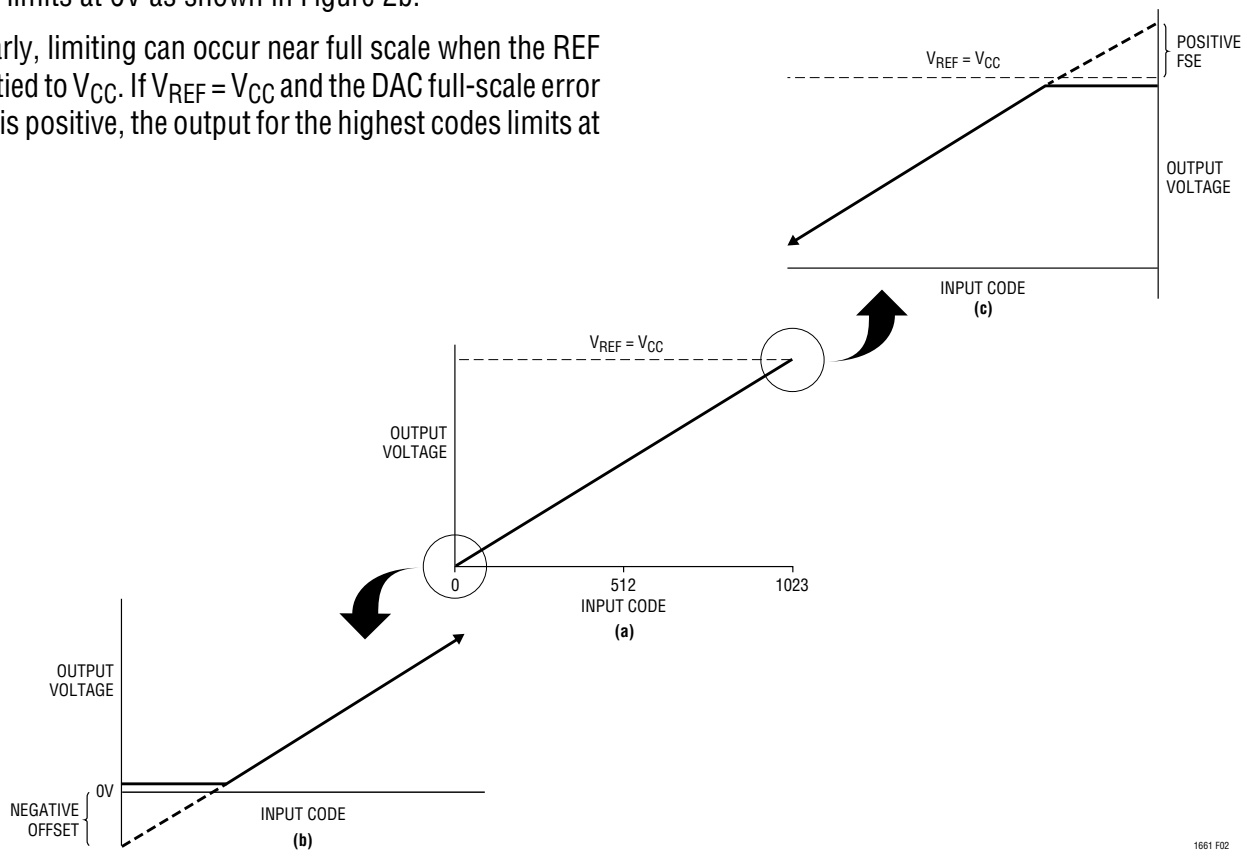
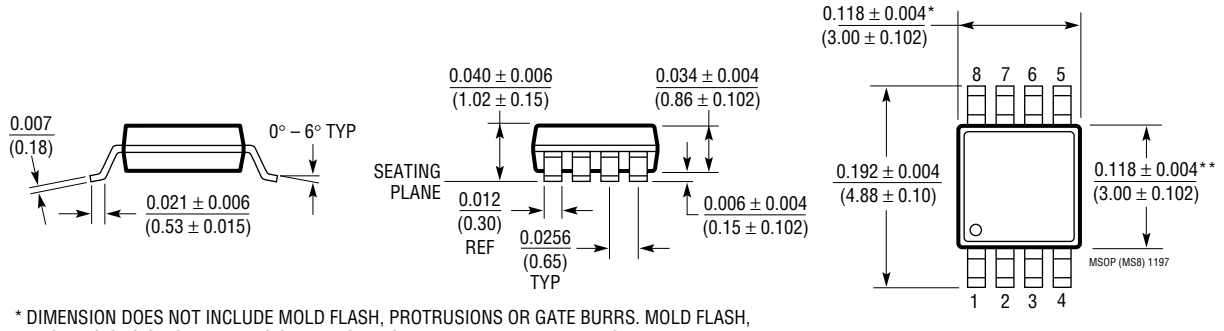


Figure 2. Effects of Rail-to-Rail Operation On a DAC Transfer Curve. (a) Overall Transfer Function (b) Effect of Negative Offset for Codes Near Zero Scale (c) Effect of Positive Full-Scale Error for Input Codes Near Full Scale When $V_{REF} = V_{CC}$

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

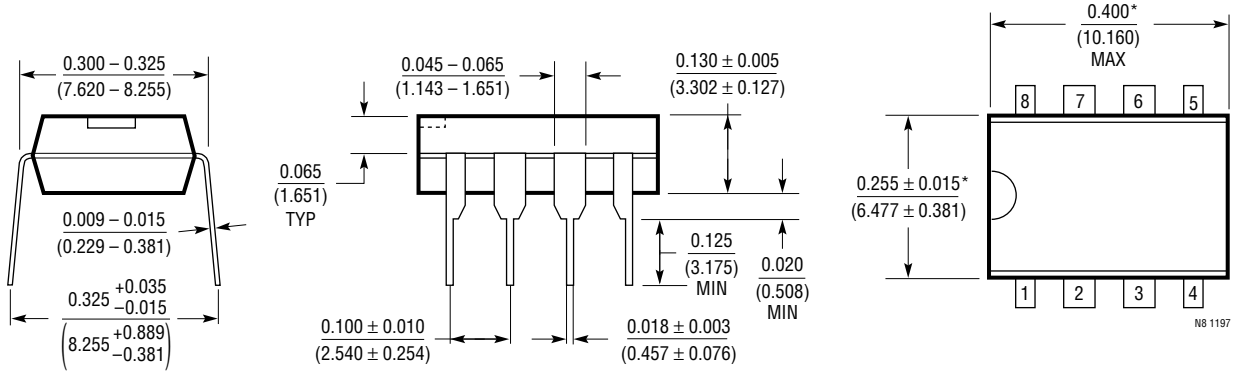
MS8 Package
8-Lead Plastic MSOP
(LTC DWG # 05-08-1660)



* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1446/LTC1446L	Dual 12-Bit V_{OUT} DACs in SO-8 Package with Internal Reference	LTC1446: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1446L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1448	Dual 12-Bit V_{OUT} DAC in SO-8 Package	V_{CC} = 2.7V to 5.5V, External Reference Can Be Tied to V_{CC}
LTC1454/LTC1454L	Dual 12-Bit V_{OUT} DACs in SO-16 Package with Added Functionality	LTC1454: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1454L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1458/LTC1458L	Quad 12-Bit Rail-to-Rail Output DACs with Added Functionality	LTC1458: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1458L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1659	Single Rail-to-Rail 12-Bit V_{OUT} DAC in 8-Lead MSOP Package V_{CC}: 2.7V to 5.5V	Low Power Multiplying V_{OUT} DAC. Output Swings from GND to REF. REF Input Can Be Tied to V_{CC}
LTC1660	Octal 10-Bit V_{OUT} DAC in 16-Pin Narrow SSOP	V_{CC} = 2.7V to 5.5V, Micropower, Rail-to-Rail Output