SLUS634B − NOVEMBER 2004 − REVISED MAY 2005

QUAD INTEGRATED POWER SOURCING EQUIPMENT POWER MANAGER

FEATURES

- Quad-Port Power Management With Integrated Switches and Sense Resistors
- Compliant to IEEE 802.3af Standard
- Operates from a Single 48-V Input Supply
- Individual Port 15-bit A/D
- Auto, Semi-Auto and Power Management Operating Modes
- Controlled Current Ramps for Reduced EMI and Charging of PD's Bulk Capacitance
- I²C Clock and Oscillator Watch Dog Timers
- Over-Temperature Protection
- DC and DC Modulated Disconnect
- Supports Legacy Detection for Non-Compliant PD
- Supports AC Disconnect
- High-Speed 400-kHz I²C Interface
- Comprehensive Power Management Software Available
- Operating Temperature Range −40°C to 125°C

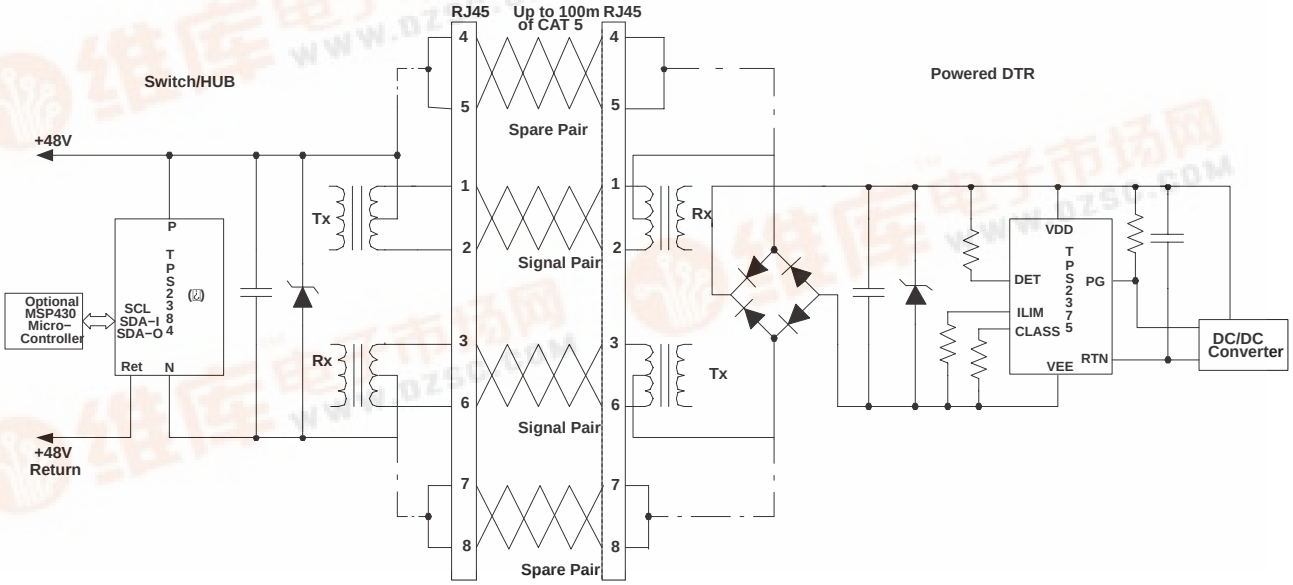
APPLICATIONS

- Ethernet Enterprise Switches
- Ethernet Hubs
- SOHO Hubs
- Ethernet Mid-Spans
- PSE Injectors

DESCRIPTION

The TPS2384 is a quad-port power sourcing equipment power manager (PSEPM) and is compliant to the Power-over-Ethernet (PoE) IEEE 802.3af standard. The TPS2384 operates from a single 48-V supply and over a wide temperature range (−40°C to +125°C). The integrated output eliminates 2 external components per port (FET and sense resistor) and will survive 100-V transient. Four individual 15-bit A/D converters are used to measure port resistance, voltage, current and die temperature making PSE solution simple and robust. The TPS2384 comes with a comprehensive software solution to meet the most demanding application which can serve as a core for all PoE system designs.

TYPICAL APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DESCRIPTION (CONTINUED)

The TPS2384 has three internal supply buses (10 V, 6.3 V and 3.3 V) generated from the 48-V input supply. These supplies are used to bias all internal digital and analog circuitry. Each supply has been brought out separately for proper bypassing to insure high performance. The digital supply (3.3 V) is available for powering external loads up to 2 mA. For more demanding loads it is highly recommended to use external buffers to prevent system degradation. When the TPS2384 is initially powered up an internal Power-on-Reset (POR) circuit resets all registers and sets all ports to the off state to ensure that the device is powered up in a known safe operating state.

The TPS2384 has three modes of operation; auto mode (AM), semi-auto mode (SAM) and power management mode (PMM).

- In auto mode the TPS2384 performs discovery, classification and delivery of power autonomously to a compliant PD without the need of a micro-controller.
- In semi-auto mode the TPS2384 operates in auto mode but users can access the contents of all read status registers and A/D registers thru the I^2C serial interface. All write control registers are active except for D0 thru D3 of port register 1 (Address 0010) for limited port control. The semi-auto mode allows the TPS2384 to detect valid PD without micro-controller intervention but adds a flexibility to perform power management activities.
- Power management mode (with a micro-controller) allows users additional capabilities of discovering non-compliant (legacy) PDs, performing AC disconnect and advanced power management system control that are based on real time port voltages and currents. All functions in this mode are programmed and controlled through read/write registers over the I^2C interface. This allows users complete freedom in detecting and powering devices. A comprehensive software package is available that mates the power of the TPS2384 with the MSP430 micro-controller.

TPS2384 integrated output stage provides port power and low-side control. The internal low-side circuitry is designed with internal current sensing so there are no external resistors required. The output design ensures the power switches operate in the fully enhanced mode for low power dissipation.

The I^2C interface allows easy application of opto-coupler circuitry to maintain Ethernet port isolation when a ground based micro-controller is required. The TPS2384 five address pins (A1 − A5) allow the device to be addressed at one of 31 possible I^2C addresses. Per-port write registers separately control each port state (discovery, classification, legacy, power up, etc) while the read registers contain status information of the entire process along with parametric values of discovery, classification, and real-time port operating current, voltage and die temperature.

The proprietary 15-bit integrating A/D converter is designed to meet the harsh environment where the PSEPM resides. The converter is set for maximum rejection of power line noise allowing it to make accurate measurements of line currents during discovery, classification and power delivery for reliable power management decisions.

The TPS2384 is available in a 64-pin Power PAD™ package.

ORDERING INFORMATION

TEMPERATURE RANGE $T_A = T_J$	PACKAGED DEVICES†
	TQFP − 64 (PAP)‡
−40°C to 125°C	TPS2384

† The PAP package is available taped and reeled. Add R suffix to device type (e.g.TPS2384PAPR) to order quantities of 2,500devices per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted)†‡

PARAMETER	SYMBOL	RATING	UNITS
V10 current sourced		100	µA
V3.3 current sourced		5	mA
Applied voltage on CINT#, CT, RBIAS		−0.5 to +10	V
Applied voltage on SCL_I, SDA_I, SDA_O, INTB, A1, A2, A3, A4, A5, MS, PORB, WD_DIS, ALT_A/B, AC_LO, AC_HI		−0.5 to +6	
Applied voltage on V48, P#, N#		−0.5 to +80	
Junction operating temperature	T_J	−40 to 125	°C
Storage temperature	T_{stg}	−55 to 150	
Lead temperature (soldering, 10 sec.)	T_{sol}	260	

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute−maximum−rated conditions for extended periods may affect device reliability.

‡ All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATION CONDITIONS

Parameter	MIN	TYP	MAX	UNITS
Input voltage, V_{DD}	44	48	57	V
Junction temperature, T_J	−40		125	°C

ELECTRO STATIC DISCHARGE (ESD) PROTECTION

	MAX	UNITS
Human body model	1.5	kV
CDM	1	
Machine model	0.2	

DISSIPATION RATING TABLE†

PACKAGE	THERMAL RESISTANCE JUNCTION TO CASE θ_{JC}	THERMAL RESISTANCE JUNCTION TO AMBIENT θ_{JA}
PAP	0.38 °C/W	21.47 °C/W

† Thermal Resistance measured using 2-oz copper trace and copper pad solder following layout recommendation in TI Publication PowerPad™ Thermally Enhance Package Technical Brief SLMA002.

ELECTRICAL CHARACTERISTICS:

V48 = 48 V, R_T = 124 kΩ, C_T = 220 pf, C_{INT} = 0.027 μF (low leakage), −40°C to −125°C and $T_A = T_j$ (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Power Supply					
V48 quiescent current	Off mode (all ports)	4	9	12	mA
V48 quiescent current	Powered mode (all ports)		10	14	
V10, internal analog supply	I_{LOAD} = 0	9.75	10.5	11.5	V
V3.3, internal digital supply	I_{LOAD} = 0 to 3 mA	3	3.3	3.7	
V3.3 short circuit current	V = 0	3		12	mA
V6.3, internal supply	Iload = 0	5	6.3	7	V
V2.5, internal reference supply	Iload = 0	2.46	2.5	2.54	
Input UVLO			26	32	
Internal POR time out(I^2C)	After all supplies are good I^2C activity is valid		8		Pulses
Internal POR time out (Port)	After all supplies are good Port active to I^2C commands		66000		
Port Discovery					
Port off #P to #N input resistance		400			kΩ
Discovery open circuit voltage			22	30	V
Discovery 1 voltage loop control	70 μA < I_{PORT} < 3 mA	2.8	4.4		
Discovery 2 voltage loop control	70 μA < I_{PORT} I < 3 mA		8.8	10	
Discovery current limit	P = N = 48 V	3	4	5	mA
Auto-mode discovery resistance acceptance Band		19		26.5	kΩ
Auto-mode discovery resistance low end rejection		0		15	
Auto-mode discovery resistance high end rejection		33			
Discovery1,2 A/D conversion scale factor	100 μA < I_{PORT} < 3 mA	5.30	6.10	6.75	count/μA
Discovery1,2 A/D conversion time	I_{PORT}= 120 μA		18	22	ms

ELECTRICAL CHARACTERISTICS:

V48 = 48 V, R_T = 124 kΩ, C_T = 220 pf, C_{INT} = 0.027 µF (low leakage), −40°C to −125°C and $T_A = T_j$ (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Port Classification					
Classification voltage loop control	100 µA < I_{PORT} < 50 mA	15	17.5	20	V
Classification current limit	P = N = 48 V	50	60	100	mA
Class 0 to 1 detection threshold		5.5	6.5	7.5	
Class 1 to 2 detection threshold		13	14.5	16	
Class 2 to 3 detection threshold		21	23	25	
Class 3 to 4 detection threshold		31	33	35	
Class 4 to 0 detection threshold		45	48	51	
Classification A/D conversion scale factor		375	424	475	Count/ mA
Classification A/D conversion time	I_{PORT} = 50 mA		18	22	ms
Port Legacy Detection					
Legacy current limit	P = N = 48 V	2.6	3.5	4.3	mA
Legacy voltage A/D conversion scale factor	100 mV < V_{PORT} < 17.5 V	1365	1400	1445	Count/V
Legacy A/D conversion time	0 V < V_{PORT} < 15 V		18	22	ms
Port Powered Mode					
Port on resistance	20 mA < I_{PORT} < 300 mA		1.3		Ω
Over current threshold	R_{BIAS} = 124 kΩ, C_T = 200 pF Time > 75 ms, −25 ≤ T_j ≤ 105	350	375	400	mA
Output current limit	R_{BIAS} = 124 kΩ, C_T = 200 pF Time > 75 ms, −25 ≤ T_j ≤ 105		425	450	
Average min current trip	R_{BIAS} = 124 kΩ, C_T = 200 pF Current pulse > 100 ms		7.5	10	
Port output UV		42.0	42.7	44.0	V
Port output OV		54	55	56	
Over current time Limit	R_{BIAS} = 124 kΩ, C_T = 200 pF	50		75	ms
Short circuit time Limit	R_{BIAS} = 124 kΩ, C_T = 200 pF	50		75	
Turn−off delay from UV/OV faults	R_{BIAS} = 124 kΩ, C_T = 200 pF After port enabled and ramped up		3		
Port current A/D conversion scale factor	20 mA < I_{PORT} I < 300 mA	31	36.41	40	Count/ mA
Port current A/D conversion time	I_{PORT} < 300mA		18	22	ms
Port voltage A/D conversion scale factor	45 V < V_{PORT} < 56 V	335	353	370	Count/V
Port voltage A/D conversion time	45 V < V_{PORT} < 56 V		18	22	ms
Port temperature A/D conversion scale factor			300		Count/ °C

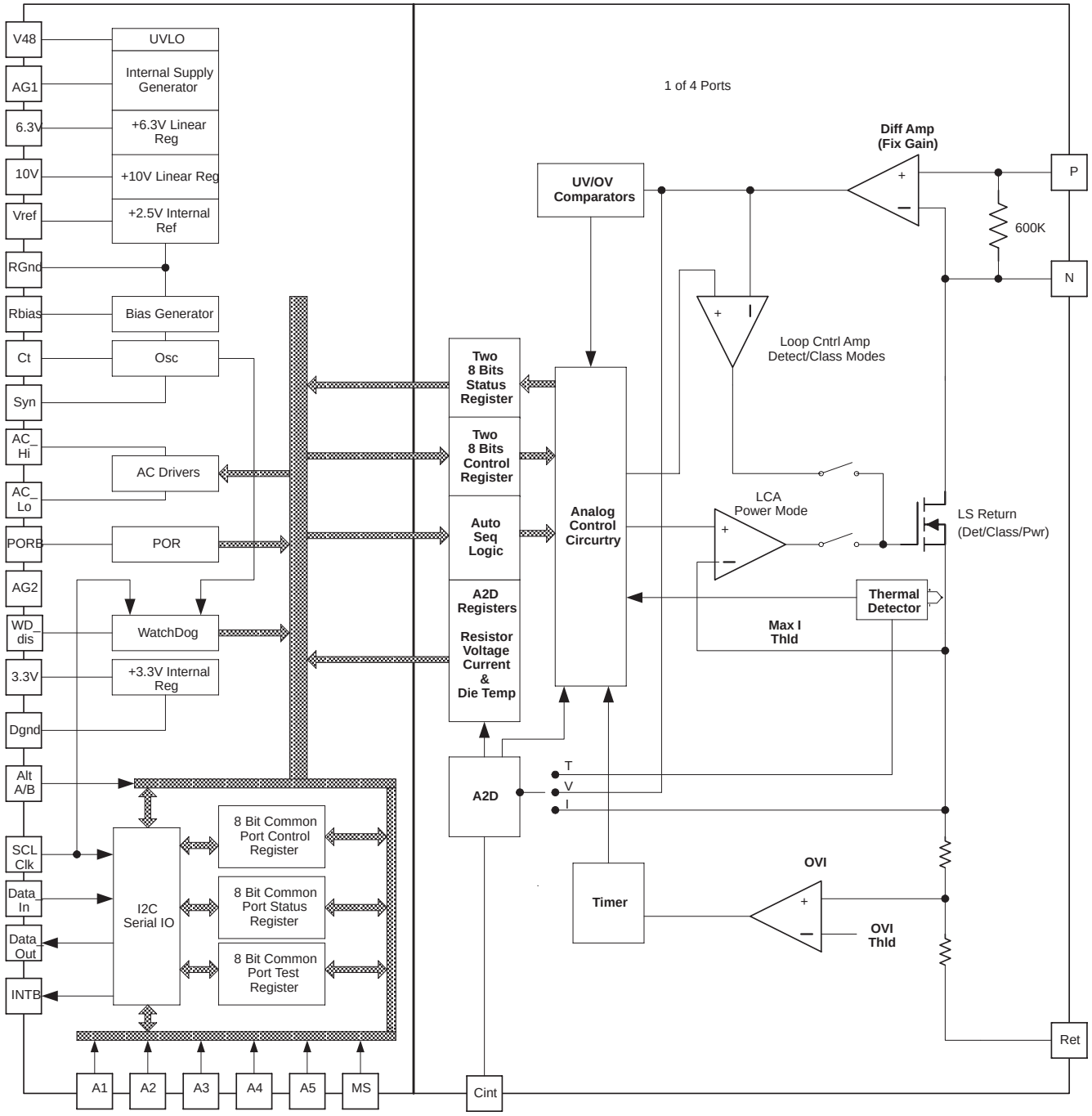
ELECTRICAL CHARACTERISTICS:

V48 = 48 V, R_T = 124 kΩ, C_T = 220 pf, C_{INT} = 0.027 μF (low leakage), −40°C to −125°C and $T_A = T_j$ (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Port Disable Mode					
Port N voltage	P = 48 V	47			V
AC Low & AC High Specification					
AC_lo, AC_hi − low output voltage		0		0.5	V
AC_lo − high output voltage		3.0		5.0	
AC_hi − high output voltage		5.0		7.0	
Digital I^2C DC Specifications					
SCL, SDA_I, A1−A5 ,WD_DIS, ALTA/B, MS, PORB logic input threshold			1.5		V
SCL, SDA_I input hysteresis			250		mV
MS, PORB input hysteresis			150		
WD_DIS,ALT A/B, MS, PORB input pull-down resistance	Input voltage 0.5 to 3 V		50		kΩ
A1−A5 pull-down current			10		μA
SDA_O logic high leakage	Drain = 5 V		100		nA
SDA_O logic low	I_{SINK} = 10 mA		200		mV
INTB logic high leakage	Drain = 6 V		10		μA
INTB logic low	I_{SINK} = 10 mA		200		mV
Digital I^2C Timing					
SCL clock frequency		0		400	kHz
Pulse duration	SCL high	0.6			μs
Pulse duration	SCL low	1.3			
Rise time, SCL toSDA				300	
Fall time, SCL to SDA				300	
Setup time, SDA to SCL		250			
Hold time, SCL to SDA		300		900	
Bus free time between start and stop		1.3			
Setup time, SCL to Start condition		0.6			
Hold time, start condition to SCL		0.6			
Setup time, SCL to stop condition		0.6			

NOTES: 1. Probe test only. TPx numbers are internal device test points only available at wafer probe
2. Ensured by design. Not 100% tested in production.

TPS2384 SINGLE PORT BLOCK DIAGRAM



TERMINAL FUNCTIONS

Power and Ground

Pin Name	Pin #	I/O	Description
V48	60	I	48-V input to the device. This supply can have a range of 44 to 57 V. This pin should be de-coupled with a 0.1-μF capacitor from V48 to AG1 placed as close to the device as possible.
V10	58	O	10-V analog supply. The 10-V reference is generated internally and connects to the main internal analog power bus. A 0.1-μF de-coupling capacitor should terminate as close to this node and the AG1 pin as possible. Do not use for an external supply.
V6.3	59	O	6.3-V analog supply. A 0.1-μF de-coupling capacitor should terminate as close to this pin and the AG1 pin as possible. Do not use for an external supply.
V3.3	24	O	3.3-V logic supply. The 3.3-V supply is generated internally and connects to the internal logic power bus. A 0.1-μF de-coupling capacitor should terminate as close to this node and the DG pin as possible. This output can be used as a low current supply to external logic.
V2.5	54	O	2.5-V reference supply. The V2.5 is generated internally and connects to the internal reference power bus. This pin should not be tied to any external supplies. A 0.1-μF de-coupling capacitor should terminate as close to this node and the RG pin as possible. Do not use for an external supply.
AG1	57	GND	Analog ground 1. This is the analog ground of the V6.3, V10 and V48 power systems. It should be externally tied to the common copper 48-V return plane. This pin should carry the low side of three de-coupling capacitors tied to V48, V10 and V6.3.
AG2	61	GND	Analog ground 2. This is the analog ground which ties to the substrate and ESD structures of the device. It should be externally tied to the common copper 48-V return plane. AG1 and AG2 must be tied together directly for the best noise immunity.
DG	23	GND	Digital ground. This pin connects to the internal logic ground bus. It should be externally tied to the common copper 48-V return plane.
RG	56	GND	Reference ground. This is a precision sense of the external ground plane. The integration capacitor (CINT#) and the biasing resistor (RBIAS pin) should be tied to this ground. This ground should also be used to form a printed wiring board ground guard ring around the active node of the integration capacitor (CINT#). It should tie to common copper 48-V return plane.

Port Analog Signal

Pin Name	Pin #	I/O	Description
P1	7	I	Port Positive. 48-V load sense pin. Terminal voltage is monitored and controlled differentially with respect to each Port N pin. Optionally, if the application warrants, this high side path can be protected with the use of a self−resetting poly fuse.
P2	10	I	
P3	39	I	
P4	42	I	
N1	6	I	Port negative. 48-V load return pin. The low side of the load is switched and protected by internal circuitry that will limit the current.
N2	11	I	
N3	38	I	
N4	43	I	
Ret1	5	I	48-V return pin
Ret2	12	I	
Ret3	37	I	
Ret4	44	I	
Cint1	4	I	Integration capacitor. This capacitor is used for the ramp A/D converter signal integration. Connect a 0.027-μF capacitor from this pin to #RG. To minimize errors use a polycarbonate, polypropylene, polystyrene or teflon capacitor type to prevent leakage. Other types of capacitors can be used with increased conversion error.
Cint2	13	I	
Cint3	36	I	
Cint4	45	I	

TERMINAL FUNCTIONS

Analog Signals

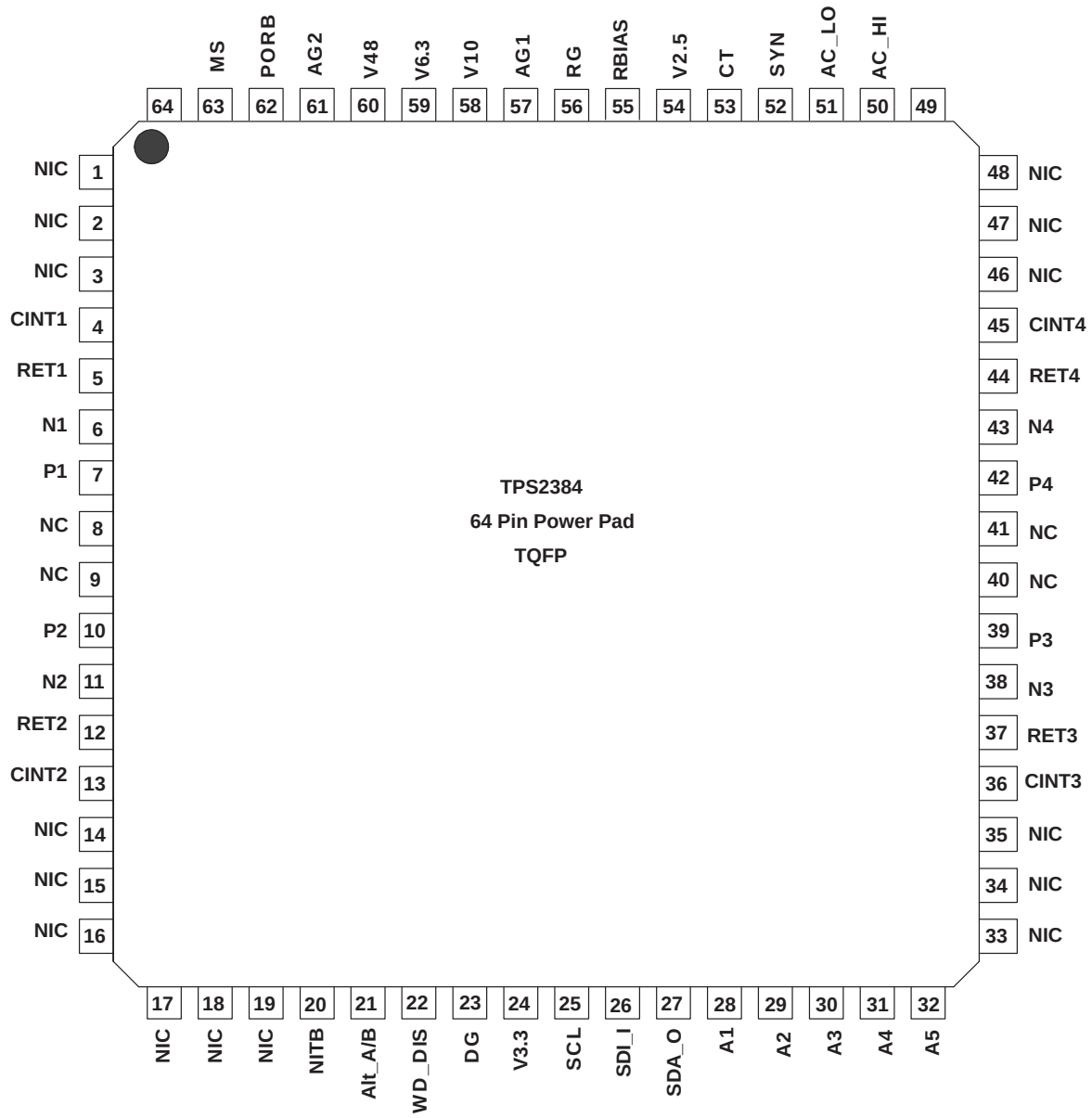
Pin Name	Pin #	I/O	Description
CT	53	I	This is a dual-purpose pin. When tied to an external capacitor this pin sets the internal clock. When the CT pin is grounded the SYN pin turns from a output to an input (see SYN pin description) The timing capacitor and the resistor on the RBIAS pin sets the internal clock frequency of the device. This internal clock is used for the internal state machine, integrating A/D counters, POR time out, faults and delay timers of each port. Using a 220-pF capacitor for CT and a 124-kΩ resistor for RBIAS sets the internal clock to 245 kHz and ensure IEEE 802.3af compliance along with maximizing the rejection of 60-Hz line frequency noise from A/D measurements.
RBIAS	55	I	Bias set resistor. This resistor sets all precision bias currents within the chip. This pin will regulate to 1.25V (V2.5/2) when a resistor is connected between RBIAS and RG. This voltage and RBIAS generates a current which is replicated and used throughout the chip. This resistor also works in conjunction with the capacitors on CT and CINT to set internal timing values. The RBIAS resistor should be connected to RG. RBIAS is a high impedance input and care needs to be taken to avoid signal injection from the SYN pin or I^2C signals.
SYN	52	I/O	This is a dual purpose pin. When the CT pin is connected to a timing capacitor this output pin is a 0 to 3.3 V pulse of the internal clock which can be used to drive other TPS2384 SYN pins for elimination of a timing capacitor. When the CT pin is grounded this pin becomes an input pin that can be driven from a master TPS2384 or any other clock generate signal.
AC_LO	51	O	Open drain output pin for AC disconnect excitation
AC_HI	50	O	Totem poll output pin for AC disconnect excitation.

Digital Signals

Pin Name	Pin #	I/O	Description
SCL	25	I	Serial clock input pin for the I^2C interface.
SDA_I	26	I	Serial data input pin for the I^2C interface. When tied to the SDA_O pin, this connection becomes the standard bi-directional serial data line (SDA)
SDA_O	27	O	Serial data open drain output for the I^2C interface. When tied to the SDA_I pin, this connection becomes the standard bi-directional serial data line (SDA). This is a open drain output that can drive opto-coupler LEDs directly from the 48-V bus with an external, series current limiting resistor.
WD_DIS	22	I	The WD_DIS pin disables the watchdog timer function when connected to 3.3 V. The pin has internal 50-kΩ resistor to digital ground. The watchdog timer monitors the I^2C clock pin (SCL) and the internal oscillator activity in power management mode and only the internal oscillator activity in auto mode.
INTB	20	O	This is an open-drain output that goes low if a fault condition occurs on any of the 4 ports.
ALT A/B	21	I	When this input is set to logic low there is no back-off time after a discovery failure. When this pin set to a logic high there is a back-off time (approximately 2 seconds) before initiating another discovery cycle. This pin has an internal 50-kΩ resistor pull-down to digital ground.
A1	28	I	Address 1 through 5. This is the I^2C address select input. Select the appropriate binary address on these pins by connecting this pin to chip ground for a logic low and tying this pin to the V3.3 pin for a logic high. Each address line has an internal current source pull-down to digital ground.
A2	29	I	
A3	30	I	
A4	31	I	
A5	32	I	
MS	63	I	The MS pin selects either the auto mode (MS Low) or the power management mode, PMM, (MS High). This pin can be held low for controller-less standalone applications. When MS is Low and the POR timing cycle is complete the chip will sequentially *Discover, Classify* and *Power on* each port. When MS is set high the ports are controlled by register setting via the I^2C bus. The MS pin has an internal 50-kΩ resistor pull-down to analog ground.
PORB		I	This pin can be used to override the internal POR. When held low, the I^2C interface, all the state machines, and registers are held in reset. When all internal and external supplies are within specification, and this pin is set to a logic high level, the POR delay will begin. The I^2C interface and registers will become active within 70 μs of this event and communications to read or preset registers can begin. The reset delay for the remainder of the chip then extinguishes in 1 second. This pin has an internal 50-kΩ resistor pull-down to analog ground.

CONNECTION DIAGRAM

TQFP PACKAGE (TQFP−64)(1)(2)
(TOP VIEW)



NOTES: 1. NIC = No internal connection.
2. NIC pins can be tied to the ground plane for improved thermal characteristics and to prevent noise injection from unused pins.

AUTO MODE FUNCTIONAL DESCRIPTION

Auto Mode

Auto mode (AM, MS = 0) operation is the basic approach for applying power to IEEE compliant PD's. When AM has been selected the TPS2384 automatically performs the following functions;

- Discovery of IEEE 802.3af compliant power devices (PD)
- Classification
- Power delivery
- Port over/under voltage detection
- Port over current detection (350 mA < I_{PORT} < 400 mA)
- Port maximum current limit (400 mA < I_{PORT} < 450 mA)
- DC disconnect (5 mA < I_{PORT}< 10 mA)
- Thermal shutdown protection (Tj > 150° C)
- Internal oscillator watch dog

In AM the contents of all read registers are available via the I^2C interface. In addition all control registers except for the function bits can be written. This supports a semi-auto mode where the TPS2384 auto detects compliant PD's while a host can access the A/D registers and class information and then implement power management (including turning a port off, responding to faults, etc).

The write registers that are still active in AM are;

- All ports disable – common write register 0001
- Over/Under Voltage Faults − common write register 0001
- Software reset − common write register 0001
- Disconnect disable – write register 0001
- Discovery fault disable – write register 0001
- Port enable – write register 0011
- Power mode class over current threshold enable − write register 0011

AUTO MODE FUNCTIONAL DESCRIPTION

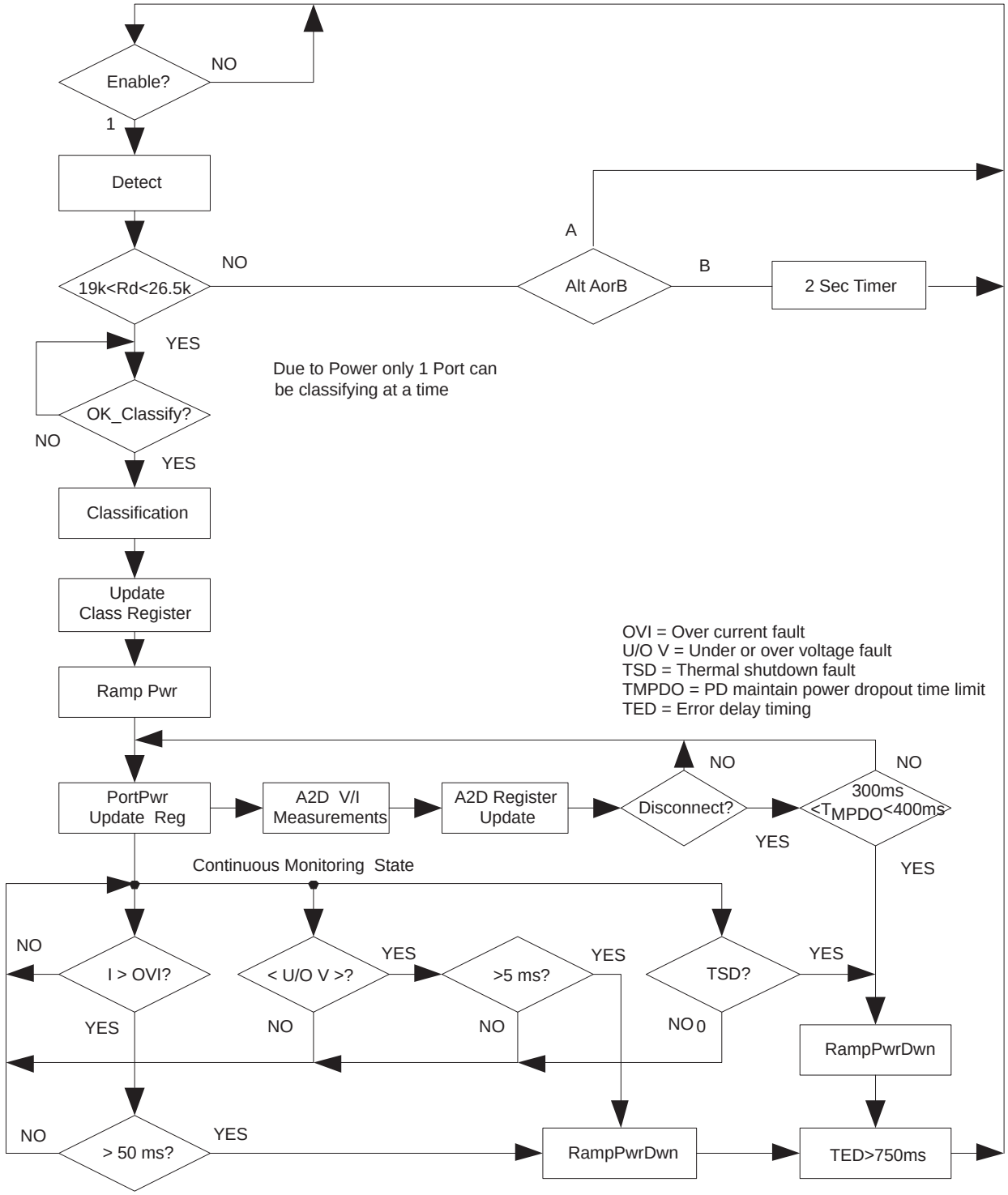


Figure 1. The Basic Flow for Auto Mode

AUTO MODE FUNCTIONAL DESCRIPTION

AM Discovery

The TPS2384 uses two low level probe signals (typically 4.4 V and 8.8 V) during the discovery process to determine whether a valid PD is present. The use of multi point detection method for the PD resistor measurement allows accurate detection even when series steering diodes are present. The low level probe voltages also prevent damage to non-802.3 devices. When a valid PD has been detected the TPS2384 moves to classification. If a valid PD has not been detected the TPS2384 continues to cycle through the discovery process. The waveform in Figure 2 shows typical N-pin waveforms for the discovery of a valid PD and the failure to discovery due to a discovery resistor of 15 kΩ and 33 kΩ.

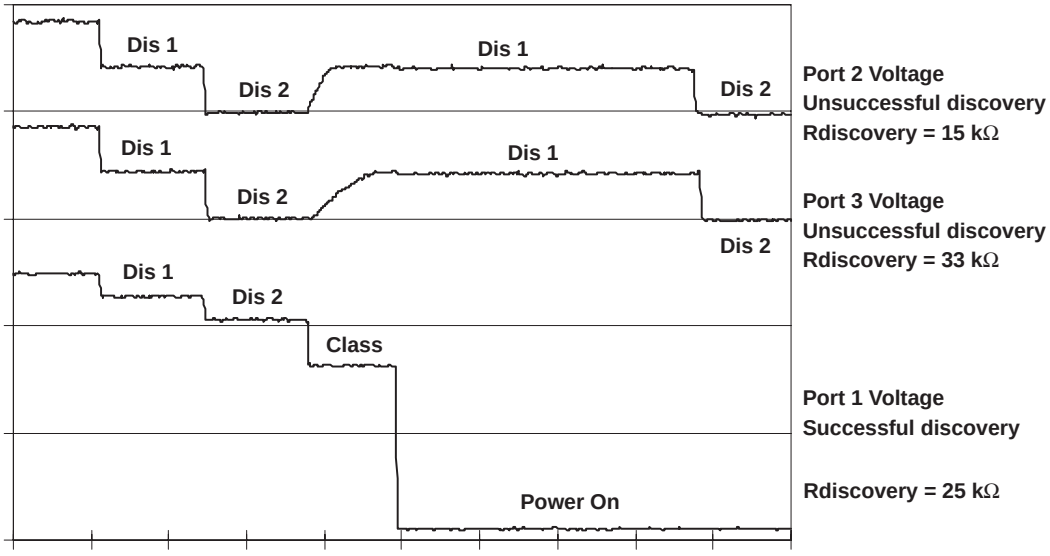


Figure 2.

AUTO MODE FUNCTIONAL DESCRIPTION

AM Classification

After a successful discovery of a valid PD the TPS2384 enters the classification function that identifies the power level based on the PD's current signature. The classification current level is measured at a reduced terminal voltage of 17.5 V and classified with 15 bits of resolution. During classification the power consumption can be at its highest so to prevent over temperature shutdown in auto mode only one port classifies at a time. When multi-ports successfully discovery and enter classification at the same time the auto sequencer processes each request separately allowing only one port to enter classification. Figure 3 shows all 4 ports successfully detecting a valid PD at the same time and than the classification of each port occurring separately.

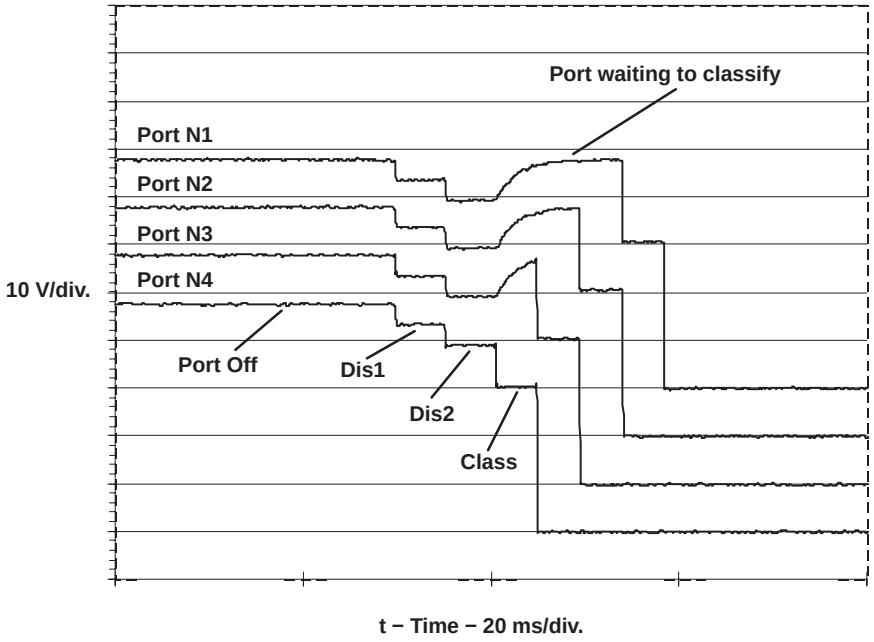


Figure 3.

AUTO MODE FUNCTIONAL DESCRIPTION

Upon completion of classification the port classification register is updated. In AM mode this information is not used but for semi-auto mode the class information can be used for power management and the over current threshold can be set to correspond to the PD's classification by setting Bit 7 in the individual port control register address 0011. The Figure 4 shows actual class currents and the class assignment which where stored in the register. These assignments are compliant with the IEEE 802.3af Standard

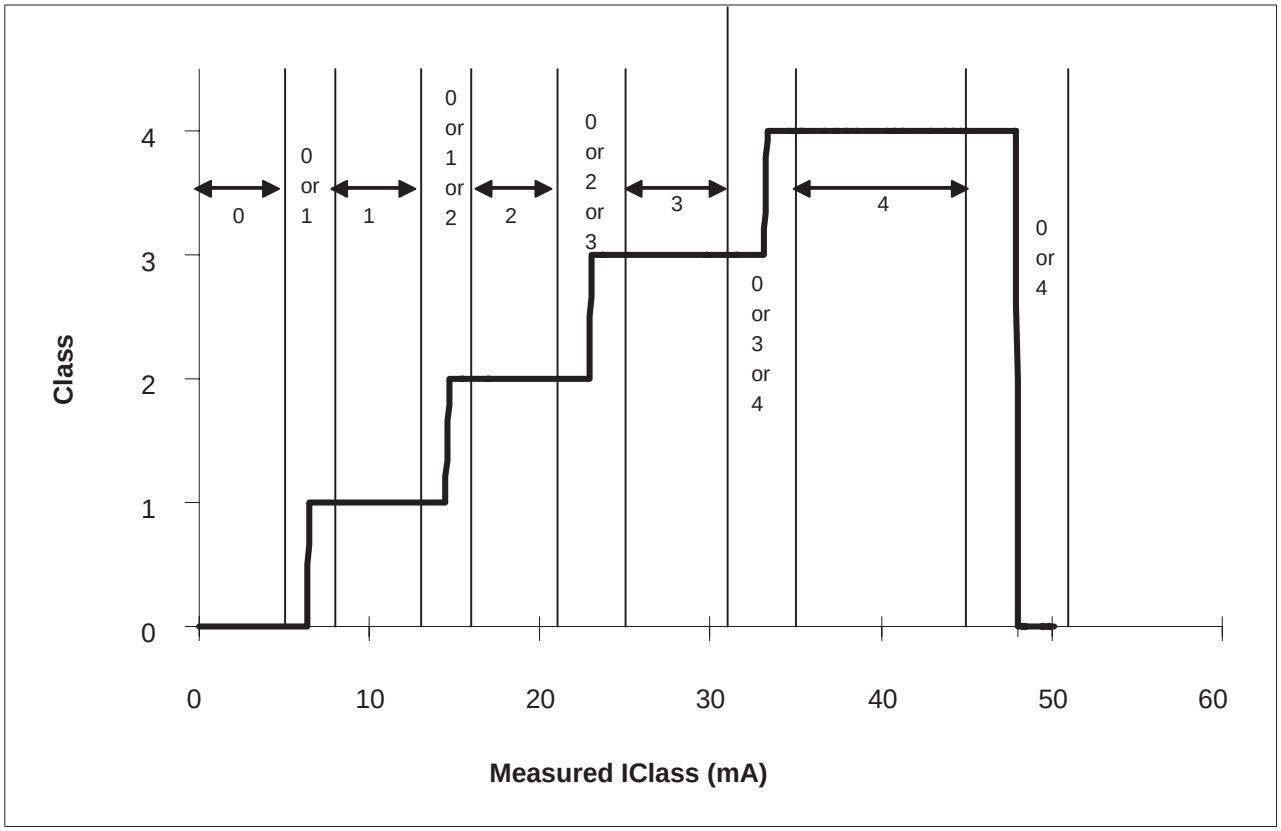


Figure 4.

AUTO MODE FUNCTIONAL DESCRIPTION

AM Power Delivery

After successfully discovery and classification of a valid PD the power is delivered by controlling the current to the PD until its current requirements are met or until the internal current limit is reached (approximately 425 mA). The power switch is fully enhanced after 500 μs. Figure 5 show the voltage and the current that is being applied to the PD during power-up and reaching the PD load of 250 mA.

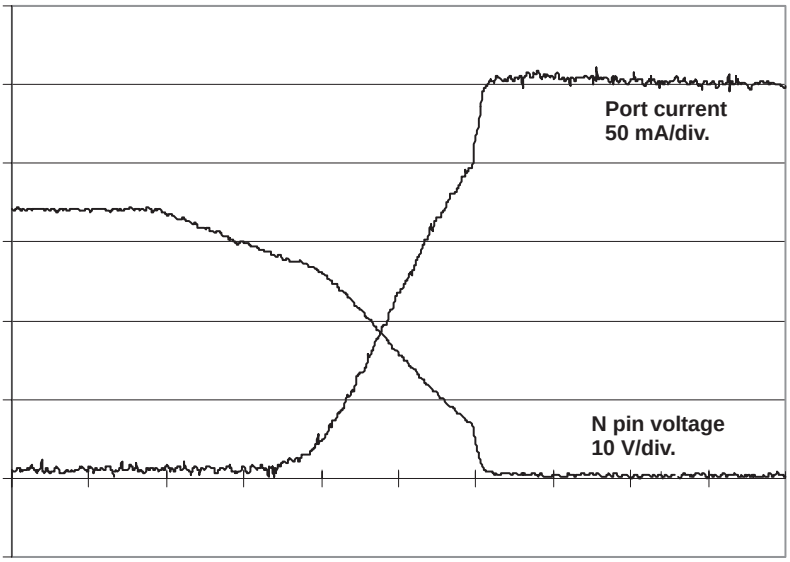


Figure 5.

After power has been applied to the PD the TPS2384 automatically enters the current and voltage sample mode. The sample mode performs 31 current measurements and a 1 voltage measurement. Each measurement takes approximately 18 ms to complete. The port remains powered and the current/voltage measurement cycle continues until a fault condition occurs. The current and voltage measurements are both stored in the A/D current and voltage registers and can be access through the I^2C pins. This allows power management in the AM if it is desired.

AUTO MODE FUNCTIONAL DESCRIPTION

AM Faults

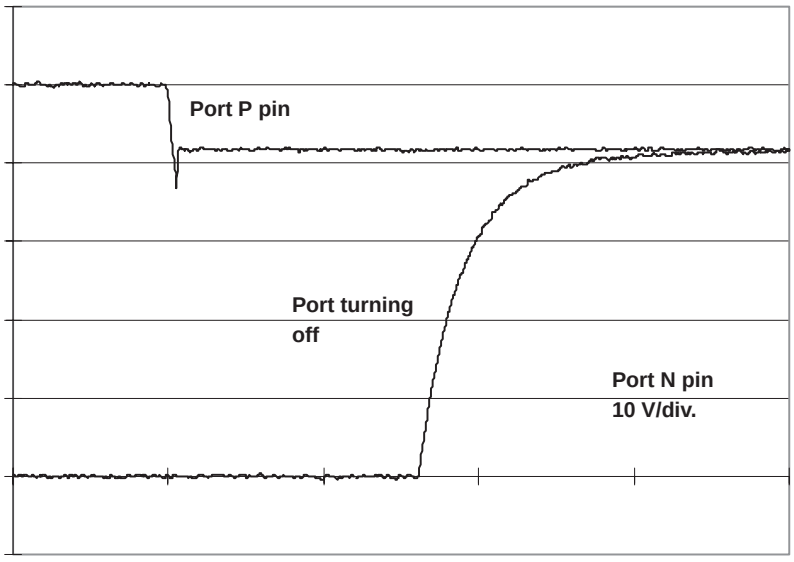
AM faults are;

- Under and over voltage faults
- Over current faults
- Under current (dc modulated) fault
- Thermal shutdown fault
- Watch dog oscillator fault

Any one of these faults will cause the port to shutdown.

Over/Under Voltage Fault

Over/under voltage faults are only processed after power up has completed. The TPS2384 measures the voltage between the P and N pin and if this voltage drops below the under voltage threshold (typical 43 V) or increases above the over voltage threshold (53 V) the voltage timer is turned on. When the voltage timer reaches its time out limit that is set between 2 ms to 5 ms the corresponding port will be turned off and the UV/OV fault bit is set in the port status register. If the over/under voltage condition goes away prior to the voltage timer reaching its limit the timer is reset and waits for the next event. Figure 6 shows a voltage fault lasting for more then 2 ms that has caused the port to shutdown.



t − Time − 2 ms/div.

Figure 6.

AUTO MODE FUNCTIONAL DESCRIPTION

Over Current or Current Limit Faults

Over current or current limit faults are conditions when the load current that is being sensed trips either the over current comparator (350 mA to 400 mA) or the max current comparator (400 mA to 450 mA) and turns on the over current timer. When the over current timer reaches its time out limit that is set between 50 ms to 80 ms the corresponding port is turned off and the over current bit is set in the port status register. If the over current condition goes away prior to the over current timer reaching its limit the timer is reset and waits for the next event. Figure 7 shows an over current fault lasting more than 50 ms that has caused the port to shut off.

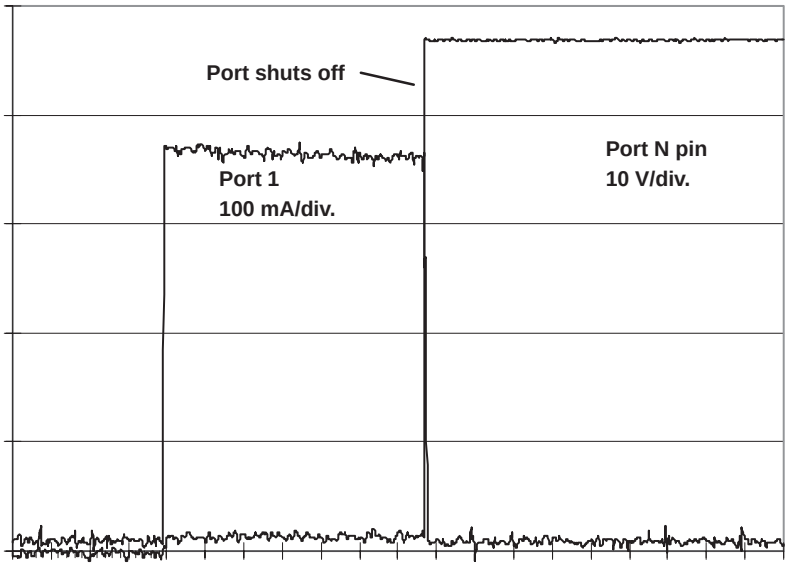


Figure 7.

Under Current Fault (DC Modulated Disconnect)

Under current fault (dc modulated disconnect) is a condition when the load current that is being measured drops below 7.5 mA and turns on the disconnect timer. If the disconnect timer reaches its time out limit that is set between 300 ms to 400 ms the corresponding port is turned off and the load disconnect bit is set in the port status register. If the under current condition goes away prior to the disconnect timer reaching its limit the timer is reset and the port remains powered.

AUTO MODE FUNCTIONAL DESCRIPTION

Figure 8 shows dc disconnect event. In this setup the load current was set right above the 7.5 mA threshold. The duty cycle of the load was then adjusted until the point within the disconnect window of 300 ms to 400 ms.

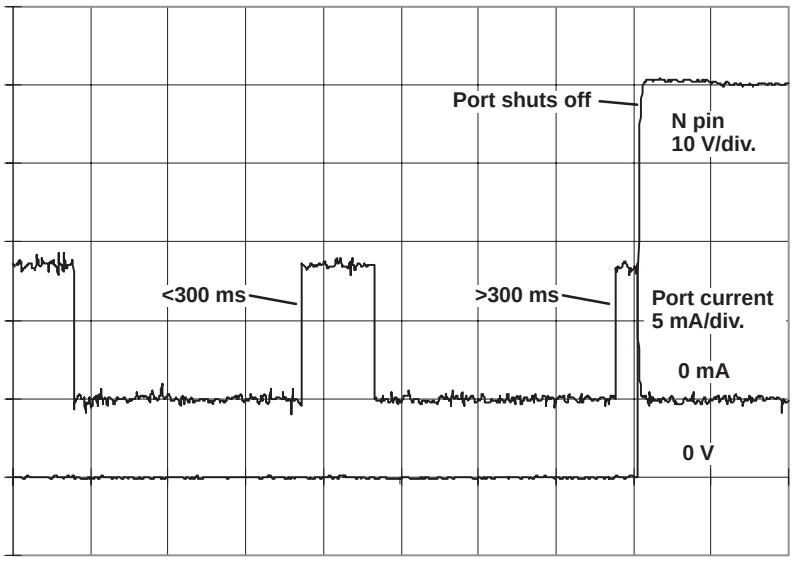


Figure 8.

POWER MANAGEMENT MODE FUNCTIONAL DESCRIPTION

Power Management Mode (PMM)

Power management mode (PMM) has been designed to work efficiently with simple low-cost micro controllers such as those in the MPS430 family.

The power management mode uses 13 self-contained functions to implement power management. You simply write/read through the I^2C pins and wait for the function done bit to be set. If an A/D measurement was performed during the function the results can be access by going to the read mode and addressing the proper register.

13 Functions

- **Disable:** Disable the port and reset all functions.
- **Discovery 1:** Enable the discovery 1 condition which applies a 4.4 V across the PD and measure and store the resulting current.
- **Discovery 2:** Enable the discovery 2 condition which applies a 8.8 V across the PD and measure and store the resulting current.
- **V Sample:** Measure the voltage between the P and N pins and store the result in the A/D voltage register.
- **Legacy:** Enable the 3.5-mA current source for measuring capacitance and measure the voltage across the P and N terminals and store the result in the A/D voltage register.
- **Classify:** Enable the classification condition which applies 17.7 V across the PD and measure and store the resulting current.
- **Rup Pwr:** Turn on the output switch while controlling the current being delivered to the PD until the PD current needs are met or the max current is reached.
- **C Sample:** Continuous cycle of 31 current measurements and 1 voltage measurement. After each measurement the contents for the appropriate register is updated.
- **Rdwn:** Turn off the output switch while controlling current until output current reaches 0 mA.
- **AC Low:** Turns on open drain output FET and measures voltage between P and N pin and store result in A/D voltage registers.
- **AC High:** Turns on high side output FET and measures voltage between P and N pin and store result in A/D voltage registers.
- **ISample:** Measure the current and store the result in the A/D current register.
- **TSample:** Measure the internal die temperature and store the result in the A/D temperature register.

POWER MANAGEMENT MODE FUNCTIONAL DESCRIPTION

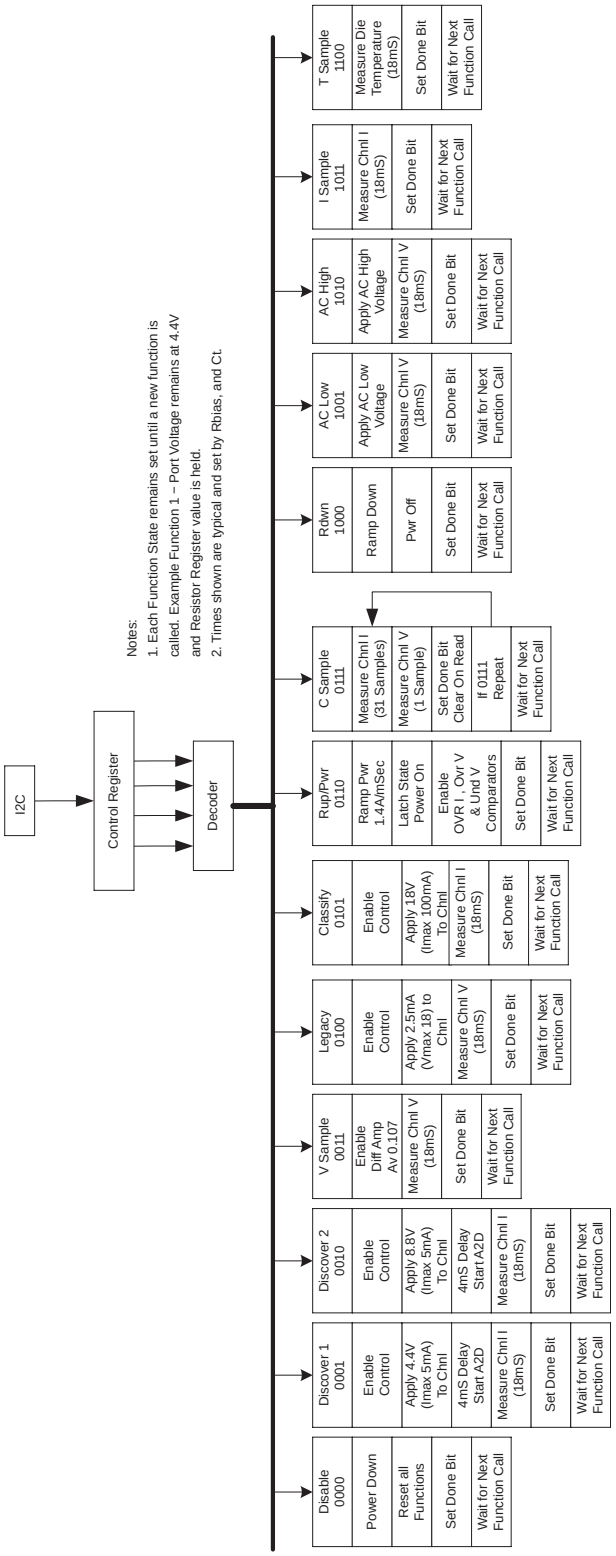


Figure 9.

POWER MANAGEMENT MODE FUNCTIONAL DESCRIPTION

PMM Discovery 1

PMM discovery 1 function waveforms for the N and CINT pins are shown in Figure 10. The measurement is being performed using 25 kΩ impedance between the P and N pin. The discovery 1 voltage is allowed to settle for approximately 5 ms before the A/D begins integrating. The voltage on the CINT pin shows the A/D cycle. There are 4 distinct regions to any A/D cycle: pre-charge (to a known starting voltage), charge, coarse discharge, and fine discharge. CINT pin is very high impedance therefore extreme care must be taken to avoid any noise or leakage affecting this pin. For the measurements where CINT voltage is shown a buffer was used to prevent performance degradation. The A/D measurement time is approximately 18 ms. The entire discovery 1 function takes approximately 22 ms to complete. The function remains set and the data in the register remains until another function is called. At the end of the fine discharge ramp the data is stored in the resistor register and the done bit is set.

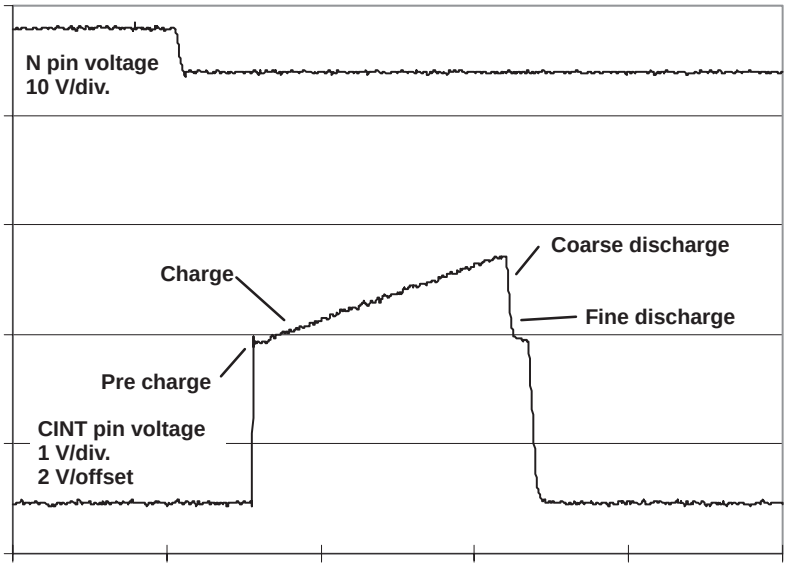


Figure 10.

POWER MANAGEMENT MODE FUNCTIONAL DESCRIPTION

PMM Discovery 2

PMM discovery 2 function waveforms for the N and CINT pins are shown in Figure 11. Again the measurement is being performed using 25 kΩ impedance between the P and N pin. The discovery 2 function was call after a discovery 1 function so the voltage ramps from 4.4 V to 8.8 V below the P pin. The discovery 2 voltage is given 5 ms to settle before the A/D begins to integrate. At the end of the fine discharge ramp the data is stored in the resistor register and the done bit is set.

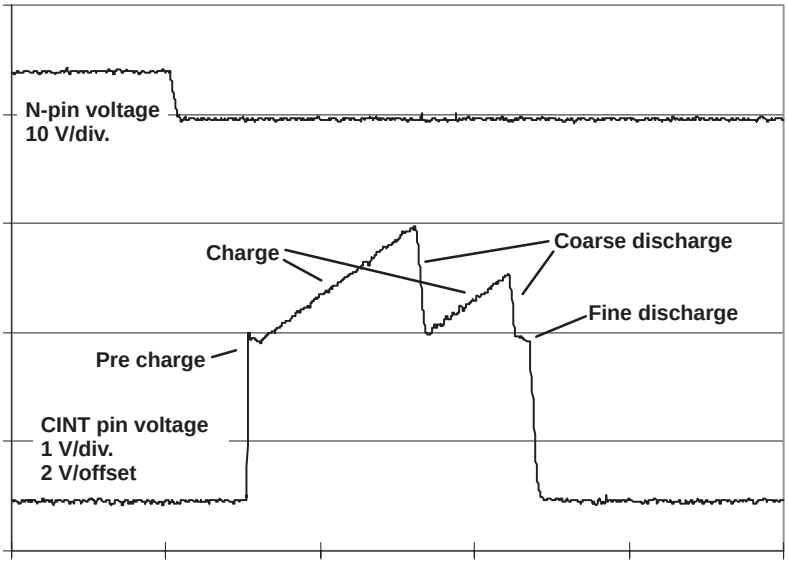


Figure 11.

POWER MANAGEMENT MODE FUNCTIONAL DESCRIPTION

PMM Classification

PMM classification function looks similar to discovery 1 and 2 except that the voltage between the P and N pins regulates to approximately 17.5 V.

PMM Legacy

PMM legacy function is used to detect PDs that are non compliant. Legacy detection uses a current source (typically 3.5 mA) as a test current while the A/D measures the average voltage for approximately 18 ms. The waveform shown in Figure 12 is the legacy function charging a 10-µF capacitor. The capacitance charges to a value that is no greater than 20 V below the P port voltage. As the capacitor is charging the A/D is accumulating counts in the voltage A/D register. Figure 13 shows the relationship between port capacitance and the number of counts. A user can characterize non-compliant PD's signatures and use the legacy function to power these devices.

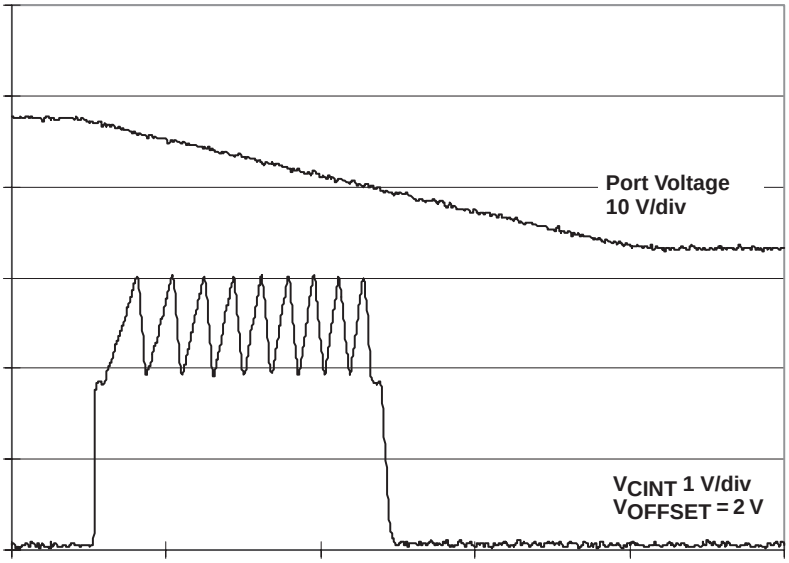


Figure 12.

POWER MANAGEMENT MODE FUNCTIONAL DESCRIPTION

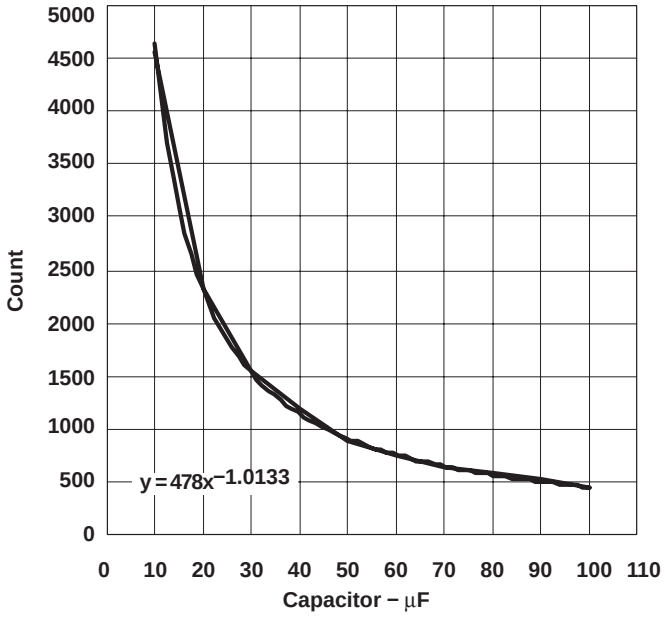


Figure 13.

PMM Rup Pwr

PMM R_{UP} power function turns on the port power by ramping up the current that is being delivered to the load in a controlled fashion. The output current ramps from 0 mA to I_{MAX} (typically 425 mA) in approximately 500 µs. Figure 14 shows the output voltage and current turning on for a 250-mA load.

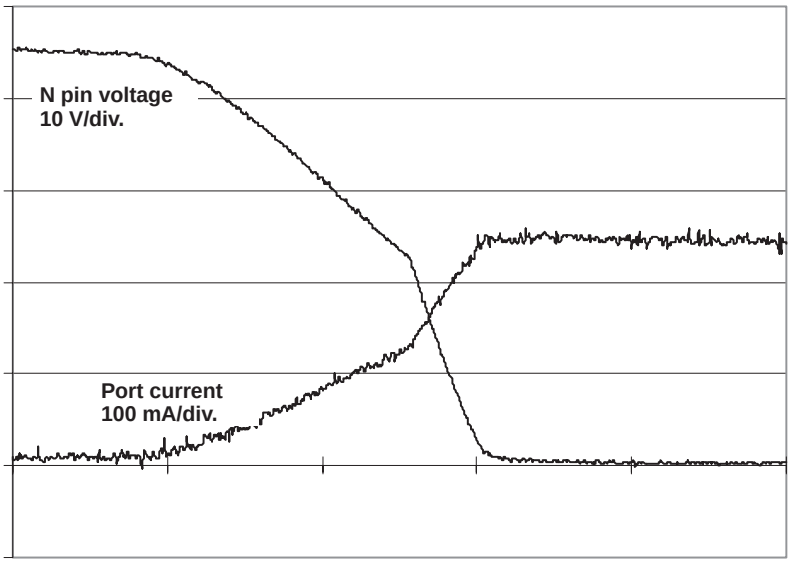


Figure 14.

POWER MANAGEMENT MODE FUNCTIONAL DESCRIPTION

PMM R_{DWN}

PMM R_{DWN} function turns off the port power by ramping down the current in a controlled fashion. The output current ramps from I_{MAX} (typically 425 mA) to 0 mA in approximately 500 μs. Figure 15 shows the output voltage and current shutting down for a 250-mA load.

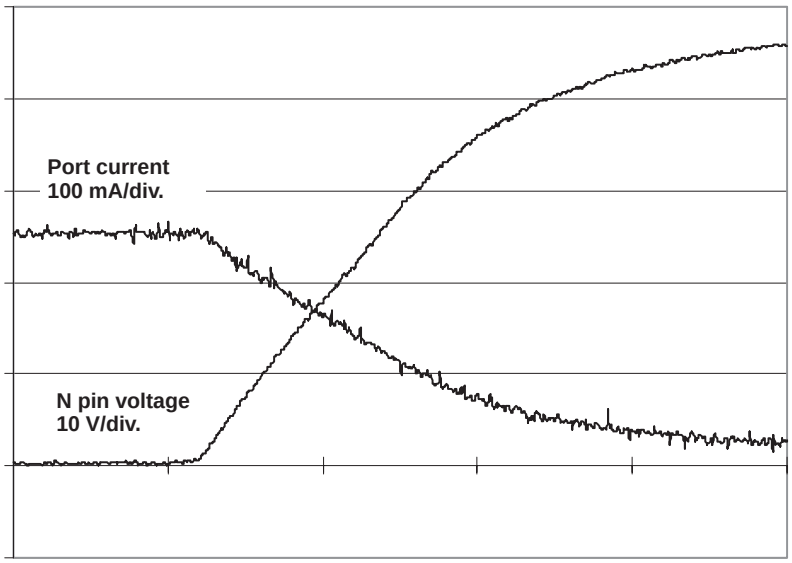


Figure 15.

MISCELLANEOUS FUNCTIONAL DESCRIPTION

Watch Dog Timer

TPS2384 has two watchdog timers. One monitors the I^2C clock and the other monitors the internal clock. When auto mode is selected and the watchdog timer has not been disable only the internal clock is monitored. When in power management mode and the watchdog timer has not been disabled then both the I^2C and internal clocks are monitored. If there is no I^2C clock activity for approximately 2 seconds then all ports are disable. There are three means to enable ports after a I^2C clock fault and they are:

1. Hard power reset
2. PORB pulse
3. Writing a software reset to the common control register.

In both auto mode and power management mode if the internal oscillator is lost for more than 20 ms all ports are disabled.

Loss of these signals is considered catastrophe since the system loses its ability to talk to each port. Therefore the WD timers disabling all ports protects the system from potential catastrophe failures.

This function can be easily over ridden by setting the WD_DIS pin high.

MISCELLANEOUS FUNCTIONAL DESCRIPTION

I²C Interface Description

The serial interface used in the TPS2384 is a standard 2-wire I²C slave architecture. The standard bi-directional SDA lines of the I²C architecture are broken out into independent input and output data paths. This feature simplifies earth grounded controller applications that require opto-isolators to keep the 48-V return of the Ethernet power system floating. For applications where opto-isolation is not required, the bi-directional property of the SDA line can be restored by connecting SDA_I to SDA_O. The SCL line is a unidirectional input only line as the TPS2384 is always accessed as a slave device and it never masters the bus.

Data transfers that require a data-flow reversal on the SDA line are 4-byte operations. This occurs during a TPS2384 port read cycle where a slave address byte is sent, followed by a port/register address byte write. A second slave address byte is sent followed by the data byte read using the port/register setup from the second byte in the sequence.

The I²C interface and the port read write registers are held in active reset until all input voltages are within specifications (V10, V6.3, V3.3 & V2.5) and the internal POR timer has timed out (see electrical specifications).

The I²C read cycle consists of the following steps 1 through 14 and is shown in Figure 20:

1. Start Sequence (S)
2. Device address field
3. Write
4. Acknowledge
5. Register/Port address
6. Acknowledge
7. Stop
8. Start
9. Device address field
10. Read
11. Aknowledge
12. Data Transfer
13. Acknowledge
14. Stop

MISCELLANEOUS FUNCTIONAL DESCRIPTION

Data write transfers to the TPS2384 do not require a data-flow reversal and as such only a 3-byte operation is required. The sequence in this case would be to send a slave device address byte, followed by a write of the port/register address followed by a write of the data byte for the addressed port.

The I^2C write cycle consists of the following steps 1 through 9 and is also shown in Figure 20:

1. Start Sequence (S)
2. Device address field
3. Write
4. Acknowledge
5. Register/Port address
6. Acknowledge
7. Data for TPS2384
8. Acknowledge
9. Stop

Start/Stop

The high-to-low transition of SDA while SCL is high defines the start condition. The low to high transition of SDA while SCL is high defines the stop condition. The master device initiates all start and stop conditions.

A first serial packet enclosed within start and stop bits, consists of a 7-bit address field, read/write bit, and the acknowledge bit. The acknowledge bit is always generated by the device receiving the address or data field. Five of the seven address bits are used by the TPS2384. The sixth and seventh bits are placeholders for future expansion. During a write operation to the TPS2384 from the master device, the data field is 8 bits long. During a read operation where the TPS2384 is writing to the master device, the data field is also 8 bits long.

MISCELLANEOUS FUNCTIONAL DESCRIPTION

Chip Address

The address field of the TPS2384 is 8 bits long and contains 5 bits of device address select and a read/write bit as and two spare bits per Table 1. The leading two bits are not used and are reserved for future port expansion. The five device address select bits follow this plan. These bits are compared against the hard-wired state of the corresponding device address select pins (A1−A5). When the field contents are equivalent to the pin logic states, the device is addressed. These bits are followed by LSB bit, which is used to set the read or write condition (1 for read and 0 for write). Following a start condition and an address field, the TPS2384 responds with an acknowledge by pulling the SDA line low during the 9th clock cycle if the address field is equivalent to the value programmed by the pins. The SDA line remains a stable low while the 9th clock pulse is high.

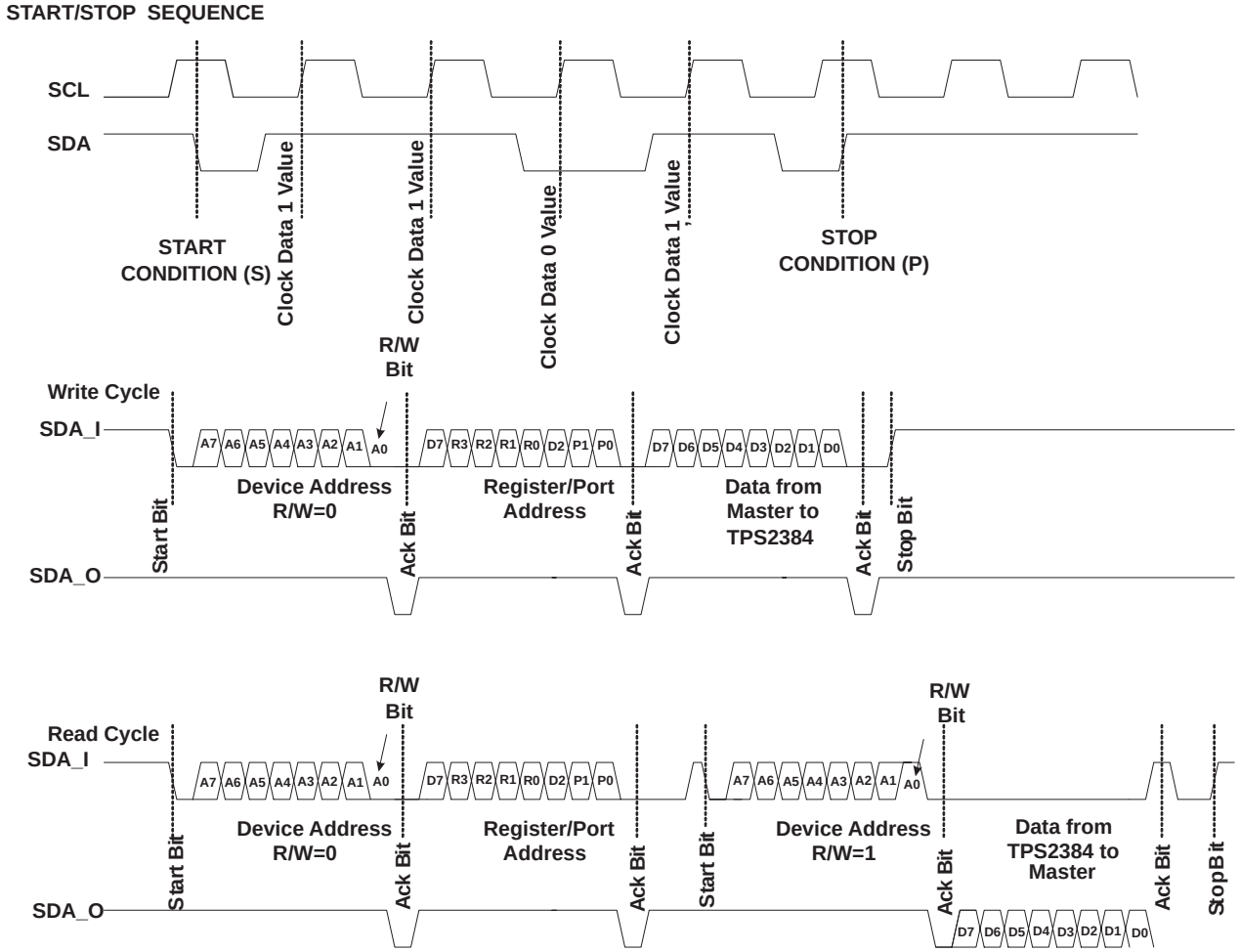


Figure 16. I^{2}C Read/Write Cycles

MISCELLANEOUS FUNCTIONAL DESCRIPTION

Chip Addressing

Table 1 shows the bit assignments during the addressing cycle.

Table 1. Address Selection Field

BIT	FUNCTION
A7	Future expansion (not used)
A6	Future expansion (not used)
A5	Device address. Compared with pin A5
A4	Device address. Compared with pin A4
A3	Device address. Compared with pin A3
A2	Device address. Compared with pin A2
A1	Device address LSB. Compared with pin A1
A0	Read/Write

Port/Register Cycle

After the chip address cycle, the TPS2384 accepts eight bits of port/register select data as defined in Table 2. The SCL line high-to-low transition after the eighth data bit then latches the selection of the appropriate internal register for the follow on data read or write operation. After latching the eight-bit data field, the TPS2384 pulls the SDA line low for one clock cycle, for the acknowledge pulse.

Data Write Cycle

For a data write sequence, after the Port/Register address cycle, the TPS2384 accepts the eight bits of data as defined in the tables below. The data is latched into the previously selected Write Register, and the TPS2384 generates a data acknowledge pulse by pulling the SDA line low for one clock cycle. Common register functions act on all ports simultaneously. Per port registers are specific to the target port only.

To reset the interface, the host or master subsequently generates a stop bit by releasing the SDA line during the clock-high portion of an SCL pulse.

Data Read Cycle

For a data read sequence, after the register acknowledge bit, the master device generates a stop condition. This is followed by a second start condition, and retransmitting the device address as described in chip address above. For this cycle, however, the R/W bit is set to a 1 to signal the read operation. The TPS2384 again responds with an acknowledge pulse. The address acknowledge is then followed by sequentially presenting each of the eight data bits on the SDA line (MSB first), to be read by the host device on the rising edges of SCL. After eight bits are transmitted, the host acknowledges by pulling the SDA line high for one clock pulse. The completed data transfer is terminated with the host generating a stop condition.

MISCELLANEOUS FUNCTIONAL DESCRIPTION

Table 2. Common Write Register Port /Register Addressing

BIT	FUNCTION	STATE	PRESET STATE
D7	Future expansion		0
D6	Register select MSB	0000 = common read − port fault status, ID and rev 0001 = common control write – software reset, ports shutdown and ac disc 0010 = write control reg 1 − function calls and discovery, disable fault disable 0011 = write control reg 2 – classify current limit, power over I cntrl & AD abort 0100 = read status reg 1 – fault status, class Infor, power Infor 0101 = read status reg 2 – detection status 0110 = read R result reg 1 – A/D resistor register (lower bits) 0111 = read R result reg 2 – A/D resistor register (upper bits) 1000 = read V result reg 1 – A/D voltage register (lower bits) 1001 = read V result reg 2 – A/D voltage register (upper bits) 1010 = read I result reg 1– A/D current register (lower bits) 1011 = read I result reg 2 – A/D current register (upper bits) 1100 = read T result reg 1 – A/D temperature register (lower bits) 1101 = read T result reg 2 – A/D temperature register (upper bits) 1110 = spare 1111 = common write – test disable timer, discovery loop	0000
D5	Register select Bit 3		
D4	Register select Bit 2		
D3	Register select LSB		
D2	Future expansion		0
D1	Port address MSB	00 = port 1 01 = port 2 10 = port 3 11 = port 4	00
D0	Port address		

Table 3. Common Register Read Register, Address = 0000 Port Fault Status &Chip ID/Rev

BIT	FUNCTION	STATE	PRESET STATE
D7	Port 4 general Fault status	0 = no fault 1 = port fault See Notes 1 and 2	0
D6	Port 3 general Fault status	0 = no fault 1 = port fault See Notes 1 and 2	0
D5	Port 2 general Fault status	0 = no fault 1 = port fault See Notes 1 and 2	0
D4	Port 1 general Fault status	0 = no fault 1 = port fault See Notes 1 and 2	0
D3	Chip rev	00 = rev − 01 = rev 1 10 = rev 2 11 = rev 3	00
D2			
D1	Chip ID	00 = TPS2383 01= TPS2383A 10 = TPS2384 11 = TPS2384A	10
D0			

NOTES: 1. PMM faults cleared by disable function.
2. AM faults cleared by TED timer.

MISCELLANEOUS FUNCTIONAL DESCRIPTION

Table 4. Common Register Write Register, Address = 1111 Test Register

BIT	FUNCTION	STATE	PRESET STATE
D7	Spare		0
D6	Thermal Shutdown Test	0 = normal operation 1 = force TSD condition (all ports off)	0
D5	POR disable	0 = normal POR timing 1 = force POR to a non-reset state	0
D4	Discovery timers	0 = normal (4-ms discovery 1 & discovery 2) 1 = timers disable	0
D3	Discovery 1 & 2	0 = normal operation 1 = all 4-port discovery 1 and discovery 2 − halt	0
D2	DC disconnect timer	0 = normal operation 1 = 300-ms disconnect timer disable	0
D1	TED timer	0 = normal operation 1 = 750-ms TED timer disable	0
D0	Spare		0

Table 5. Common Control RegisterWrite Register, address = 0001

BIT	FUNCTION	STATE	PRESET STATE
D7	Spare		0
D6	Spare		0
D5	TSD fault	0 = no fault 1 = faults disable	0
D4	AC high	0 = off 1 = AC_HI driver on	0
D3	AC low	0 = off 1 = AC_LO driver on	0
D2	Over/under voltage faults	0 = no fault 1 = faults disable	0
D1	All Ports Disable	0 = normal operation 1 = all ports shut down (no ramp)	0
D0	Software RESET	0 = normal operation 1 = reset all circuits and start a POR timing cycle	0

MISCELLANEOUS FUNCTIONAL DESCRIPTION

Table 6. Individual Port Write Control Register 1 Address 0010 (One Per Port)

Bit	FUNCTION	State	PRESET STATE
D7	Spare		0
D6	Spare		0
D5	Discovery Fault Disable	0 = normal mode 1 = disable internal discovery fault limits (19 kΩ to 29.5 kΩ)	0
D4	Disconnect Disable	0 = normal mode 1 = disable the effect of the logic signal from the disconnect detection circuits (used for test only)	0
D3	Function Bit 3	0000 = disable function (power down & reset all functions) 0001 = discovery 1 function 0010 = discovery 2 function 0011 = port voltage sample function (V sample) 0100 = legacy detection function 0101 = classification function 0110 = ramp up/power function (rup pwr) 0111 = continuous sample function (C sample) 1000 = ramp power down function (Rdwn) 1001 = ac low 1010 = ac high 1011 = port current sample function (I sample) 1100 = die temperature sample function (T sample) 1101 = spare 1110 = spare 1111 = spare	0000
D2	Function Bit 2		
D1	Function Bit 1		
D0	Function Bit 0		

Table 7. Individual Port Write Control 2 Write register, address = 0011 (One Per Port)

BIT	FUNCTION	STATE	PRESET STATE
D7	Spare		0
D6	Spare		0
D5	Spare		0
D4	Port Enable	0 = normal 1 = port disable	0
D3	A/D Start	0 = normal 1 = start A/D (self clearing)	0
D2	A/D Abort	0 = normal 1 = abort	0
D1	Power Mode Class Over Current Threshold Enable	0 = full current (375 mA) over current threshold 1 = deny current beyond class 1 (90 mA) or class 2 (160 mA) depending on class contents in register 4.	0
D0	Spare		0

MISCELLANEOUS FUNCTIONAL DESCRIPTION

Table 8. Port Status Port 1 through 4 Read Register, address = 0100 (One Per Port)

BIT	FUNCTION	STATE	PRESET STATE
D7	Discovery Status	0 = normal 1 = discovery fail	0
D6	Function Done Bit	0 = normal 1 = function complete (self clearing by new a function write)	0
D5	Port Class	000 = class 0 001 = class 1 010 = class 2 011 = class 3 100 = class 4	000
D4	Port Class		
D3	Port Class		
D2	Fault status (MSB)	000 = no faults 001 = UV/OV fault 010 = thermal fault 011 = overload current > 50-ms fault 100 = load disconnect 101 = reserved for future 110 = reserved for future 111 = reserved for future	000
D1	Fault status		
D0	Fault status (LSB)		

Table 9. Port Mode Status Port 1 through 4 Read Register, address = 0101 (One Per Port)

BIT	FUNCTION	STATE	PRESET STATE
D7	Spare		0
D6	Spare		0
D5	Spare		0
D4	Watch dog timer	0 = not active 1 = active	0
D3	A/D status	0 = not active 1 = active	0
D2	Detection status (MSB)	000 = disable 001 = searching 010 = power delivery 011 = fault 100 = test 101= other fault 110 = undefined 111 = undefined	000
D1	Detection status		
D0	Detection status (LSB)		

MISCELLANEOUS FUNCTIONAL DESCRIPTION

A/D Register (Resistance, Voltage, Current & Temperature)

Table 10. Analog to Digital Lower Bits Resistor Register / Read Register, Address = 0110 (One Per Port)

Bit	Function	State	PRESET STATE
D7	A/D bit 7	A/D lower bits	0
D6	A/D bit 6		
D5	A/D bit 5		
D4	A/D bit 4		
D3	A/D bit 3		
D2	A/D bit 2		
D1	A/D bit 1		
D0	A/D bit 0		

Table 11. Common Analog to Digital Upper Bits Resistor Register/Read Register, Address = 0111 (One Per Port)

Bit	Function	State	PRESET STATE
D7	Resistor measurement complete	0 = measurement active (bit set low at the start of discovery 1 or discovery 2) 1 = measurement complete (bit set high after A/D is completed during discovery 1 or discovery 2)	0
D6	A/D bit 14	A/D upper bits	0
D5	A/D bit 13		
D4	A/D bit 12		
D3	A/D bit 11		
D2	A/D bit 10		
D1	A/D bit 9		
D0	A/D bit 8		

MISCELLANEOUS FUNCTIONAL DESCRIPTION

Table 12. Analog to Digital Lower Bits Voltage Register/Read Register, Address = 1000 (One Per Port)

Bit	Function	State	PRESET STATE
D7	A/D bit 7	A/D lower bits	0
D6	A/D bit 6		
D5	A/D bit 5		
D4	A/D bit 4		
D3	A/D bit 3		
D2	A/D bit 2		
D1	A/D bit 1		
D0	A/D bit 0		

Table 13. Common Analog to Digital Upper Bits Voltage Register/Read Register, Address = 1001 (One Per Port)

BIT	FUNCTION	STATE	PRESET STATE
D7	Voltage measure complete	0 = measurement active (bit set low when A/D begins a voltage measurement) 1 = measurement complete (bit set high after A/D has completed a voltage measurement)	0
D6	A/D bit 14	A/D upper bits	0
D5	A/D bit 13		
D4	A/D bit 12		
D3	A/D bit 11		
D2	A/D bit 10		
D1	A/D bit 9		
D0	A/D bit 8		

MISCELLANEOUS FUNCTIONAL DESCRIPTION

Table 14. Analog to Digital Lower Bits Current Register/Read Register, Address = 1010 (One per port)

BIT	FUNCTION	STATE	PRESET STATE
D7	A/D bit 7	A/D lower bits	0
D6	A/D bit 6		
D5	A/D bit 5		
D4	A/D bit 4		
D3	A/D bit 3		
D2	A/D bit 2		
D1	A/D bit 1		
D0	A/D bit 0		

Table 15. Common Analog to Digital Upper Bits Current Register/Read Register, Address = 1011 (One Per Port)

BIT	FUNCTION	STATE	PRESET STATE
D7	Current Measure Complete	0 = measurement active (bit set low when A/D begins a current measurement) 1 = measurement complete (bit set high after A/D has completed a current measurement)	0
D6	A/D bit 14	A/D upper bits	0
D5	A/D bit 13		
D4	A/D bit 12		
D3	A/D bit 11		
D2	A/D bit 10		
D1	A/D bit 9		
D0	A/D bit 8		

MISCELLANEOUS FUNCTIONAL DESCRIPTION

Table 16. Analog to Digital Lower Bits Temperature Register/Read Register, Address = 1100 (One Per Port)

BIT	FUNCTION	STATE	PRESET STATE
D7	A/D bit 7	A/D lower bits	0
D6	A/D bit 6		
D5	A/D bit 5		
D4	A/D bit 4		
D3	A/D bit 3		
D2	A/D bit 2		
D1	A/D bit 1		
D0	A/D bit 0		

Table 17. Common Analog to Digital Upper Bits Temperature Register/Read Register, Address = 1101 (One Per Port)

BIT	FUNCTION	STATE	PRESET STATE
D7	Temperature Measure Complete	0 = measurement active (bit set low when A/D begins a temperature measurement) 1 = measurement complete (bit set high after A/D has completed a temperature measurement)	0
D6	A/D bit 14	A/D upper bits	0
D5	A/D bit 13		
D4	A/D bit 12		
D3	A/D bit 11		
D2	A/D bit 10		
D1	A/D bit 9		
D0	A/D bit 8		

TPS 2384 AC DRIVE APPLICATION SCHEMATIC

AC_Hi & Low W/O External FET Configurations

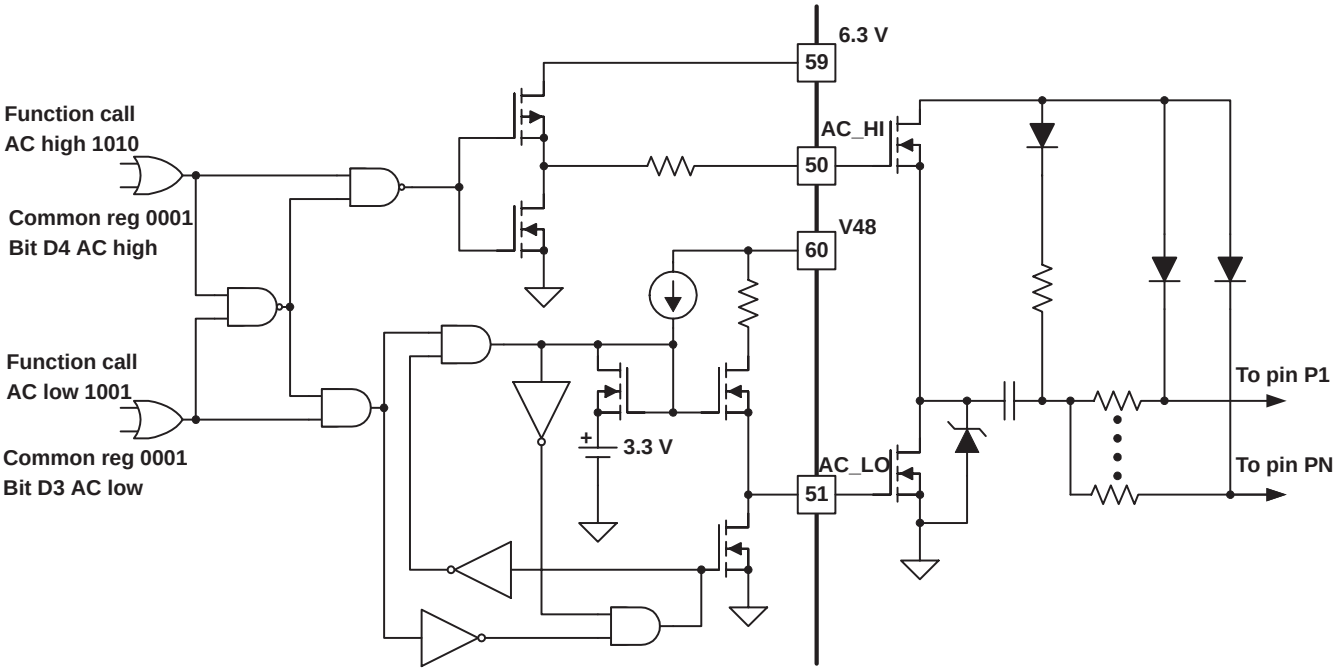


Figure 17.

TPS2384 SYSTEM BLOCK DIAGRAM

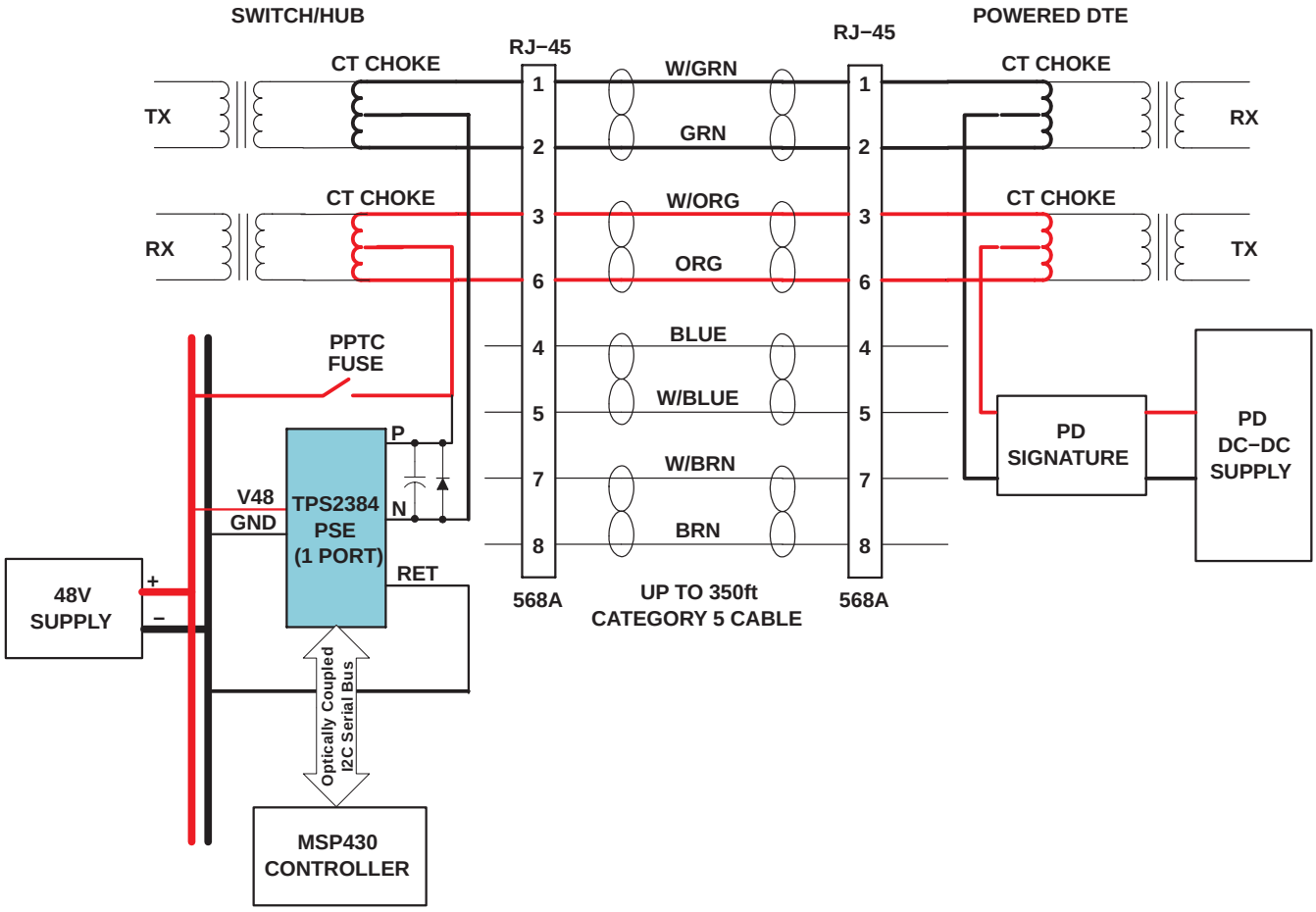


Figure 18.

TPS2384 BASIC 4 PORT (PMM) ISOLATED CONFIGURATION WITH AC DISCONNECT

TPS2384 basic 4-port isolated configuration with ac disconnect.

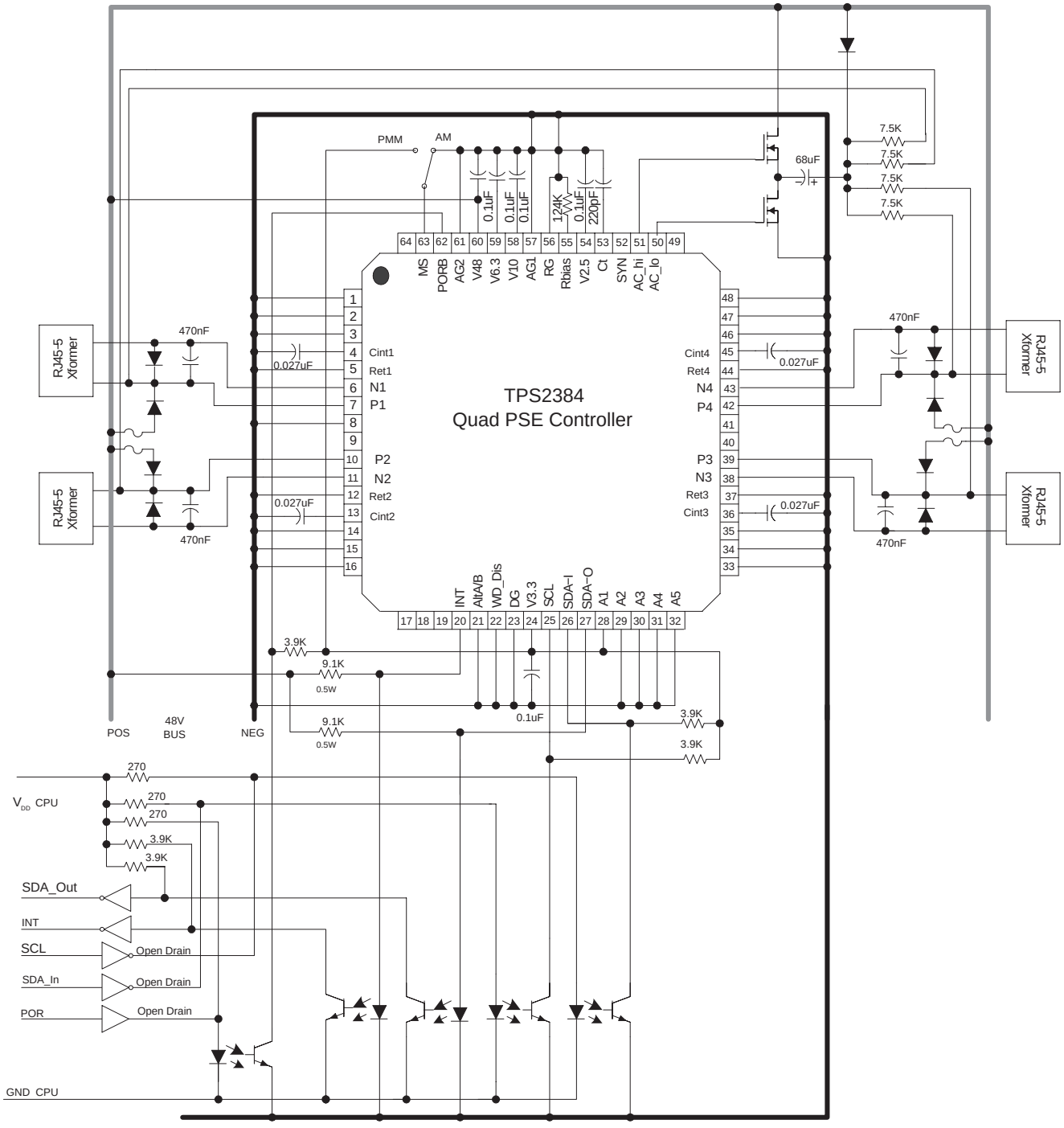


Figure 19.

PACKAGING INFORMATION

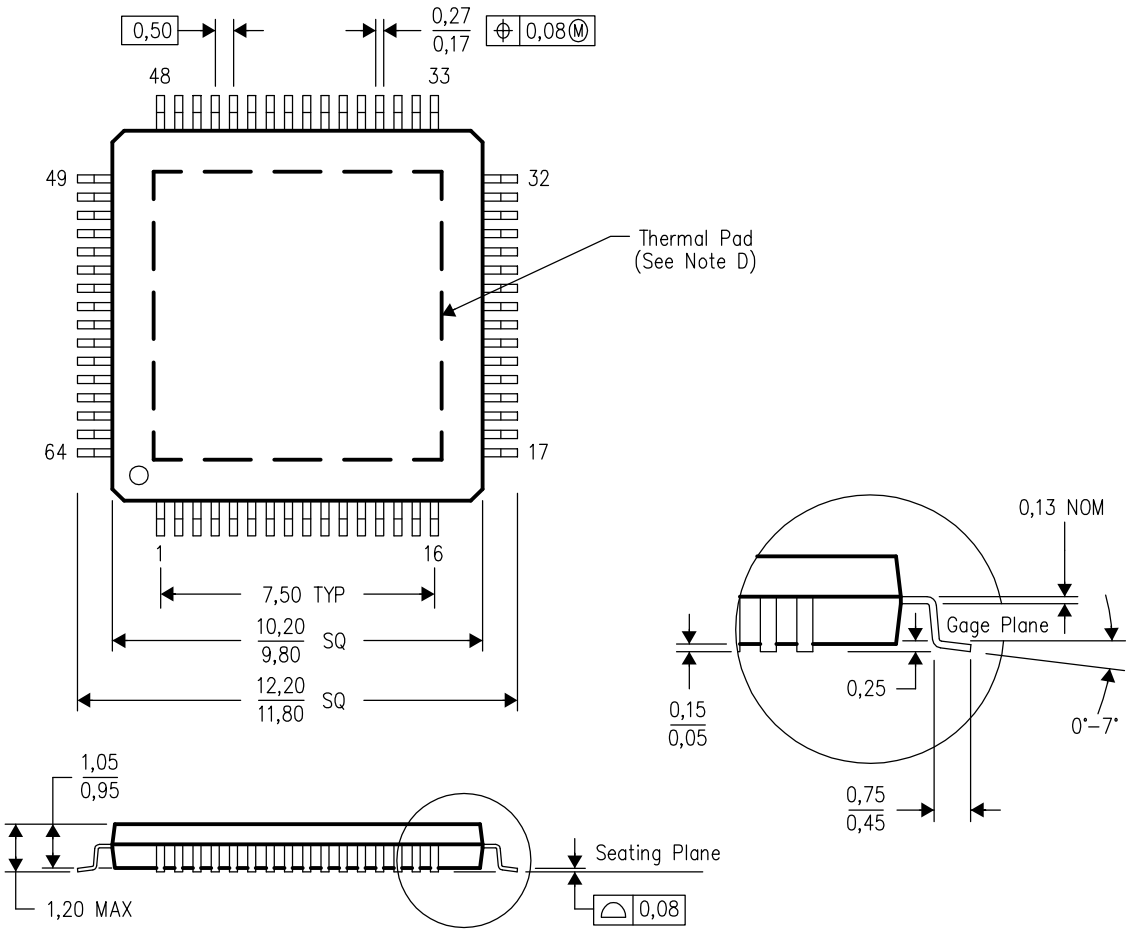
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS2384PAP	ACTIVE	HTQFP	PAP	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS2384PAPG4	ACTIVE	HTQFP	PAP	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS2384PAPR	ACTIVE	HTQFP	PAP	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS2384PAPRG4	ACTIVE	HTQFP	PAP	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS2384PJD	ACTIVE	HTQFP	PJD	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS2384PJDG4	ACTIVE	HTQFP	PJD	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS2384PJDR	ACTIVE	HTQFP	PJD	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS2384PJDRG4	ACTIVE	HTQFP	PJD	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



4147702/C 08/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

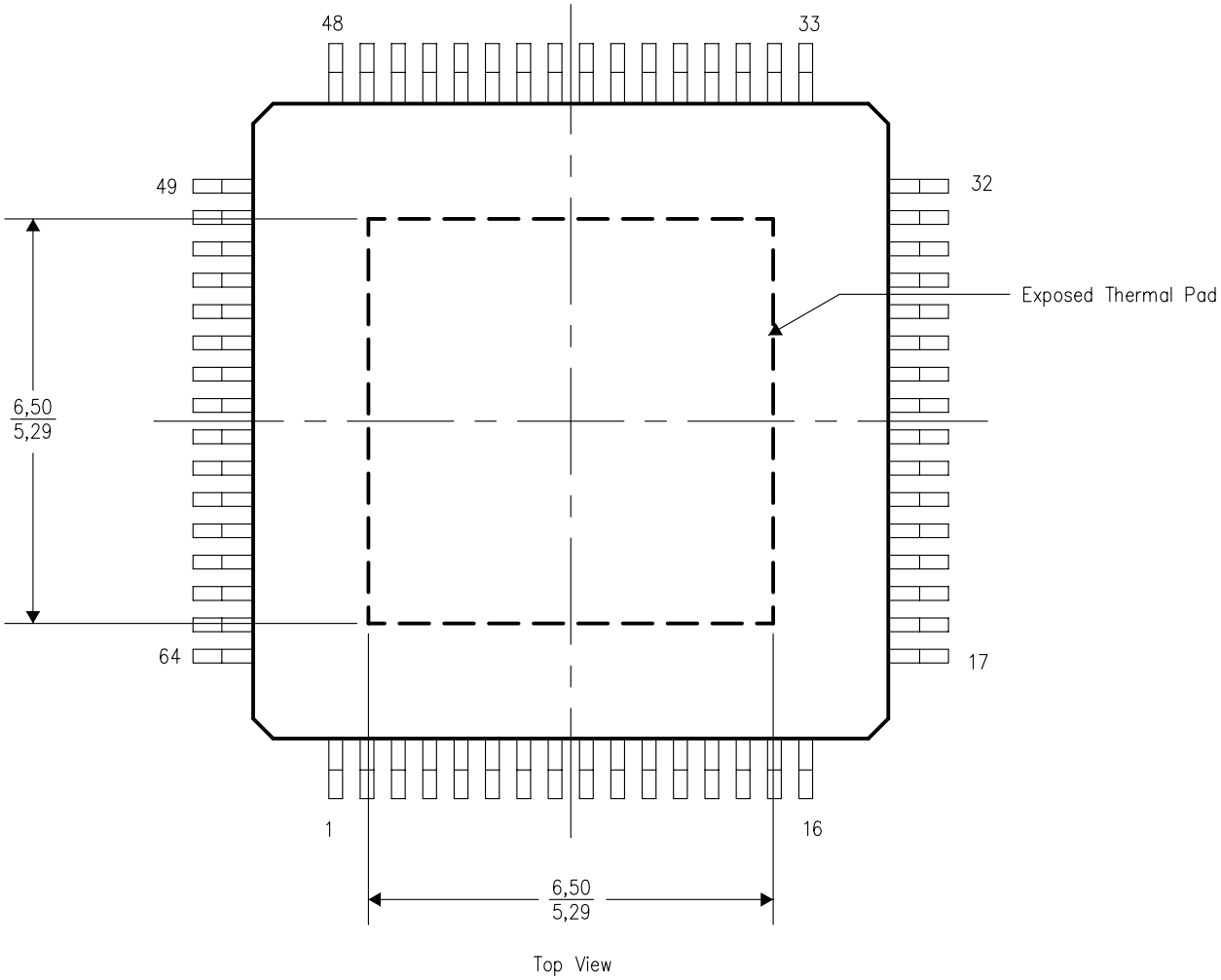
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. When the thermal pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

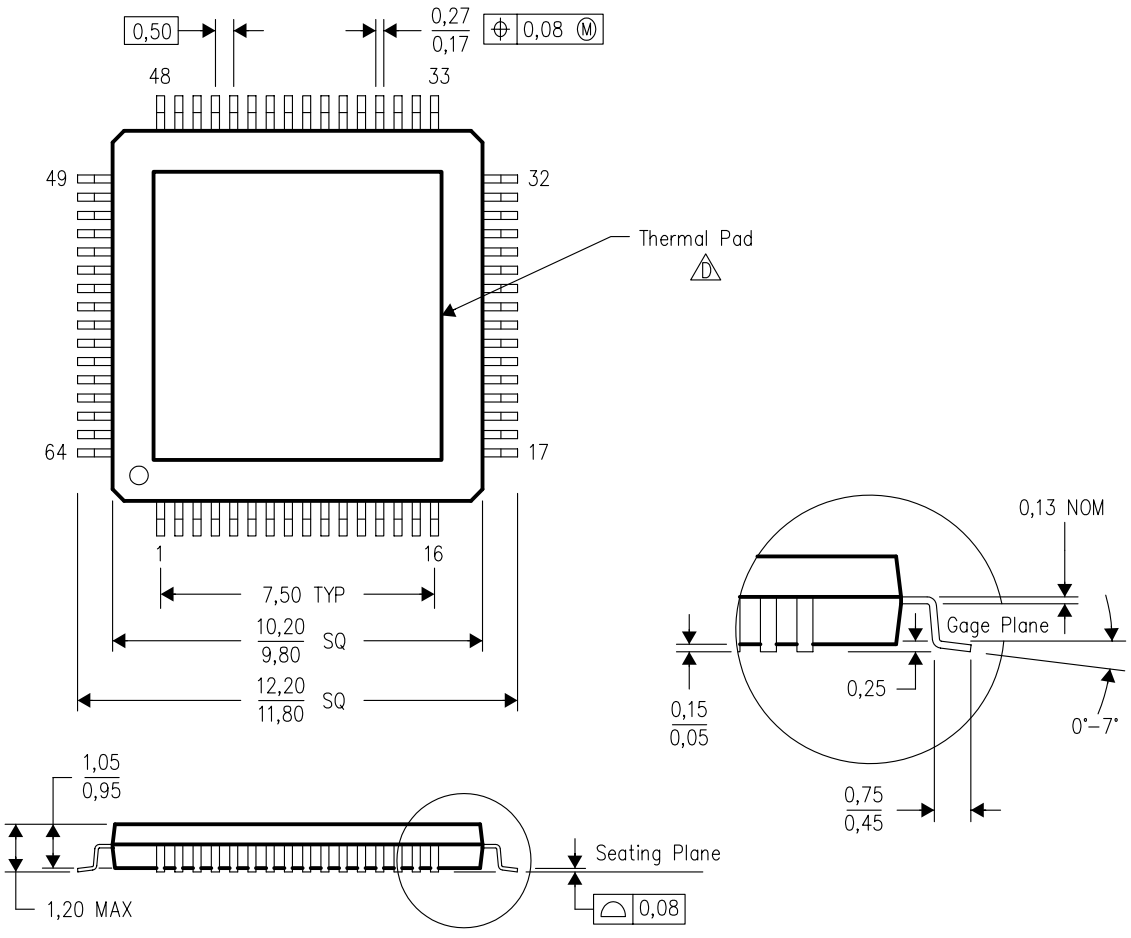


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PJD (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

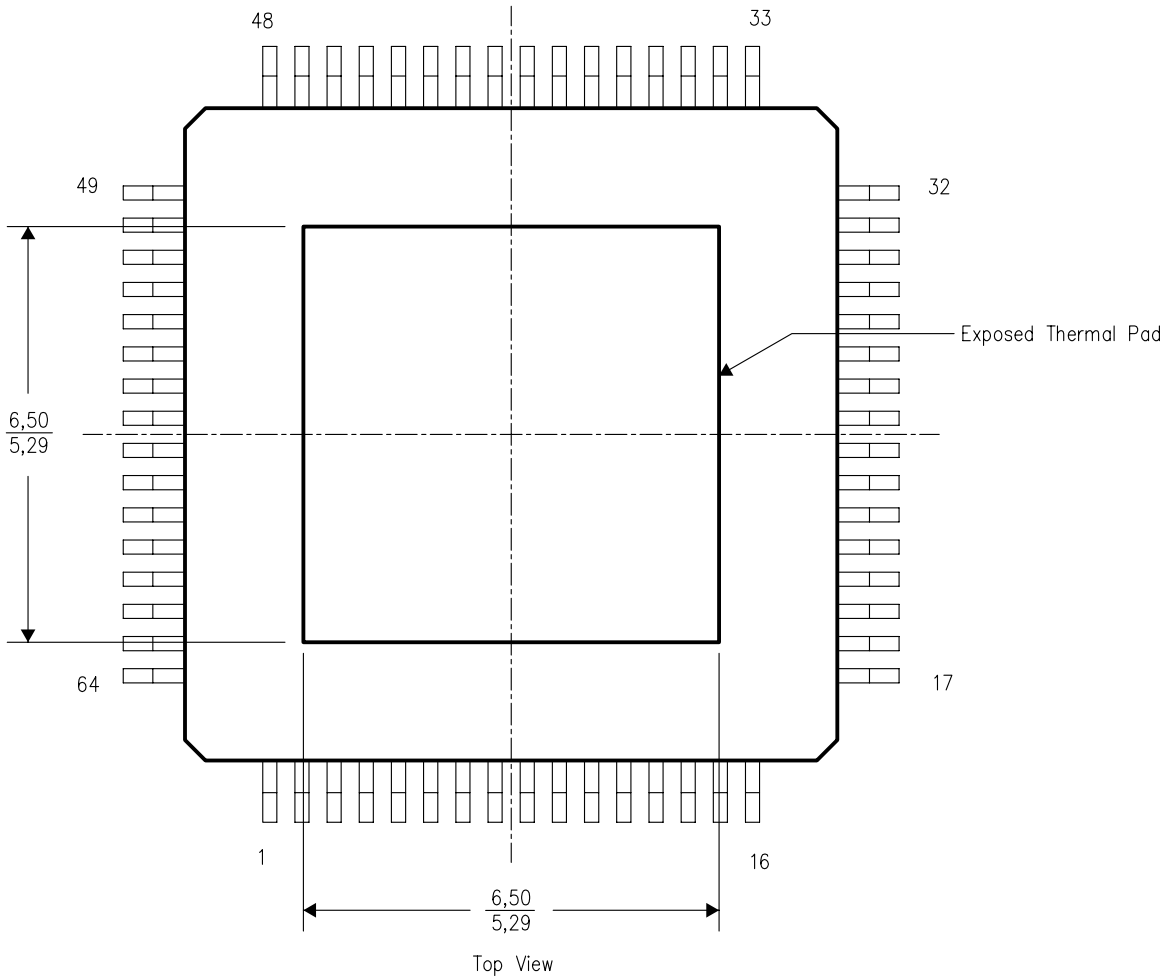
PJD (S–PQFP–G64)

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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