

### SPST 4-Channel Analog Switch

The DG211 is a low cost, CMOS monolithic, Quad SPST analog switch. It can be used in general purpose switching applications for communications, instrumentation, process control and computer peripheral equipment and provides true bidirectional performance in the ON condition and blocks signals to 30V<sub>P-P</sub> in the OFF condition.

### Part Number Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG211CJ	DG211CJ	0 to 70	16 Ld PDIP	E16.3
DG211CJZ (Notes 1, 2)	DG211CJZ	0 to 70	16 Ld PDIP* (Pb-free)	E16.3
DG211CY (Note 2)	DG211CY	0 to 70	16 Ld SOIC	M16.15
DG211CZY (Notes 1, 2)	DG211CZY	0 to 70	16 Ld SOIC (Pb-free)	M16.15

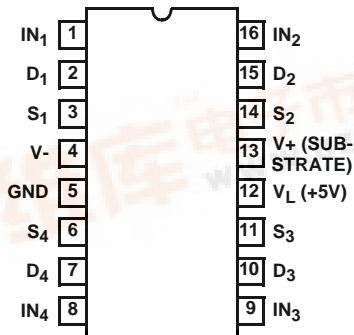
\*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTES:

1. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Add "T" suffix for Tape and Reel.

### Pinout

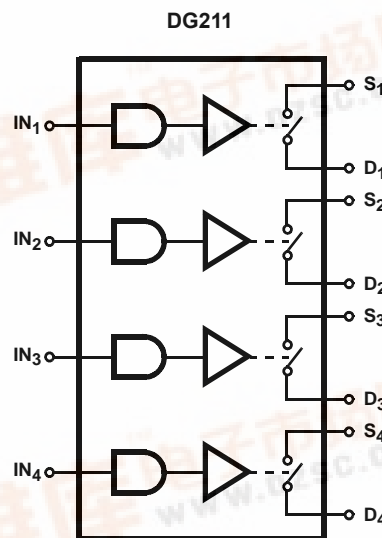
DG211  
(PDIP, SOIC)  
TOP VIEW



### Features

- Switches ±15V Analog Signals
- TTL Compatibility
- Logic Inputs Accept Negative Voltages
- r<sub>ON</sub> (Max) . . . . . 175Ω
- Pb-Free Plus Anneal Available (RoHS Compliant)

### Functional Block Diagrams



TRUTH TABLE

LOGIC	DG211
0	ON
1	OFF

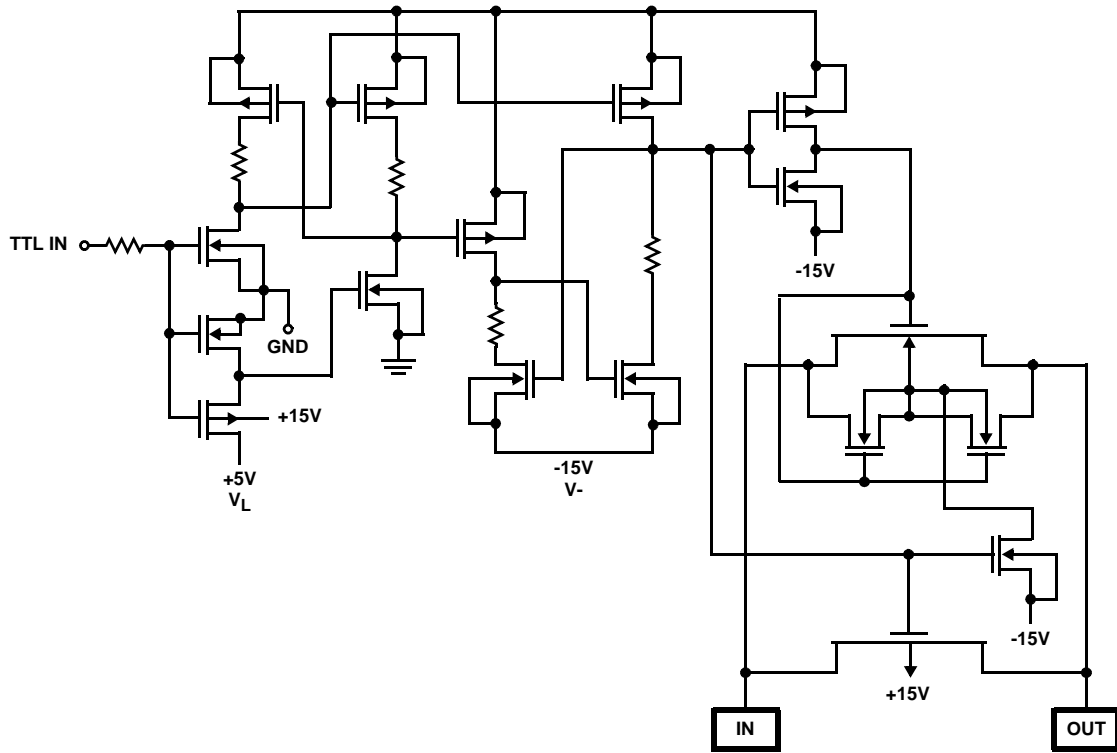
Logic "0" ≤ 0.8V, Logic "1" ≥ 2.4V



# DG211

## Schematic Diagram

DG211 ( $1/4$  AS SHOWN)



# DG211

## Absolute Maximum Ratings

V+ to V-	44V
V <sub>IN</sub> to Ground	V- to V+
V <sub>L</sub> to Ground	-0.3V to 25V
V <sub>S</sub> or V <sub>D</sub> to V+	0 to -36V
V <sub>S</sub> or V <sub>D</sub> to V-	0 to 36V
V+ to Ground	25V
V- to Ground	-25V
Current, any Terminal Except S or D	30mA
Continuous Current, S or D	20mA
Peak Current, S or D (Pulsed 1ms, 10% Duty Cycle Max)	70mA

## Thermal Information

Thermal Resistance (Typical, Note 3)	$\theta_{JA}$ (°C/W)
PDIP Package*	100
SOIC Package	120
Maximum Junction Temperature	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C (SOIC - Lead Tips Only)

\*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

## Operating Conditions

Temperature Range	0°C to 70°C
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**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications V+ = +15V, V- = -15V, V<sub>L</sub> = +5V, GND, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	(NOTE 4) MIN	(NOTE 5) TYP	MAX	UNITS	
<b>DYNAMIC CHARACTERISTICS</b>						
Turn-ON Time, t <sub>ON</sub>	See Figure 1 V <sub>S</sub> = 10V, R <sub>L</sub> = 1k $\Omega$ , C <sub>L</sub> = 35pF	-	460	-	ns	
Turn-OFF Time, t <sub>OFF1</sub>		-	360	-	ns	
t <sub>OFF2</sub>		-	450	-	ns	
OFF Isolation, OIRR (Note 7)	V <sub>IN</sub> = 5V, R <sub>L</sub> = 1k $\Omega$ , C <sub>L</sub> = 15pF, V <sub>S</sub> = 1V <sub>RMS</sub> , f = 100kHz	-	70	-	dB	
Crosstalk (Channel to Channel), CCRR		-	-90	-	dB	
Source OFF Capacitance, C <sub>S(OFF)</sub>	V <sub>D</sub> = V <sub>S</sub> = 0V, V <sub>IN</sub> = 5V, f = 1MHz	-	5	-	pF	
Drain OFF Capacitance, C <sub>D(OFF)</sub>		-	5	-	pF	
Channel ON Capacitance, C <sub>D(ON)</sub> + C <sub>S(ON)</sub>		-	16	-	pF	
<b>DIGITAL INPUT CHARACTERISTICS</b>						
Input Current with Voltage High, I <sub>IH</sub>	V <sub>IN</sub> = 2.4V	-1.0	-0.0004	-	$\mu$ A	
	V <sub>IN</sub> = 15V	-	0.003	1.0	$\mu$ A	
Input Current with Voltage Low, I <sub>IL</sub>	V <sub>IN</sub> = 0V	-1.0	-0.0004	-	$\mu$ A	
<b>ANALOG SWITCH CHARACTERISTICS</b>						
Analog Signal Range, V <sub>ANALOG</sub>		-15	-	15	V	
Drain-Source ON Resistance, r <sub>DS(ON)</sub>	V <sub>D</sub> = $\pm$ 10V, I <sub>S</sub> = 1mA, V <sub>IN</sub> = 0.8V	-	150	175	$\Omega$	
Source OFF Leakage Current, I <sub>S(OFF)</sub>	V <sub>IN</sub> = 2.4V	V <sub>S</sub> = 14V, V <sub>D</sub> = -14V	-	0.01	5.0	nA
		V <sub>S</sub> = -14V, V <sub>D</sub> = 14V	-5.0	-0.02	-	nA
Drain OFF Leakage Current, I <sub>D(OFF)</sub>	V <sub>IN</sub> = 2.4V	V <sub>S</sub> = -14V, V <sub>D</sub> = 14V	-	0.01	5.0	nA
		V <sub>S</sub> = 14V, V <sub>D</sub> = -14V	-5.0	-0.02	-	nA
Drain ON Leakage Current, I <sub>D(ON)</sub> (Note 6)	V <sub>IN</sub> = 0.8V	V <sub>S</sub> = V <sub>D</sub> = 14V	-	0.1	5.0	nA
		V <sub>S</sub> = V <sub>D</sub> = -14V	-5.0	-0.15	-	nA

# DG211

## Electrical Specifications $V_+ = +15V, V_- = -15V, V_L = +5V, GND, T_A = 25^\circ C$ (Continued)

PARAMETER	TEST CONDITIONS	(NOTE 4) MIN	(NOTE 5) TYP	MAX	UNITS
<b>POWER SUPPLY CHARACTERISTICS</b>					
Positive Supply Current, $I_+$	$V_{IN} = 0V$ or $2.4V$	-	0.1	10	$\mu A$
Negative Supply Current, $I_-$		-	0.1	10	$\mu A$
Logic Supply Current, $I_L$		-	0.1	10	$\mu A$

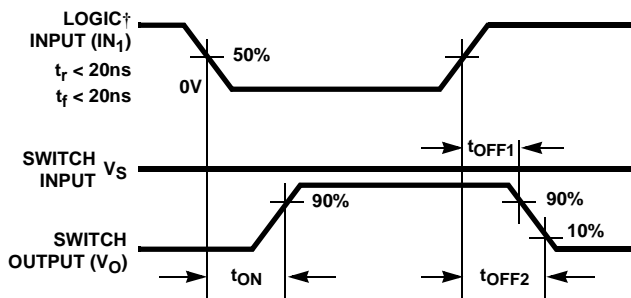
### NOTES:

- The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
- For design reference only, not 100% tested.
- $I_{D(ON)}$  is leakage from driver into ON switch.
- OFF Isolation =  $20 \log \frac{V_S}{V_D}$ ,  $V_S$  = Input to OFF switch,  $V_D$  = output.

## Test Circuits and Waveforms

Switch output waveform shown for  $V_S =$  constant with logic input waveform as shown. Note the  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with

switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



† Logic shown for DG211.

FIGURE 1. SWITCHING TIME MEASUREMENT POINTS

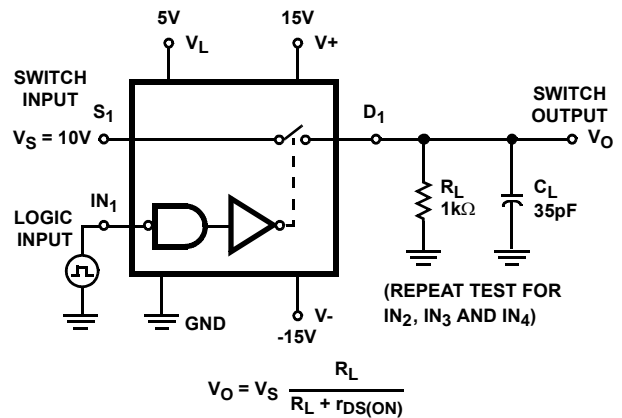


FIGURE 2. SWITCHING TIME TEST CIRCUIT

# DG211

## Die Characteristics

### DIE DIMENSIONS:

2159 $\mu$ m x 2235 $\mu$ m

### METALLIZATION:

Type: Al

Thickness: 10k $\text{\AA}$   $\pm$  1k $\text{\AA}$

### PASSIVATION:

Type: PSG/Nitride

PSG Thickness: 7k $\text{\AA}$   $\pm$  1.4k $\text{\AA}$

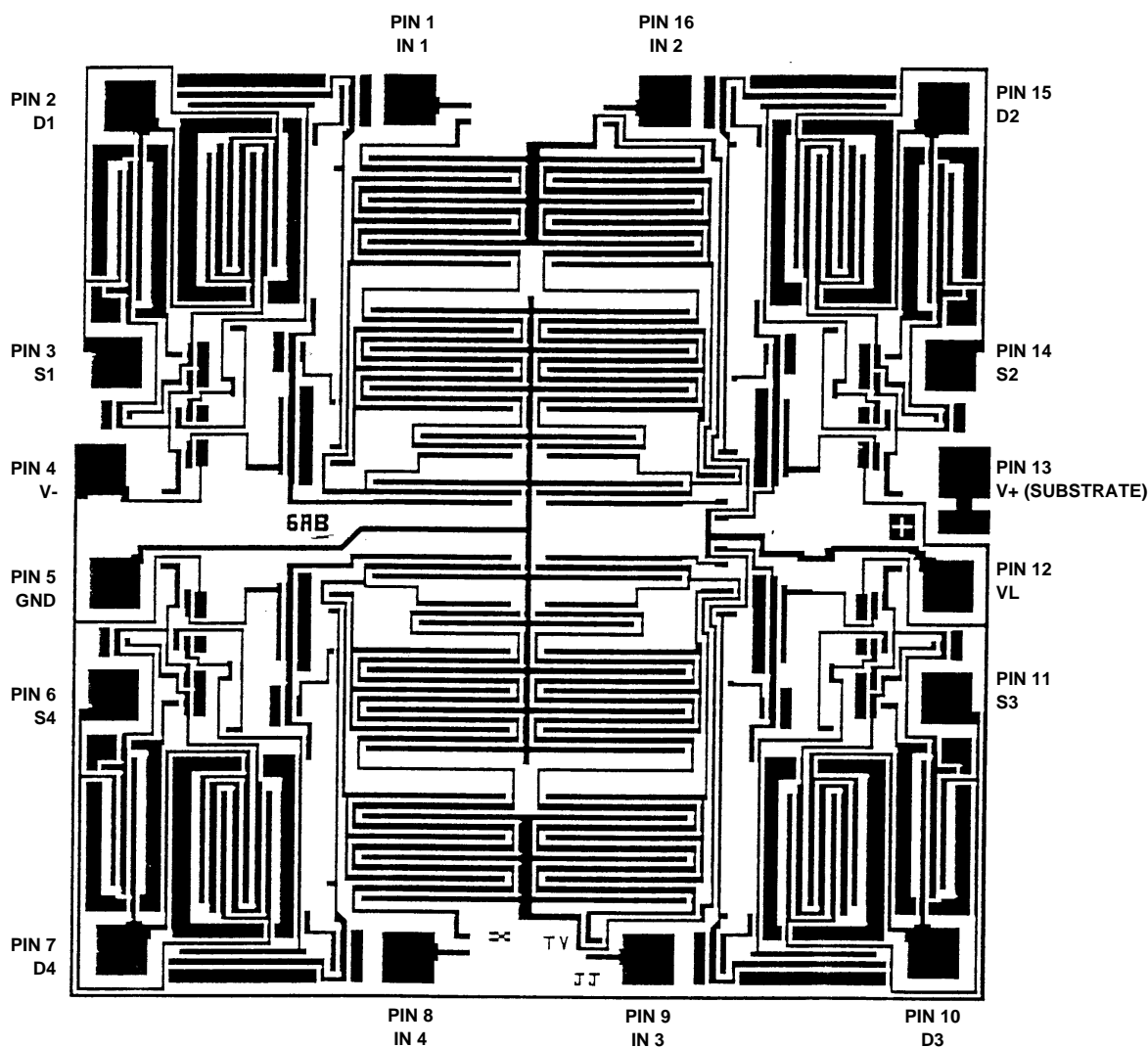
Nitride Thickness: 8k $\text{\AA}$   $\pm$  1.2k $\text{\AA}$

### WORST CASE CURRENT DENSITY:

9.1 x 10<sup>4</sup> A/cm<sup>2</sup>

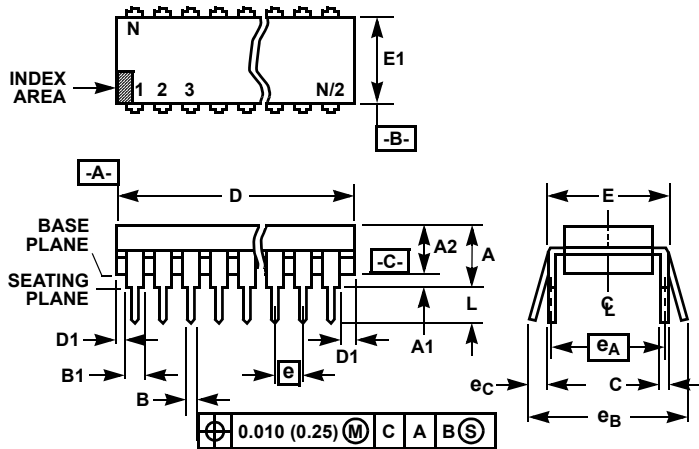
## Metallization Mask Layout

DG211



# DG211

## Dual-In-Line Plastic Packages (PDIP)



### NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and  $e_A$  are measured with the leads constrained to be perpendicular to datum  $-C-$ .
7.  $e_B$  and  $e_C$  are measured at the lead tips with the leads unconstrained.  $e_C$  must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

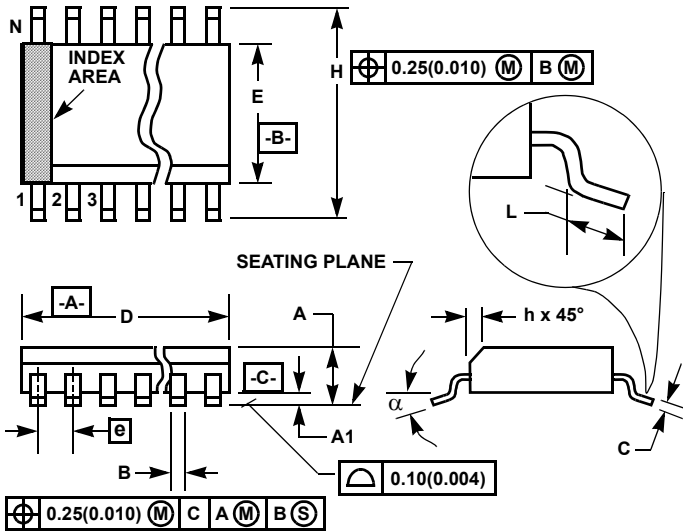
### E16.3 (JEDEC MS-001-BB ISSUE D) 16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
$e_A$	0.300 BSC		7.62 BSC		6
$e_B$	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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# DG211

## Small Outline Plastic Packages (SOIC)



**M16.15 (JEDEC MS-012-AC ISSUE C)**  
**16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
alpha	0°	8°	0°	8°	-

**NOTES:**

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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