3.3 V Slew Rate Limited, Half and Full Duplex, RS-485/RS-422 Transceivers

ADM3483/ADM3485/ADM3488/ADM3490

FEATURES

- Operate with 3.3 V supply
- Interoperable with 5 V logic
- EIA RS-422 and RS-485 compliant over full CM range
- Data rate options
  - ADM3483/ADM3488: 250 kbps
  - ADM3485/ADM3490: 10 Mbps
- Half and full duplex options
- Reduced slew rates for low EMI (ADM3483 and ADM3488)
- 2 nA supply current in shutdown mode (ADM3483/ADM3485)
- Up to 32 transceivers on the bus
- –7 V to +12 V bus common-mode range
- Specified over –40°C to +85°C temperature range
- 8 ns skew (ADM3485/ADM3490)
- 8-lead SOIC packages

APPLICATIONS

- Low power RS-485 applications
- Telecom
- Industrial control

GENERAL DESCRIPTION

The ADM3483/ADM3485/ADM3488/ADM3490 are low power, differential line transceivers designed to operate using a single 3.3 V power supply. Low power consumption, coupled with a shutdown mode, makes the ADM3483/ADM3485/ADM3488/ADM3490 ideal for power-sensitive applications. ADM3483/ADM3485/ADM3488/ADM3490 are suitable for communication on multipoint bus transmission lines.

The ADM3488/ADM3490 feature full duplex communication, while the ADM3483/ADM3485 are designed for half duplex communication.

The ADM3483/ADM3488 feature slew rate limited drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission at data rates up to 250 kbps.

FUNCTIONAL BLOCK DIAGRAMS

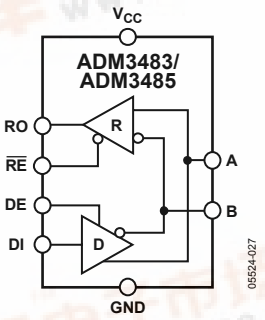

Figure 1

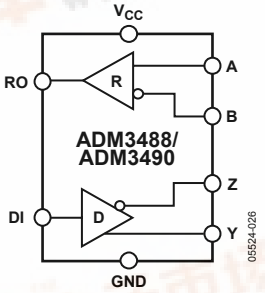

Figure 2.

The ADM3485/ADM3490 transmit at up to 10 Mbps.

The receiver input impedance is 12 kΩ, allowing up to 32 transceivers to be connected on the bus. A thermal shutdown circuit prevents excessive power dissipation caused by bus contention or by output shorting. If a significant temperature increase is detected in the internal driver circuitry during fault conditions, then the thermal shutdown circuit forces the driver output into a high impedance state. If the inputs are unconnected (floating) then the receiver contains a fail-safe feature that results in a logic high output state. All parts are fully specified over the commercial and industrial temperature ranges and are available in an 8-lead SOIC_N package.

Table 1. ADM34xx Part Comparison

Part No.	Guaranteed Data Rate (Mbps)	Supply Voltage (V)	Half/Full Duplex	Slew Rate Limited	Driver/Receiver Enable	Shutdown Current (nA)	Pin Count
ADM3483	0.25	3.0 to 3.6	Half	Yes	Yes	2	8
ADM3485	10	3.0 to 3.6	Half	No	Yes	2	8
ADM3488	0.25	3.0 to 3.6	Full	Yes	No	Not applicable	8
ADM3490	10	3.0 to 3.6	Full	No	No	Not applicable	8

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REVISION HISTORY

10/05—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 3.3 V ± 0.3 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments	
DRIVER						
Differential Output Voltage, V_{OD}	2.0			V	R_L = 100 Ω (RS-422), V_{CC} = 3.3 V ± 5% (see Figure 5)	
	1.5			V	R_L = 54 Ω (RS-485) (see Figure 5)	
	1.5			V	R_L = 60 Ω (RS-485), V_{CC} = 3.3 V (see Figure 6)	
Δ $\|V_{OD}\|$ for Complementary Output States[1]			0.2	V	R_L = 54 Ω or 100 Ω (see Figure 5)	
Common-Mode Output Voltage, V_{OC}			3	V	R_L = 54 Ω or 100 Ω (see Figure 5)	
Δ $\|V_{OC}\|$ for Common-Mode Output Voltage[1]			0.2	V	R_L = 54 Ω or 100 Ω (see Figure 5)	
DRIVER INPUT LOGIC						
CMOS Input Logic Threshold Low, V_{IH}			0.8	V	DE, DI, $\overline{RE}$	
CMOS Input Logic Threshold High, V_{IL}	2.0			V	DE, DI, $\overline{RE}$	
CMOS Logic Input Current, I_{N1}			±2	μA	DE, DI, $\overline{RE}$	
Input Current (A, B), I_{N2}			1.0	mA	V_{IN} = 12 V	DE = 0 V, V_{CC} = 0 V or 3.6 V
			−0.8	mA	V_{IN} = −7 V	
RECEIVER						
Differential Input Threshold Voltage, V_{TH}	−0.2		+0.2	V	−7 V < V_{CM} < + 12 V	
Input Hysteresis, Δ V_{TH}		50		mV	V_{CM} = 0 V	
CMOS Output Voltage High, V_{OH}	V_{CC} − 0.4			V	I_{OUT} = −1.5 mA, V_{ID} = 200 mV (see Figure 7)	
CMOS Output Voltage Low, V_{OL}			0.4	V	I_{OUT} = 2.5 mA, V_{ID} = 200 mV (see Figure 7)	
Three-State Output Leakage Current, I_{OZR}			±1	μA	V_{CC} = 3.6 V, 0 V ≤ V_{OUT} ≤ V_{CC}	
Input Resistance, R_{IN}	12			kΩ	−7 V < V_{CM} < + 12 V	
POWER SUPPLY CURRENT						
Supply Current, I_{CC}		1.1	2.2	mA	DE = V_{CC}, $\overline{RE}$ = 0 V or V_{CC}	No load, DI = 0 V or V_{CC}
		0.95	1.9	mA	DE = 0 V, $\overline{RE}$ = 0 V	
Supply Current in Shutdown Mode, I_{SHDN}		0.002	1	μA	DE = 0 V, $\overline{RE}$ = V_{CC}, DI = V_{CC} or 0 V	
Driver Short-Circuit Output Current, I_{OSD}			−250	mA	V_{OUT} = −7 V	
			250	mA	V_{OUT} = 12 V	
Receiver Short-Circuit Output Current, I_{OSR}	±8		±60	mA	0 V < V_{RO} < V_{CC}	

[1] ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when DI input changes state.

TIMING SPECIFICATIONS—ADM3485/ADM3490

V_{CC} = 3.3 V, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Differential Output Delay, t_{DD}	1	22	35	ns	R_L = 60 Ω (see Figure 8 and Figure 14)
Differential Output Transition Time, t_{TD}	3	8	25	ns	R_L = 60 Ω (see Figure 8 and Figure 14)
Propagation Delay, Low-to-High Level, t_{PLH}	7	22	35	ns	R_L = 27 Ω (see Figure 9 and Figure 15)
Propagation Delay, High-to-Low Level, t_{PHL}	7	22	35	ns	R_L = 27 Ω (see Figure 9 and Figure 15)
$\lvert t_{PLH} - t_{PHL} \rvert$ Propagation Delay Skew,[1] t_{PDS}			8	ns	R_L = 27 Ω (see Figure 9 and Figure 15)
DRIVER OUTPUT ENABLE/DISABLE TIMES (ADM3485 only)					
Output Enable Time to Low Level, t_{PZL}		45	90	ns	R_L = 110 Ω (see Figure 11 and Figure 17)
Output Enable Time to High Level, t_{PZH}		45	90	ns	R_L = 110 Ω (see Figure 10 and Figure 16)
Output Disable Time from High Level, t_{PHZ}		40	80	ns	R_L = 110 Ω (see Figure 10 and Figure 16)
Output Disable Time from Low Level, t_{PLZ}		40	80	ns	R_L = 110 Ω (see Figure 11 and Figure 17)
Output Enable Time from Shutdown to Low Level, t_{PSL}		650	900	ns	R_L = 110 Ω (see Figure 11 and Figure 17)
Output Enable Time from Shutdown to High Level, t_{PSH}		650	900	ns	R_L = 110 Ω (see Figure 10 and Figure 16)

[1] Measured on $\lvert t_{PLH}(Y) - t_{PHL}(Y) \rvert$ and $\lvert t_{PLH}(Z) - t_{PHL}(Z) \rvert$.

TIMING SPECIFICATIONS—ADM3483/ADM3488

V_{CC} = 3.3 V, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
DRIVER					
Differential Output Delay, t_{DD}	600	900	1400	ns	R_L = 60 Ω (see Figure 8 and Figure 14)
Differential Output Transition Time, t_{TD}	400	700	1200	ns	R_L = 60 Ω (see Figure 8 and Figure 14)
Propagation Delay, Low-to-High Level, t_{PLH}	700	1000	1500	ns	R_L = 27 Ω (see Figure 9 and Figure 15)
Propagation Delay, High-to-Low Level, t_{PHL}	700	1000	1500	ns	R_L = 27 Ω (see Figure 9 and Figure 15)
$\lvert t_{PLH} - t_{PHL} \rvert$ Propagation Delay Skew,[1] t_{PDS}		100		ns	R_L = 27 Ω (see Figure 9 and Figure 15)
DRIVER OUTPUT ENABLE/DISABLE TIMES (ADM3483 only)					
Output Enable Time to Low Level, t_{PZL}		900	1300	ns	R_L = 110 Ω (see Figure 11 and Figure 17)
Output Enable Time to High Level, t_{PZH}		600	800	ns	R_L = 110 Ω (see Figure 10 and Figure 16)
Output Disable Time from High Level, t_{PHZ}		50	80	ns	R_L = 110 Ω (see Figure 10 and Figure 16)
Output Disable Time from Low Level, t_{PLZ}		50	80	ns	R_L = 110 Ω (see Figure 11 and Figure 17)
Output Enable Time from Shutdown to Low Level, t_{PSL}		1.9	2.7	µs	R_L = 110 Ω (see Figure 11 and Figure 17)
Output Enable Time from Shutdown to High Level, t_{PSH}		2.2	3.0	µs	R_L = 110 Ω (see Figure 10 and Figure 16)

[1] Measured on $\lvert t_{PLH}(Y) - t_{PHL}(Y) \rvert$ and $\lvert t_{PLH}(Z) - t_{PHL}(Z) \rvert$.

TIMING SPECIFICATIONS—ADM3483/ADM3485/ADM3488/ADM3490

V_{CC} = 3.3 V, T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RECEIVER					
Time to Shutdown					
t_{SHDN} ADM3483/ADM3485[1]	80	190	300	ns	
Propagation Delay, Low-to-High Level					
t_{RPLH} ADM3485/ADM3490	25	65	90	ns	V_{ID} = 0 V to 3.0 V, C_L = 15 pF (see Figure 12 and Figure 18)
t_{RPLH} ADM3483/ADM3488	25	75	120	ns	
Propagation Delay, High-to-Low Level					
t_{RPHL} ADM3485/ADM3490	25	65	90	ns	V_{ID} = 0 V to 3.0 V, C_L = 15 pF (see Figure 12 and Figure 18)
t_{RPHL} ADM3483/ADM3488	25	75	120	ns	
$\lvert t_{PLH} - t_{PHL} \rvert$ Propagation Delay Skew					
t_{RPDS} ADM3485/ADM3490			10	ns	V_{ID} = 0 V to 3.0 V, C_L = 15 pF, (see Figure 12 and Figure 18)
t_{RPDS} ADM3483/ADM348			20	ns	
RECEIVER OUTPUT ENABLE/DISABLE TIMES (ADM3483/ADM3485 only)					
Output Enable Time to Low Level, t_{PRZL}		25	50	ns	C_L = 15 pF (see Figure 13 and Figure 19)
Output Enable Time to High Level, t_{PRZH}		25	50	ns	C_L = 15 pF (see Figure 13 and Figure 19)
Output Disable Time from High Level, t_{PRHZ}		25	45	ns	C_L = 15 pF (see Figure 13 and Figure 19)
Output Disable Time from Low Level, t_{PRLZ}		25	45	ns	C_L = 15 pF (see Figure 13 and Figure 19)
Output Enable Time from Shutdown to Low Level, t_{PRSL}		720	1400	ns	C_L = 15 pF (see Figure 13 and Figure 19)
Output Enable Time from Shutdown to High Level, t_{PRSH}		720	1400	ns	C_L = 15 pF (see Figure 13 and Figure 19)

[1] The transceivers are put into shutdown by bringing the $\overline{RE}$ high and DE low. If the inputs are in this state for less than 80 ns, the parts are guaranteed not to enter shutdown. If the parts are in this state for at least 300 ns, the parts are guaranteed to have entered shutdown.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{CC} to GND	7 V
Digital I/O Voltage (DE, $\overline{RE}$, DI)	−0.3 V to V_{CC} + 0.3 V
Digital I/O Voltage (R_{OUT})	V_{CC} − 0.5 V to V_{CC} + 0.5 V
Driver Output/Receiver Input Voltage	−7.5 V to +12.5 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
θ_{JA} Thermal Impedance	
8-Lead SOIC	121°C/W
Lead Temperature	
Soldering (10 seconds)	300°C
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

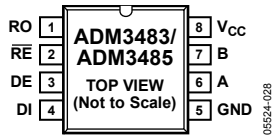


Figure 3. ADM3483/ADM3485 Pin Configuration

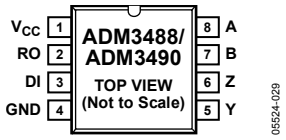


Figure 4. ADM3488/ADM3490 Pin Configuration

Table 7. Pin Function Descriptions

ADM3483/ADM3485 Pin No.	ADM3488/ADM3490 Pin No.	Mnemonic	Description
1	2	RO	Receiver Output. When enabled, if A > B by 200 mV, then RO = high. If A < B by 200 mV, then RO = low.
2	N/A	$\overline{RE}$	Receiver Output Enable. A low level enables the receiver output, RO. A high level places it in a high impedance state. If $\overline{RE}$ is high and DE is low, the device enters a low power shutdown mode.
3	N/A	DE	Driver Output Enable. A high level enables the driver differential Outputs A and B. A low level places it in a high impedance state. If $\overline{RE}$ is high and DE is low, the device enters a low power shutdown mode.
4	3	DI	Driver Input. With a half duplex part when the driver is enabled, a logic low on DI forces A low and B high while a logic high on DI forces A high and B low. With a full duplex part when the driver is enabled, a logic low on DI forces Y low and Z high while a logic high on DI forces Y high and Z low.
5	4	GND	Ground.
N/A	5	Y	Noninverting Driver Output.
N/A	6	Z	Inverting Driver Output.
6	N/A	A	Noninverting Receiver Input A and Noninverting Driver Output A.
N/A	8	A	Noninverting Receiver Input A.
7	N/A	B	Inverted Receiver Input B and Inverted Driver Output B.
N/A	7	B	Inverted Receiver Input B.
8	1	V_{CC}	Power Supply, 3.3 V ± 0.3 V.

TEST CIRCUITS

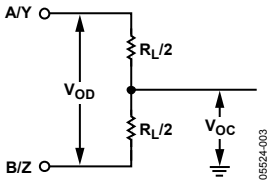


Figure 5. Driver V_{OD} and V_{OC}

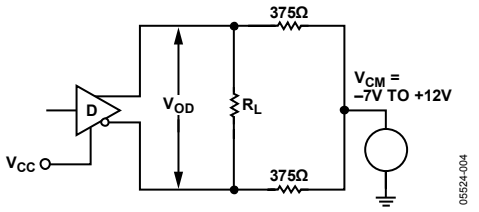


Figure 6. Driver V_{OD} with Varying Common-Mode Voltage

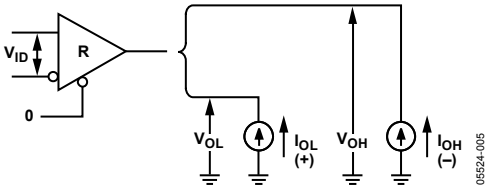


Figure 7. Receiver V_{OH} and V_{OL}

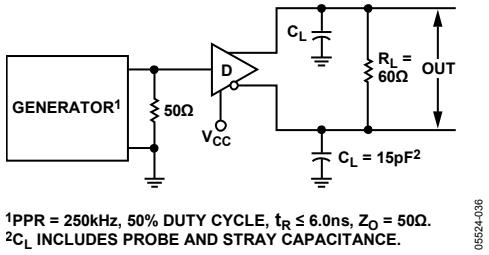


Figure 8. Driver Differential Output Delay and Transition Times

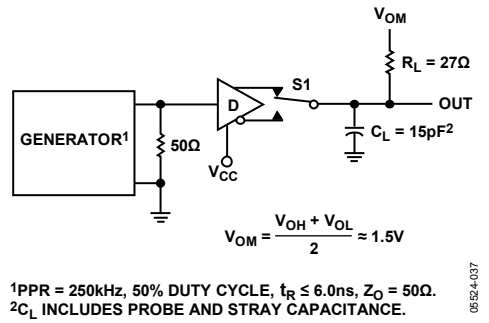


Figure 9. Driver Propagation Delays

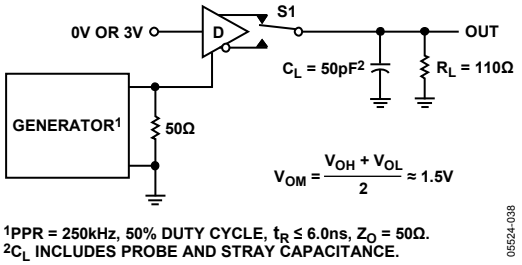


Figure 10. Driver Enable and Disable Times (t_{PZH}, t_{PSH}, t_{PHZ})

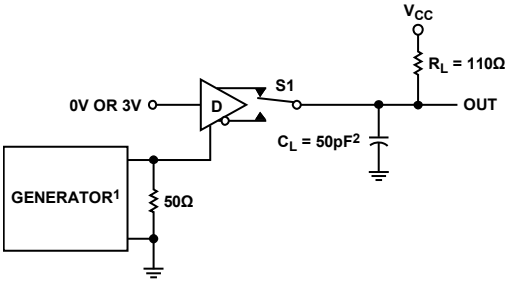


Figure 11. Driver Enable and Disable Times (t_{PZL}, t_{PSL}, t_{PLZ})

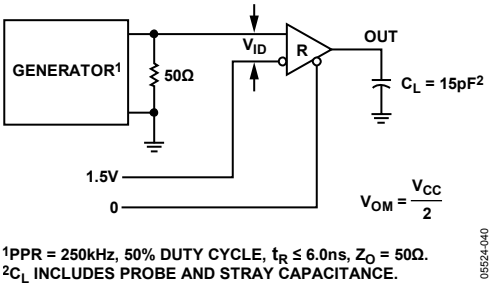


Figure 12. Receiver Propagation Delay

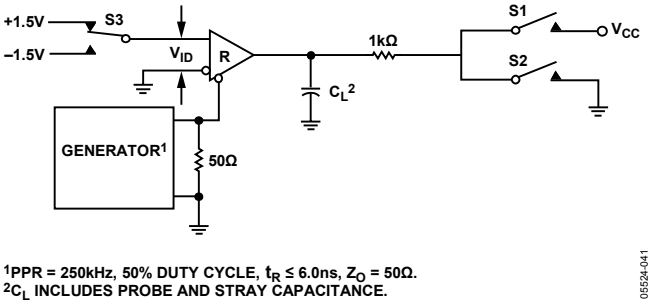


Figure 13. Receiver Enable and Disable Times

SWITCHING CHARACTERISTICS

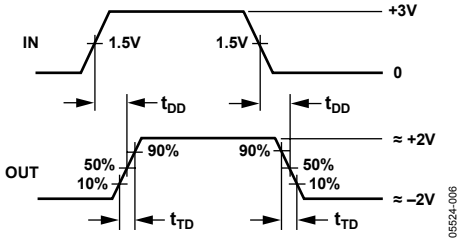


Figure 14. Driver Differential Output Delay and Transition Times

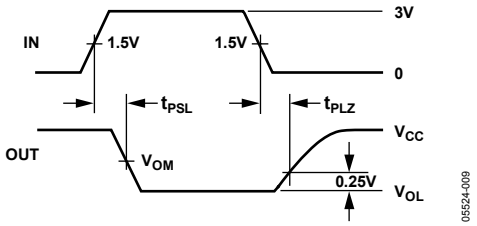


Figure 17. Driver Enable and Disable Times (t_{PZL}, t_{PSL}, t_{PLZ})

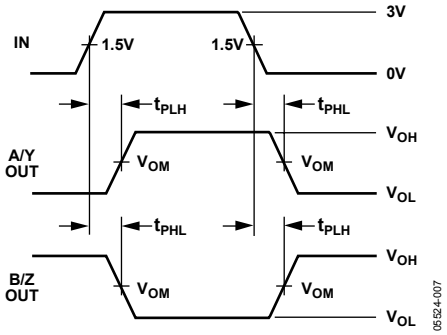


Figure 15. Driver Propagation Delays

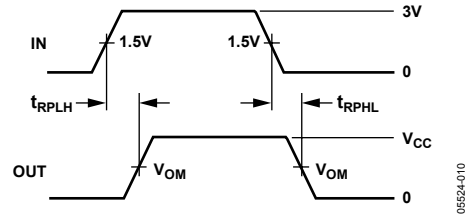


Figure 18. Receiver Propagation Delay

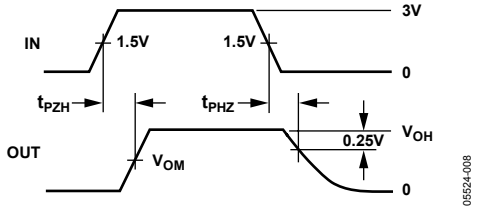


Figure 16. Driver Enable and Disable Times (t_{PZH}, t_{PSH}, t_{PHZ})

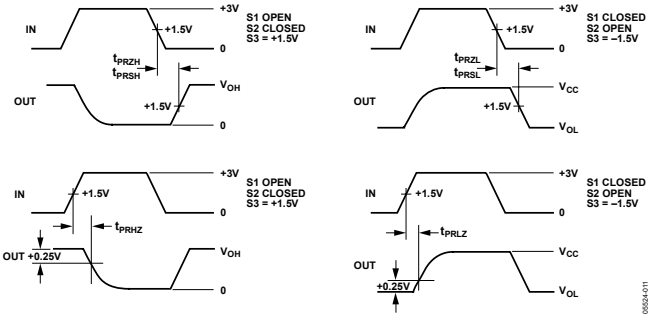


Figure 19. Receiver Enable and Disable Times

TYPICAL PERFORMANCE CHARACTERISTICS

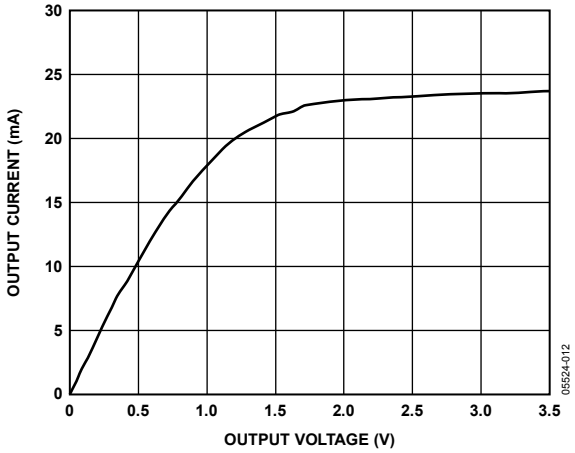


Figure 20. Output Current vs. Receiver Output Low Voltage

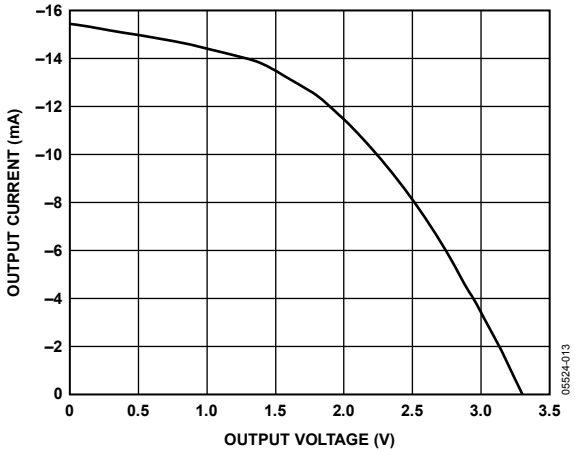


Figure 21. Output Current vs. Receiver Output High Voltage

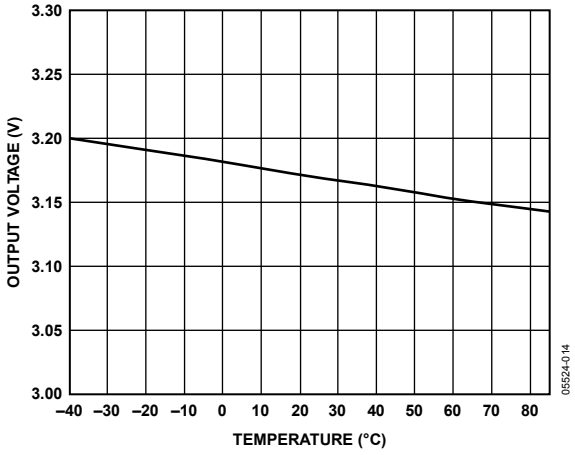


Figure 22. Receiver Output High Voltage vs. Temperature, I_O = 1.5 mA

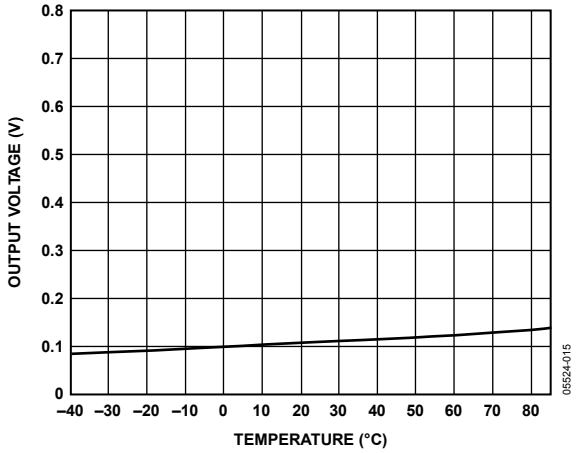


Figure 23. Receiver Output Low Voltage vs. Temperature, I_O = 2.5 mA

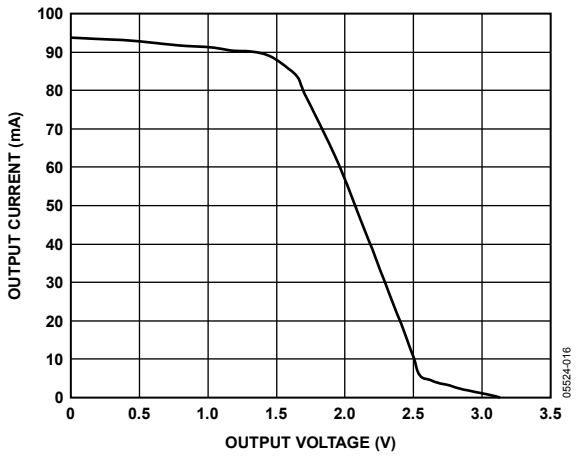


Figure 24. Driver Output Current vs. Differential Output Voltage

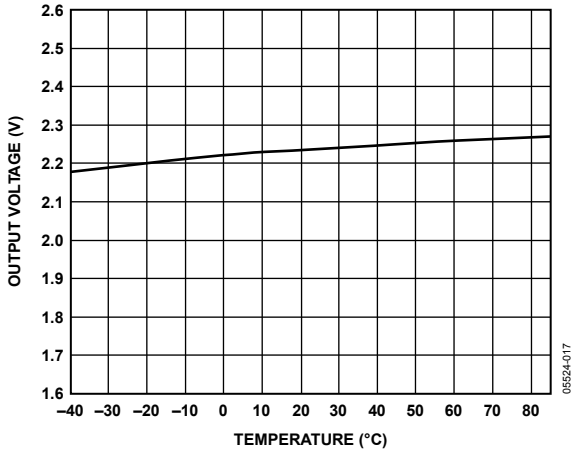


Figure 25. Driver Differential Output Voltage vs. Temperature, RI = 54 Ω

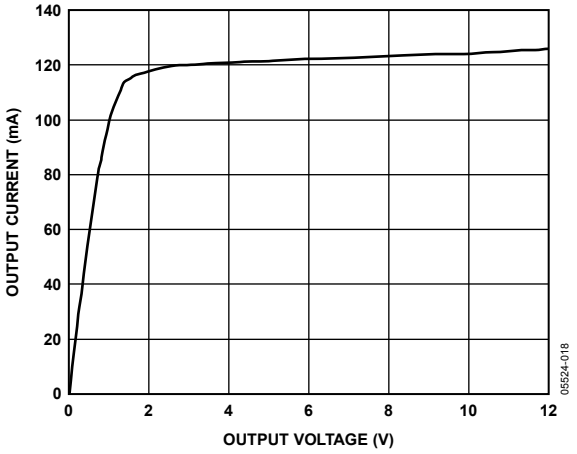


Figure 26. Output Current vs. Driver Output Low Voltage

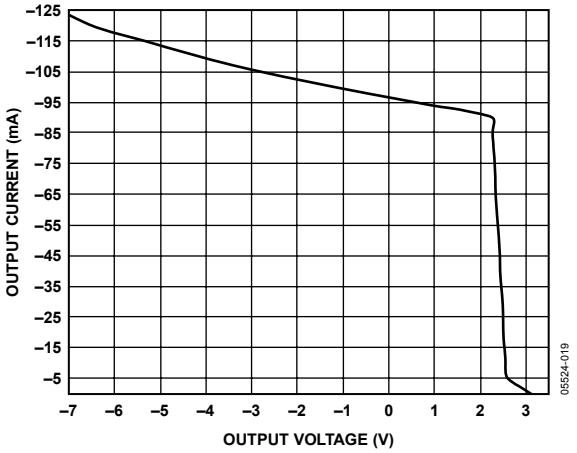


Figure 27. Output Current vs. Driver Output High Voltage

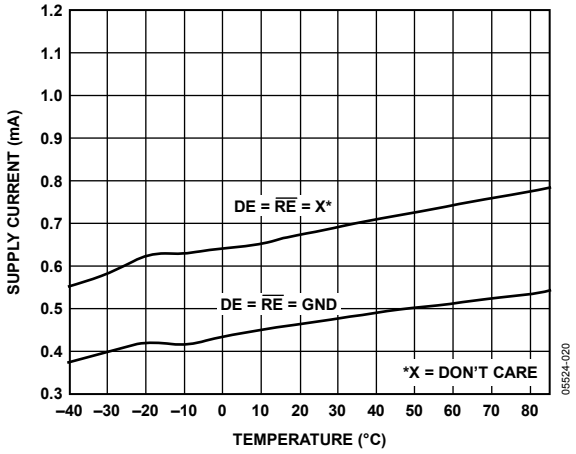


Figure 28. Supply Current vs. Temperature

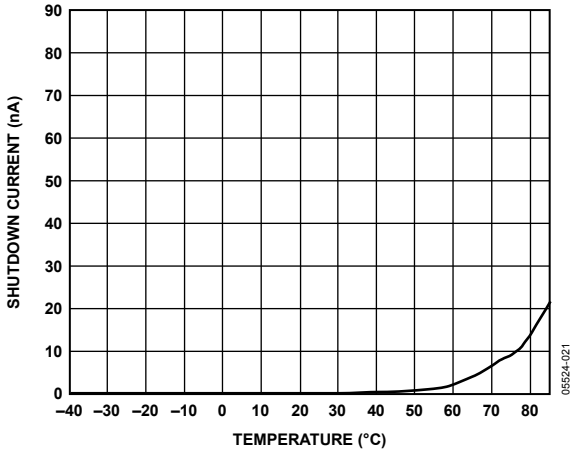


Figure 29. Shutdown Current vs. Temperature

CIRCUIT DESCRIPTION

The ADM3483/ADM3485/ADM3488/ADM3490 are low power transceivers for RS-485 and RS-422 communications. The ADM3483/ADM3488 transmit and receive at data rates up to 250 kbps; the ADM3485/ADM3490 transmit at up to 10 Mbps. The ADM3488/ADM3490 are full duplex transceivers, while the ADM3483/ADM3485 are half duplex transceivers. Driver enable (DE) and receiver enable ($\overline{RE}$) pins are included on the ADM3483/ADM3485. When disabled, the driver and receiver outputs are high impedance.

DEVICES WITH RECEIVER/DRIVER ENABLES

(ADM3483/ADM3485)

Table 8. Transmitting Truth Table

Transmitting Inputs			Transmitting Outputs		
$\overline{RE}$	DE	DI	B	A	Mode
X[1]	1	1	0	1	Normal
X[1]	1	0	1	0	Normal
0	0	X[1]	High-Z[2]	High-Z[2]	Normal
1	0	X[1]	High-Z[2]	High-Z[2]	Shutdown

[1] X = Don't care.
[2] High-Z = High impedance.

Table 9. Receiving Truth Table

Receiving Inputs			Receiving Outputs	
$\overline{RE}$	DE	A–B	R_O	Mode
0	0	≥ +0.2 V	1	Normal
0	0	≤ −0.2 V	0	Normal
0	0	Inputs Open	1	Normal
1	0	X[1]	High-Z[2]	Shutdown

[1] X = Don't care.
[2] High-Z = High impedance.

DEVICES WITHOUT RECEIVER/DRIVER ENABLES

(ADM3488/ADM3490)

Table 10. Transmitting Truth Table

Transmitting Inputs	Transmitting Outputs	
DI	Z	Y
1	0	1
0	1	0

Table 11. Receiving Truth Table

Receiving Inputs	Receiving Outputs
A–B	R_O
≥ +0.2 V	1
≤ −0.2 V	0
Inputs Open	1

REDUCED EMI AND REFLECTIONS

(ADM3483/ADM3488)

The ADM3483/ADM3488 are slew rate limited transceivers, minimizing EMI and reducing reflections caused by improperly terminated cables.

LOW POWER SHUTDOWN MODE

(ADM3483/ADM3485)

A low power shutdown mode is initiated by bringing both $\overline{RE}$ high and DE low. The devices do not shut down unless both the driver and receiver are disabled (high impedance). In shutdown, the devices typically draw only 2 nA of supply current. For these devices, the t_{PSH} and t_{PSL} enable times assume the part was in the low power shutdown mode; the t_{PZH} and t_{PZL} enable times assume the receiver or driver was disabled, but the part was not shut down.

DRIVER OUTPUT PROTECTION

Two methods are implemented to prevent excessive output current and power dissipation caused by faults or by bus contention. Current limit protection on the output stage provides immediate protection against short circuits over the whole common-mode voltage range (see Typical Performance Characteristics). In addition, a thermal shutdown circuit forces the driver outputs into a high impedance state if the die temperature rises excessively.

PROPAGATION DELAY

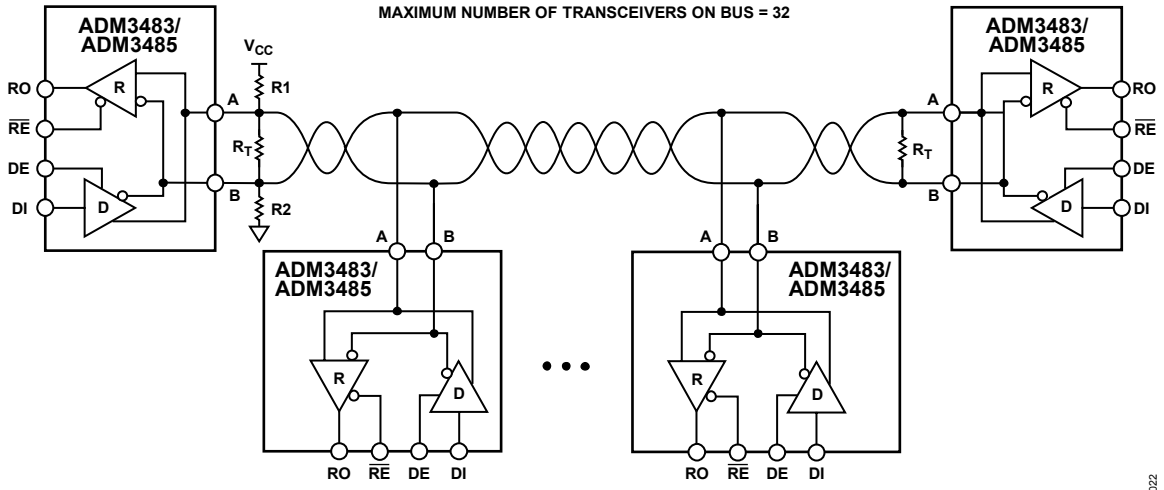
Skew time is the difference between the low-to-high and high-to-low propagation delays. Small driver/receiver skew times help maintain a symmetrical mark-space ratio (50% duty cycle). The receiver skew time, $|t_{PRLH} - t_{PRHL}|$, is under 10 ns (20 ns for ADM3483/ADM3488). The driver skew times are 8 ns for ADM3485/ADM3490, and typically under 100 ns for ADM3483/ADM3488.

TYPICAL APPLICATIONS

The ADM3483/ADM3485/ADM3488/ADM3490 transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figure 30 and Figure 31 show typical network applications circuits. These parts can also be used as line repeaters, with cable lengths longer than 4000 feet, as shown in Figure 32. To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible. The slew rate limited ADM3483/ADM3488 are more tolerant of imperfect termination.

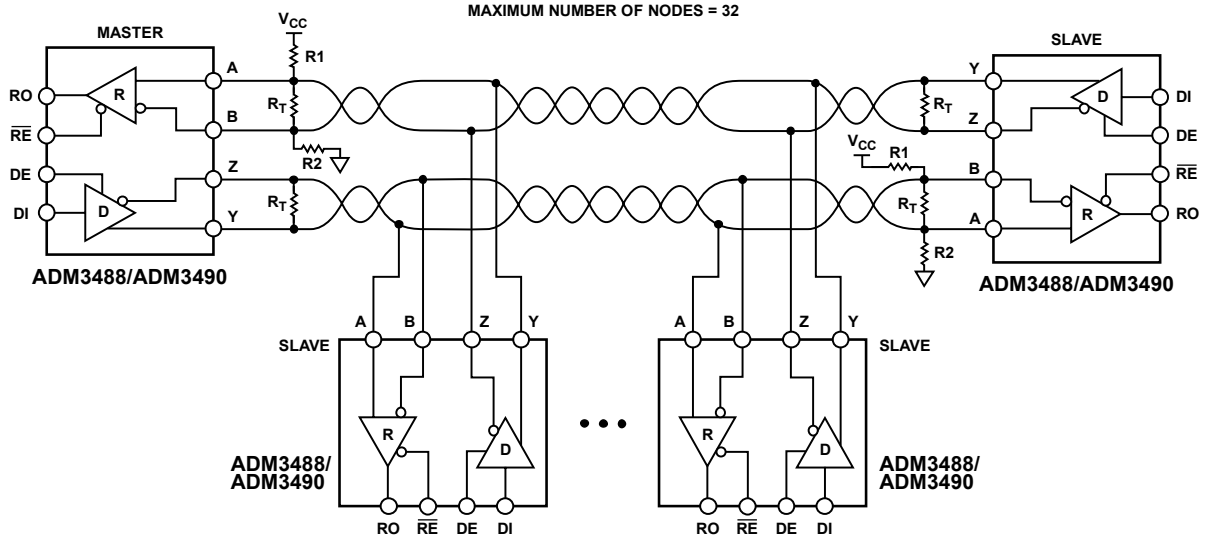
LINE LENGTH VS. DATA RATE

The RS-485 and RS-422 standards cover line lengths up to 4000 feet. For line lengths greater than 4000 feet, see Figure 32.



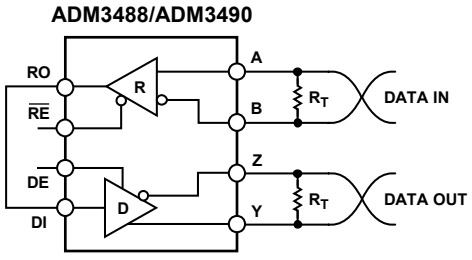
NOTES
1. R_T IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE.

Figure 30. ADM3483/ADM3485 Typical Half Duplex RS-485 Network



NOTES
1. R_T IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE.

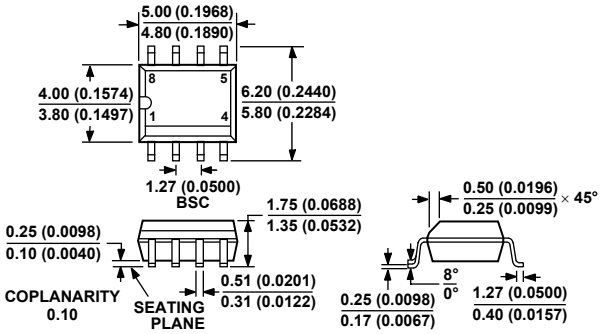
Figure 31. ADM3488/ADM3490 Full Duplex RS-485 Network



NOTES
1. R_T IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE.

Figure 32. Line Repeater for ADM3488/ADM3490

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 33. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
ADM3483ARZ[1]	−40°C to +85°C	8-Lead Narrow Body Small Outline (SOIC_N)	R-8	
ADM3483ARZ–REEL7[1]	−40°C to +85°C	8-Lead Narrow Body Small Outline (SOIC_N)	R-8	1,000
ADM3485ARZ[1]	−40°C to +85°C	8-Lead Narrow Body Small Outline (SOIC_N)	R-8	
ADM3485ARZ–REEL7[1]	−40°C to +85°C	8-Lead Narrow Body Small Outline (SOIC_N)	R-8	1,000
ADM3488ARZ[1]	−40°C to +85°C	8-Lead Narrow Body Small Outline (SOIC_N)	R-8	
ADM3488ARZ–REEL7[1]	−40°C to +85°C	8-Lead Narrow Body Small Outline (SOIC_N)	R-8	1,000
ADM3490ARZ[1]	−40°C to +85°C	8-Lead Narrow Body Small Outline (SOIC_N)	R-8	
ADM3490ARZ–REEL7[1]	−40°C to +85°C	8-Lead Narrow Body Small Outline (SOIC_N)	R-8	1,000

[1] Z = Pb-free part.

NOTES

NOTES

D05524-0-10/05(0)