Active Receive Mixer 400 MHz to 1.2 GHz

AD8344

FEATURES

Broadband RF port: 400 MHz to 1.2 GHz
Conversion gain: 4.5 dB
Noise figure: 10.5 dB
Input IP3: 24 dBm
Input P1dB: 8.5 dBm
LO drive: 0 dBm
External control of mixer bias for low power operation
Single-ended, 50 Ω RF and LO input ports
Single-supply operation: 5 V @ 84 mA
Power-down mode
Exposed paddle LFCSP: 3 mm × 3 mm

APPLICATIONS

Cellular base station receivers
ISM receivers
Radio links
RF Instrumentation

FUNCTIONAL BLOCK DIAGRAM

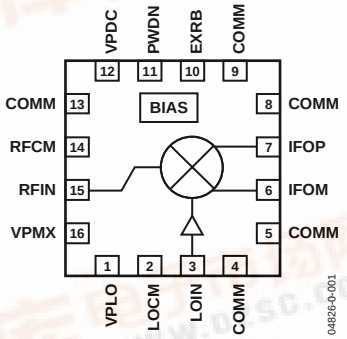

Figure 1.

GENERAL DESCRIPTION

The AD8344 is a high performance, broadband active mixer. It is well suited for demanding receive-channel applications that require wide bandwidth on all ports and very low intermodulation distortion and noise figure.

The AD8344 provides a typical conversion gain of 4.5 dB at 890 MHz. The integrated LO driver supports a 50 Ω input impedance with a low LO drive level, helping to minimize external component count.

The single-ended 50 Ω broadband RF port allows for easy interfacing to both active devices and passive filters. The RF input accepts input signals as large as 1.7 V p-p or 8.5 dBm (re: 50 Ω) at P1dB.

The open-collector differential outputs provide excellent balance and can be used with a differential filter or IF amplifier, such as the AD8369 or AD8351. These outputs may also be converted to a single-ended signal through the use of a matching network or a transformer (balun). When centered on the VPOS supply voltage, each of the differential outputs may swing 2.5 V p-p.

The AD8344 is fabricated on an Analog Devices proprietary, high performance SiGe IC process. The AD8344 is available in a 16-lead LFCSP package. It operates over a −40°C to +85°C temperature range. An evaluation board is also available.

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REVISION HISTORY

6/04—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, f_{RF} = 890 MHz, f_{LO} = 1090 MHz, LO power = 0 dBm, Z_O = 50 Ω, R_{BIAS} = 2.43 kΩ, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
RF INPUT INTERFACE	(Pin 15, RFIN and Pin 14, RFCM)				
Return Loss			10		dB
DC Bias Level	Internally generated; port must be ac-coupled		2.6		V
OUTPUT INTERFACE					
Output Impedance	Differential impedance, f = 200 MHz		9‖1		kΩ‖pF
DC Bias Voltage	Externally generated	4.75	V_S	5.25	V
Power Range	Via a 4:1 balun			13	dBm
LO INTERFACE					
LO Power		−10	0	+4	dBm
Return Loss			10		dB
DC Bias Voltage	Internally generated; port must be ac-coupled		V_S – 1.6		V
POWER-DOWN INTERFACE					
PWDN Threshold			V_S – 1.4		V
PWDN Response Time	Device enabled, IF output to 90% of its final level		0.4		µs
	Device disabled, supply current < 5 mA		0.01		µs
PWDN Input Bias Current	Device enabled		−80		µA
	Device disabled		100		µA
POWER SUPPLY					
Positive Supply Voltage		4.75	V_S	5.25	V
Quiescent Current					
VPDC	Supply current for bias cells		5		mA
VPMX, IFOP, IFOM	Supply current for mixer, R_{BIAS} = 2.43 kΩ		44		mA
VPLO	Supply current for LO limiting amplifier		35		mA
Total Quiescent Current		73	84	95	mA
Power-Down Current	Device disabled		500		µA

AC PERFORMANCE

V_S = 5 V, T_A = 25°C, LO power = 0 dBm, Z_O = 50 Ω, R_{BIAS} = 2.43 kΩ, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
RF Frequency Range		400		1200	MHz
LO Frequency Range	High Side LO	470		1600	MHz
IF Frequency Range		70		400	MHz
Conversion Gain	f_{RF} = 450 MHz, f_{LO} = 550 MHz, f_{IF} = 100 MHz		9.25		dB
	f_{RF} = 890 MHz, f_{LO} = 1090 MHz, f_{IF} = 200 MHz		4.5		dB
SSB Noise Figure	f_{RF} = 450 MHz, f_{LO} = 550 MHz, f_{IF} = 100 MHz		7.75		dB
	f_{RF} = 890 MHz, f_{LO} = 1090 MHz, f_{IF} = 200 MHz		10.5		dB
Input Third-Order Intercept	f_{RF1} = 450 MHz, f_{RF2} = 451 MHz, f_{LO} = 550 MHz, f_{IF} = 100 MHz, each RF tone = −10 dBm		14		dBm
	f_{RF1} = 890 MHz, f_{RF2} = 891 MHz, f_{LO} = 1090 MHz, f_{IF} = 200 MHz, each RF tone = −10 dBm		24		dBm
Input Second-Order Intercept	f_{RF1} = 450 MHz, f_{RF2} = 500 MHz, f_{LO} = 550 MHz, f_{IF} = 100 MHz		36		dBm
	f_{RF1} = 890 MHz, f_{RF2} = 940 MHz, f_{LO} = 1090 MHz, f_{IF} = 200 MHz		51		dBm
Input 1 dB Compression Point	f_{RF} = 450 MHz, f_{LO} = 550 MHz, f_{IF} = 100 MHz		2.5		dBm
	f_{RF} = 890 MHz, f_{LO} = 1090 MHz, f_{IF} = 200 MHz		8.5		dBm
LO to IF Output Feedthrough	LO Power = 0 dBm, f_{RF} = 890 MHz, f_{LO} = 1090 MHz		−23		dBc
LO to RF Input Leakage	LO Power = 0 dBm, f_{RF} = 890 MHz, f_{LO} = 1090 MHz		−48		dBc
RF to IF Output Feedthrough	RF Power = −10 dBm, f_{RF} = 890 MHz, f_{LO} = 1090 MHz		−32		dBc
IF/2 Spurious	RF Power = −10 dBm, f_{RF} = 890 MHz, f_{LO} = 1090 MHz		−66		dBm

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage, V_S	5.5 V
RF Input Level	12 dBm
LO Input Level	12 dBm
PWDN Pin	V_S + 0.5 V
IFOP, IFOM Bias Voltage	5.5 V
Minimum Resistor from EXRB to COMM	2.4 kΩ
Internal Power Dissipation	580 mW
θ_{JA}	77°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

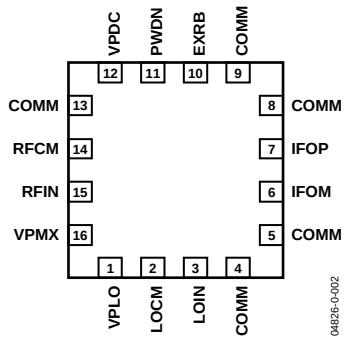

Figure 2. 16-Lead LFCSP

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	VPLO	Positive Supply Voltage for the LO Buffer: 4.75 V to 5.25 V.
2	LOCM	AC Ground for Limiting LO Amplifier, AC-Coupled to Ground.
3	LOIN	LO Input. Nominal input level 0 dBm, input level range −10 dBm to +4 dBm, re: 50 Ω, ac-coupled.
4, 5, 8, 9, 13	COMM	Device Common (DC Ground).
6, 7	IFOM, IFOP	Differential IF Outputs; Open Collectors, Each Requires DC Bias of 5.00 V (Nominal).
10	EXRB	Mixer Bias Voltage, Connect Resistor from EXRB to Ground, Typical Value of 2.43 kΩ Sets Mixer Current to Nominal Value. Minimum resistor value from EXRB to ground = 2.4 kΩ.
11	PWDN	Connect to Ground for Normal Operation. Connect pin to V_S for disable mode.
12	VPDC	Positive Supply Voltage for the DC Bias Cell: 4.75 V to 5.25 V.
14	RFCM	AC Ground for RF Input, AC-Coupled to Ground.
15	RFIN	RF Input. Must be ac-coupled.
16	VPMX	Positive Supply Voltage for the Mixer: 4.75 V to 5.25 V.

TYPICAL PERFORMANCE CHARACTERISTICS

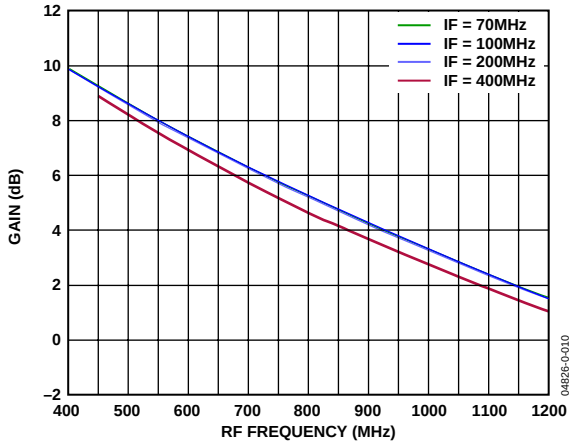

Figure 3. Conversion Gain vs. RF Frequency

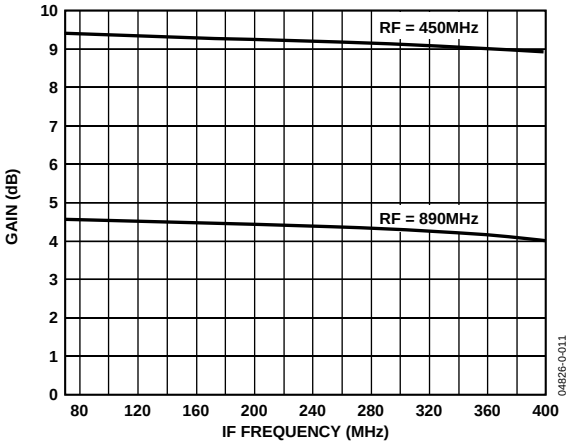

Figure 6. Conversion Gain vs. IF Frequency

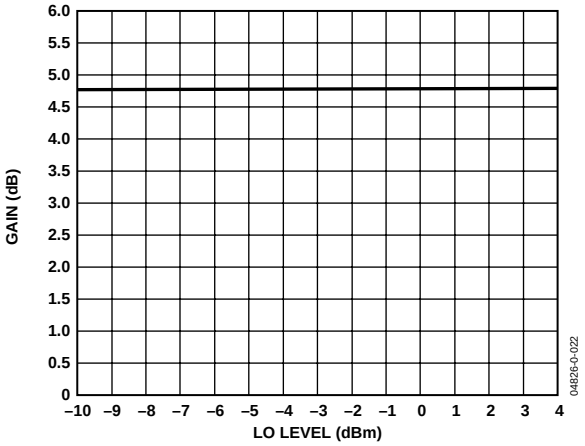

Figure 4. Conversion Gain vs. LO Power, F_{RF} = 890 MHz, F_{IF} = 200 MHz

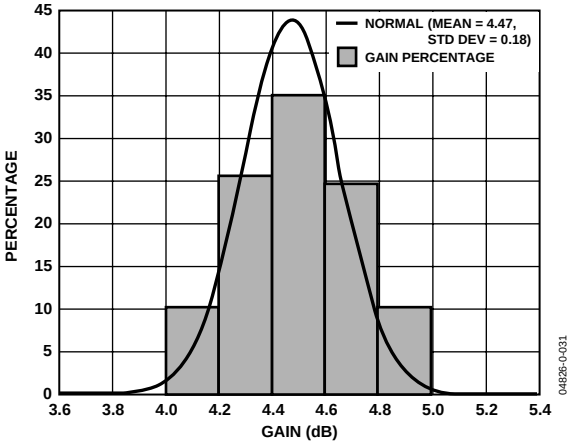

Figure 7. Conversion Gain Distribution, F_{RF} = 890 MHz, F_{IF} = 200 MHz

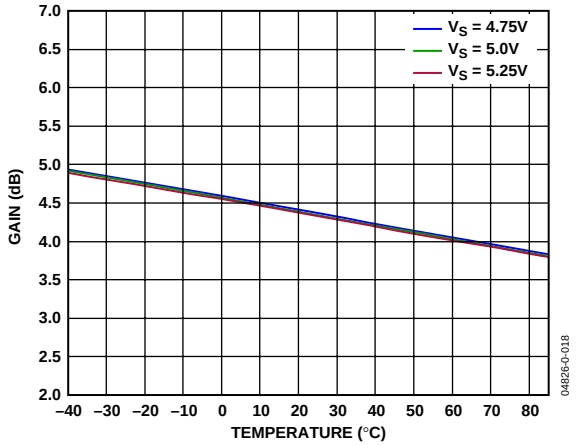

Figure 5. Conversion Gain vs. Temperature, F_{RF} = 890 MHz, F_{LO} = 1090 MHz

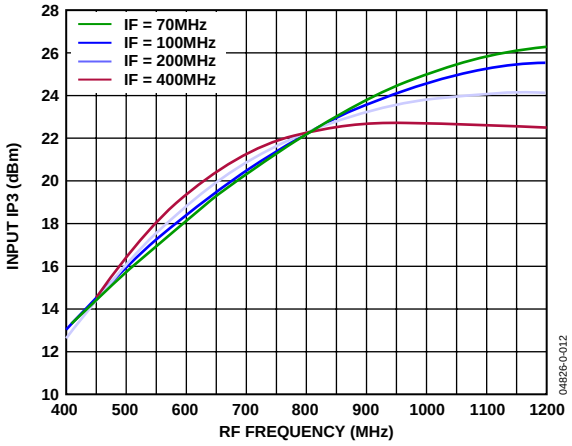

Figure 8. Input IP3 vs. RF Frequency (RF Tone Spacing = 1 MHz)

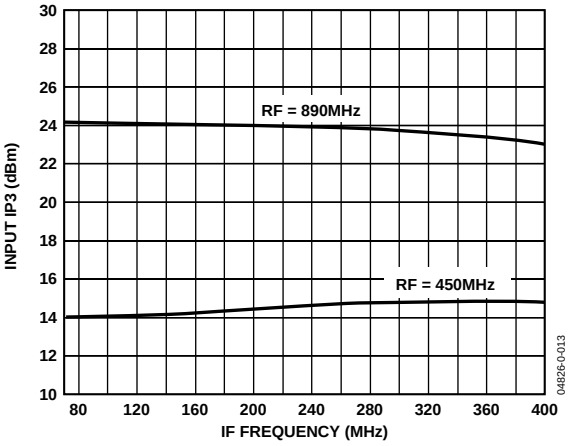

Figure 11. Input IP3 vs. IF Frequency (RF Tone Spacing = 1 MHz)

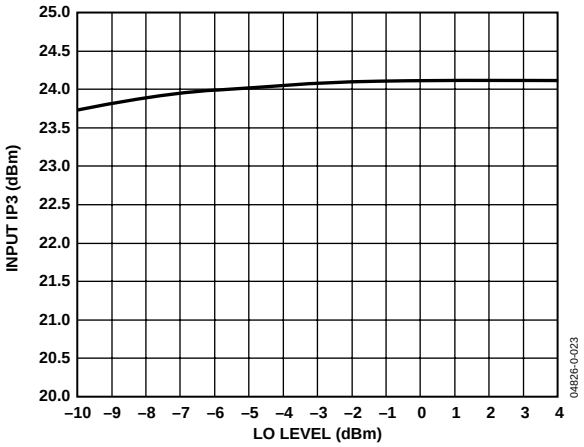

Figure 9. Input IP3 vs. LO Power,
F_{RF1} = 890 MHz, F_{RF2} = 891 MHz, F_{LO} = 1090 MHz

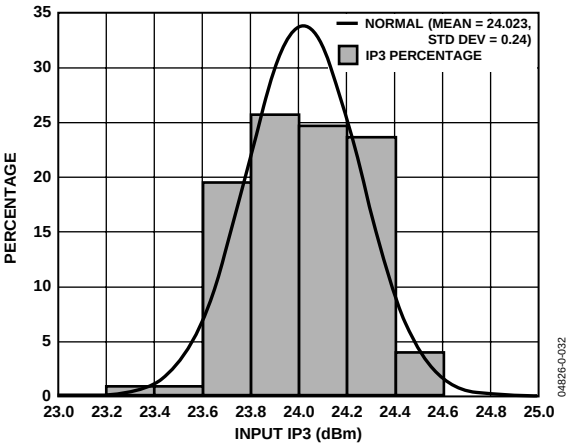

Figure 12. Input IP3 Distribution,
F_{RF1} = 890 MHz, F_{RF2} = 891 MHz, F_{LO} = 1090 MHz

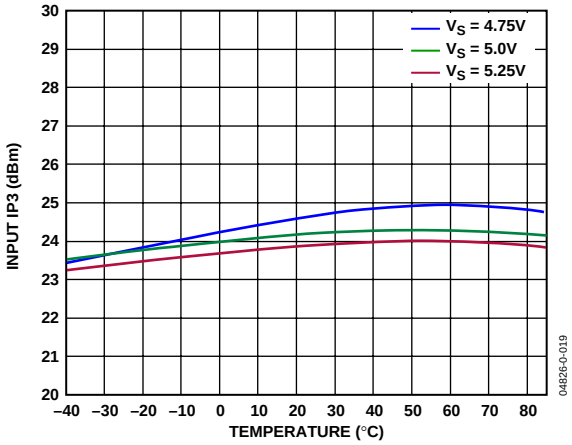

Figure 10. Input IP3 vs. Temperature,
F_{RF1} = 890 MHz, F_{RF2} = 891 MHz, F_{LO} = 1090 MHz

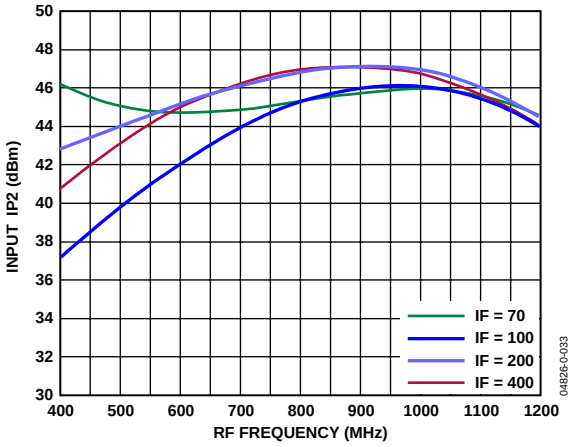

Figure 13. Input IP2 vs. RF Frequency (RF Tone Spacing = 50 MHz)

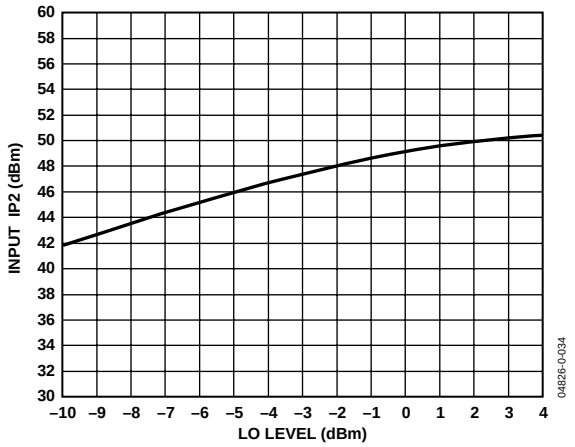

Figure 14. Input IP2 vs. LO Power,
F_{RF} = 890 MHz, F_{LO} = 1090 MHz (RF Tone Spacing = 50 MHz)

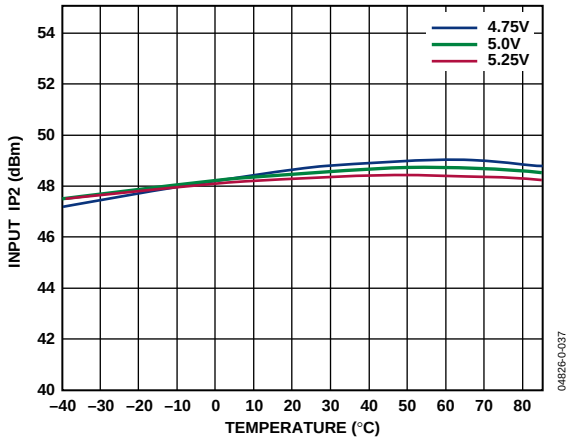

Figure 15. Input IP2 vs. Temperature, F_{RF} = 890 MHz,
F_{LO} = 1090 MHz (RF Tone Spacing = 50 MHz)

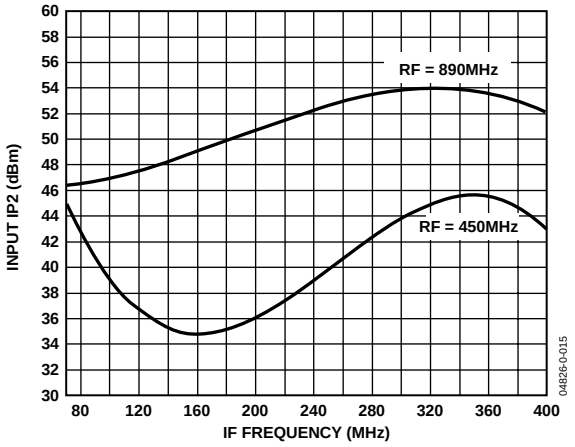

Figure 16. Input IP2 vs. IF Frequency (RF Tone Spacing = 50 MHz)

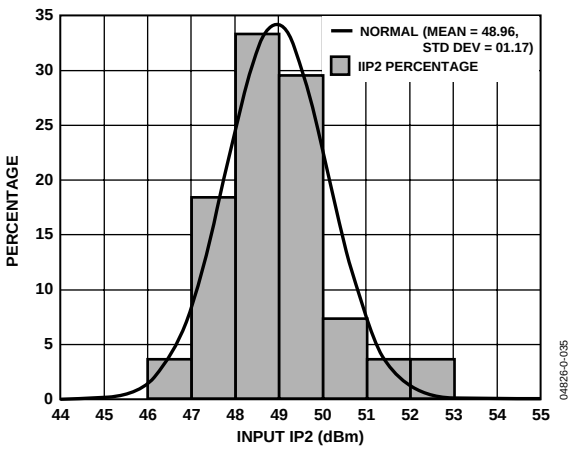

Figure 17. Input IP2 Distribution, F_{RF} = 890 MHz,
F_{LO} = 1090 MHz (RF Tone Spacing = 50 MHz)

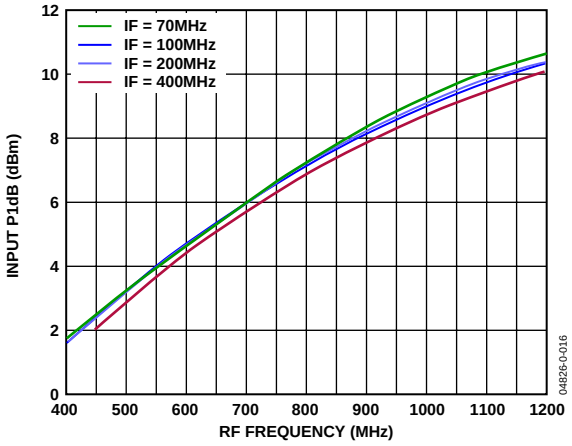

Figure 18. Input P1dB vs. RF Frequency

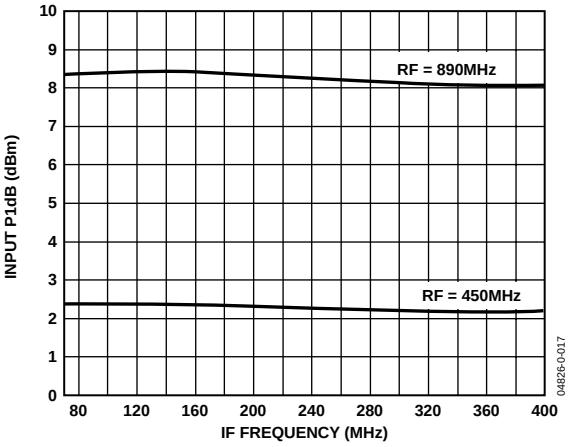

Figure 21. Input P1dB vs. IF Frequency

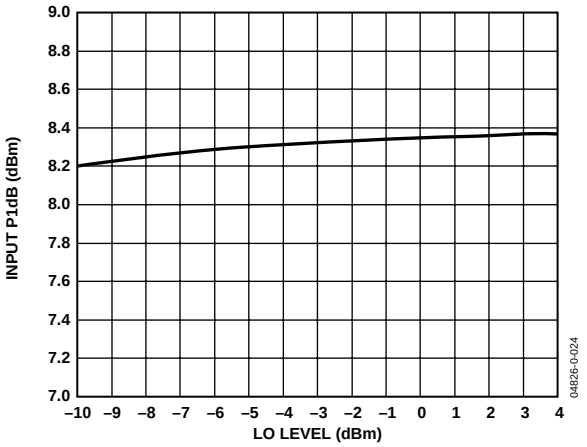

Figure 19. Input P1dB vs. LO Power, F_{RF} = 890 MHz, F_{LO} = 1090 MHz

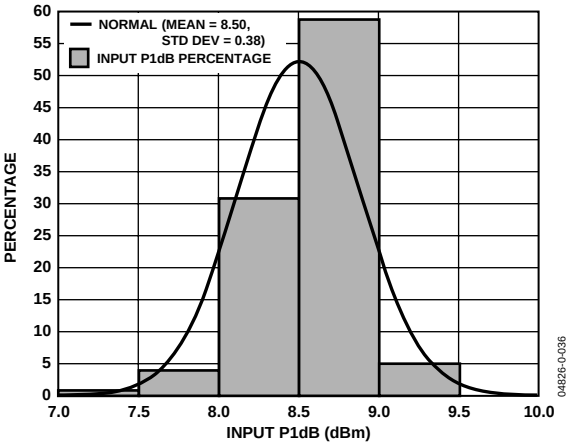

Figure 22. Input P1dB Distribution, F_{RF} = 890 MHz, F_{LO} = 1090 MHz

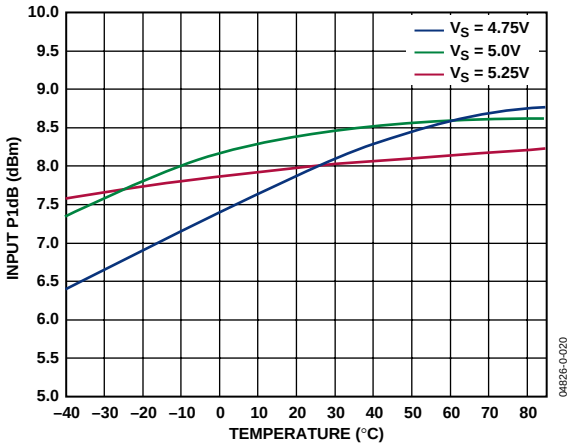

Figure 20. Input P1dB vs. Temperature, F_{RF} = 890 MHz, F_{LO} = 1090 MHz

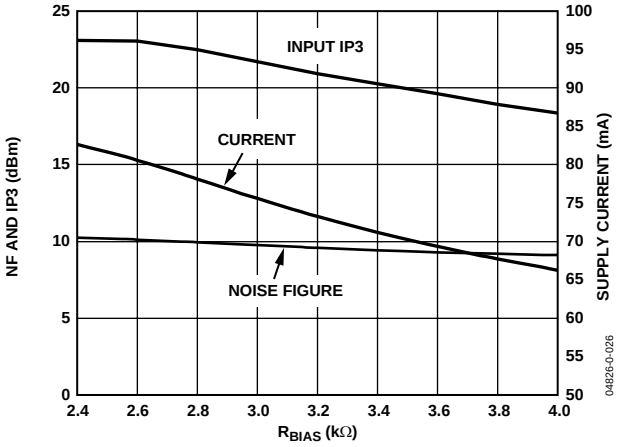

Figure 23. Noise Figure, Input IP3 and Supply Current vs. R_{BIAS}, F_{RF1} = 890 MHz, F_{RF2} = 891 MHz, F_{LO} = 1090 MHz

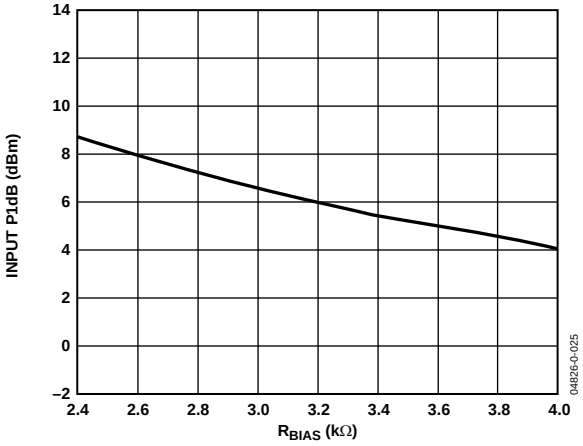

Figure 26. Input P1dB vs. R_{BIAS}, F_{RF} = 890 MHz, F_{LO} = 1090 MHz

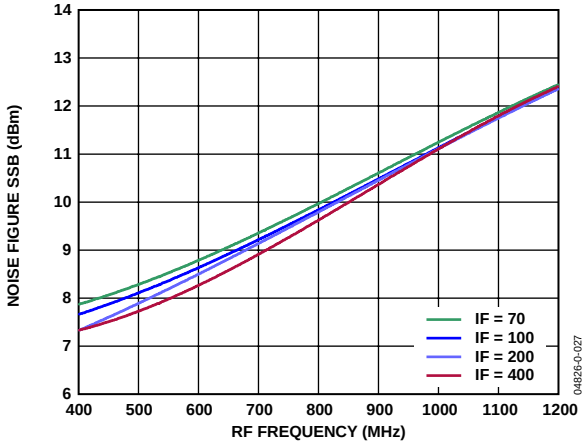

Figure 24. Noise Figure vs. RF Frequency

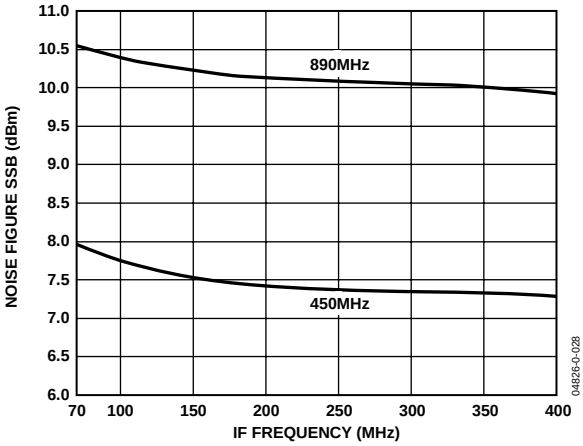

Figure 27. Noise Figure vs. IF Frequency

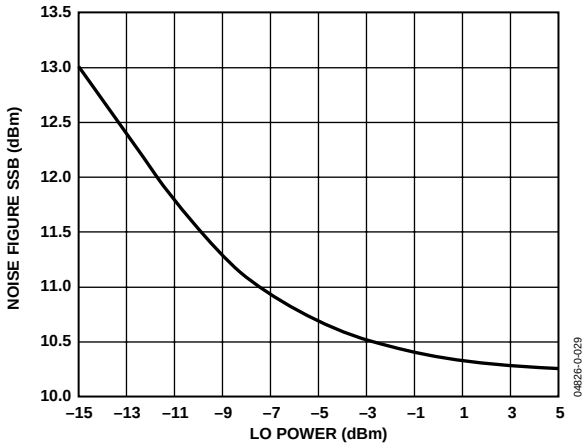

Figure 25. Noise Figure vs. LO Power, F_{RF} = 890 MHz, F_{LO} = 1090 MHz

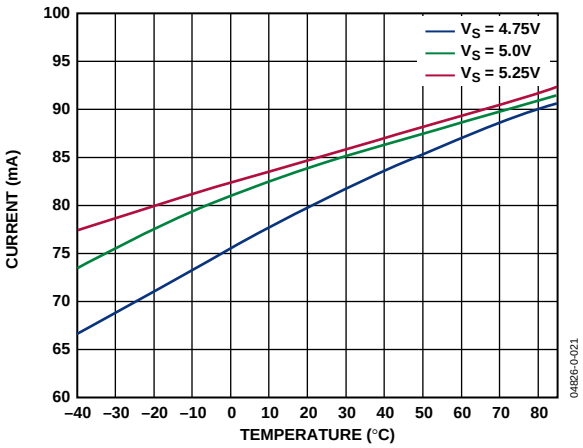

Figure 28. Total Supply Current vs. Temperature

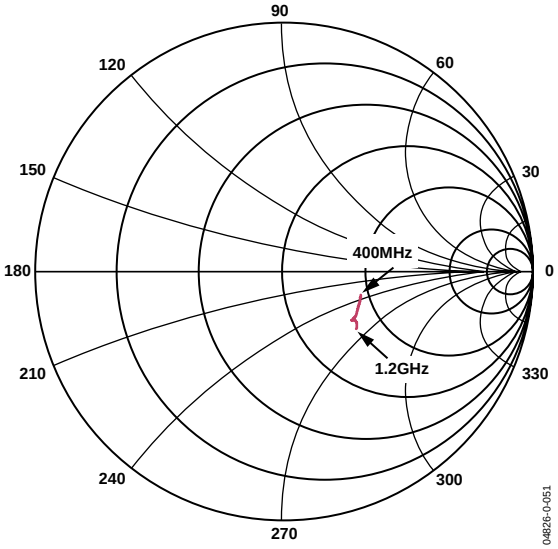

Figure 29. RFIN Return Loss vs. RF Frequency

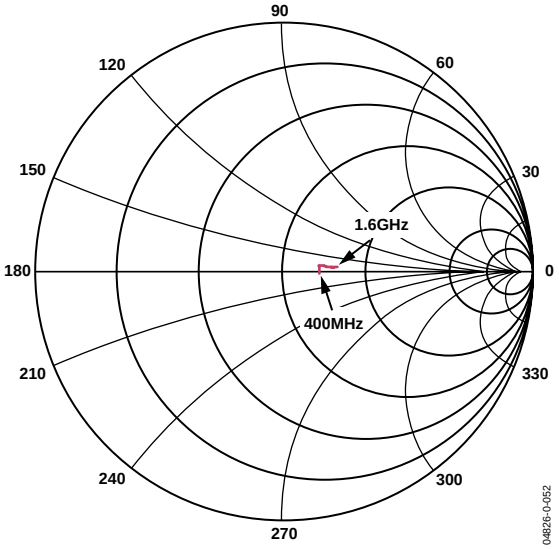

Figure 32. LOIN Return Loss vs. LO Frequency

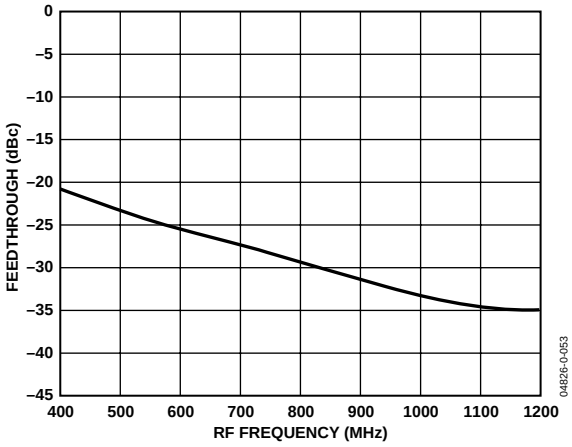

Figure 30. RF to IF Feedthrough vs. RF Frequency, F_{LO} = 1090 MHz, RF Power = –10 dBm

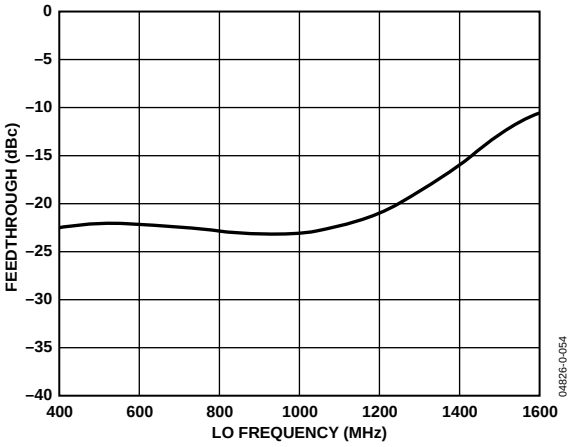

Figure 33. LO to IF Feedthrough vs. LO Frequency, LO Power = 0 dBm

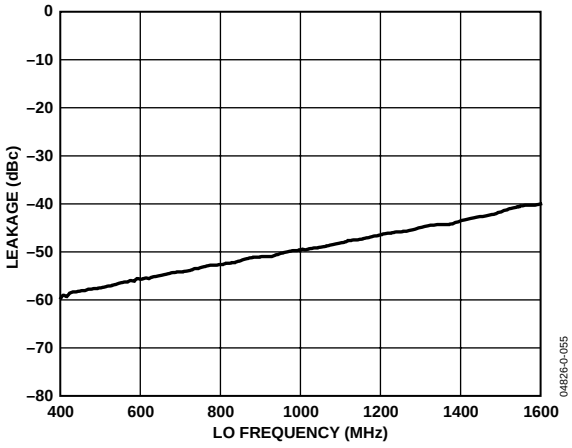

Figure 31. LO to RF Leakage vs. LO Frequency, LO Power = 0 dBm

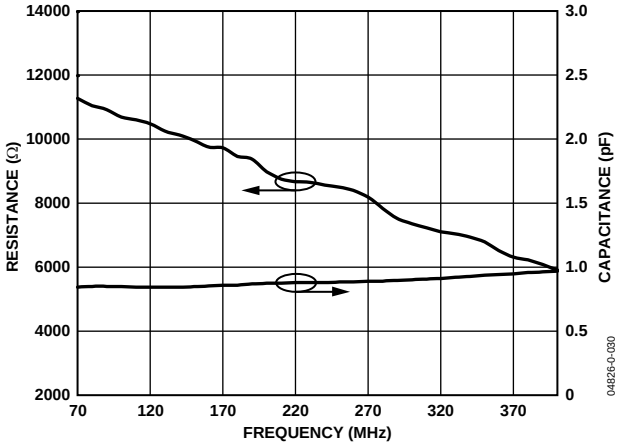

Figure 34. IF Port Output Resistance and Capacitance vs. IF Frequency

CIRCUIT DESCRIPTION

The AD8344 is a down converting mixer optimized for operation within the input frequency range of 400 MHz to 1.2 GHz. It has a single-ended, 50 Ω RF input, as well as a single-ended, 50 Ω local oscillator (LO) input. The IF outputs are differential open collectors. The mixer current can be adjusted by the value of an external resistor to optimize performance for gain compression and intermodulation or for low power operation. Figure 35 shows the basic blocks of the mixer, which includes the LO buffer, RF voltage-to-current converter, bias cell, and mixing core.

The RF voltage to RF current conversion is done via an inductively degenerated differential pair. When one side of the differential pair is ac grounded, the other input can be driven single-ended. The RF inputs can also be driven differentially. The voltage-to-current converter then drives the emitters of a four-transistor switching core. This switching core is driven by an amplified version of the local oscillator signal connected to the LO input. There are three limiting gain stages between the external LO signal and the switching core. The first stage converts the single-ended LO drive to a well balanced differential drive. The differential drive then passes through two more gain stages, which ensures a limited signal drives the switching core. This affords the user a lower LO drive requirement, while maintaining excellent distortion and compression performance. The output signal of these three LO gain stages drives the four transistors within the mixer core to commutate at the rate of the local oscillator frequency. The output of the mixer core is taken directly from these open collectors. The open collector outputs present a high impedance at the IF frequency. The conversion gain of the mixer depends directly on the impedance presented to these open collectors. In characterization, a 200 Ω load was presented to the part via a 4:1 impedance transformer.

The AD8344 also features a power-down function. Application of a logic low at the PWDN pin allows normal operation. A high logic level at the PWDN pin shuts down the AD8344. Power consumption when the part is disabled is less than 10 mW.

The bias for the mixer is set with an external resistor from the EXRB pin to ground. The value of this resistor directly affects the dynamic range of the mixer. The external resistor should not be lower than 2.4 kΩ. Permanent damage to the part will result if values below 2.4 kΩ are used.

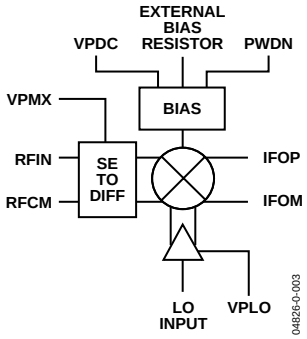

Figure 35. AD8344 Simplified Schematic

As shown in Figure 36, the IF output pins, IFOP and IFOM, are directly connected to the open collectors of the NPN transistors in the mixer core so the differential and single-ended impedances looking into this port are relatively high, on the order of several kΩ. A connection between the supply voltage and these output pins is required for proper mixer core operation.

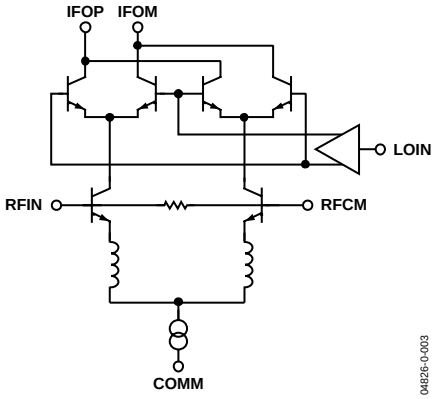

Figure 36. Mixer Core Simplified Schematic

The AD8344 has three pins for the supply voltage: VPDC, VPMX, and VPLO. These pins are separated to minimize or eliminate possible parasitic coupling paths within the AD8344 that could cause spurious signals or reduced interport isolation. Consequently, each of these pins should be well bypassed and decoupled as close to the AD8344 as possible.

AC INTERFACES

The AD8344 is a high-side downconverter. It is designed to downconvert radio frequencies (RF) to lower intermediate frequencies (IF) using a high-side local oscillator (LO). The LO is injected into the mixer core at a frequency greater than the desired input RF frequency. The difference between the LO and RF frequencies, $f_{LO} - f_{RF,}$ is the IF frequency, f_{IF}. In addition to the desired RF signal, an RF image will be downconverted to the same IF frequency. The image frequency is at $f_{LO} + f_{IF}$. The conversion gain of the AD8344 decreases with increasing input frequency. By choosing to use a high-side LO the image frequency at $f_{LO} + f_{IF}$ is translated with less conversion gain than the desired RF signal at $f_{LO} - f_{IF}$. Additionally, any wideband noise present at the image frequency will be downconverted with less conversion gain than would be the case if a low-side LO was applied. In general, a high-side LO should be used with the AD8344 to ensure optimal noise performance and image rejection.

The AD8344 is designed to operate using RF frequencies in the 400 MHz to 1200 MHz frequency range, with high-side LO injection within the 470 MHz to 1600 MHz range. It is essential to ac-couple RF and LO ports to prevent dc offsets from skewing the mixer core in an asymmetrical manner, potentially degrading linear input swing and impacting distortion and input compression characteristics.

The AD8344 RFIN port presents a 50 Ω impedance relative to RFCM. In order to ensure a good impedance match, the RFIN ac-coupling capacitor should be large enough in value so that the presented reactance is negligible at the intended RF frequency. Additionally, the RFCM bypassing capacitor should be sufficiently large to provide a low impedance return path to board ground. Low inductance ceramic grade capacitors of no more than 330 pF are sufficient for most applications.

Similarly the LOIN port provides a 50 Ω load impedance with common-mode decoupling on LOCM. Again, common grade ceramic capacitors will provide sufficient signal coupling and bypassing of the LO interface.

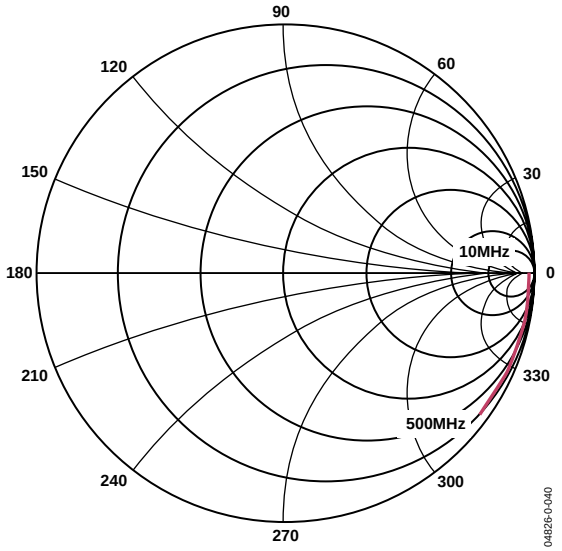

Figure 37. IF Port Reflection Coefficient from 10 MHz to 500 MHz

IF PORT

The IF port uses an open collector differential output interface. The NPN open collectors can be modeled as high impedance current sources. The stray capacitance associated with the IC package presents a slightly capacitive source impedance as in Figure 37. In general, the IFOP and IFOM output ports can be modeled as current sources with an impedance of ~10 kΩ in parallel with ~1 pF of shunt capacitance. Circuit board traces connecting the IF outputs to the load should be narrow and short to prevent excessive capacitive loading. In order to maintain the specified conversion gain of the mixer, the IF output ports should be loaded into 200 Ω. It is not necessary to attempt to provide a conjugate match to the IF port output source impedance. If the IF signal needs to be delivered to a remote load, more than a few centimeters away, it may be necessary to use an appropriate buffer amplifier to present a real 200 Ω loading impedance at the IF output interface. The buffer amplifier should have the appropriate source impedance to match the characteristic impedance of the selected transmission line. An example is provided in Figure 38, where the AD8351 differential amplifier is used to drive a pair of 75 Ω transmission lines. The gain of the buffer can be independently set by choosing an appropriate gain resistor, R_G.

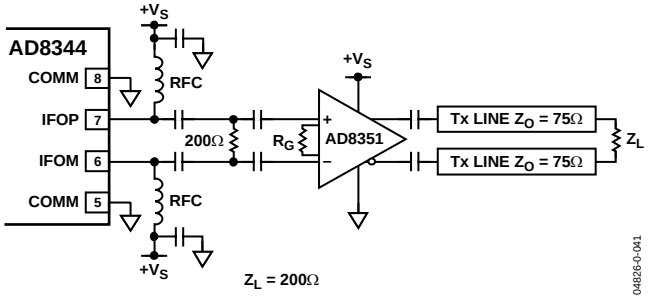

Figure 38. AD8351 Used as Transmission Line Driver and Impedance Buffer

The high input impedance of the AD8351 allows for a shunt differential termination to provide the desired 200 Ω load to the AD8344 IF output port.

It is necessary to bias the open collector outputs using one of the schemes presented in Figure 39 and Figure 40. Figure 39 illustrates the application of a center-tapped impedance transformer. The turns ratio of the transformer should be selected to provide the desired impedance transformation. In the case of a 50 Ω load impedance, a 4-to-1 impedance ratio transformer should be used to transform the 50 Ω load into a 200 Ω differential load at the IF output pins. Figure 40 illustrates a differential IF interface where pull-up choke inductors are used to bias the open-collector outputs. The shunting impedance of the choke inductors used to couple dc current into the mixer core should be large enough at the IF frequency of operation as to not load down the output current before reaching the intended load. Additionally, the dc current handling capability of the selected choke inductors needs to be at least 45 mA. The self resonant frequency of the selected choke should be higher than the intended IF frequency. A variety of suitable choke inductors are commercially available from manufacturers such as Murata and Coilcraft. An impedance transforming network may be required to transform the final load impedance to 200 Ω at the IF outputs. There are several good reference books that explain general impedance matching procedures, including:

- Chris Bowick, *RF Circuit Design*, Newnes, Reprint Edition, 1997.
- David M. Pozar, *Microwave Engineering*, Wiley Text Books, Second Edition, 1997.
- Guillermo Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*, Prentice Hall, Second Edition, 1996.

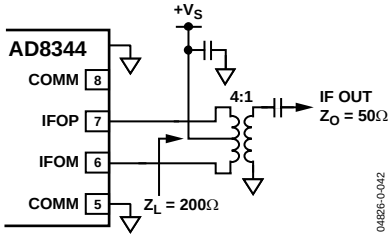

Figure 39. Biasing the IF Port Open Collector Outputs Using a Center-Tapped Impedance Transformer

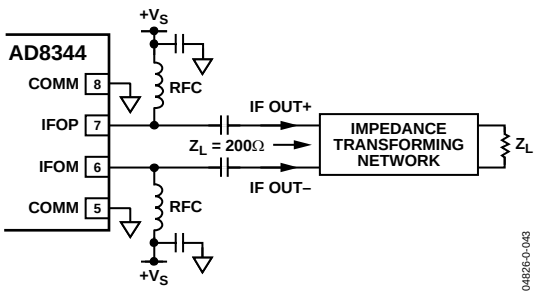

Figure 40. Biasing the IF Port Open Collector Outputs Using Pull-Up Choke Inductors

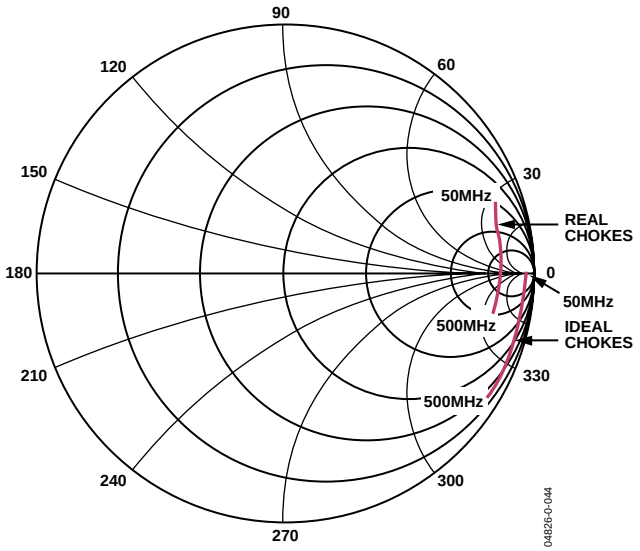

Figure 41. IF Port Loading Effects due to Finite-Q Pull-Up Inductors (Murata BLM18HD601SN1D Chokes)

LO CONSIDERATIONS

The LO signal needs to have adequate phase noise characteristics and reasonable low second harmonic content to prevent degradation of the noise figure performance of the AD8344. A LO plagued with poor phase noise can result in reciprocal mixing, a mechanism that causes spectral spreading of the downconverted signal, limiting the sensitivity of the mixer at frequencies close-in to any large input signals. The internal LO buffer provides enough gain to hard limit the input LO and provide fast switching of the mixer core. Odd harmonic content present on the LO drive signal should not impact mixer performance; however, even-order harmonics cause the mixer core to commutate in an unbalanced manner, potentially degrading noise performance. Simple lumped element low-pass filtering can be applied to help reject the harmonic content of a given local oscillator, as illustrated in Figure 42. The filter depicted is a common 3-pole Chebyshev, designed to maintain a 1-to-1 source-to-load impedance ratio with no more than 0.5 dB of ripple in the pass band. Other filter structures can be effective as long as the second harmonic of the LO is filtered to negligible levels, e.g., ~30 dB below the fundamental. The measured frequency response of the Chebyshev filter for a 1200 MHz −3 dB cutoff frequency is presented in Figure 43.

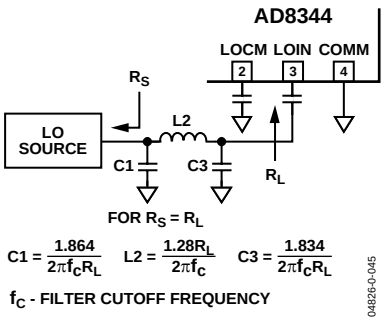

Figure 42. Using a Low-Pass Filter to Reduce LO Second Harmonic

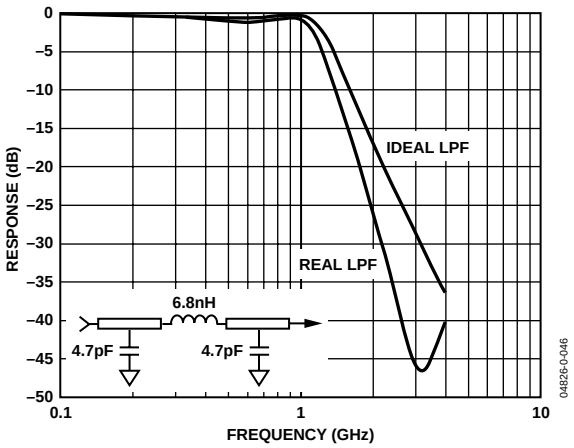

Figure 43. Measured and Ideal LO Filter Frequency Response

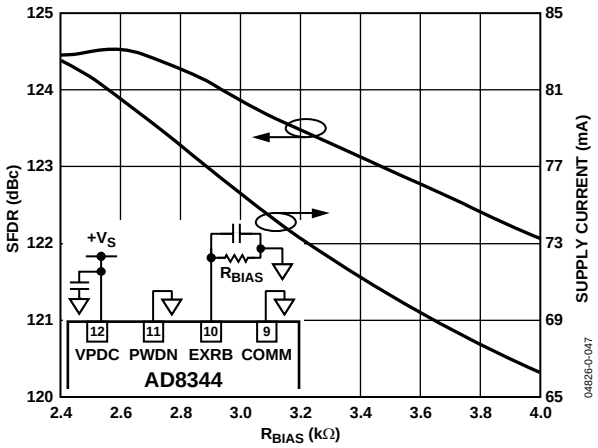

Figure 44. Impact of R_{BIAS} Resistor Selection vs. Spurious-Free Dynamic Range and Power Consumption, F_{RF} = 890 MHz and F_{LO} = 1090 MHz

BIAS RESISTOR SELECTION

An external bias resistor is used to set the dc current in the mixer core. This provides the ability to reduce power consumption at the expense of decreased dynamic range. Figure 44 shows the spurious-free dynamic range (SFDR) of the mixer for a 1 Hz noise bandwidth versus the R_{BIAS} resistor value. SFDR was calculated using NF and IIP3 data collected at 900 MHz.

By definition,

$$SFDR = \tfrac{2}{3}\left(IIP3 - NF - kT - 10\log(B)\right)$$

where *IIP3* is the input third-order intercept in dBm. *NF* is the noise figure in dB. *kT* is the thermal noise power density and is −173.86 dBm/Hz at 298°K. *B* is the noise bandwidth in Hz.

In order to calculate the anticipated SFDR for a given application, it is necessary to factor in the actual noise bandwidth. For instance, if the IF noise bandwidth was 5 MHz, the anticipated SFDR using a 2.43 kΩ R_{BIAS} would be 6.66 log10 (5 MHz) less than the 1 Hz data in Figure 44 or ~80 dBc. Using a 2.43 kΩ bias resistor will set the quiescent power dissipation to ~415 mW for a 5 V supply. If the R_{BIAS} resistor value was raised to 3.9 kΩ, the SFDR for the same 5 MHz bandwidth would be reduced to ~77.5 dBc and the power dissipation would be reduced to ~335 mW. In low power portable applications it may be advantageous to reduce power consumption by using a larger value of R_{BIAS}, assuming reduced dynamic range performance is acceptable.

CONVERSION GAIN AND IF LOADING

The AD8344 is optimized for driving a 200 Ω differential load. Although the device is capable of driving a wide variety of loads, in order to maintain optimum distortion and noise performance, it is advised that the presented load at the IF outputs is reasonably close to 200 Ω. Figure 45 illustrates the effect of IF loading on conversion gain. The mixer outputs behave like Norton equivalent sources, where the conversion gain is the effective transconductance of the mixer multiplied by the loading impedance. The linear differential voltage conversion gain of the mixer can be modeled as

$$Av = -0.46 \times R_{LOAD} \times \frac{g_m}{1 + j \times g_m \times 37.70 \times f_{RF}}$$

where R_{LOAD} is the differential loading impedance. g_m is the mixer transconductance and is equal to 4070/R_{BIAS}. f_{RF} is the frequency of the signal applied to the RF port in GHz.

Large impedance loads cause the conversion gain to increase, resulting in a decrease in input linearity and allowable signal swing. In order to maintain positive conversion gain and preserve spurious-free dynamic range performance, the differential load presented at the IF port should remain within a range of ~100 Ω to 250 Ω.

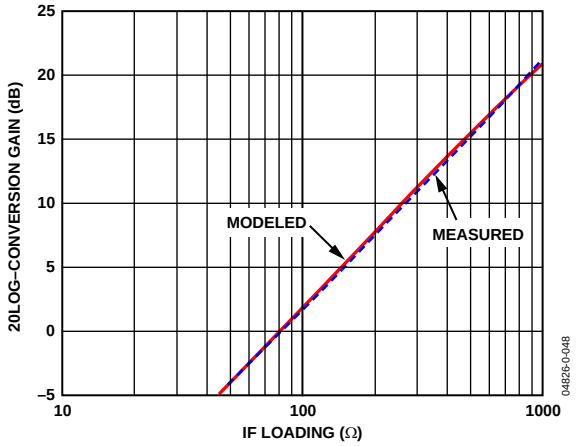

Figure 45. Conversion Gain vs. IF Loading

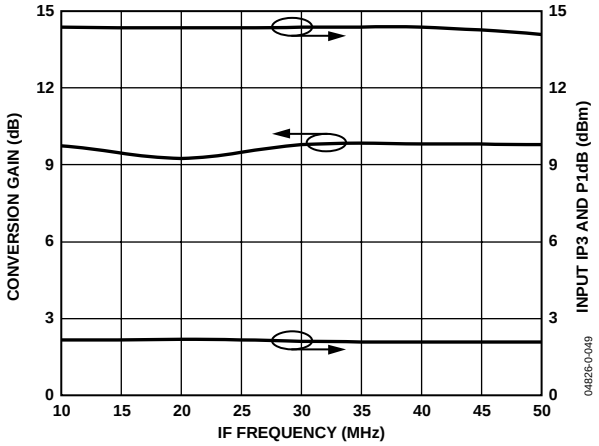

Figure 46. Conversion Gain, Input IP3, and P1dB vs. IF Frequency, F_{RF} = 450 MHz

LOW IF FREQUENCY OPERATION

The AD8344 may be used down to arbitrarily low IF frequencies. The conversion gain, noise, and linearity characteristics remain quite flat as IF frequency is reduced, as indicated in Figure 46 and Figure 47. Larger value pull-up inductors need to be used at the lower IF frequencies. A 1 µH choke inductor would present a common-mode loading impedance of 63 Ω at an IF frequency of 10 MHz, severely loading down the mixer outputs, reducing conversion gain, and sacrificing output power. At low IF frequencies, choke inductors of several hundred µH should be used for biasing the IF outputs.

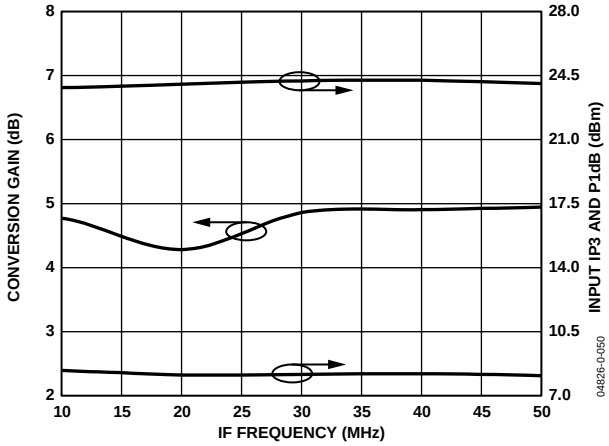

Figure 47. Conversion Gain, Input IP3, and P1dB vs. IF Frequency, F_{RF} = 890 MHz

EVALUATION BOARD

An evaluation board is available for the AD8344. The evaluation board is configured for single-ended signaling at the IF output port via a balun transformer. The schematic for the evaluation board is presented in Figure 48.

Table 5. Evaluation Boards Configuration Options

Component	Function	Default Conditions
R1, R2, R7, C2, C4, C5, C6, C12, C13, C14, C15	**Supply Decoupling**. Jumpers or power supply decoupling resistors and filter capacitors.	R1, R2, R7 = 0 Ω (Size 0603) C4, C6, C13, C14 = 100 pF (Size 0603) C2, C5, C12, C15 = 0.1 µF (Size 0603)
R3, R4	Jumpers in Single-Ended IF Output Circuit.	0 Ω (Size 0603)
R6, C11	R_{BIAS} resistor that sets the bias current for the mixer core. The capacitor provides ac bypass for R6.	R6 = 2.43 kΩ (Size 0603) C11 = 100 pF (Size 0603)
R8	Jumper for pull down of the PWDN pin.	R8 = 10 kΩ (Size 0603)
R9	Jumper.	R9 = 0 Ω (Size 0603)
C3	**RF Input AC Coupling**. Provides dc block for RF input.	C3 = 100 pF (Size 0402)
C1	**RF Common AC Coupling**. Provides dc block for RF input common connection.	C1 = 100 pF (Size 0402)
C8	**LO Input AC Coupling**. Provides dc block for the LO input.	C8 = 100 pF (Size 0402)
C7	**LO Common AC Coupling**. Provides dc block for LO input common connection.	C7 = 100 pF (Size 0402)
SW1	**Power Down**. The part is on when the PWDN is connected to ground via SW1. The part is disabled when PWDN is connected to the positive supply (V_S) via SW1.	
T1	**IF Output Balun Transformer**. Converts differential, high impedance IF output to single-ended. When loaded with 50 Ω, this balun presents a 200 Ω load to the mixers collectors. The center tap of the primary is used to supply the bias voltage (V_S) to the IF output pins.	T1 = TC4-1W, 4:1 (Mini-Circuits)
R11, Z3, Z4 R12, Z1, Z2	**IF Output Interface**—IFOP, IFOM. These positions can be used to modify the impedance presented to the IF outputs.	R11 = 0 Ω (Size 0603) Z3, Z4 = Open R12 = 0 Ω (Size 0603) Z1, Z2 = Open

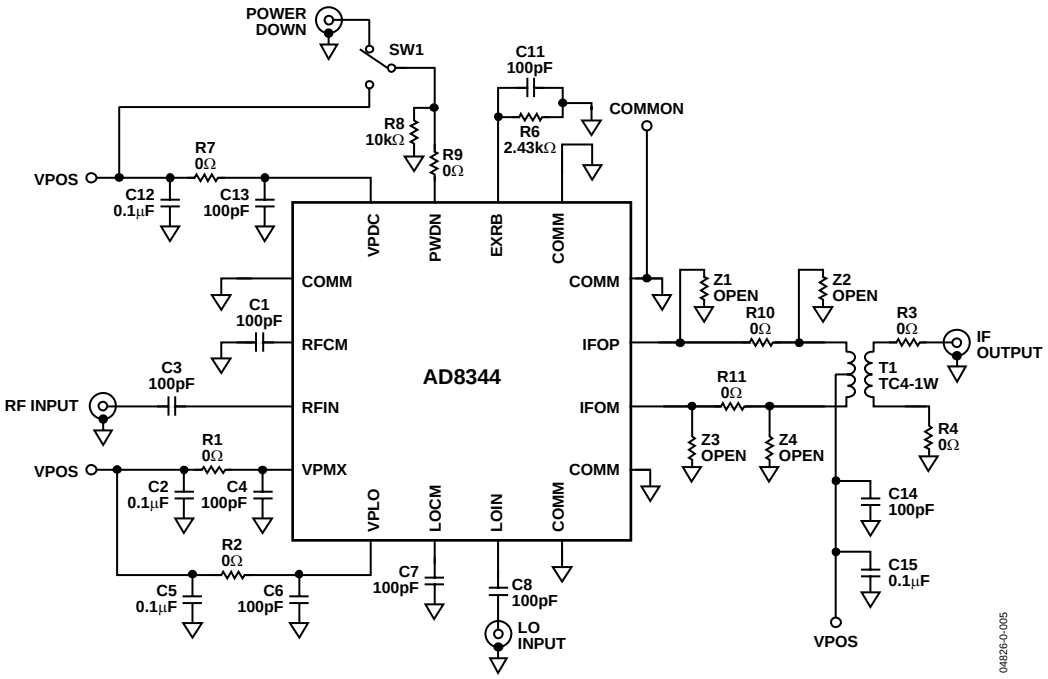

Figure 48. Evaluation Board Schematic—Single-Ended IF Output

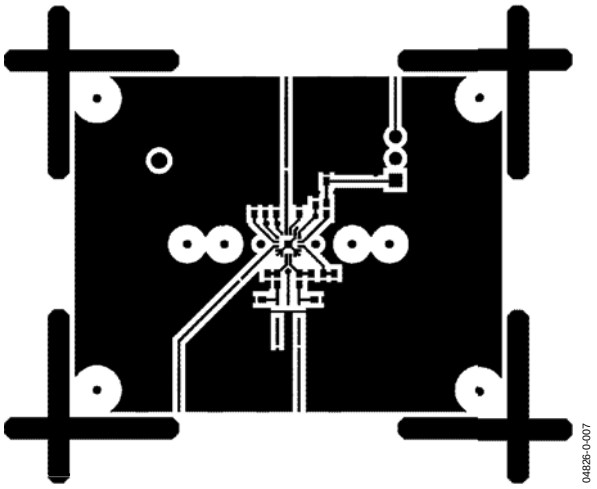

Figure 49. Single-Ended Evaluation Board, Component Side Layout

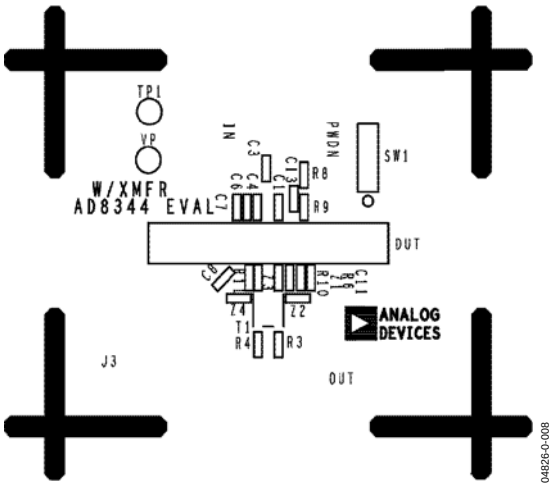

Figure 50. Single-Ended Evaluation Board, Component Side Silkscreen

OUTLINE DIMENSIONS

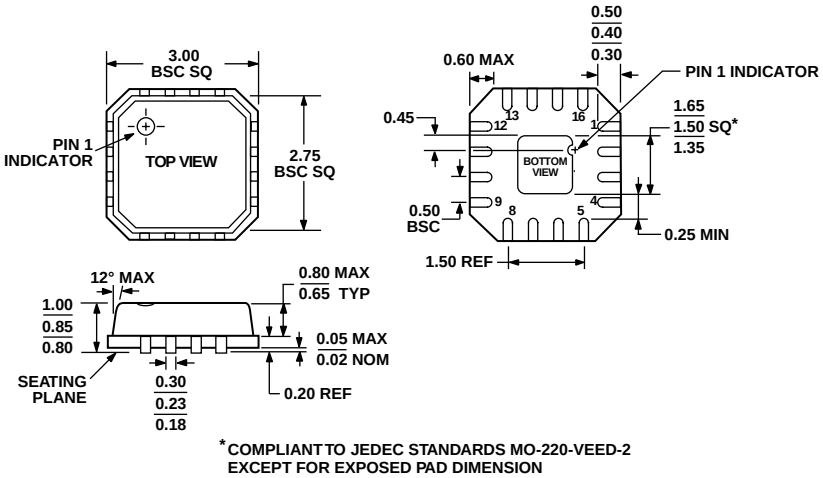

Figure 51. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body (CP-16-3)
Dimensions in millimeters

ORDERING GUIDE

Models	Temperature Range	Package Description	Package Option	Branding
AD8344ACPZ-REEL7[1]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package (LFCSP)	CP-16-3	JHA
AD8344ACPZ-WP[1, 2]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package (LFCSP)	CP-16-3	JHA
AD8344-EVAL		Evaluation Board		

[1] Z = Pb-free part.
[2] WP = Waffle pack.

D04826–0–6/04(0)