16-Bit 500 kSPS PulSAR Unipolar ADC with Referen

AD7666

FEATURES

2.5 V internal reference: typical drift 3 ppm/°C
Guaranteed max drift 15 ppm/°C
Throughput: 500 kSPS
INL: –2.0 LSB max (–0.0038% of full scale)
16-bit resolution with no missing codes
S/(N+D): 88 dB min @ 20 kHz
THD: 96 dB max @ 20 kHz
Analog input voltage range: 0 V to 2.5 V
Both AC and DC specifications
No pipeline delay
Parallel and serial 5 V/3 V interface
SPI/QSPI™/MICROWIRE™/DSP compatible
Single 5 V supply operation
Power dissipation
66 mW typ, 132 µW @ 1 kSPS without REF
81 mW typ with REF
48-lead LQFP and 48-lead LFCSP packages
Pin-to-pin compatible with PulSAR ADCs

APPLICATIONS

Data acquisition
Medical instruments
Digital signal processing
Spectrum analysis
Instrumentation
Battery-powered systems
Process control

GENERAL DESCRIPTION

The AD7666* is a 16-bit, 500 kSPS, charge redistribution SAR analog-to-digital converter that operates from a single 5 V power supply. The part contains a high speed, 16-bit sampling ADC, an internal conversion clock, internal reference, error correction circuits, and both serial and parallel system interface ports. The AD7666 is hardware factory-calibrated and comprehensively tested to ensure ac parameters such as signal-to-noise ratio (SNR) and total harmonic distortion (THD), in addition to the more traditional dc parameters of gain, offset, and linearity.

The AD7666 is available in a 48-lead LQFP and a tiny 48-lead LFCSP, with operation specified from –40°C to +85°C.

*Patent Pending.

FUNCTIONAL BLOCK DIAGRAM

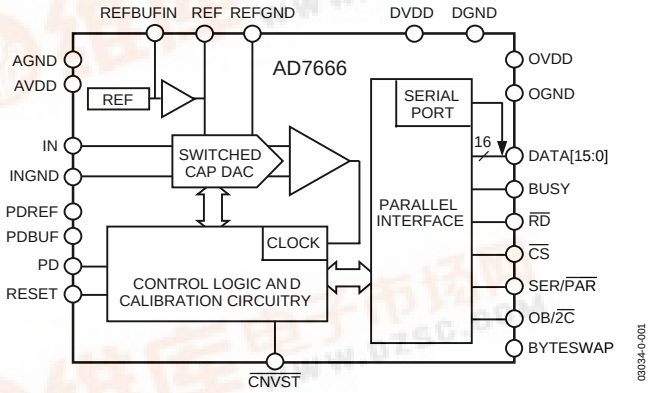

Figure 1. Functional Block Diagram

Table 1. PulSAR Selection

Type/kSPS	100 250	500 570	800 1000
Pseudo-Differential	AD7651 AD7660/AD7661	AD7650/AD7652 AD7664/AD7666	AD7653 AD7667
True Bipolar	AD7663	AD7665	AD7671
True Differential	AD7675	AD7676	AD7677
18-Bit	AD7678	AD7679	AD7674
Multichannel/ Simultaneous		AD7654 AD7655	

PRODUCT HIGHLIGHTS

1. Fast Throughput.
The AD7666 is a 500 kSPS, charge redistribution, 16-bit SAR ADC with internal error correction circuitry.
2. Superior INL.
The AD7666 has a maximum integral nonlinearity of 2.0 LSB with no missing 16-bit codes.
3. Internal Reference.
The AD7666 has an internal reference with a typical temperature drift of 3 ppm/°C.
4. Single-Supply Operation.
The AD7666 operates from a single 5V supply. Its power dissipation decreases with throughput.
5. Serial or Parallel Interface.
Versatile parallel or 2-wire serial interface arrangement is compatible with both 3V and 5V logic.

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REVISION HISTORY

Revision 0: Initial Version

SPECIFICATIONS

Table 2. …40°C to +85°C, AVDD = DVDD = 5 V, VDD = 2.7 V to 5.25 V, unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION			16		Bits
ANALOG INPUT					
Voltage Range	V_{IN} … V_{GND}	0		V_{REF}	V
Operating Input Voltage	V_{IN}	…0.1		+3	V
	V_{INGND}	…0.1		+0.5	V
Analog Input CMRR	f_{IN} = 10 kHz		65		dB
Input Current	500 kSPS Throughput		7.7		µA
Input Impedance[1]					
THROUGHPUT SPEED					
Complete Cycle				2	µs
Throughput Rate		0		500	kSPS
DC ACCURACY					
Integral Linearity Error		…2.0		+2.0	[2]LSB
No Missing Codes		16			Bits
Differential Linearity Error		…1.0		+1.5	LSB
Transition Noise			0.7		LSB
Unipolar Zero Error, T_{MIN} to T_{MAX}[3]				±5	LSB
Unipolar Zero Error Temperature Drift			±0.5		ppm/°C
Full-Scale Error, T_{MIN} to T_{MAX}[3]	REF = 2.5 V			±0.08	% of FSR
Full-Scale Error Temperature Drift			±1.4		ppm/°C
Power Supply Sensitivity	AVDD = 5 V ± 5%		±2		LSB
AC ACCURACY					
Signal-to-Noise	f_{IN} = 20 kHz	88	89.2		[4]dB
Spurious Free Dynamic Range	f_{IN} = 20 kHz	96	107		dB
Total Harmonic Distortion	f_{IN} = 20 kHz		…106	…96	dB
Signal-to-(Noise + Distortion)	f_{IN} = 20 kHz	88	89.1		dB
	…60 dB Input, f_{IN} = 20 kHz		30		dB
…3 dB Input Bandwidth			12		MHz
SAMPLING DYNAMICS					
Aperture Delay			2		ns
Aperture Jitter			5		ps rms
Transient Response	Full-Scale Step			750	ns
REFERENCE					
Internal Reference Voltage	V_{REF} @ 25°C	2.493	2.5	2.507	V
Internal Reference Temperature Drift[2]	…40°C to +85°C		±3	±15	ppm/°C
Output Voltage Hysteresis	…40°C to +85°C		50		ppm
Long Term Drift			100		ppm/1000 Hours
Line Regulation	AVDD = 5 V ± 5%		±15		ppm/V
Turn-On Settling Time	C_{REF} = 10 µF		5		ms
Temperature Pin					
Voltage Output @ 25°C			300		mV
Temperature Sensitivity			1		mV/°C
Output Resistance			4		k
External Reference Voltage Range		2.3	2.5	AVDD … 1.85	V
External Reference Current Drain	500 kSPS Throughput		120		µA

Parameter	Conditions	Min	Typ	Max	Unit
DIGITAL INPUTS					
Logic Levels					
V_{IL}		…0.3		+0.8	V
V_{IH}		2.0		DVDD + 0.3	V
I_{IL}		…1		+1	µA
I_{IH}		…1		+1	µA
DIGITAL OUTPUTS					
Data Format[5]					
Pipeline Delay[6]					
V_{OL}	I_{SINK} = 1.6 mA			0.4	V
V_{OH}	I_{SOURCE} = …500 µA	OVDD … 0.6			V
POWER SUPPLIES					
Specified Performance					
AVDD		4.75	5	5.25	V
DVDD		4.75	5	5.25	V
OVDD		2.7		5.25[7]	V
Operating Current	500 kSPS Throughput				
AVDD[8]	With Reference and Buffer		12.2		mA
AVDD[9]	Reference and Buffer Alone		3		mA
DVDD[10]			4.1		mA
OVDD[10]			102		µA
Power Dissipation without REF[8, 10]	500 kSPS Throughput		66	75	mW
	1 kSPS Throughput		132		µW
Power Dissipation with REF[8, 10]	500 kSPS Throughput		81	90	mW
TEMPERATURE RANGE[11]					
Specified Performance	T_{MIN} to T_{MAX}	…40		+85	°C

[1] See Analog Input section.
[2] LSB means least significant bit. With the 0 V to 2.5 V input range, 1 LSB is 38.15 µV.
[3] See the Definitions of Specifications section. These specifications do not include the error contribution from the external reference.
[4] All specifications in dB are referred to a full-scale input FS. Tested with an input signal at 0.5 dB below full-scale unless otherwise specified.
[5] Parallel or Serial 16-Bit.
[6] Conversion results are available immediately after completed conversion.
[7] The max should be the minimum of 5.25 V and DVDD + 0.3 V.
[8] With REF, PDREF and PDBUF are LOW, with REF, PDREF and PDBUF are HIGH.
[9] With PDREF, PDBUF LOW and PD HIGH.
[10] Tested in parallel reading mode.
[11] Consult factory for extended temperature range.

TIMING SPECIFICATIONS

Table 3. …40°C to +85°C, AVDD = DVDD = 5.0 V, OVDD = 2.7 V to 5.25 V, unless otherwise noted

Parameter	Symbol	Min	Typ	Max	Unit
Refer to Figure 33 and Figure 34					
Convert Pulse Width	t_1	10			ns
Time between Conversions	t_2	2			µs
$\overline{CNVST}$ LOW to BUSY HIGH Delay	t_3			35	ns
BUSY HIGH All Modes Except Master Serial Read after Convert	t_4			1.25	µs
Aperture Delay	t_5		2		ns
End of Conversion to BUSY LOW Delay	t_6	10			ns
Conversion Time	t_7			1.25	µs
Acquisition Time	t_8	750			ns
RESET Pulse Width	t_9	10			ns
Refer to Figure 35, Figure 36, and Figure 37 (Parallel Interface Modes)					
$\overline{CNVST}$ LOW to DATA Valid Delay	t_{10}			1.25	µs
DATA Valid to BUSY LOW Delay	t_{11}	12			ns
Bus Access Request to DATA Valid	t_{12}			45	ns
Bus Relinquish Time	t_{13}	5		15	ns
Refer to Figure 39 and Figure 40 (Master Serial Interface Modes)[1]					
$\overline{CS}$ LOW to SYNC Valid Delay	t_{14}			10	ns
$\overline{CS}$ LOW to Internal SCLK Valid Delay[2]	t_{15}			10	ns
$\overline{CS}$ LOW to SDOUT Delay	t_{16}			10	ns
$\overline{CNVST}$ LOW to SYNC Delay	t_{17}		525		ns
SYNC Asserted to SCLK First Edge Delay	t_{18}	3			ns
Internal SCLK Period[2]	t_{19}	25		40	ns
Internal SCLK HIGH[2]	t_{20}	12			ns
Internal SCLK LOW[2]	t_{21}	7			ns
SDOUT Valid Setup Time[2]	t_{22}	4			ns
SDOUT Valid Hold Time[2]	t_{23}	2			ns
SCLK Last Edge to SYNC Delay[2]	t_{24}	3			ns
$\overline{CS}$ HIGH to SYNC HI-Z	t_{25}			10	ns
$\overline{CS}$ HIGH to Internal SCLK HI-Z	t_{26}			10	ns
$\overline{CS}$ HIGH to SDOUT HI-Z	t_{27}			10	ns
BUSY HIGH in Master Serial Read after Convert[2]	t_{28}		See Table 4		
$\overline{CNVST}$ LOW to SYNC Asserted Delay	t_{29}		1.25		µs
SYNC Deasserted to BUSY LOW Delay	t_{30}		25		ns
Refer to Figure 41 and Figure 42 (Slave Serial Interface Modes)[1]					
External SCLK Setup Time	t_{31}	5			ns
External SCLK Active Edge to SDOUT Delay	t_{32}	3		18	ns
SDIN Setup Time	t_{33}	5			ns
SDIN Hold Time	t_{34}	5			ns
External SCLK Period	t_{35}	25			ns
External SCLK HIGH	t_{36}	10			ns
External SCLK LOW	t_{37}	10			ns

[1] In serial interface mode, the SYNC, SCLK, and SDOUT timings are defined with a maximum load C_L of 10 pF; otherwise, the load is 60 pF maximum.
[2] In serial master read during convert mode. See Table 4 for serial master read after convert mode.

Table 4. Serial Clock Timings in Master Read after Convert

DIVSCLK[1] DIVSCLK[0]	Symbol	0 0	0 1	1 0	1 1	Unit
SYNC to SCLK First Edge Delay Minimum	t_{18}	3	17	17	17	ns
Internal SCLK Period Minimum	t_{19}	25	50	100	200	ns
Internal SCLK Period Maximum	t_{19}	40	70	140	280	ns
Internal SCLK HIGH Minimum	t_{20}	12	22	50	100	ns
Internal SCLK LOW Minimum	t_{21}	7	21	49	99	ns
SDOUT Valid Setup Time Minimum	t_{22}	4	18	18	18	ns
SDOUT Valid Hold Time Minimum	t_{23}	2	4	30	80	ns
SCLK Last Edge to SYNC Delay Minimum	t_{24}	3	55	130	290	ns
BUSY HIGH Width Maximum	t_{24}	2	2.5	3.5	5.75	µs

ABSOLUTE MAXIMUM RATINGS

Table 5. AD7666 Stress Ratings[1]

Parameter	Rating
IN[2], TEMP[2], REF, REFBUFIN, INGND[2], REFGND to AGND	AVDD + 0.3 V to AGND … 0.3 V
Ground Voltage Differences	
AGND, DGND, OGND	±0.3 V
Supply Voltages	
AVDD, DVDD, OVDD	…0.3 V to +7 V
AVDD to DVDD, AVDD to OVDD	±7 V
DVDD to OVDD	…0.3 V to +7 V
Digital Inputs	…0.3 V to DVDD + 0.3 V
PDREF, PDBUF[3]	±20 mA
Internal Power Dissipation[4]	700 mW
Internal Power Dissipation[5]	2.5 W
Junction Temperature	150°C
Storage Temperature Range	…65°C to +150°C
Lead Temperature Range (Soldering 10 sec)	300°C

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2] See Analog Input section.
[3] See the Voltage Reference Input section.
[4] Specification is for the device in free air: 48-Lead LQFP; θ_{JA} = 91°C/W, θ_{JC} = 30°C/W
[5] Specification is for the device in free air: 48-Lead LFCSP; θ_{JA} = 26°C/W.

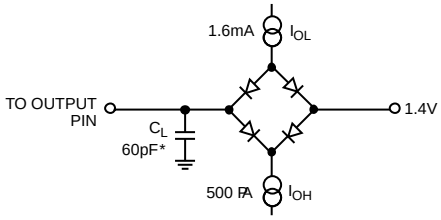


Figure 2. Load Circuit for Digital Interface Timing, SDOUT, SYNC, SCLK Outputs, C_L = 10 pF

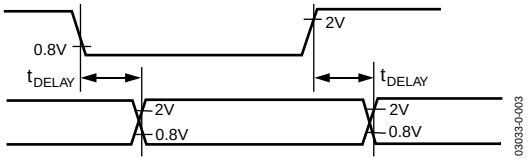


Figure 3. Voltage Reference Levels for Timing

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

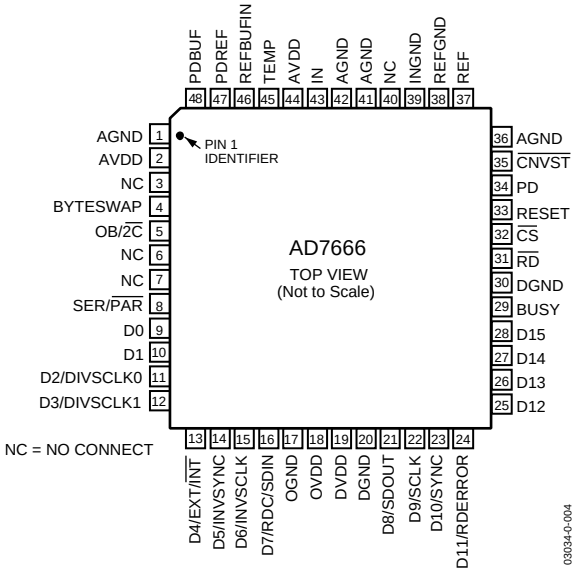


Figure 4. 48-Lead LQFP (ST-48) and 48-Lead LFCSP (CP-48)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 36, 41, 42	AGND	P	Analog Power Ground Pin.
2, 44	AVDD	P	Input Analog Power Pin. Nominally 5 V.
3, 6, 7, 40	NC		No Connect.
4	BYTESWAP	DI	Parallel Mode Selection (8-/16-bit). When LOW, the LSB is output on D[7:0] and the MSB is output on D[15:8]. When HIGH, the LSB is output on D[15:8] and the MSB is output on D[7:0].
5	OB/$\overline{2C}$	DI	Straight Binary/Binary Twos Complement. When OB/$\overline{2C}$ is HIGH, the digital output is straight binary; when LOW, the MSB is inverted, resulting in twos complement output from its internal shift register.
8	SER/$\overline{PAR}$	DI	Serial/Parallel Selection Input. When LOW, the parallel port is selected; when HIGH, the serial interface mode is selected and some bits of the DATA bus are used as a serial port.
9, 10	D[0:1]	DO	Bit 0 and Bit 1 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, these outputs are in high impedance.
11, 12	D[2:3] or DIVSCLK[0:1]	DI/O	When SER/$\overline{PAR}$ is LOW, these outputs are used as Bit 2 and Bit 3 of the parallel port data output bus. When SER/$\overline{PAR}$ is HIGH, EXT/$\overline{INT}$ is LOW, and RDC/SDIN is LOW (serial master read after convert), these inputs, part of the serial port, are used to slow down, if desired, the internal serial clock that clocks the data output. In other serial modes, these pins are not used.
13	D4 or EXT/$\overline{INT}$	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 4 of the parallel port data output bus. When SER/$\overline{PAR}$ is HIGH, this input, part of the serial port, is used as a digital select input for choosing the internal data clock or an external data clock. With EXT/$\overline{INT}$ tied LOW, the internal clock is selected on the SCLK output. With EXT/$\overline{INT}$ set to a logic HIGH, output data is synchronized to an external clock signal connected to the SCLK input.
14	D5 or INVSYNC	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 5 of the parallel port data output bus. When SER/$\overline{PAR}$ is HIGH, this input, part of the serial port, is used to select the active state of the SYNC signal. It is active in both master and slave modes. When LOW, SYNC is active HIGH. When HIGH, SYNC is active LOW.
15	D6 or INVSCLK	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 6 of the parallel port data output bus. When SER/$\overline{PAR}$ is HIGH, this input, part of the serial port, is used to invert the SCLK signal. It is active in both master and slave modes.

Pin No.	Mnemonic	Type[1]	Description
16	D7 or RDC/SDIN	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 7 of the parallel port data output bus. When SER/$\overline{PAR}$ is HIGH, this input, part of the serial port, is used as either an external data input or a read mode selection input depending on the state of EXT/$\overline{INT}$. When EXT/$\overline{INT}$ is HIGH, RDC/SDIN could be used as a data input to daisy-chain the conversion results from two or more ADCs onto a single SDOUT line. The digital data level on SDIN is output on DATA with a delay of 16 SCLK periods after the initiation of the read sequence. When EXT/$\overline{INT}$ is LOW, RDC/SDIN is used to select the read mode. When RDC/SDIN is HIGH, the data is output on SDOUT during conversion. When RDC/SDIN is LOW, the data can be output on SDOUT only when the conversion is complete.
17	OGND	P	Input/Output Interface Digital Power Ground.
18	OVDD	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (5 V or 3 V).
19	DVDD	P	Digital Power. Nominally at 5 V.
20	DGND	P	Digital Power Ground.
21	D8 or SDOUT	DO	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 8 of the parallel port data output bus. When SER/$\overline{PAR}$ is HIGH, this output, part of the serial port, is used as a serial data output synchronized to SCLK. Conversion results are stored in an on-chip register. The AD7666 provides the conversion result, MSB first, from its internal shift register. The DATA format is determined by the logic level of OB/$\overline{2C}$. In serial mode when EXT/$\overline{INT}$ is LOW, SDOUT is valid on both edges of SCLK. In serial mode when EXT/$\overline{INT}$ is HIGH, if INVSCLK is LOW, SDOUT is updated on the SCLK rising edge and valid on the next falling edge; if INVSCLK is HIGH, SDOUT is updated on the SCLK falling edge and valid on the next rising edge.
22	D9 or SCLK	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 9 of the parallel port data or SCLK output bus. When SER/$\overline{PAR}$ is HIGH, this pin, part of the serial port, is used as a serial data clock input or output, depending upon the logic state of the EXT/$\overline{INT}$ pin. The active edge where the data SDOUT is updated depends upon the logic state of the INVSCLK pin.
23	D10 or SYNC	DO	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 10 of the parallel port data output bus. When SER/$\overline{PAR}$ is HIGH, this output, part of the serial port, is used as a digital output frame synchronization for use with the internal data clock (EXT/$\overline{INT}$ = logic LOW). When a read sequence is initiated and INVSYNC is LOW, SYNC is driven HIGH and remains HIGH while the SDOUT output is valid. When a read sequence is initiated and INVSYNC is HIGH, SYNC is driven LOW and remains LOW while the SDOUT output is valid.
24	D11 or RDERROR	DO	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 11 of the parallel port data output bus. When SER/$\overline{PAR}$ and EXT/$\overline{INT}$ are HIGH, this output, part of the serial port, is used as an incomplete read error flag. In slave mode, when a data read is started and not complete when the following conversion is complete, the current data is lost and RDERROR is pulsed HIGH.
25…28	D[12:15]	DO	Bit 12 to Bit 15 of the Parallel Port Data Output Bus. These pins are always outputs regardless of the state of SER/$\overline{PAR}$.
29	BUSY	DO	Busy Output. Transitions HIGH when a conversion is started and remains HIGH until the conversion is complete and the data is latched into the on-chip shift register. The falling edge of BUSY could be used as a data ready clock signal.
30	DGND	P	Must Be Tied to Digital Ground.
31	$\overline{RD}$	DI	Read Data. When $\overline{CS}$ and $\overline{RD}$ are both LOW, the interface parallel or serial output bus is enabled.
32	$\overline{CS}$	DI	Chip Select. When $\overline{CS}$ and $\overline{RD}$ are both LOW, the interface parallel or serial output bus is enabled. $\overline{CS}$ is also used to gate the external clock.
33	RESET	DI	Reset Input. When set to a logic HIGH, this pin resets the AD7666 and the current conversion, if any, is aborted. If not used, this pin could be tied to DGND.
34	PD	DI	Power-Down Input. When set to a logic HIGH, power consumption is reduced and conversions are inhibited after the current one is completed.
35	$\overline{CNVST}$	DI	Start Conversion. If $\overline{CNVST}$ is HIGH when the acquisition phase (t2) is complete, the next falling edge on $\overline{CNVST}$ puts the internal sample/hold into the hold state and initiates a conversion. The mode is most appropriate if low sampling jitter is desired. If $\overline{CNVST}$ is LOW when the acquisition phase (t2) is complete, the internal sample/hold is put into the hold state and a conversion is immediately started.
37	REF	AI/O	Reference Input Voltage. On-chip reference output voltage.
38	REFGND	AI	Reference Input Analog Ground.
39	INGND	AI	Analog Input Ground.

Pin No.	Mnemonic	Type[1]	Description
43	IN	AI	Primary Analog Input with a Range of 0 V to 2.5 V.
45	TEMP	AO	Temperature Sensor Voltage Output.
46	REFBUFIN	AI/O	Reference Input Voltage. The reference output and the reference buffer input.
47	PDREF	DI	This pin allows the choice of internal or external voltage references. When LOW, the on-chip reference is turned on. When HIGH, the internal reference is switched off and an external reference must be used.
48	PDBUF	DI	This pin allows the choice of buffering an internal or external reference with the internal buffer. When LOW, the buffer is selected. When HIGH, the buffer is switched off.

[1]AI = Analog Input; AI/O = Bidirectional Analog; AO = Analog Output; DI = Digital Input; DI/O = Bidirectional Digital; DO = Digital Output; P = Power.

DEFINITIONS OF SPECIFICATIONS

Integral Nonlinearity Error (INL)

Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity Error (DNL)

In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Full-Scale Error

The last transition (from 011…10 to 011…11 in two's complement coding) should occur for an analog voltage 1½ LSB below the nominal full scale (2.49994278 V for the 0 V to 2.5 V range). The full-scale error is the deviation of the actual level of the last transition from the ideal level.

Unipolar Zero Error

The first transition should occur at a level ½ LSB above analog ground (19.073 µV for the 0 V to 2.5 V range). Unipolar zero error is the deviation of the actual transition from that point.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number Of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to S/(N+D) and is expressed in bits by the following formula:

$$ENOB = (S/[N+D]\,dB - 1.76)/6.02$$

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal, and is expressed in decibels.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (S/[N+D])

S/(N+D) is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N+D) is expressed in decibels.

Aperture Delay

Aperture delay is a measure of the acquisition performance and is measured from the falling edge of the $\overline{CNVST}$ input to when the input signal is held for a conversion.

Transient Response

Transient response is the time required for the AD7666 to achieve its rated accuracy after a full-scale step function is applied to its input.

Reference Voltage Temperature Coefficient

Reference voltage temperature coefficient is derived from the maximum and minimum reference output voltage (V_{REF}) measured at T_{MIN}, T(25°C), and T_{MAX}. It is expressed in ppm/°C using the following equation:

$$TCV_{REF}(ppm/°C) = \frac{V_{REF}(Max) - V_{REF}(Min)}{V_{REF}(25°C) \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:
$V_{REF}(Max)$ = Maximum V_{REF} at T_{MIN}, T(25°C), or T_{MAX}
$V_{REF}(Min)$ = Minimum V_{REF} at T_{MIN}, T(25°C), or T_{MAX}
$V_{REF}(25°C) = V_{REF}$ at +25°C
T_{MAX} = +85°C
T_{MIN} = –40°C

Thermal Hysteresis

Thermal hysteresis is defined as the absolute maximum change of reference output voltage after the device is cycled through temperature from either

$$T\_HYS+ = +25°C \text{ to } T_{MAX} \text{ to } +25°C$$
$$T\_HYS- = +25°C \text{ to } T_{MIN} \text{ to } +25°C$$

It is expressed in ppm using the following equation:

$$V_{HYS}(ppm) = \left| \frac{V_{REF}(25°C) - V_{REF}(T\_HYS)}{V_{REF}(25°C)} \right| \times 10^6$$

where:
$V_{REF}(25°C) = V_{REF}$ at 25°C
$V_{REF}(T\_HYS)$ = Maximum change of V_{REF} at T_HYS+ or T_HYS–.

TYPICAL PERFORMANCE CHARACTERISTICS

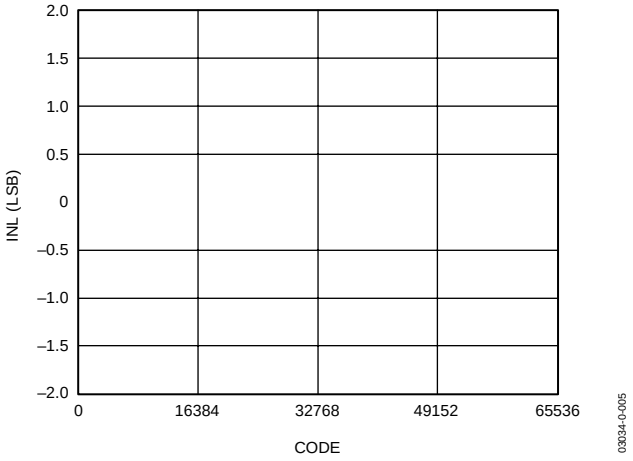


Figure 5. Integral Nonlinearity vs. Code

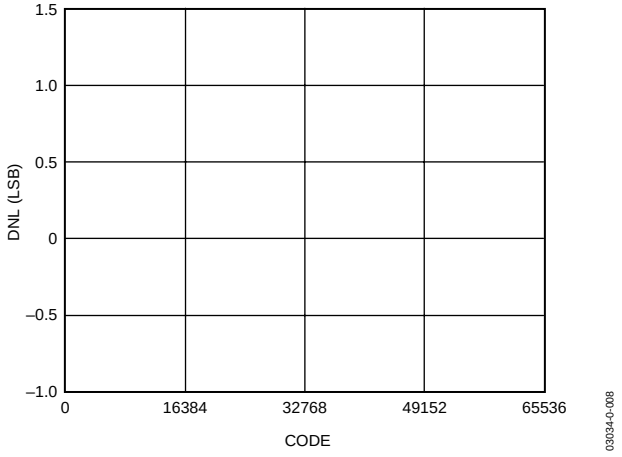


Figure 8. Differential Nonlinearity vs. Code

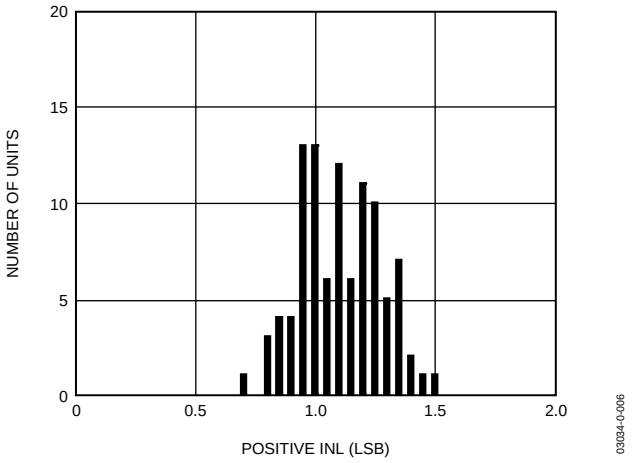


Figure 6. Typical Positive INL Distribution (99 Units)

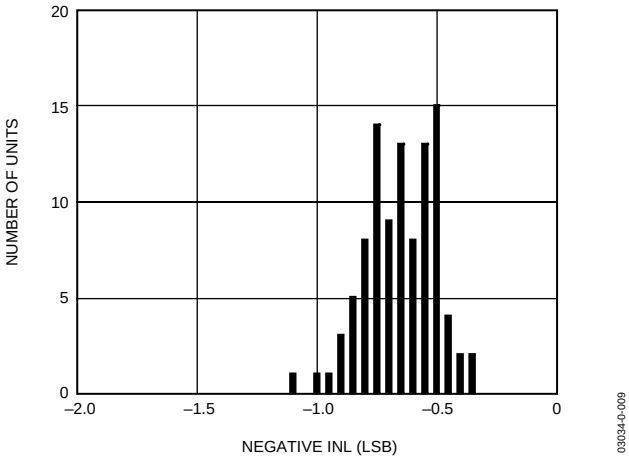


Figure 9. Typical Negative INL Distribution (99 Units)

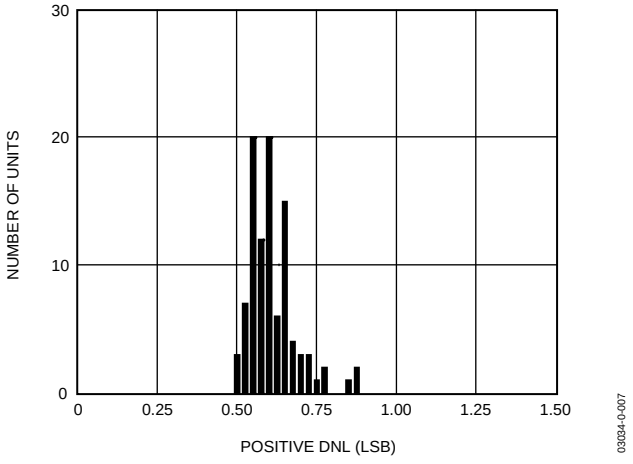


Figure 7. Typical Positive DNL Distribution (99 Units)

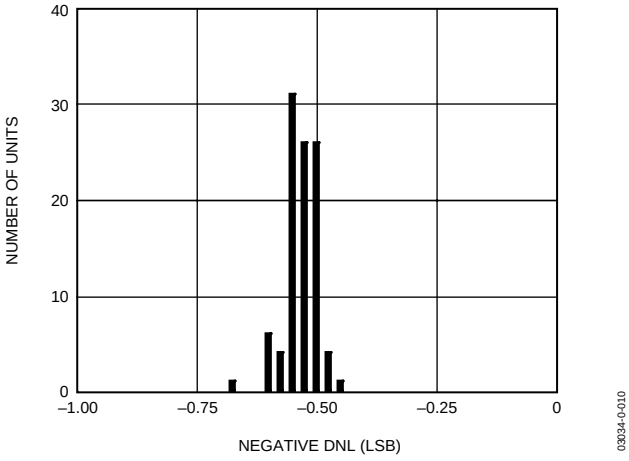


Figure 10. Typical Negative DNL Distribution (99 Units)

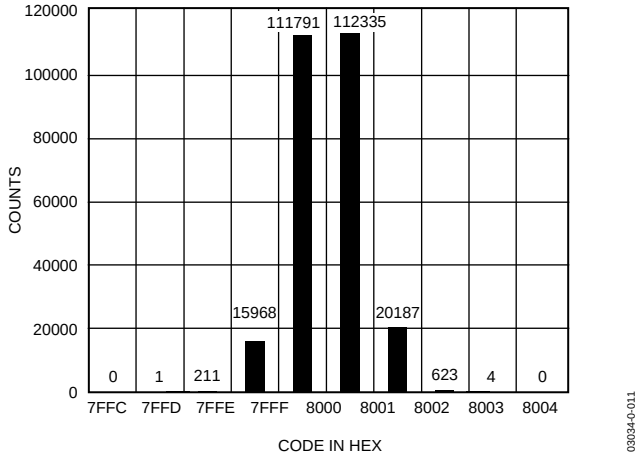


Figure 11. Histogram of 261,120 Conversions of a DC Input at the Code Transition

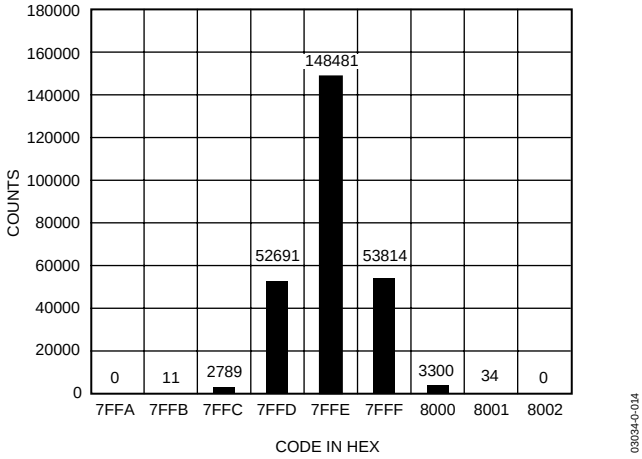


Figure 14. Histogram of 261,120 Conversions of a DC Input at the Code Center

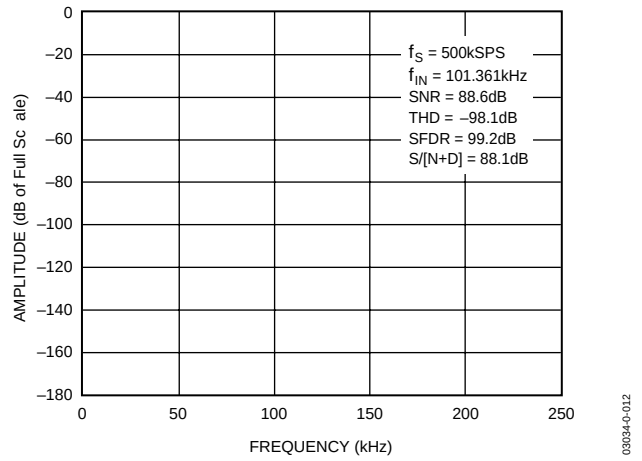


Figure 12. FFT Plot

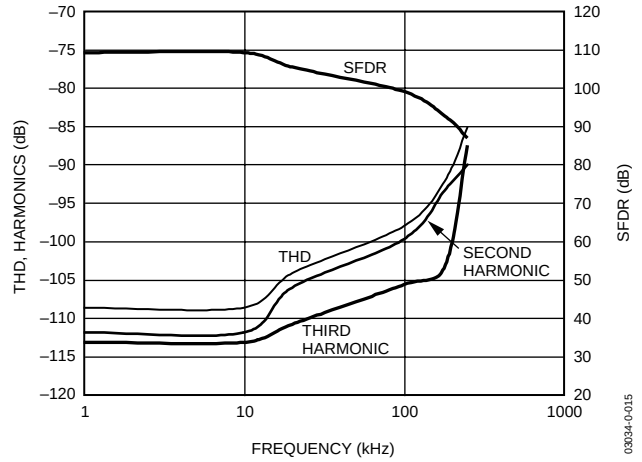


Figure 15. THD, Harmonics, and SFDR vs. Frequency

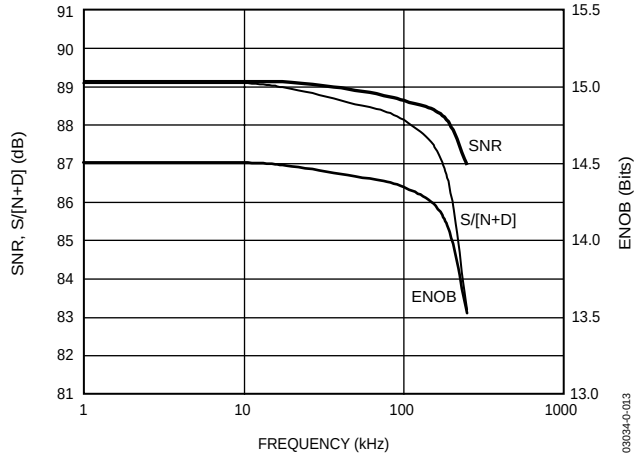


Figure 13. SNR, S/(N+D), and ENOB vs. Frequency

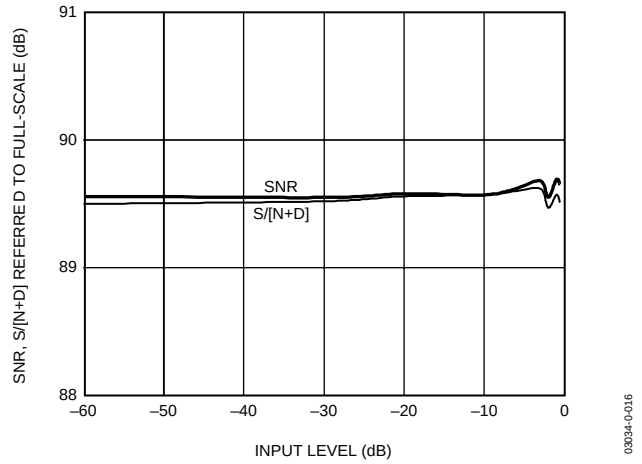


Figure 16. SNR and S/(N+D) vs. Input Level (Referred to Full Scale)

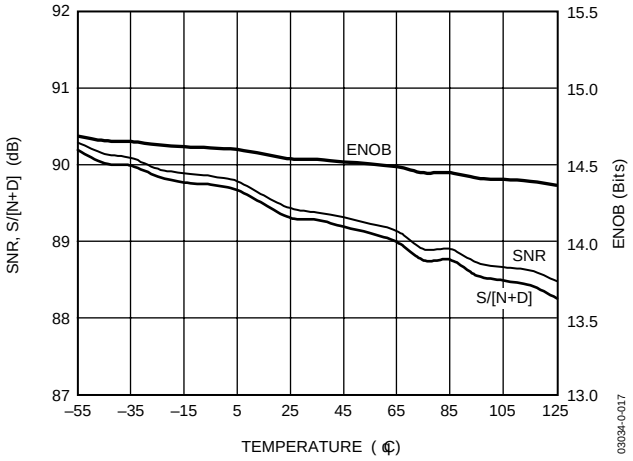


Figure 17. SNR, S/(N+D), and ENOB vs. Temperature

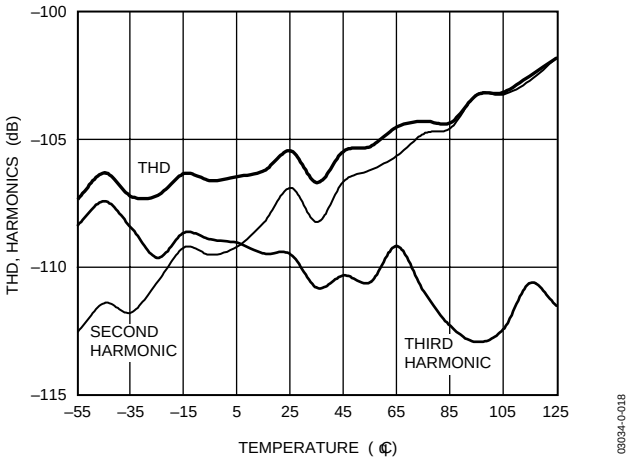


Figure 18. THD and Harmonics vs. Temperature

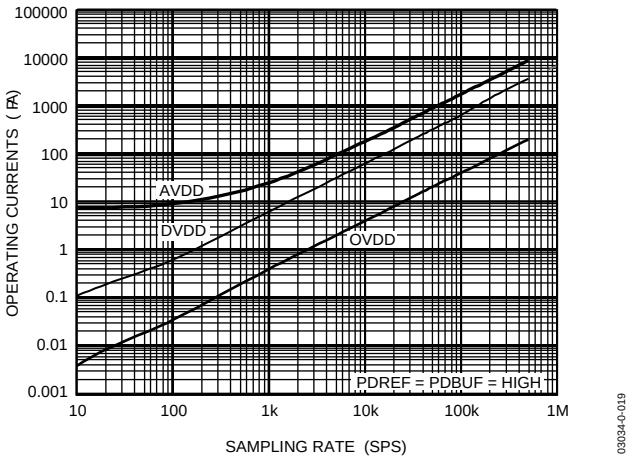


Figure 19. Operating Currents vs. Sample Rate

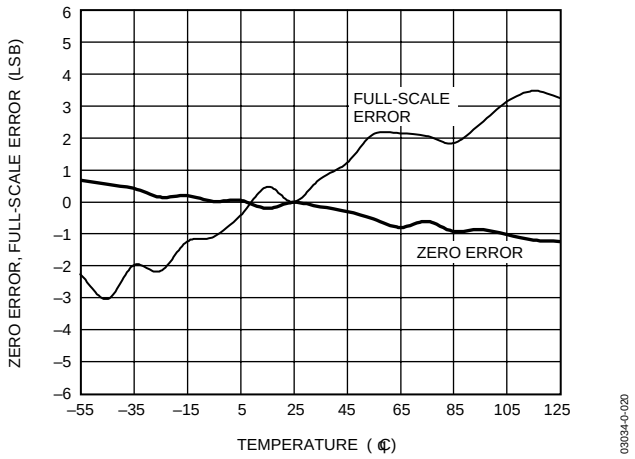


Figure 20. Zero Error, Full-Scale Error without Reference vs. Temperature

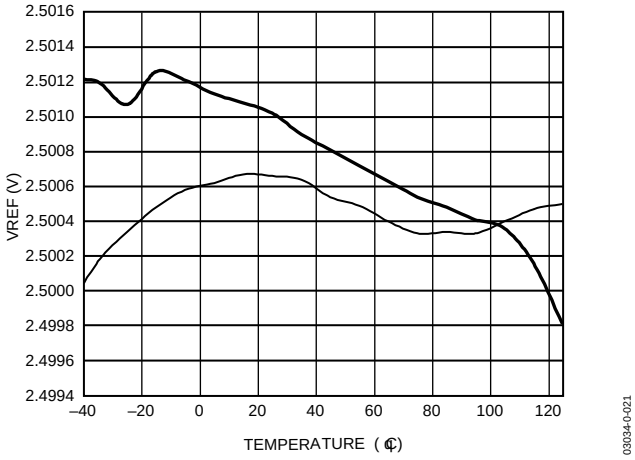


Figure 21. Typical Reference Voltage Output vs. Temperature (2 Units)

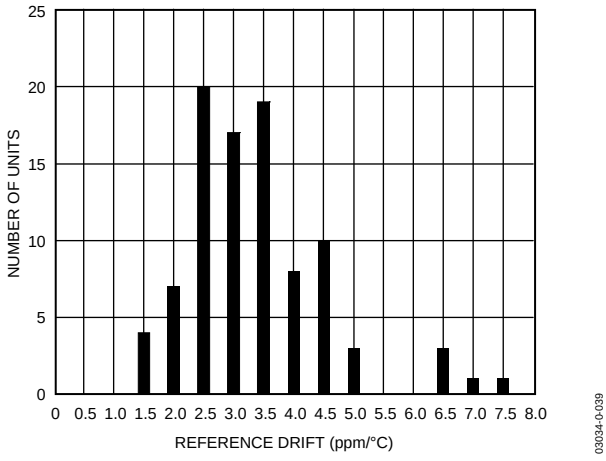


Figure 22. Reference Voltage Temperature Coefficient Distribution (93 Units)

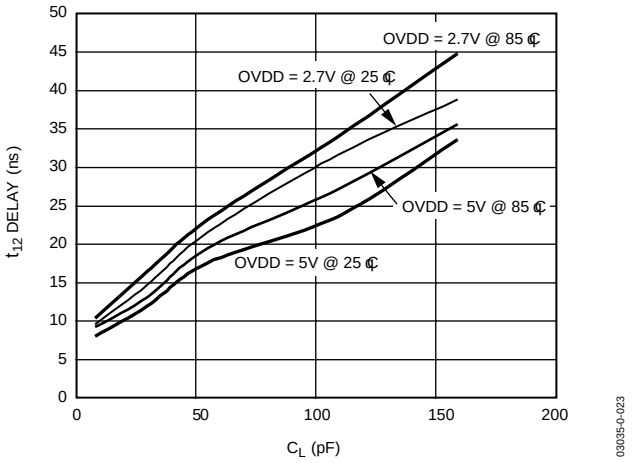


Figure 23. Typical Delay vs. Load Capacitance, C_L

CIRCUIT INFORMATION

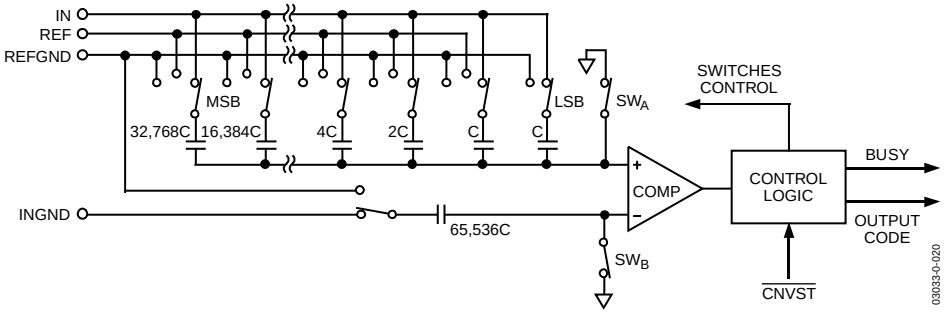


Figure 24. ADC Simplified Schematic

The AD7666 is a very fast, low power, single supply, precise 16-bit analog-to-digital converter (ADC). The AD7666 is capable of converting 100,000 samples per second (500 kSPS) and allows power savings between conversions.

The AD7666 provides the user with an on-chip track/hold, successive approximation ADC that does not exhibit any pipeline or latency, making it ideal for multiple multiplexed channel applications.

The AD7666 can be operated from a single 5V supply and can be interfaced to either 5V or 3V digital logic. It is housed in either a 48-lead LQFP or a 48-lead LFCSP that saves space and allows flexible configurations as either a serial or parallel interface. The AD7666 is pin-to-pin compatible with PulSAR ADCs and is an upgrade of the AD7661 and AD7664.

CONVERTER OPERATION

The AD7666 is a successive-approximation ADC based on a charge redistribution DAC. Figure 24 shows a simplified schematic of the ADC. The capacitive DAC consists of an array of 16 binary weighted capacitors and an additional LSB capacitor. The comparator's negative input is connected to a dummy capacitor of the same value as the capacitive DAC array.

During the acquisition phase, the common terminal of the array tied to the comparator's positive input is connected to AGND via SW_A. All independent switches are connected to the analog input IN. Thus, the capacitor array is used as a sampling capacitor and acquires the analog signal on IN. Similarly, the dummy capacitor acquires the analog signal on INGND.

When $\overline{CNVST}$ goes LOW, a conversion phase is initiated. When the conversion phase begins, SW_A and SW_B are opened. The capacitor array and dummy capacitor are then disconnected from the inputs and connected to REFGND. Therefore, the differential voltage between IN and INGND captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between REFGND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$, ... $V_{REF}/65536$). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition.

After this process is completed, the control logic generates the ADC output code and brings the BUSY output LOW.

Transfer Functions

Using the OB/$\overline{2C}$ digital input, the AD7666 offers two output codings: straight binary and twos complement. The LSB size is V_{REF}/65536, which is about 38.15 µV. The AD7666's ideal transfer characteristic is shown in Figure 25 and Table 7.

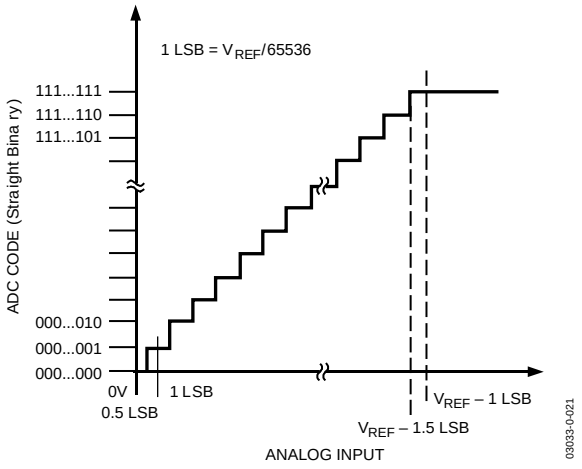


Figure 25. ADC Ideal Transfer Function

Table 7. Output Codes and Ideal Input Voltages

Description	Analog Input	Digital Output Code (Hex)	
		Straight Binary	Twos Complement
FSR …1 LSB	2.499962 V	FFFF	7FFF
FSR … 2 LSB	2.499923 V	FFFE	7FFE
Midscale + 1 LSB	1.250038 V	8001	0001
Midscale	1.25 V	8000	0000
Midscale … 1 LSB	1.249962 V	7FFF	FFFF
…FSR + 1 LSB	38 µV	0001	8001
…FSR	0 V	0000[2]	8000[2]

[1] This is also the code for overrange analog input (V_{IN} … V_{INGND} above V_{REF} … V_{REFGND}).
[2] This is also the code for underrange analog input (V_{IN} below V_{INGND}).

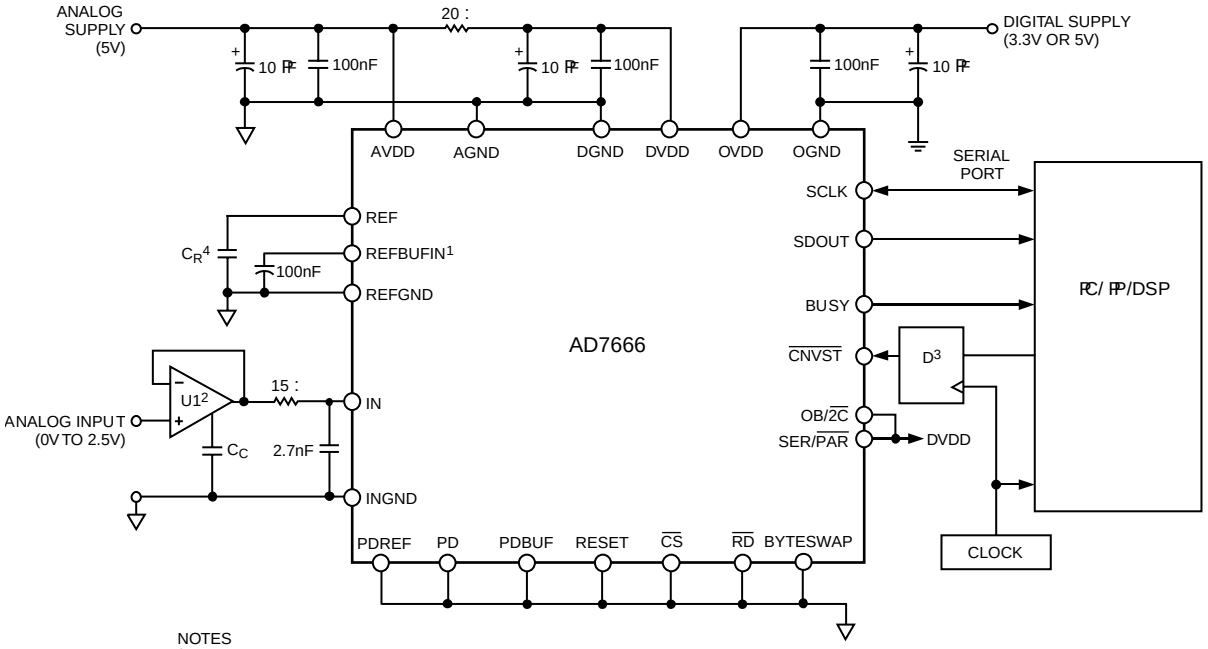


Figure 26. Typical Connection Diagram

TYPICAL CONNECTION DIAGRAM

Figure 26 shows a typical connection diagram for the AD7666.

Analog Input

Figure 27 shows an equivalent circuit of the input structure of the AD7666.

The two diodes, D1 and D2, provide ESD protection for the analog inputs IN and INGND. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 0.3V. This will cause these diodes to become forward-biased and start conducting current. These diodes can handle a forward-biased current of 100 mA maximum. For instance, these conditions could eventually occur when the input buffer's (U1) supplies are different from AVDD. In such a case, an input buffer with a short-circuit current limitation can be used to protect the part.

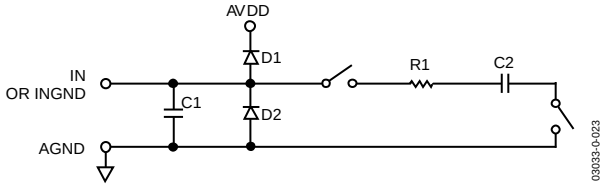


Figure 27. Equivalent Analog Input Circuit

This analog input structure allows the sampling of the differential signal between IN and INGND. Unlike other converters, INGND is sampled at the same time as IN. By using this differential input, small signals common to both inputs are rejected, as shown in Figure 28, which represents the typical CMRR over frequency with on-chip and external references. For instance, by using INGND to sense a remote signal ground, ground potential differences between the sensor and the local ADC ground are eliminated.

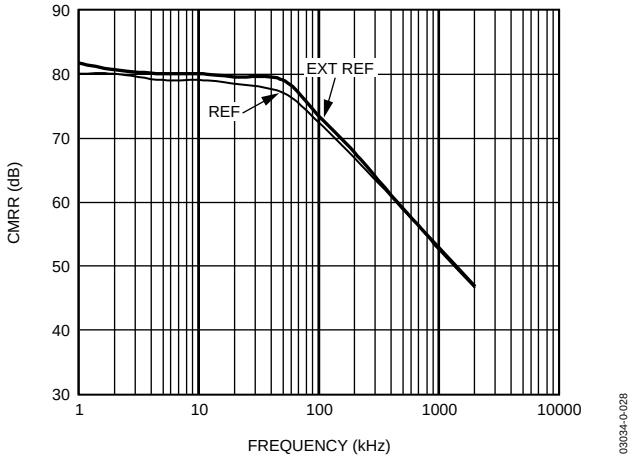


Figure 28. Analog Input CMRR vs. Frequency

During the acquisition phase, the impedance of the analog input IN can be modeled as a parallel combination of capacitor C1 and the network formed by the series connection of R1 and C2. C1 is primarily the pin capacitance. R1 is typically 168 and is a lumped component made up of some serial resistors and the on resistance of the switches. C2 is typically 60 pF and is mainly the ADC sampling capacitor. During the conversion phase, where the switches are opened, the input impedance is limited to C1. R1 and C2 make a 1-pole low-pass filter that reduces undesirable aliasing effect and limits the noise.

When the source impedance of the driving circuit is low, the AD7666 can be driven directly. Large source impedances will significantly affect the ac performance, especially total harmonic distortion (THD). The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency, as shown in Figure 29.

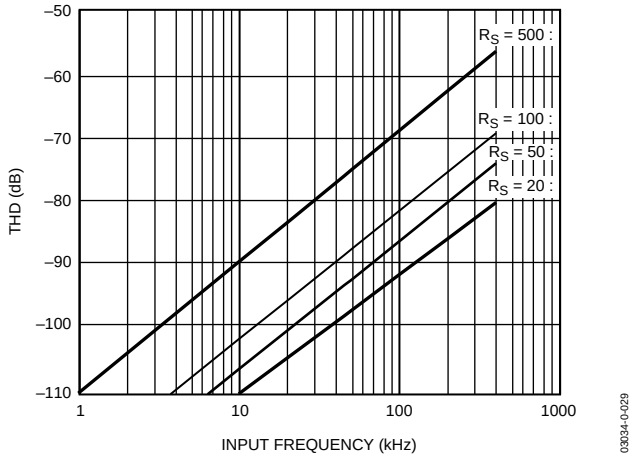


Figure 29. THD vs. Analog Input Frequency and Source Resistance

Driver Amplifier Choice

Although the AD7666 is easy to drive, the driver amplifier needs to meet the following requirements:

- The driver amplifier and the AD7666 analog input circuit must be able to settle for a full-scale step of the capacitor array at a 16-bit level (0.0015%). In the amplifier's data sheet, settling at 0.1% to 0.01% is more commonly specified. This could differ significantly from the settling time at a 16-bit level and should be verified prior to driver selection. The tiny op amp AD8021, which combines ultra low noise and high gain-bandwidth, meets this settling time requirement even when used with gains up to 13.

- The noise generated by the driver amplifier needs to be kept as low as possible in order to preserve the SNR and transition noise performance of the AD7666. The noise coming from the driver is filtered by the AD7666 analog input circuit, 1-pole, low-pass filter made by R1 and C2 or by the external filter, if one is used. The SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20\log\left(\frac{28}{\sqrt{784 + \frac{S}{2}f_{-3dB}(Ne_N)^2}}\right)$$

where:

f_{-3dB} is the input bandwidth of the AD7666 (13 MHz) or the cutoff frequency of the input filter (3.9 MHz), if one is used.

N is the noise factor of the amplifier (+1 in buffer configuration).

e_N is the equivalent input noise voltage of the op amp, in nV/ Hz.

For instance, a driver with an equivalent input noise of 2 nV/ Hz, like the AD8021 with a noise gain of +1 when configured as a buffer, degrades the SNR by only 0.13 dB when using the filter shown in Figure 26, and by 0.43 dB without the filter shown in Figure 26.

- The driver needs to have a THD performance suitable to that of the AD7666. Figure 15 gives the THD versus frequency that the driver should exceed.

The AD8021 meets these requirements and is appropriate for almost all applications. The AD8021 needs a 10 pF external compensation capacitor that should have good linearity as an NPO ceramic or mica type. Moreover, the use of a noninverting +1 gain arrangement is recommended and helps to obtain the best signal-to-noise ratio.

The AD8022 could also be used if a dual version is needed and gain of 1 is present. The AD829 is an alternative in applications where high frequency (above 100 kHz) performance is not required. In gain of 1 applications, it requires an 82 pF compensation capacitor. The AD8610 is an option when low bias current is needed in low frequency applications.

Voltage Reference Input

The AD7666 allows the choice of either a very low temperature drift internal voltage reference or an external 2.5 V reference.

Unlike many ADCs with internal references, the internal reference of the AD7666 provides excellent performance and can be used in almost all applications.

To use the internal reference along with the internal buffer, PDREF and PDBUF should both be LOW. This will produce 1.2 V on REFBUFIN which, amplified by the buffer, will result in a 2.5 V reference on the REF pin.

The output impedance of REFBUFIN is 11 k (minimum) when the internal reference is enabled. It is necessary to decouple REFBUFIN with a ceramic capacitor greater than 10 nF. Thus the capacitor provides an RC filter for noise reduction.

To use an external reference along with the internal buffer, PDREF should be HIGH and PDBUF should be LOW. This powers down the internal reference and allows the 2.5 V reference to be applied to REFBUFIN.

To use an external reference directly on REF pin, PDREF and PDBUF should both be HIGH.

PDREF and PDBUF power down the internal reference and the internal reference buffer, respectively. Note that the PDREF and PDBUF input current should never exceed 20 mA. This could eventually occur when input voltage is above AVDD (for instance at power up). In this case, a 100 series resistor is recommended.

The internal reference is temperature compensated to 2.5 V ± 7 mV. The reference is trimmed to provide a typical drift of 3 ppm/°C . This typical drift characteristic is shown in Figure 22. For improved drift performance, an external reference, such as the AD780, can be used.

The AD7666 voltage reference input REF has a dynamic input impedance; it should therefore be driven by a low impedance source with efficient decoupling between the REF and REFGND inputs. This decoupling depends on the choice of the voltage reference, but usually consists of a low ESR tantalum capacitor connected to REF and REFGND, with minimum parasitic inductance. A 10 µF (X5R, 1206 size) ceramic chip capacitor (or 47 µF tantalum capacitor) is appropriate when using either the internal reference or one of these recommended reference voltages:

- The low noise, low temperature drift ADR421 and AD780
- The low power ADR291
- The low cost AD1582

For applications that use multiple AD7666s, it is more effective to use the internal buffer to buffer the reference voltage.

Care should be taken with the voltage reference's temperature coefficient, which directly affects the full-scale accuracy if this parameter matters. For instance, a ±15 ppm/°C temperature coefficient of the reference changes full scale by ±1 LSB/°C.

Note that V_{REF} can be increased to AVDD … 1.85V. Since the input range is defined in terms of V_{REF}, this would essentially increase the range to 0V to 3V with an AVDD above 4.85V. The AD780 can be selected with a 3V reference voltage.

The TEMP pin, which measures the temperature of the AD7666, can be used as shown in Figure 30. The output of TEMP pin is applied to one of the inputs of the analog switch (e.g., ADG779), and the ADC itself is used to measure its own temperature. This configuration is very useful for improving the calibration accuracy over the temperature range.

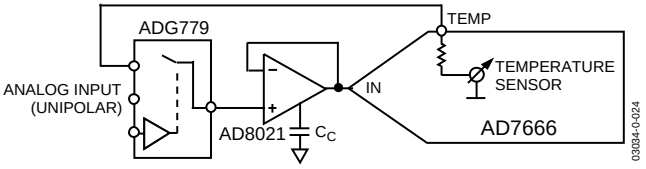


Figure 30. Temperature Sensor Connection Diagram

Power Supply

The AD7666 uses three power supply pins: an analog 5V supply AVDD, a digital 5V core supply DVDD, and a digital input/output interface supply OVDD. OVDD allows direct interface with any logic between 2.7V and DVDD + 0.3V. To reduce the supplies needed, the digital core (DVDD) can be supplied through a simple RC filter from the analog supply, as shown in Figure 26. The AD7666 is independent of power supply sequencing once OVDD does not exceed DVDD by more than 0.3V, and is thus free of supply voltage induced latch-up. Additionally, it is very insensitive to power supply variations over a wide frequency range, as shown in Figure 31, which represents PSRR over frequency with on-chip and external references.

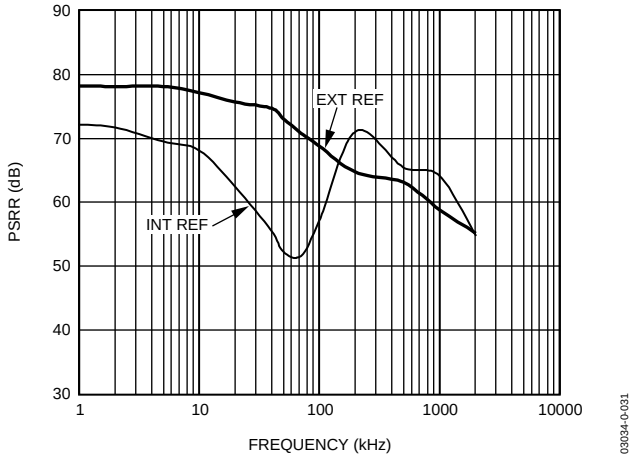


Figure 31. PSRR vs. Frequency

POWER DISSIPATION VERSUS THROUGHPUT

Operating currents are very low during the acquisition phase, allowing significant power savings when the conversion rate is reduced (see Figure 32). The AD7666 automatically reduces its power consumption at the end of each conversion phase. This makes the part ideal for very low power battery applications. The digital interface and the reference remain active even during the acquisition phase. To reduce operating digital supply currents even further, digital inputs need to be driven close to the power supply rails (i.e., DVDD or DGND), and OVDD should not exceed DVDD by more than 0.3V.

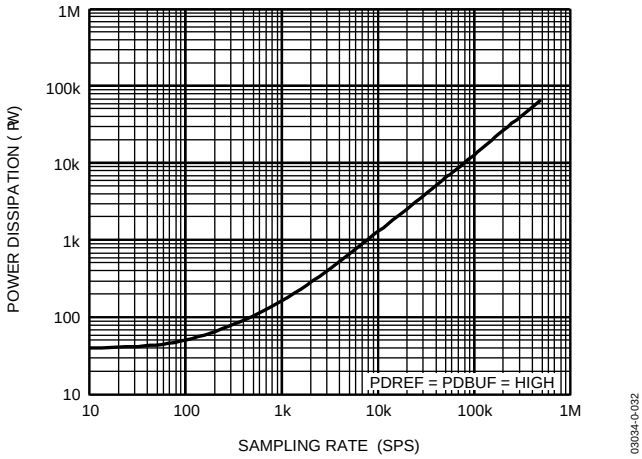


Figure 32. Power Dissipation vs Sampling Rate

CONVERSION CONTROL

Figure 33 shows the detailed timing diagrams of the conversion process. The AD7666 is controlled by the $\overline{CNVST}$ signal, which initiates conversion. Once initiated, it cannot be restarted or aborted, even by the power-down input PD, until the conversion is complete. $\overline{CNVST}$ operates independently of $\overline{CS}$ and $\overline{RD}$.

Conversions can be automatically initiated with the AD7666. If $\overline{CNVST}$ is held LOW when BUSY is LOW, the AD7666 controls the acquisition phase and automatically initiates a new conversion. By keeping $\overline{CNVST}$ LOW, the AD7666 keeps the conversion process running by itself. It should be noted that the analog input must be settled when BUSY goes LOW. Also, at power-up, $\overline{CNVST}$ should be brought LOW once to initiate the conversion process. In this mode, the AD7666 can run slightly faster than the guaranteed 500 kSPS.

Although $\overline{CNVST}$ is a digital signal, it should be designed with special care with fast, clean edges, and levels with minimum overshoot and undershoot or ringing.

The $\overline{CNVST}$ trace should be shielded with ground and a low value serial resistor (i.e., 50) termination should be added close to the output of the component that drives this line.

For applications where SNR is critical, the $\overline{CNVST}$ signal should have very low jitter. This may be achieved by using a dedicated oscillator for $\overline{CNVST}$ generation, or to clock $\overline{CNVST}$ with a high frequency, low jitter clock, as shown in Figure 26.

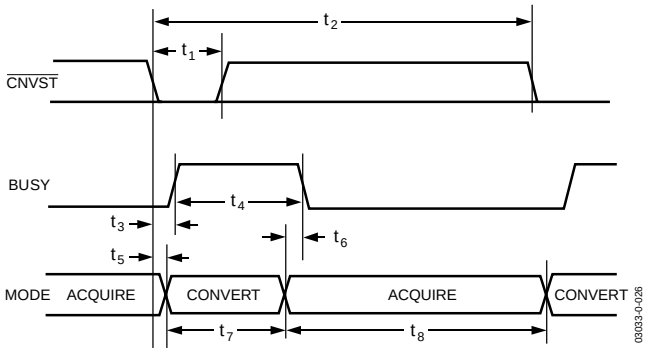


Figure 33. Basic Conversion Timing

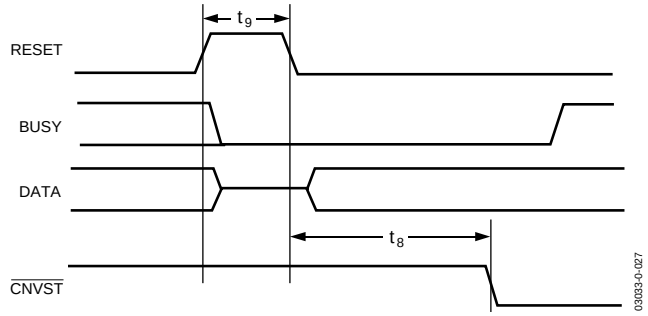


Figure 34. RESET Timing

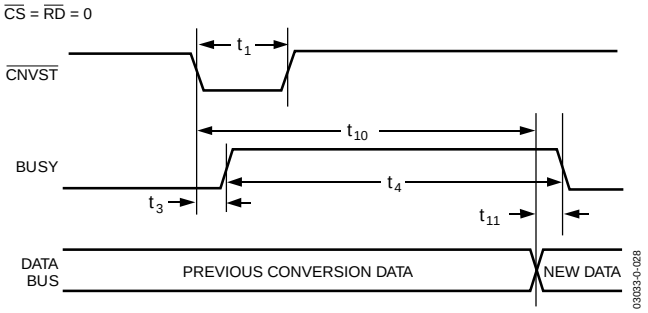


Figure 35. Master Parallel Data Timing for Reading (Continuous Read)

DIGITAL INTERFACE

The AD7666 has a versatile digital interface; it can be interfaced with the host system by using either a serial or a parallel interface. The serial interface is multiplexed on the parallel data bus. The AD7666 digital interface also accommodates both 3V and 5V logic by simply connecting the OVDD supply pin of the AD7666 to the host system interface digital supply. Finally, by using the OB/$\overline{2C}$ input pin, both two's complement or straight binary coding can be used.

The two signals, $\overline{CS}$ and $\overline{RD}$, control the interface. $\overline{CS}$ and $\overline{RD}$ have a similar effect because they are OR'ed together internally. When at least one of these signals is HIGH, the interface outputs are in high impedance. Usually $\overline{CS}$ allows the selection of each AD7666 in multicircuit applications and is held low in a single AD7666 design. $\overline{RD}$ is generally used to enable the conversion result on the data bus.

PARALLEL INTERFACE

The AD7666 is configured to use the parallel interface when SER/$\overline{PAR}$ is held LOW. The data can be read either after each conversion, which is during the next acquisition phase, or during the following conversion, as shown in Figure 36 and Figure 37, respectively. When the data is read during the conversion, however, it is recommended that it is read only during the first half of the conversion phase. This avoids any potential feedthrough between voltage transients on the digital interface and the most critical analog conversion circuitry.

The BYTESWAP pin allows a glueless interface to an 8-bit bus. As shown in Figure 38, the LSB byte is output on D[7:0] and the MSB is output on D[15:8] when BYTESWAP is LOW. When BYTESWAP is HIGH, the LSB and MSB bytes are swapped and the LSB is output on D[15:8] and the MSB is output on D[7:0]. By connecting BYTESWAP to an address line, the 16-bit data can be read in two bytes on either D[15:8] or D[7:0].

SERIAL INTERFACE

The AD7666 is configured to use the serial interface when SER/$\overline{PAR}$ is held HIGH. The AD7666 outputs 16 bits of data, MSB first, on the SDOUT pin. This data is synchronized with the 16 clock pulses provided on the SCLK pin. The output data is valid on both the rising and falling edges of the data clock.

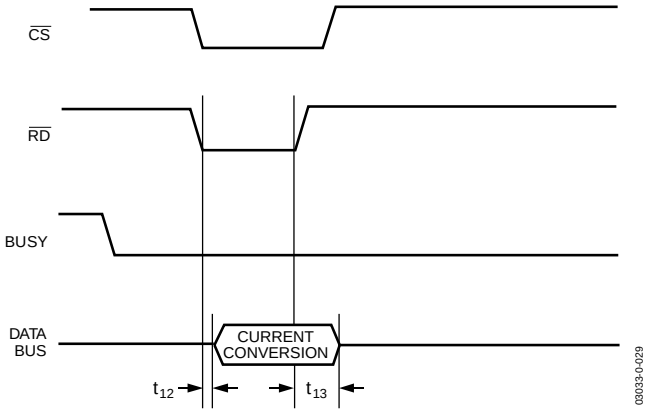


Figure 36. Slave Parallel Data Timing for Reading (Read after Convert)

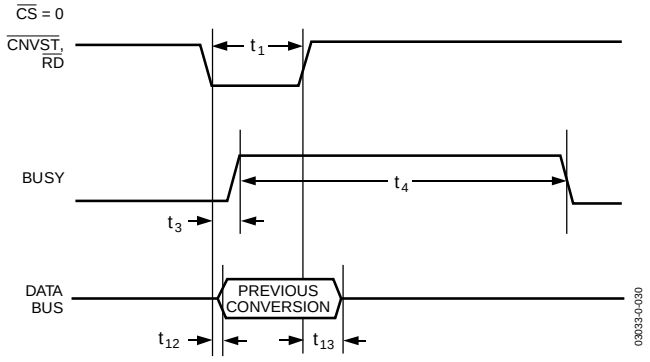


Figure 37. Slave Parallel Data Timing for Reading (Read during Convert)

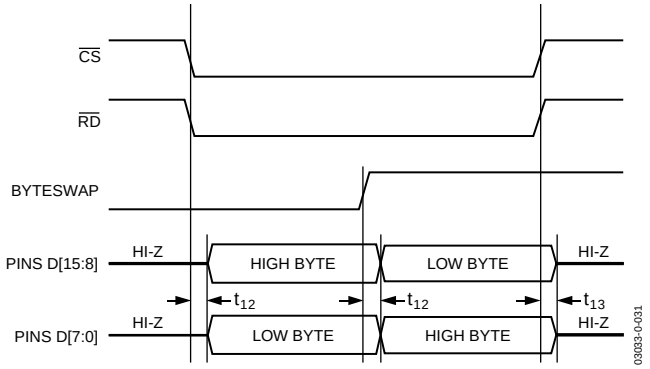


Figure 38 8-Bit Parallel Interface

MASTER SERIAL INTERFACE

Internal Clock

The AD7666 is configured to generate and provide the serial data clock SCLK when the EXT/$\overline{INT}$ pin is held LOW. The AD7666 also generates a SYNC signal to indicate to the host when the serial data is valid. The serial clock SCLK and the SYNC signal can be inverted if desired. Depending on the RDC/SDIN input, the data can be read after each conversion or during the following conversion. Figure 39 and Figure 40 show detailed timing diagrams of these two modes.

Usually, because the AD7666 is used with a fast throughput, the Master Read During Conversion mode is the most recommended serial mode. In this mode, the serial clock and data toggle at appropriate instants, minimizing potential feedthrough between digital activity and critical conversion decisions.

In Read After Conversion mode, it should be noted that unlike in other modes, the BUSY signal returns LOW after the 16 data bits are pulsed out and not at the end of the conversion phase, which results in a longer BUSY width.

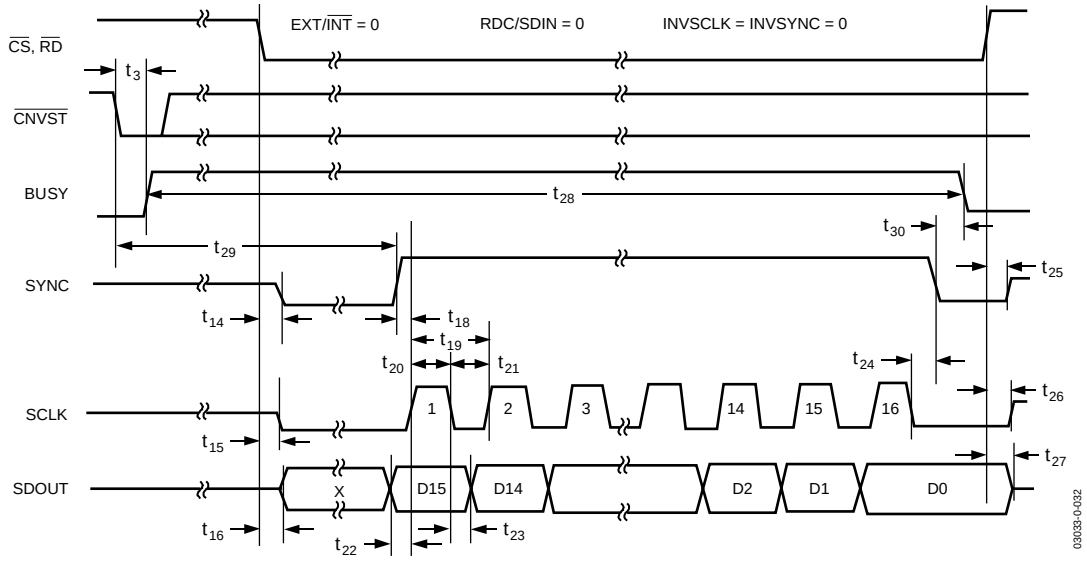


Figure 39. Master Serial Data Timing for Reading (Read after Convert)

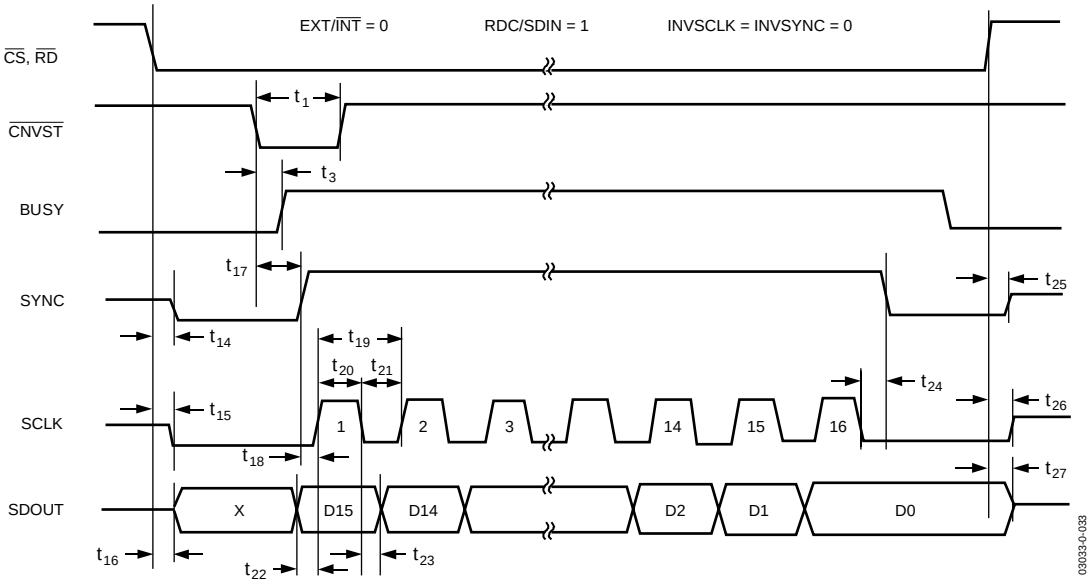


Figure 40. Master Serial Data Timing for Reading (Read Previous Conversion during Convert)

SLAVE SERIAL INTERFACE

External Clock

The AD7666 is configured to accept an externally supplied serial data clock on the SCLK pin when the EXT/$\overline{INT}$ pin is held HIGH. In this mode, several methods can be used to read the data. The external serial clock is gated by $\overline{CS}$. When $\overline{CS}$ and $\overline{RD}$ are both LOW, the data can be read after each conversion or during the following conversion. The external clock can be either a continuous or a discontinuous clock. A discontinuous clock can be either normally HIGH or normally LOW when inactive. Figure 41 and Figure 42 show the detailed timing diagrams of these methods. Usually, because the AD7666 has a longer acquisition phase than conversion phase, the data are read immediately after conversion.

While the AD7666 is performing a bit decision, it is important that voltage transients be avoided on digital input/output pins or degradation of the conversion result could occur. This is particularly important during the second half of the conversion phase because the AD7666 provides error correction circuitry that can correct for an improper bit decision made during the first half of the conversion phase. For this reason, it is recommended that when an external clock is being provided, it is a discontinuous clock that is toggling only when BUSY is LOW, or, more importantly, that it does not transition during the latter half of BUSY HIGH.

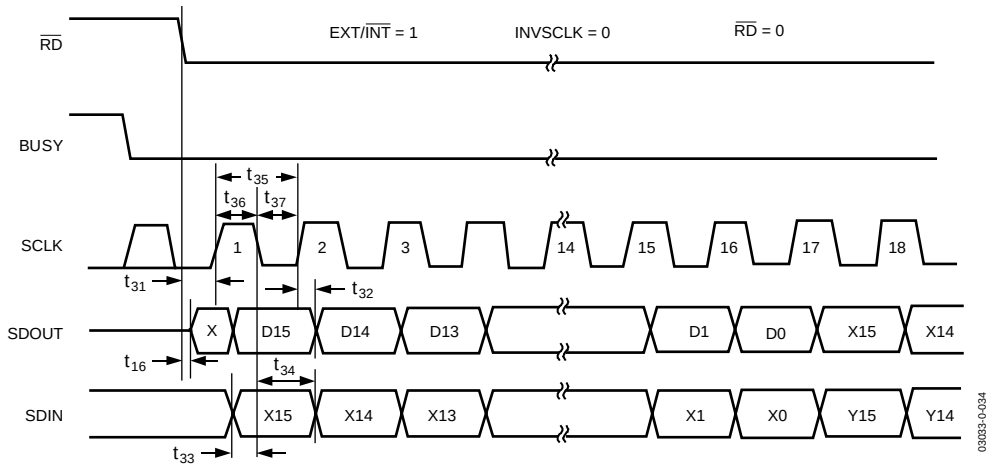


Figure 41. Slave Serial Data Timing for Reading (Read after Convert)

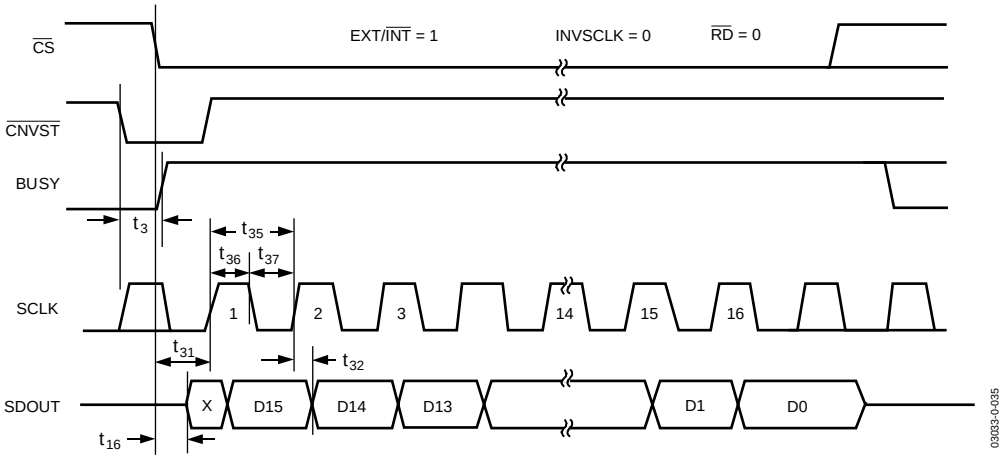


Figure 42. Slave Serial Data Timing for Reading (Read Previous Conversion during Convert)

External Discontinuous Clock Data Read After Conversion

Though the maximum throughput cannot be achieved using this mode, it is the most recommended of the serial slave modes. Figure 41 shows the detailed timing diagrams of this method. After a conversion is complete, indicated by BUSY returning LOW, the conversion's result can be read while both $\overline{CS}$ and $\overline{RD}$ are LOW. Data is shifted out MSB first with 16 clock pulses and is valid on the rising and falling edges of the clock.

Among the advantages of this method is the fact that conversion performance is not degraded because there are no voltage transients on the digital interface during the conversion process. Another advantage is the ability to read the data at any speed up to 40 MHz, which accommodates both the slow digital host interface and the fastest serial reading.

Finally, in this mode only, the AD7666 provides a daisy-chain feature using the RDC/SDIN pin for cascading multiple converters together. This feature is useful for reducing component count and wiring connections when desired, as, for instance, in isolated multiconverter applications.

An example of the concatenation of two devices is shown in Figure 43. Simultaneous sampling is possible by using a common $\overline{CNVST}$ signal. It should be noted that the RDC/SDIN input is latched on the opposite edge of SCLK of the one used to shift out the data on SDOUT. Therefore, the MSB of the "upstream" converter just follows the LSB of the "downstream" converter on the next SCLK cycle.

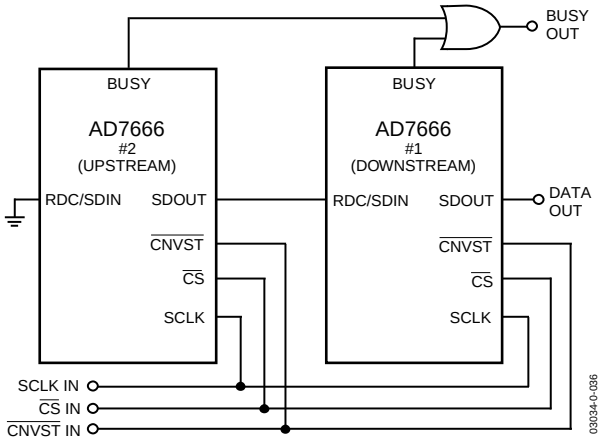


Figure 43. Two AD7666s in a Daisy-Chain Configuration

External Clock Data Read During Conversion

Figure 42 shows the detailed timing diagrams of this method. During a conversion, while both $\overline{CS}$ and $\overline{RD}$ are LOW, the result of the previous conversion can be read. The data is shifted out MSB first with 16 clock pulses, and is valid on both the rising and falling edges of the clock. The 16 bits must be read before the current conversion is complete; otherwise, RDERROR is pulsed HIGH and can be used to interrupt the host interface to prevent incomplete data reading. There is no daisy-chain feature in this mode and the RDC/SDIN input should always be tied either HIGH or LOW.

To reduce performance degradation due to digital activity, a fast discontinuous clock of at least 18 MHz is recommended to ensure that all the bits are read during the first half of the conversion phase. It is also possible to begin to read data after conversion and continue to read the last bits after a new conversion has been initiated. This allows the use of a slower clock speed like 14 MHz.

MICROPROCESSOR INTERFACING

The AD7666 is ideally suited for traditional dc measurement applications supporting a microprocessor, and for ac signal processing applications interfacing to a digital signal processor. The AD7666 is designed to interface either with a parallel 8-bit or 16-bit wide interface, or with a general-purpose serial port or I/O ports on a microcontroller. A variety of external buffers can be used with the AD7666 to prevent digital noise from coupling into the ADC. The following section discusses the use of an AD7666 with an ADSP-219x SPI equipped DSP.

SPI Interface (ADSP-219x)

Figure 44 shows an interface diagram between the AD7666 and the SPI equipped ADSP-219x. To accommodate the slower speed of the DSP, the AD7666 acts as a slave device and data must be read after conversion. This mode also allows the daisy-chain feature. The convert command can be initiated in response to an internal timer interrupt. The reading process can be initiated in response to the end-of-conversion signal (BUSY going LOW) using an interrupt line of the DSP. The serial interface (SPI) on the ADSP-219x is configured for master mode (MSTR) = 1, Clock Polarity bit (CPOL) = 0, Clock Phase bit (CPHA) = 1, and SPI Interrupt Enable (TIMOD) = 00 by writing to the SPI control register (SPICLTx). To meet all timing requirements, the SPI clock should be limited to 17 Mbps, which allows it to read an ADC result in less than 1 µs. When a higher sampling rate is desired, use of one of the parallel interface modes is recommended.

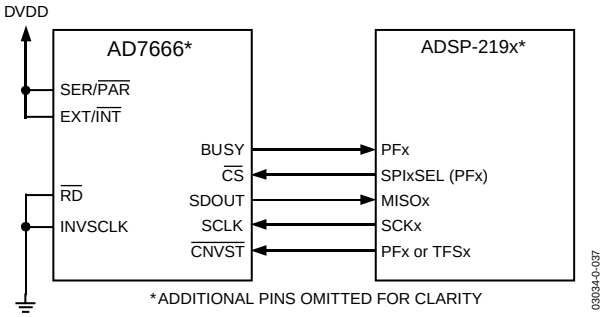


Figure 44. Interfacing the AD7666 to an SPI Interface

APPLICATION HINTS

BIPOLAR AND WIDER INPUT RANGES

In some applications, it is desirable to use a bipolar or wider analog input range such as ±10 V, ±5 V, or 0 V to 5 V. Although the AD7666 has only one unipolar range, simple modifications of input driver circuitry allow bipolar and wider input ranges to be used without any performance degradation. Figure 45 shows a connection diagram that allows this. Component values required and resulting full-scale ranges are shown in Table 8.

When desired, accurate gain and offset can be calibrated by acquiring a ground and voltage reference using an analog multiplexer (U2), as shown in Figure 45.

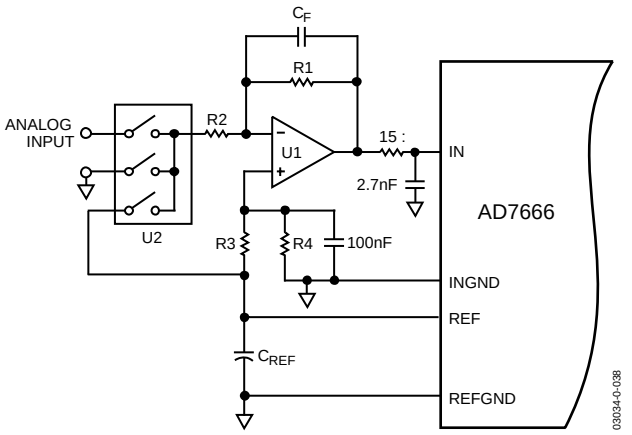


Figure 45. Using the AD7666 in 16-Bit Bipolar and/or Wider Input Ranges

Table 8. Component Values and Input Ranges

Input Range	R1 ( )	R2 (k)	R3 (k)	R4 (k)
±10 V	500	4	2.5	2
±5 V	500	2	2.5	1.67
0 V to …V	500	1	None	0

LAYOUT

The AD7666 has very good immunity to noise on the power supplies. However, care should still be taken with regard to grounding layout.

The printed circuit board that houses the AD7666 should be designed so the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be separated easily. Digital and analog ground planes should be joined in only one place, preferably underneath the AD7666, or as close as possible to the AD7666. If the AD7666 is in a system where multiple devices require analog-to-digital ground connections, the connection should still be made at one point only, a star ground point that should be established as close as possible to the AD7666.

Running digital lines under the device should be avoided since these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7666 to avoid noise coupling. Fast switching signals like $\overline{CNVST}$ or clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and should never run near analog signal paths. Crossover of digital and analog signals should be avoided. Traces on different but close layers of the board should run at right angles to each other. This will reduce the effect of crosstalk through the board.

The power supply lines to the AD7666 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Good decoupling is also important to lower the supply's impedance presented to the AD7666 and to reduce the magnitude of the supply spikes. Decoupling ceramic capacitors, typically 100 nF, should be placed on each power supply pin„ AVDD, DVDD, and OVDD„ close to, and ideally right up against these pins and their corresponding ground pins. Additionally, low ESR 10 µF capacitors should be located near the ADC to further reduce low frequency ripple.

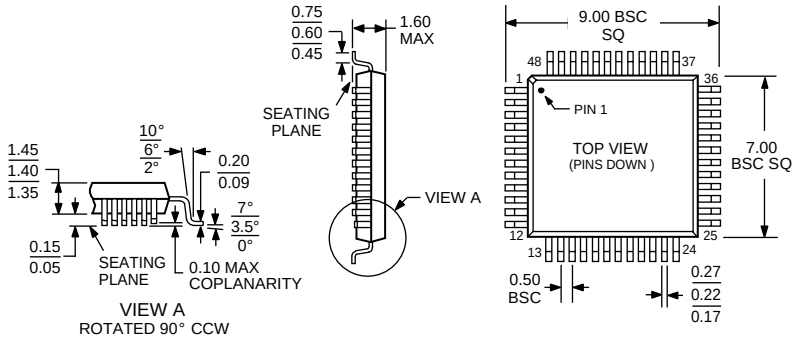
The DVDD supply of the AD7666 can be a separate supply, or can come from the analog supply AVDD or the digital interface supply OVDD. When the system digital supply is noisy or when fast switching digital signals are present, if no separate supply is available, the user should connect DVDD to AVDD through an RC filter (see Figure 26) and the system supply to OVDD and the remaining digital circuitry. When DVDD is powered from the system supply, it is useful to insert a bead to further reduce high frequency spikes.

The AD7666 has five different ground pins: INGND, REFGND, AGND, DGND, and OGND. INGND is used to sense the analog input signal. REFGND senses the reference voltage and, because it carries pulsed currents, should be a low impedance return to the reference. AGND is the ground to which most internal ADC analog signals are referenced; it must be connected with the least resistance to the analog ground plane. DGND must be tied to the analog or digital ground plane depending on the configuration. OGND is connected to the digital system ground.

EVALUATING THE AD7666•S PERFORMANCE

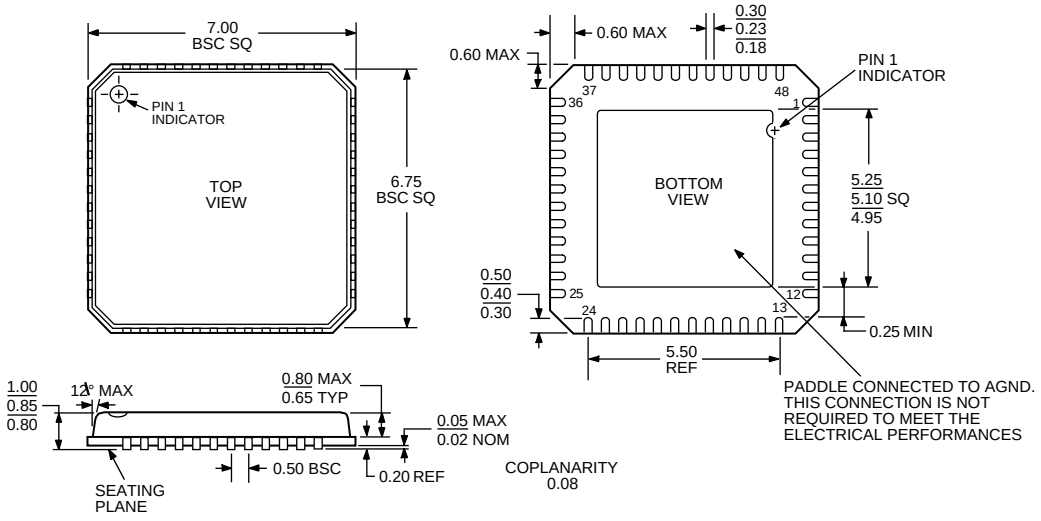
A recommended layout for the AD7666 is outlined in the EVAL-AD7666 evaluation board for the AD7666. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the EVAL-CONTROL BRD2.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026BBC

Figure 46. 48-Lead Quad Flatpack (LQFP) [ST-48]
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VKKD-2

Figure 47. 48-Lead Frame Chip Scale Package (LFCSP) [CP-48]
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7666AST	…40°C to +85°C	Quad Flatpack (LQFP)	ST-48
AD7666ASTRL	…40°C to +85°C	Quad Flatpack (LQFP)	ST-48
AD7666ACP	…40°C to +85°C	Lead Frame Chip Scale (LFCSP)	CP-48
AD7666ACPRL	…40°C to +85°C	Lead Frame Chip Scale (LFCSP)	CP-48
EVAL-AD7666CB[1]		Evaluation Board	
EVAL-CONTROL BRD2[2]		Controller Board	

[1]This board can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BRD2 for evaluation/demonstration purposes.
[2]This board allows a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

D03034…0…1/04(0)

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