LTC2442

24-Bit High Speed 4-Channel ΔΣ ADC with Integrated Amplifier

FEATURES

- **1ppm Linearity with No Missing Codes**
- **Integrated Amplifier for Direct Sensor Digitization**
- **2 Differential or 4 Single-Ended Input Channels**
- **Up to 8kHz Output Rate**
- **Up to 4kHz Multiplexing Rate**
- **Selectable Speed/Resolution**
  - **2μV_{RMS} Noise at 1.76kHz Output Rate**
  - **220nV_{RMS} Noise at 13.8Hz Output Rate with Simultaneous 50Hz/60Hz Rejection**
- Guaranteed Modulator Stability and Lock-Up Immunity for any Input and Reference Conditions
- <5μV Offset (4.5V < V_{CC} < 5.5V, –40°C to 85°C)
- Differential Input and Differential Reference with GND to V_{CC} Common Mode Range
- No Latency Mode, Each Conversion is Accurate Even After a New Channel is Selected
- Internal Oscillator—No External Components
- 36-Lead SSOP Package

APPLICATIONS

- Auto Ranging 6-Digit DVMs
- High Speed Multiplexing
- Weight Scales
- Direct Temperature Measurement
- High Speed Data Acquisition

DESCRIPTION

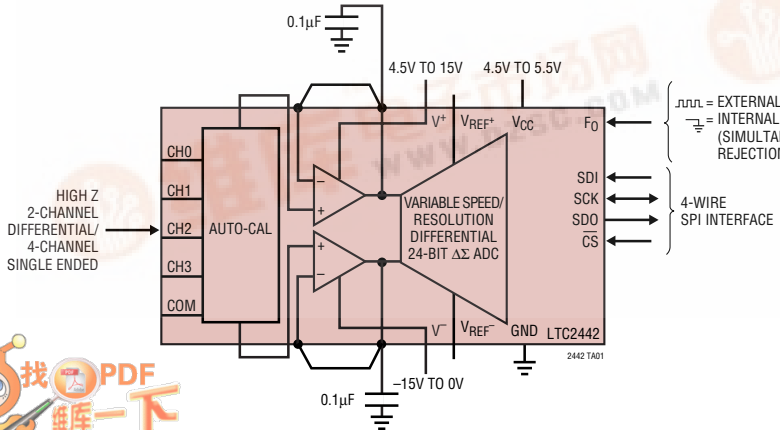
The LTC®2442 is an ultra high precision, variable speed, 24-bit ΔΣ™ ADC with integrated amplifier. The amplifier can be configured as a buffer for easy input drive of high impedance sensors. 1 part-per-million (ppm) linearity is achievable when the amplifier is configured in unity gain. External resistors can be used to set a gain for increased resolution of low level input signals. The positive and negative amplifier supply pins may be tied directly to V_{CC} (4.5V to 5.5V) and GND or biased above V_{CC} and below GND for rail-to-rail input signals.

The proprietary ΔΣ architecture ensures stable DC accuracy through continuous transparent calibration. Ten speed/resolution combinations from 6.9Hz/220nV_{RMS} to 3.5kHz/25μV_{RMS} can be selected with no latency or shift in DC accuracy. Additionally, a 2X speed mode can be selected enabling output rates up to 7kHz (8kHz with an external oscillator) with one cycle latency.

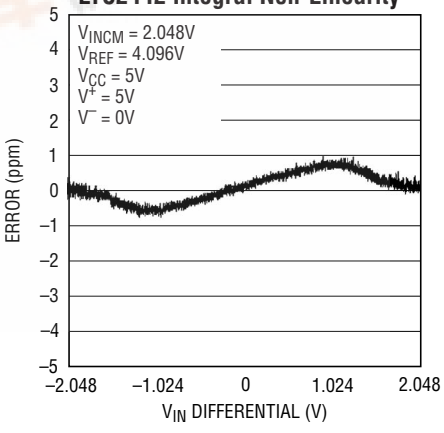
Any combination of single-ended (up to 4 inputs) or differential (up to 2 inputs) can be selected with a common mode input range from ground to V_{CC}. While operating in the 1X speed mode the first conversion following a new speed/resolution or channel selection is valid.

TYPICAL APPLICATION

High Precision Data Acquisition System



LTC2442 Integral Non-Linearity

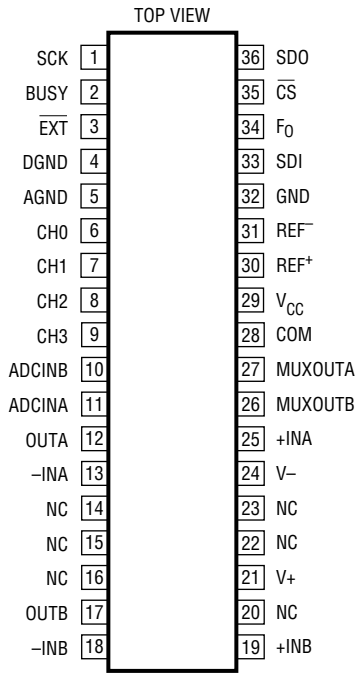


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) to GND ..... –0.3V to 6V
Analog Input Pins Voltage
to GND ..... –0.3V to (V_{CC} + 0.3V)
Reference Input Pins Voltage
to GND ..... –0.3V to (V_{CC} + 0.3V)
Digital Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Digital Output Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Operating Temperature Range
LTC2442CG ..... 0°C to 70°C
LTC2442IG ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Amplifier Supply Voltage (V^+ to V^-) 36V

PACKAGE/ORDER INFORMATION



G PACKAGE
36-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 160°C/W

ORDER PART NUMBER	PART MARKING
LTC2442CG LTC2442IG	LTC2442CG LTC2442IG

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4, 15)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	0.1V ≤ V_{REF} ≤ V_{CC}, –0.5 • V_{REF} ≤ V_{IN} ≤ 0.5 • V_{REF} (Note 5)	●	24			Bits
Integral Nonlinearity	V_{CC} = 5V, REF^+ = 5V, REF^- = GND, V_{INCM} = 2.5V (Note 6, 14) V_{CC} = 5V, REF^+ = 2.5V, REF^- = GND, V_{INCM} = 1.25V (Note 6, 14) REF^+ = 4.096V, REF^- = GND, V_{INCM} = 2.048V (Note 6, 14)	● ● 		2 2 1	10 7 	ppm of V_{REF} ppm of V_{REF} ppm of V_{REF}
Offset Error	2.5V ≤ REF^+ ≤ V_{CC}, REF^- = GND, GND ≤ SEL^+ = SEL^- ≤ V_{CC} (Note 12)	●		2.5	5	µV
Offset Error Drift	2.5V ≤ REF^+ ≤ V_{CC}, REF^- = GND, GND ≤ SEL^+ = SEL^- ≤ V_{CC}			20		nV/°C
Positive Full-Scale Error	REF^+ = 5V, REF^- = GND, SEL^+ = 3.75V, SEL^- = 1.25V REF^+ = 2.5V, REF^- = GND, SEL^+ = 1.875V, SEL^- = 0.625V	● ●		10 10	50 50	ppm of V_{REF} ppm of V_{REF}
Positive Full-Scale Error Drift	2.5V ≤ REF^+ ≤ V_{CC}, REF^- = GND, SEL^+ = 0.75 • REF^+, SEL^- = 0.25 • REF^+			0.2		ppm of V_{REF}/°C

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4, 15)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Negative Full-Scale Error	REF^+ = 5V, REF^- = GND, SEL^+ = 1.25V, SEL^- = 3.75V REF^+ = 2.5V, REF^- = GND, SEL^+ = 0.625V, SEL^- = 1.875V	● ●		10 10	50 50	ppm of V_{REF} ppm of V_{REF}
Negative Full-Scale Error Drift	2.5V ≤ REF^+ ≤ V_{CC}, REF^- = GND, SEL^+ = 0.25 • REF^+, SEL^- = 0.75 • REF^+			0.2		ppm of V_{REF}/°C
Total Unadjusted Error	5V ≤ V_{CC} ≤ 5.5V, REF^+ = 2.5V, REF^- = GND, V_{INCM} = 1.25V (Note 6) 5V ≤ V_{CC} ≤ 5.5V, REF^+ = 5V, REF^- = GND, V_{INCM} = 2.5V (Note 6) REF^+ = 2.5V, REF^- = GND, V_{INCM} = 1.25V (Note 6)			12 12 12		ppm of V_{REF} ppm of V_{REF} ppm of V_{REF}
Input Common Mode Rejection DC	2.5V ≤ REF^+ ≤ V_{CC}, REF^- = GND, GND ≤ SEL^- = SEL^+ ≤ V_{CC}			120		dB

ANALOG INPUT AND REFERENCE

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 15)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SEL^+	Absolute/Common Mode SEL^+ Voltage	SEL^+ is the Positive Selected Input Channel, see Table 3	●	GND – 0.3		V_{CC} + 0.3	V
SEL^-	Absolute/Common Mode SEL^- Voltage	SEL^- is the Negative Selected Input Channel, see Table 3	●	GND – 0.3		V_{CC} + 0.3	V
V_{IN}	Input Differential Voltage Range ($SEL^+ – SEL^-$)		●	$–V_{REF}/2$		$V_{REF}/2$	V
REF^+	Absolute/Common Mode REF^+ Voltage		●	0.1		V_{CC}	V
REF^-	Absolute/Common Mode REF^- Voltage		●	GND		V_{CC} – 0.1	V
V_{REF}	Reference Differential Voltage Range ($REF^+ – REF^-$)		●	0.1		V_{CC}	V
$C_{S(ADCINA)}$	ADCINA Sampling Capacitance				2		pF
$C_{S(ADCINB)}$	ADCINB Sampling Capacitance				2		pF
$C_{S(REF^+)}$	REF^+ Sampling Capacitance				2		pF
$C_{S(REF^-)}$	REF^- Sampling Capacitance				2		pF
$I_{DC\_LEAK(SEL^+, SEL^-, REF^+, REF^-)}$	Leakage Current, Inputs and Reference	$\overline{CS}$ = V_{CC}, SEL^+ = GND, SEL^- = GND, REF^+ = 5V, REF^- = GND	●	–15	1	15	nA
t_{OPEN}	MUX Break-Before-Make				50		ns
QIRR	MUX Off Isolation	V_{IN} = $2V_{P-P}$ DC to 1.8MHz			120		dB

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage $\overline{CS}$, F_O, $\overline{EXT}$, SDI	4.5V ≤ V_{CC} ≤ 5.5V	●	2.5			V
V_{IL}	Low Level Input Voltage $\overline{CS}$, F_O, $\overline{EXT}$, SDI	4.5V ≤ V_{CC} ≤ 5.5V	●			0.8	V
V_{IH}	High Level Input Voltage SCK	4.5V ≤ V_{CC} ≤ 5.5V (Note 8)	●	2.5			V
V_{IL}	Low Level Input Voltage SCK	4.5V ≤ V_{CC} ≤ 5.5V (Note 8)	●			0.8	V
I_{IN}	Digital Input Current $\overline{CS}$, F_O, $\overline{EXT}$, SDI	0V ≤ V_{IN} ≤ V_{CC}	●	–10		10	µA
I_{IN}	Digital Input Current SCK	0V ≤ V_{IN} ≤ V_{CC} (Note 8)	●	–10		10	µA
C_{IN}	Digital Input Capacitance $\overline{CS}$, F_O, $\overline{EXT}$, SDI				10		pF
C_{IN}	Digital Input Capacitance SCK	(Note 8)			10		pF
V_{OH}	High Level Output Voltage SDO, BUSY	I_O = –800µA	●	V_{CC} – 0.5			V
V_{OL}	Low Level Output Voltage SDO, BUSY	I_O = 1.6µA	●			0.4	V
V_{OH}	High Level Output Voltage SCK	I_O = –800µA (Note 9)	●	V_{CC} – 0.5			V
V_{OL}	Low Level Output Voltage SCK	I_O = 1.6µA (Note 9)	●			0.4	V
I_{OZ}	Hi-Z Output Leakage SDO		●	–10		10	µA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	4.5		5.5	V
V^+	Amplifier Positive Supply		●	4.5		15	V
V^-	Amplifier Negative Supply		●	–15		0	V
I_{CC}	Supply Current	Amplifiers and ADC	●		10	13	mA

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range		●	0.1		20	MHz
t_{HEO}	External Oscillator High Period		●	25		10000	ns
t_{LEO}	External Oscillator Low Period		●	25		10000	ns
t_{CONV}	Conversion Time	OSR = 256 (SDI = 0) OSR = 32768 (SDI = 1) External Oscillator (Notes 10, 13)	● ● ●	0.99 126	1.13 145 $\frac{40 \bullet OSR + 170}{f_{EOSC}\ (KHz)}$	1.33 170	ms ms ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 9) External Oscillator (Notes 9, 10)	●	0.8	0.9 $f_{EOSC}/10$	1	MHz Hz
D_{ISCK}	Internal SCK Duty Cycle	(Note 9)	●	45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 8)	●			20	MHz
fLESCK	External SCK Low Period	(Note 8)	●	25			ns
t_{HESCK}	External SCK High Period	(Note 8)	●	25			ns
t_{DOUT_ISCK}	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 9, 11) External Oscillator (Notes 9, 10)	● ●	30.9	35.3 $320/f_{EOSC}$	41.6	µs s
t_{DOUT_ESCK}	External SCK 32-Bit Data Output Time	(Note 8)	●		$32/f_{ESCK}$		s
t_1	$\overline{CS}$ ↓ to SDO Low Z	(Note 12)	●	0		25	ns
t_2	$\overline{CS}$ ↑ to SDO High Z	(Note 12)	●	0		25	ns
t_3	$\overline{CS}$ ↓ to SCK ↓	(Note 9)			5		µs
t_4	$\overline{CS}$ ↓ to SCK ↑	(Note 8, 12)	●	25			ns
t_{KQMAX}	SCK ↓ to SDO Valid		●			25	ns
t_{KQMIN}	SDO Hold After SCK ↓	(Note 5)	●	15			ns
t_5	SCK Setup Before $\overline{CS}$ ↓		●	50			ns
t_6	SCK Hold After $\overline{CS}$ ↓		●			50	ns
t_7	SDI Setup Before SCK ↑	(Note 5)	●	10			ns
t_8	SDI Hold After SCK ↑	(Note 5)	●	10			ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 4.5V to 5.5V unless otherwise specified.
$V_{REF} = REF^+ – REF^–$, $V_{REFCM} = (REF^+ + REF^–)/2$;
$V_{IN} = SEL^+ – SEL^–$, $V_{INCM} = (SEL^+ + SEL^–)/2$.

Note 4: F_O pin tied to GND or to external conversion clock source with f_{EOSC} = 10MHz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: The converter uses the internal oscillator.

Note 8: The converter is in external SCK mode of operation such that the SCK pin is used as a digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in Hz.

Note 9: The converter is in internal SCK mode of operation such that the SCK pin is used as a digital output. In this mode of operation, the SCK pin has a total equivalent load capacitance of C_{LOAD} = 20pF.

Note 10: The external oscillator is connected to the F_O pin. The external oscillator frequency, f_{EOSC}, is expressed in Hz.

Note 11: The converter uses the internal oscillator. F_O = 0V.

Note 12: Guaranteed by design and test correlation.

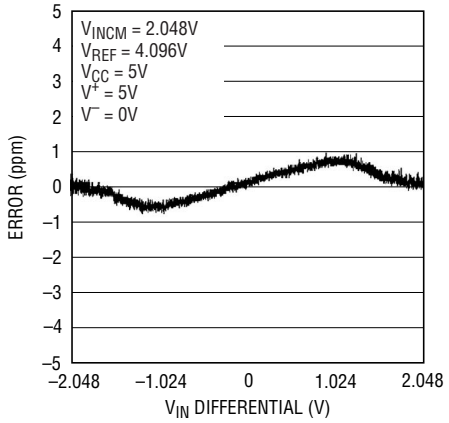
Note 13: There is an internal reset that adds an additional 1µs (typ) to the conversion time.

Note 14: In order to achieve optimum linearity, the amplifier power positive supply input (V^+) must exceed the maximum input voltage level by 2V or greater. The negative amplifier power supply input ($V^–$) must be at least 200mV below the minimum input voltage level.

Note 15: Amplifiers are externally compensated with 0.1µF.

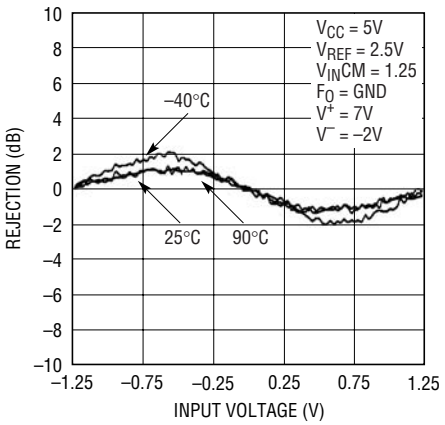
TYPICAL PERFORMANCE CHARACTERISTICS

Integral Non-Linearity



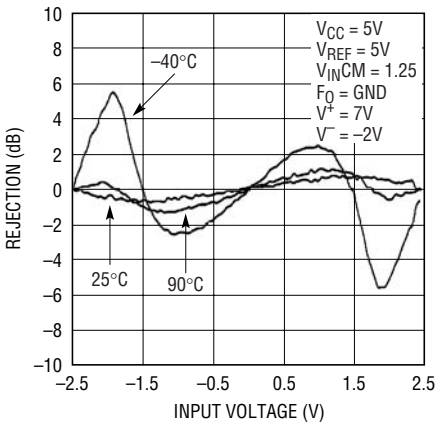
2442 TA02

Integral Non-Linearity vs Temperature



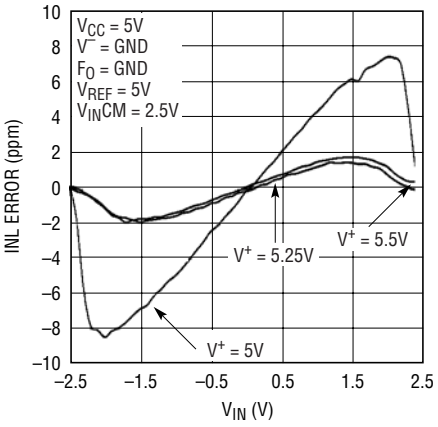
2442 G02

Integral Non-Linearity vs Temperature



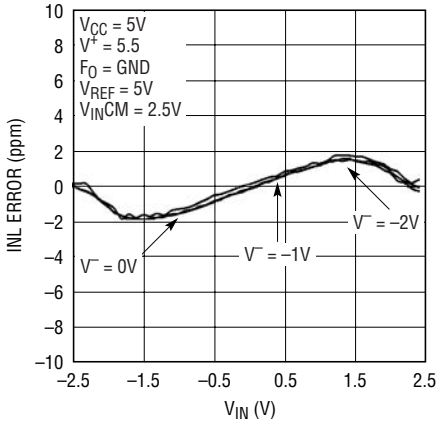
2442 G03

INL vs Op Amp Positive Supply Voltage (V^+)



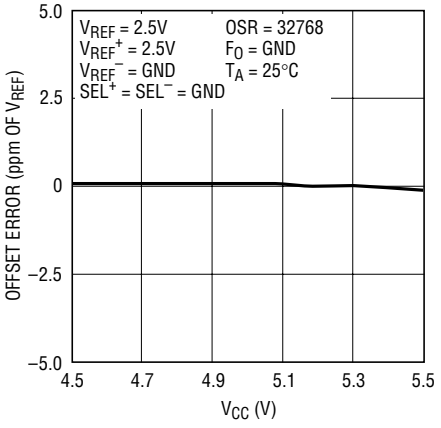
2442 G04

INL vs Op Amp Negative Supply Voltage (V^-)



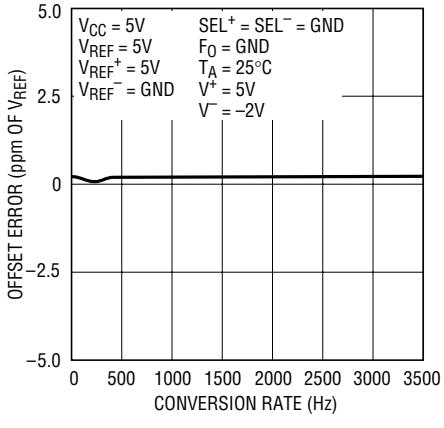
2442 G05

Offset Error vs Supply Voltage



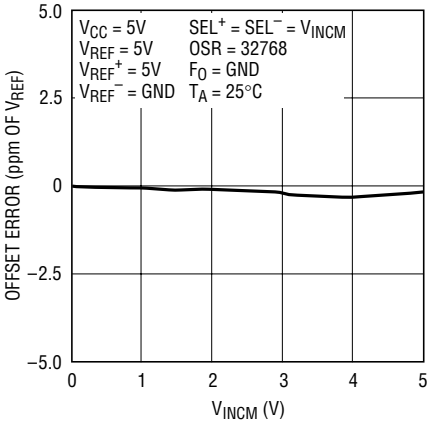
2442 G06

Offset Error vs Conversion Rate



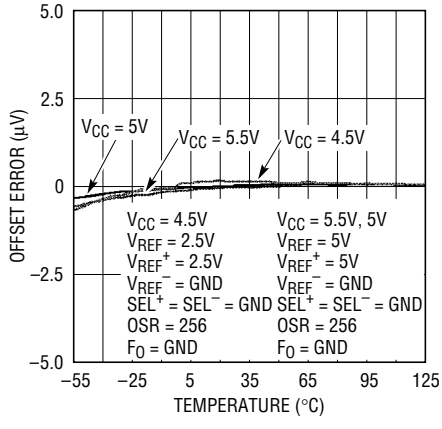
2442 G07

Offset Error vs Common Mode Input Voltage



2442 G08

Offset Error vs Temperature



2442 G09

PIN FUNCTIONS

SCK (Pin 1): Bidirectional Digital Clock Pin. In internal serial clock operation mode, SCK is used as a digital output for the internal serial interface clock during the data output period. In the external serial clock operation mode, SCK is used as the digital input for the external serial interface clock during the data output period. The serial clock operation mode is determined by the logic level applied to $\overline{EXT}$ (Pin 3).

BUSY (Pin 2): Conversion in Progress Indicator. This pin is HIGH while the conversion is in progress and goes LOW indicating the conversion is complete and data is ready. It remains LOW during the sleep and data output states. At the conclusion of the data output state, it goes HIGH indicating a new conversion has begun.

$\overline{EXT}$ (Pin 3): Internal/External SCK Selection Pin. This pin is used to select internal or external SCK for outputting/inputting data. If $\overline{EXT}$ is tied low, the device is in the external SCK mode and data is shifted out of the device under the control of a user applied serial clock. If $\overline{EXT}$ is tied high, the internal serial clock mode is selected. The device generates its own SCK signal and outputs this on the SCK pin. A framing signal BUSY (Pin 2) goes low indicating data is being output.

GND (Pins 4, 5, 32): Ground. Multiple ground pins internally connected for optimum ground current flow and V_{CC} decoupling. Connect each one of these pins to a common ground plane through a low impedance connection. All three pins must be connected to ground for proper operation.

CH0 to CH3 (Pins 6, 7, 8, 9): Analog Inputs. May be programmed for single-ended or differential mode. (See Table 3)

ANCINB (Pin 10): ADC Input. Must tie to the amplifier output, OUTB (Pin 17).

ADCINA (Pin 11): ADC Input. Must tie to the amplifier output, OUTA (Pin 12).

OUTA (Pin 12): Amplifier A output. Must be compensated with 0.1µF or greater capacitor. Drives the ADCINA ADC input (Pin 11).

–INA (Pin 13): Amplifier A negative Input. By shorting this pin to OUTA (Pin 12) the amplifier becomes a buffer with unity gain. Alternatively, an external resistor network may be added here for gains greater than 1.

NC (Pins 14, 15, 16, 20, 22, 23): No Connect. These pins should be left floating or tied to Ground.

OUTB (Pin 17): Amplifier B Output. Must be compensated with 0.1µF or greater capacitor. Drives the ADCINB ADC input (Pin 10).

–INB (Pin 18): Amplifier B negative Input. By shorting this pin to OUTB (Pin 17) the amplifier becomes a buffer with unity gain. Alternatively, an external resistor network may be added here for gains greater than 1.

+INB (Pin 19): Amplifier B positive Input. Must tie to the Multiplexer output MUXOUTB (Pin 26).

V^+ (Pin 21): Amplifier positive supply voltage input. May tie to V_{CC} or an external supply voltage up to 15V. Bypass to GND with 1µF capacitor.

$V^–$ (Pin 24): Amplifier Negative supply voltage input. May tie to GND or an external supply voltage as low as –15V. Bypass to GND with a 1µF capacitor.

+INA (Pin 25): Amplifier A positive Input. Must tie to the Multiplexer output MUXOUTA (Pin 27).

MUXOUTB (Pin 26): Multiplexer Output. Must tie to +INB amplifier input (Pin 19).

PIN FUNCTIONS

MUXOUTA (Pin 27): Multiplexer Output. Must tie to +INA amplifier input (Pin 25).

COM (Pin 28): The common negative input (SEL^-) for all single ended multiplexer configurations. The voltage on CH0-CH3 and COM pins can have any value between GND –0.3V to V_{CC} +0.3V. Within these limits, the two selected inputs (SEL^+ and SEL^-) provide a bipolar input range ($V_{IN} = SEL^+ – SEL^-$) from $–0.5 • V_{REF}$ to $0.5 • V_{REF}$. Outside this input range, the converter produces unique over-range and under-range output codes.

V_{CC} (Pin 29): Positive Supply Voltage. Bypass to GND with a 10µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor as close to the part as possible.

REF^+ (Pin 30), REF^- (Pin 31): Differential Reference Input. The voltage on these pins can have any value between GND and V_{CC} as long as the reference positive input, REF^+, is maintained more positive than the negative reference input, REF^-, by at least 0.1V. Bypass to GND with 0.1µF Ceramic capacitor as close to the part as possible.

SDI (Pin 33): Serial Data Input. This pin is used to select the speed, 1X or 2X mode, resolution and input channel for the next conversion cycle. At initial power up, the default mode of operation is CH0-CH1, OSR of 256 and 1X mode. The serial data input contains an enable bit which determines if a new channel/speed is selected. If this bit is low the following conversion remains at the same speed and selected channel. The serial data input is applied to the device under control of the serial clock (SCK) during the data output cycle. The first conversion following a new channel/speed is valid.

F_O (Pin 34): Frequency Control Pin. Digital input that controls the internal conversion clock. When F_O is connected to V_{CC} or GND, the converter uses its internal oscillator running at 9MHz. The conversion rate is determined by the selected OSR such that t_{CONV} (ms) = 40 • OSR + 170/f_{OSC} (kHz). The first digital filter null is located at 8/t_{CONV}, 7kHz at OSR = 256 and 55Hz (Simultaneous 50Hz/60Hz at OSR = 32768. This pin may be driven with a maximum external clock of 10.24MHz resulting in a maximum 8kHz output rate (OSR = 64, 2X mode).

$\overline{CS}$ (Pin 35): Active Low Chip Select. A LOW on this pin enables the SDO digital output and wakes up the ADC. Following each conversion the ADC automatically enters the sleep mode and remains in this state as long as $\overline{CS}$ is HIGH. A LOW-to-HIGH transition on $\overline{CS}$ during the Data Output aborts the data transfer and starts a new conversion.

SDO (Pin 36): Three-State Digital Output. During the data output period, this pin is used as serial data output. When the chip select $\overline{CS}$ is HIGH ($\overline{CS} = V_{CC}$) the SDO pin is in a high impedance state. During the conversion and sleep periods, this pin is used as the conversion status output. The conversion status can be observed by pulling $\overline{CS}$ LOW. This signal is HIGH while the conversion is in progress and goes LOW once the conversion is complete.

FUNCTIONAL BLOCK DIAGRAM

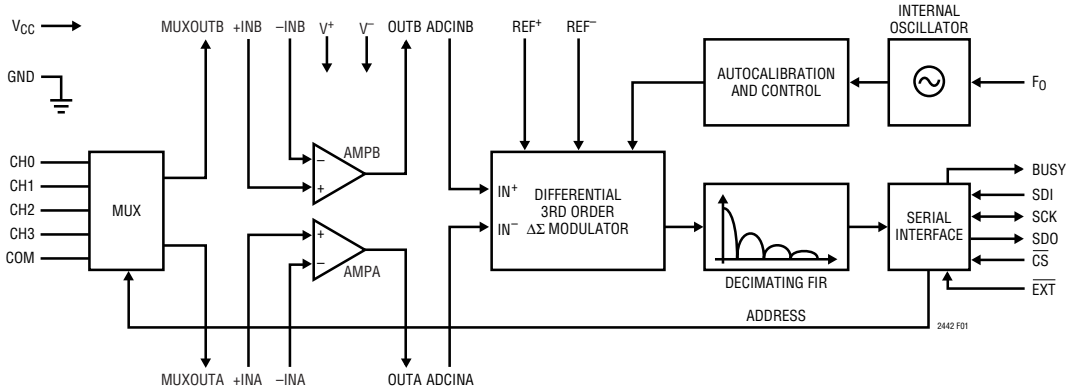
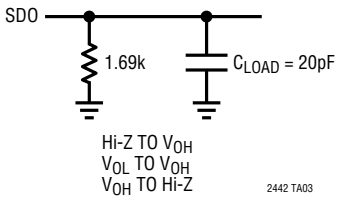
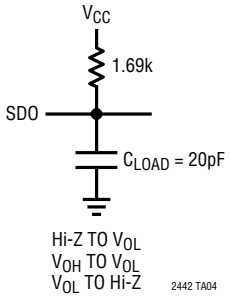


Figure 1. Functional Block Diagram

TEST CIRCUITS





APPLICATIONS INFORMATION

CONVERTER OPERATION

Converter Operation Cycle

The LTC2442 is a multi-channel, high speed, ΔΣ analog-to-digital converter with an easy to use 3- or 4-wire serial interface (see Figure 1). Its operation is made up of three states. The converter operating cycle begins with the conversion, followed by the sleep state and ends with the data output/input (see Figure 2). The 4-wire interface consists of serial data input (SDI), serial data output (SDO), serial clock (SCK) and chip select ($\overline{CS}$). The interface, timing, operation cycle and data out format is compatible with Linear's entire family of ΔΣ converters.

Initially, the LTC2442 performs a conversion. Once the conversion is complete, the device enters the sleep state. The part remains in the sleep state as long as $\overline{CS}$ is HIGH. The conversion result is held indefinitely in a static shift register while the converter is in the sleep state.

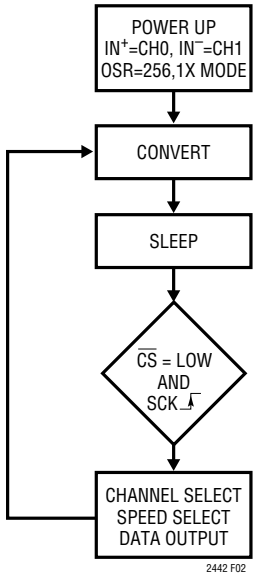


Figure 2. LTC2442 State Transition Diagram

APPLICATIONS INFORMATION

Once $\overline{CS}$ is pulled LOW, the device begins outputting the conversion result. There is no latency in the conversion result while operating in the 1X mode. The data output corresponds to the conversion just performed. This result is shifted out on the serial data out pin (SDO) under the control of the serial clock (SCK). Data is updated on the falling edge of SCK allowing the user to reliably latch data on the rising edge of SCK (see Figure 3). The data output state is concluded once 32 bits are read out of the ADC or when $\overline{CS}$ is brought HIGH. In either scenario, the device automatically initiates a new conversion and the cycle repeats.

Through timing control of the $\overline{CS}$, SCK and $\overline{EXT}$ pins, the LTC2442 offers several flexible modes of operation (internal or external SCK). These various modes do not require programming configuration registers; moreover, they do not disturb the cyclic operation described above. These modes of operation are described in detail in the Serial Interface Timing Modes section.

Ease of Use

The LTC2442 data output has no latency, filter settling delay or redundant data associated with the conversion cycle while operating in the 1X mode. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing multiple analog voltages is easy. Speed/resolution adjustments may be made seamlessly between two conversions without settling errors.

The LTC2442 performs offset and full-scale calibrations every conversion cycle. This calibration is transparent to the user and has no effect on the cyclic operation described above. The advantage of continuous calibration is extreme stability of offset and full-scale readings with respect to time, supply voltage change and temperature drift.

Power-Up Sequence

The LTC2442 automatically enters an internal reset state when the power supply voltage V_{CC} drops below approximately 2.2V. This feature guarantees the integrity of the conversion result and of the serial interface mode selection.

When the V_{CC} voltage rises above this critical threshold, the converter creates an internal power-on-reset (POR) signal with a duration of approximately 0.5ms. The POR signal clears all internal registers. The conversion immediately following a POR is performed on the input channel SEL^+ = CH0, SEL^- = CH1 at an OSR = 256 in the 1X mode. Following the POR signal, the LTC2442 starts a normal conversion cycle and follows the succession of states described above. The first conversion result following POR is accurate within the specifications of the device if the power supply voltage is restored within the operating range (4.5V to 5.5V) before the end of the POR time interval.

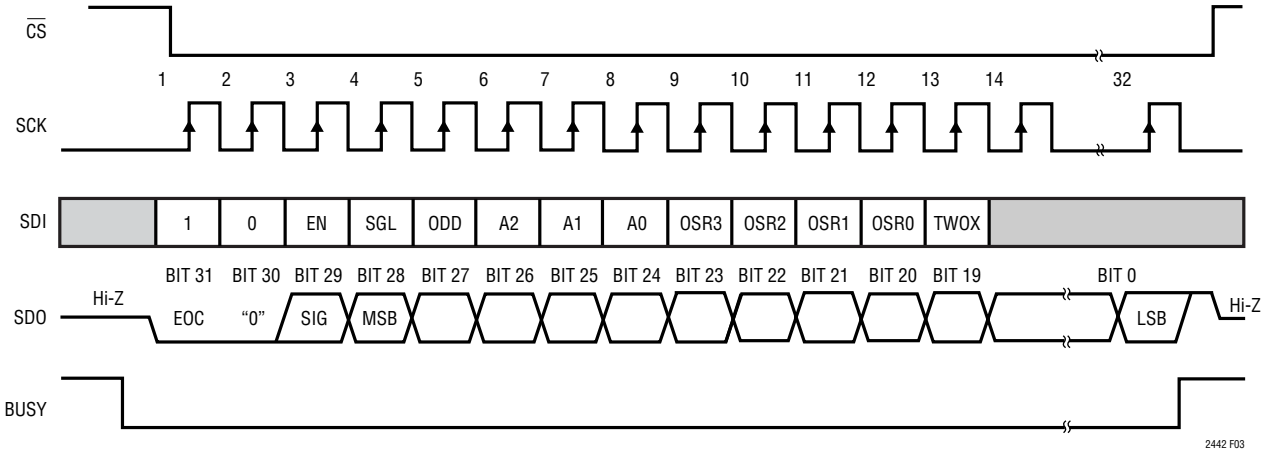


Figure 3. SDI Speed/Resolution, Channel Selection, and Data Output Timing

APPLICATIONS INFORMATION

Reference Voltage Range

The LTC2442 ΔΣ converter accepts a truly differential external reference voltage. The absolute/common mode voltage specification for the REF^+ and REF^- pins covers the entire range from GND to V_{CC}. For correct converter operation, the REF^+ pin must always be more positive than the REF^- pin.

The LTC2442 can accept a differential reference voltage from 0.1V to V_{CC}. The converter output noise is determined by the thermal noise of the front-end circuits, and as such, its value in microvolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter's effective resolution. On the other hand, a reduced reference voltage will improve the converter's overall INL performance.

Input Voltage Range

The analog input is truly differential with an absolute/common mode range for the CH0-CH3 and COM input pins extending from GND – 0.3V to V_{CC} + 0.3V. Outside these limits, the ESD protection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits, the LTC2442 converts the bipolar differential input signal, $V_{IN} = SEL^+ – SEL^-$, from –FS = –0.5 • V_{REF} to +FS = 0.5 • V_{REF} where $V_{REF} = REF^+ – REF^-$. Outside this range, the converter indicates the overrange or the underrange condition using distinct output codes.

Output Data Format

The LTC2442 serial output data stream is 32 bits long. The first three bits represent status information indicating the sign and conversion state. The next 24 bits are the conversion result, MSB first. The remaining five bits are sub LSBs beyond the 24-bit level that may be included in averaging or discarded without loss of resolution. In the case of ultrahigh resolution modes, more than 24 effective bits of performance are possible (see Table 4). Under these conditions, sub LSBs are included in the conversion result and represent useful information beyond the 24-bit level. The third and fourth bit together are also used to indicate an underrange condition (the differential input voltage is below –FS) or an overrange condition (the differential input voltage is above +FS).

Bit 31 (first output bit) is the end of conversion ($\overline{EOC}$) indicator. This bit is available at the SDO pin during the conversion and sleep states whenever the $\overline{CS}$ pin is LOW. This bit is HIGH during the conversion and goes LOW when the conversion is complete.

Bit 30 (second output bit) is a dummy bit (DMY) and is always LOW.

Bit 29 (third output bit) is the conversion result sign indicator (SIG). If V_{IN} is >0, this bit is HIGH. If V_{IN} is <0, this bit is LOW.

Bit 28 (fourth output bit) is the most significant bit (MSB) of the result. This bit in conjunction with Bit 29 also provides the underrange or overrange indication. If both Bit 29 and Bit 28 are HIGH, the differential input voltage is above +FS. If both Bit 29 and Bit 28 are LOW, the differential input voltage is below –FS.

The function of these bits is summarized in Table 1.

Table 1. LTC2442 Status Bits

Input Range	Bit 31 $\overline{EOC}$	Bit 30 DMY	Bit 29 SIG	Bit 28 MSB
$V_{IN} \geq 0.5 \cdot V_{REF}$	0	0	1	1
$0V \leq V_{IN} < 0.5 \cdot V_{REF}$	0	0	1	0
$–0.5 \cdot V_{REF} \leq V_{IN} < 0V$	0	0	0	1
$V_{IN} < –0.5 \cdot V_{REF}$	0	0	0	0

Bits 28-5 are the 24-bit conversion result MSB first.

Bit 5 is the least significant bit (LSB).

Bits 4-0 are sub LSBs below the 24-bit level. Bits 4-0 may be included in averaging or discarded without loss of resolution.

Data is shifted out of the SDO pin under control of the serial clock (SCK), see Figure 3. Whenever $\overline{CS}$ is HIGH, SDO remains high impedance and SCK is ignored.

In order to shift the conversion result out of the device, $\overline{CS}$ must first be driven LOW. $\overline{EOC}$ is seen at the SDO pin of the device once $\overline{CS}$ is pulled LOW. $\overline{EOC}$ changes real time from HIGH to LOW at the completion of a conversion. This signal may be used as an interrupt for an external microcontroller. Bit 31 ($\overline{EOC}$) can be captured on the first rising edge of SCK. Bit 30 is shifted out of the device on

APPLICATIONS INFORMATION

the first falling edge of SCK. The final data bit (Bit 0) is shifted out on the falling edge of the 31st SCK and may be latched on the rising edge of the 32nd SCK pulse. On the falling edge of the 32nd SCK pulse, SDO goes HIGH indicating the initiation of a new conversion cycle. This bit serves as $\overline{EOC}$ (Bit 31) for the next conversion cycle. Table 2 summarizes the output data format.

As long as the voltage on the SEL^+ and SEL^- pins is maintained within the –0.3V to (V_{CC} + 0.3V) absolute maximum operating range, a conversion result is generated for any differential input voltage V_{IN} from –FS = –0.5 • V_{REF} to +FS = 0.5 • V_{REF}. For differential input voltages greater than +FS, the conversion result is clamped to the value corresponding to the +FS + 1LSB. For differential input voltages below –FS, the conversion result is clamped to the value corresponding to –FS – 1LSB.

Serial Interface Pins

The LTC2442 transmits the conversion result and receives the start of conversion command through a synchronous 3- or 4-wire interface. During the conversion and sleep states, this interface can be used to access the converter status and during the data output state it is used to read the conversion result and program the speed, resolution and input channel.

Serial Clock Input/Output (SCK)

The serial clock signal present on SCK (Pin 1) is used to synchronize the data transfer. Each bit of data is shifted out the SDO pin on the falling edge of the serial clock.

In the Internal SCK mode of operation, the SCK pin is an output and the LTC2442 creates its own serial clock. In the External SCK mode of operation, the SCK pin is used as input. The internal or external SCK mode is selected by tying $\overline{EXT}$ (Pin 3) LOW for external SCK and HIGH for internal SCK.

Serial Data Output (SDO)

The serial data output pin, SDO (Pin 36), provides the result of the last conversion as a serial bit stream (MSB first) during the data output state. In addition, the SDO pin is used as an end of conversion indicator during the conversion and sleep states.

When $\overline{CS}$ (Pin 35) is HIGH, the SDO driver is switched to a high impedance state. This allows sharing the serial interface with other devices. If $\overline{CS}$ is LOW during the convert or sleep state, SDO will output $\overline{EOC}$. If $\overline{CS}$ is LOW during the conversion phase, the $\overline{EOC}$ bit appears HIGH on the SDO pin. Once the conversion is complete, $\overline{EOC}$ goes LOW. The device remains in the sleep state until the first rising edge of SCK occurs while $\overline{CS}$ = LOW.

Table 2. LTC2442 Output Data Format

Differential Input Voltage V_{IN}*	Bit 31 $\overline{EOC}$	Bit 30 DMY	Bit 29 SIG	Bit 28 MSB	Bit 27	Bit 26	Bit 25	…	Bit 0
V_{IN}* ≥ 0.5 • V_{REF}**	0	0	1	1	0	0	0	...	0
0.5 • V_{REF}** –1LSB	0	0	1	0	1	1	1	...	1
0.25 • V_{REF}**	0	0	1	0	1	0	0	...	0
0.25 • V_{REF}** –1LSB	0	0	1	0	0	1	1	...	1
0	0	0	1	0	0	0	0	...	0
–1LSB	0	0	0	1	1	1	1	...	1
–0.25 • V_{REF}**	0	0	0	1	1	0	0	...	0
–0.25 • V_{REF}** –1LSB	0	0	0	1	0	1	1	...	1
–0.5 • V_{REF}**	0	0	0	1	0	0	0	...	0
V_{IN}* < –0.5 • V_{REF}**	0	0	0	0	1	1	1	...	1

*The differential input voltage V_{IN} = SEL^+ – SEL^-. **The differential reference voltage V_{REF} = REF^+ – REF^-.

APPLICATIONS INFORMATION

Table 3. Channel Selection

MUX ADDRESS					CHANNEL SELECTION				
SGL	ODD/SIGN	A2	A1	A0	CH0	CH1	CH2	CH3	COM
0	0	0	0	0	SEL^+	SEL^-			
0	0	0	0	1			SEL^+	SEL^-	
0	1	0	0	0	SEL^-	SEL^+			
0	1	0	0	1			SEL^-	SEL^+	
1	0	0	0	0	SEL^+				SEL^-
1	0	0	0	1			SEL^+		SEL^-
1	1	0	0	0		SEL^+			SEL^-
1	1	0	0	1				SEL^+	SEL^-

Table 4. Speed/Resolution Selection

OSR3	OSR2	OSR1	OSR0	TWOX	CONVERSION RATE		RMS NOISE	ENOB	OSR	LATENCY
					INTERNAL 9MHZ Clock	EXTERNAL 10.24MHz Clock				
0	0	0	0	0	Keep Previous Speed/Resolution					
0	0	0	1	0	3.52kHz	4kHz	23µV	17.7	64	none
0	0	1	0	0	1.76kHz	2kHz	36µV	20.4	128	none
0	0	1	1	0	879Hz	1kHz	2.1µV	21.2	256	none
0	1	0	0	0	439Hz	500Hz	1.5µV	21.6	512	none
0	1	0	1	0	220Hz	250Hz	1.2µV	22	1024	none
0	1	1	0	0	110Hz	125Hz	840nV	22.5	2048	none
0	1	1	1	0	55Hz	62.5Hz	630nV	22.9	4096	none
1	0	0	0	0	27.5Hz	31.25Hz	430nV	23.5	8192	none
1	0	0	1	0	13.73Hz	15.625Hz	305nV	24	16384	none
1	1	1	1	0	6.875Hz	7.8125Hz	220nV	24.4	32768	none
0	0	0	0	1	Keep Previous Speed/Resolution					
0	0	0	1	1	7.03kHz	8kHz	23µV	17.7	64	1 cycle
0	0	1	0	1	3.52kHz	4kHz	3.6µV	20.4	128	1 cycle
0	0	1	1	1	1.76kHz	2kHz	2.1µV	21.2	256	1 cycle
0	1	0	0	1	879Hz	1kHz	1.5µV	21.6	512	1 cycle
0	1	0	1	1	439Hz	500Hz	1.2µV	22	1024	1 cycle
0	1	1	0	1	220Hz	250Hz	840nV	22.5	2048	1 cycle
0	1	1	1	1	110Hz	125Hz	630nV	22.9	4096	1 cycle
1	0	0	0	1	55Hz	62.5Hz	430nV	23.5	8192	1 cycle
1	0	0	1	1	27.5Hz	31.25Hz	305nV	24	16384	1 cycle
1	1	1	1	1	13.73Hz	15.625Hz	220nV	24.4	32768	1 cycle

APPLICATIONS INFORMATION

Chip Select Input ($\overline{CS}$)

The active LOW chip select, $\overline{CS}$ (Pin 35), is used to test the conversion status and to enable the data output transfer as described in the previous sections.

In addition, the $\overline{CS}$ signal can be used to trigger a new conversion cycle before the entire serial data transfer has been completed. The LTC2442 will abort any serial data transfer in progress and start a new conversion cycle anytime a LOW-to-HIGH transition is detected at the $\overline{CS}$ pin after the converter has entered the data output state.

Serial Data Input (SDI)

The serial data input (SDI, Pin 33) is used to select the speed/resolution and input channel of the LTC2442. SDI is programmed by a serial input data stream under the control of SCK during the data output cycle, see Figure 3.

Initially, after powering up, the device performs a conversion with SEL^+ = CH0, SEL^- = CH1, OSR = 256 (output rate nominally 879Hz), and 1X speedup mode (no Latency). Once this first conversion is complete, the device enters the sleep state and is ready to output the conversion result and receive the serial data input stream programming the speed/resolution and input channel for the next conversion. At the conclusion of each conversion cycle, the device enters this state.

In order to change the speed/resolution or input channel, the first three bits shifted into the device are 101. This is compatible with the programming sequence of all LTC multichannel differential input $\Delta\Sigma$ ADCs. If the sequence is set to 000 or 100, the following input data is ignored (don't care) and the previously selected speed/resolution and channel remain valid for the next conversion. Combinations other than 101, 100, and 000 of the three control bits should be avoided.

If the first three bits shifted into the device are 101, then the following five bits select the input channel for the following conversion (see Tables 3 and 4). The next five bits select the speed/resolution and mode 1X (no Latency) 2X (double output rate with one conversion latency), see Table 4. If these five bits are set to all 0's, the previous speed remains selected for the next conversion. This is useful in applications requiring a fixed output rate/resolution but need to change the input channel.

When an update operation is initiated the first three bits are 101. The following five bits are the channel address. The first bit, SGL, determines if the input selection is differential (SGL = 0) or single-ended (SGL = 1). For SGL = 0, two adjacent channels can be selected to form a differential input. For SGL = 1, one of 4 channels is selected as the positive input. The negative input is COM for all single ended operations. The next 4-bits (ODD, A2, A1, A0) determine which channel is selected and its polarity, (see Table 3). In order to remain software compatible with LTCs other multi-channel $\Delta\Sigma$ ADCs, A2 and A1 are unused and should be set low.

Speed Multiplier Mode

In addition to selecting the speed/resolution, a speed multiplier mode is used to double the output rate while maintaining the selected resolution. The last bit of the 5-bit speed/resolution control word (TWOX, see Table 4) determines if the output rate is 1X (no speed increase) or 2X (double the selected speed).

While operating in the 1X mode, the device combines two internal conversions for each conversion result in order to remove the ADC offset. Every conversion cycle, the offset and offset drift are transparently calibrated greatly simplifying the user interface. The resulting conversion result has no latency. The first conversion following a newly

APPLICATIONS INFORMATION

selected speed/resolution and input channel is valid. This is identical to the operation of the LTC2440 and LTC2444 through LTC2449.

While operating in the 2X mode, the device performs a running average of the last two conversion results. This automatically removes the offset and drift of the device while increasing the output rate by 2X. The resolution (noise) remains the same. If a new channel is selected, the conversion result is valid for all conversions after the first conversion (one cycle latency). If a new speed/resolution is selected, the first conversion result is valid but the resolution (noise) is a function of the running average. All subsequent conversion results are valid. If the mode is changed from either 1X to 2X or 2X to 1X without changing the resolution or channel, the first conversion result is valid.

The 2X mode can also be used to increase the settling time of the amplifier between readings. While operating in the 2X mode, the multiplexer output (input to the buffer/amplifier) is switched at the end of each conversion cycle. Prior to concluding the data out/in cycle, the analog multiplexer output is switched. This occurs at the end of the conversion cycle (just prior to the data output cycle) for auto calibration. The time required to read the conversion enables more settling time for the amplifier. The offset/offset drift of the amplifier is automatically removed by the converter's auto calibration sequence for both the 1X and 2X speed modes.

While operating in the 1X mode, if a new input channel is selected the multiplexer is switched on the falling edge of the 14th SCK (once the complete data input word is programmed). The remaining data output sequence time can be used to allow the external amplifier to settle.

BUSY

The BUSY output (Pin 2) is used to monitor the state of conversion, data output and sleep cycle. While the part is converting, the BUSY pin is HIGH. Once the conversion is complete, BUSY goes LOW indicating the conversion is complete and data out is ready. The part now enters the sleep state. BUSY remains LOW while data is shifted out of the device and SDI is shifted into the device. It goes HIGH at the conclusion of the data input/output cycle indicating a new conversion has begun. This rising edge may be used to flag the completion of the data read cycle.

Serial Interface Timing Modes

The LTC2442's 3- or 4-wire interface is SPI and MICROWIRE compatible. This interface offers several flexible modes of operation. These include internal/external serial clock, 3- or 4-wire I/O, single cycle conversion and autostart. The following sections describe each of these serial interface timing modes in detail. In all these cases, the converter can use the internal oscillator (F_O = LOW) or an external oscillator connected to the F_O pin. Refer to Table 5 for a summary.

Table 5. Interface Timing Modes

Configuration	SCK Source	Conversion Cycle Control	Data Output Control	Connection and Waveforms
External SCK, Single Cycle Conversion	External	$\overline{CS}$ and SCK	$\overline{CS}$ and SCK	Figures 4, 5
External SCK, 2-Wire I/O	External	SCK	SCK	Figure 6
Internal SCK, Single Cycle Conversion	Internal	$\overline{CS}$ ↓	$\overline{CS}$ ↓	Figures 7, 8
Internal SCK, 2-Wire I/O, Continuous Conversion	Internal	Continuous	Internal	Figure 9

APPLICATIONS INFORMATION

External Serial Clock, Single Cycle Operation (SPI/MICROWIRE Compatible)

This timing mode uses an external serial clock to shift out the conversion result and a $\overline{CS}$ signal to monitor and control the state of the conversion cycle, see Figure 4.

The serial clock mode is selected by the $\overline{EXT}$ pin. To select the external serial clock mode, $\overline{EXT}$ must be tied low.

The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$ is HIGH. At any time during the conversion cycle, $\overline{CS}$ may be pulled LOW in order to monitor the state of the converter. While $\overline{CS}$ is pulled LOW, $\overline{EOC}$ is output to the SDO pin. $\overline{EOC}$ = 1 (BUSY = 1) while a conversion is in progress and $\overline{EOC}$ = 0 (BUSY = 0) if the device is in the sleep state. Independent of $\overline{CS}$, the device automatically enters the sleep state once the conversion is complete.

When the device is in the sleep state ($\overline{EOC}$ = 0), its conversion result is held in an internal static shift register. The device remains in the sleep state until the first rising edge of SCK is seen. Data is shifted out the SDO pin on each falling edge of SCK. This enables external circuitry to latch the output on the rising edge of SCK. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 32nd rising edge of SCK. On the 32nd falling edge of SCK, the device begins a new conversion. SDO goes HIGH ($\overline{EOC}$ = 1) and BUSY goes HIGH indicating a conversion is in progress.

At the conclusion of the data cycle, $\overline{CS}$ may remain LOW and $\overline{EOC}$ monitored as an end-of-conversion interrupt. Alternatively, $\overline{CS}$ may be driven HIGH setting SDO to Hi-Z and BUSY monitored for the completion of a conversion.

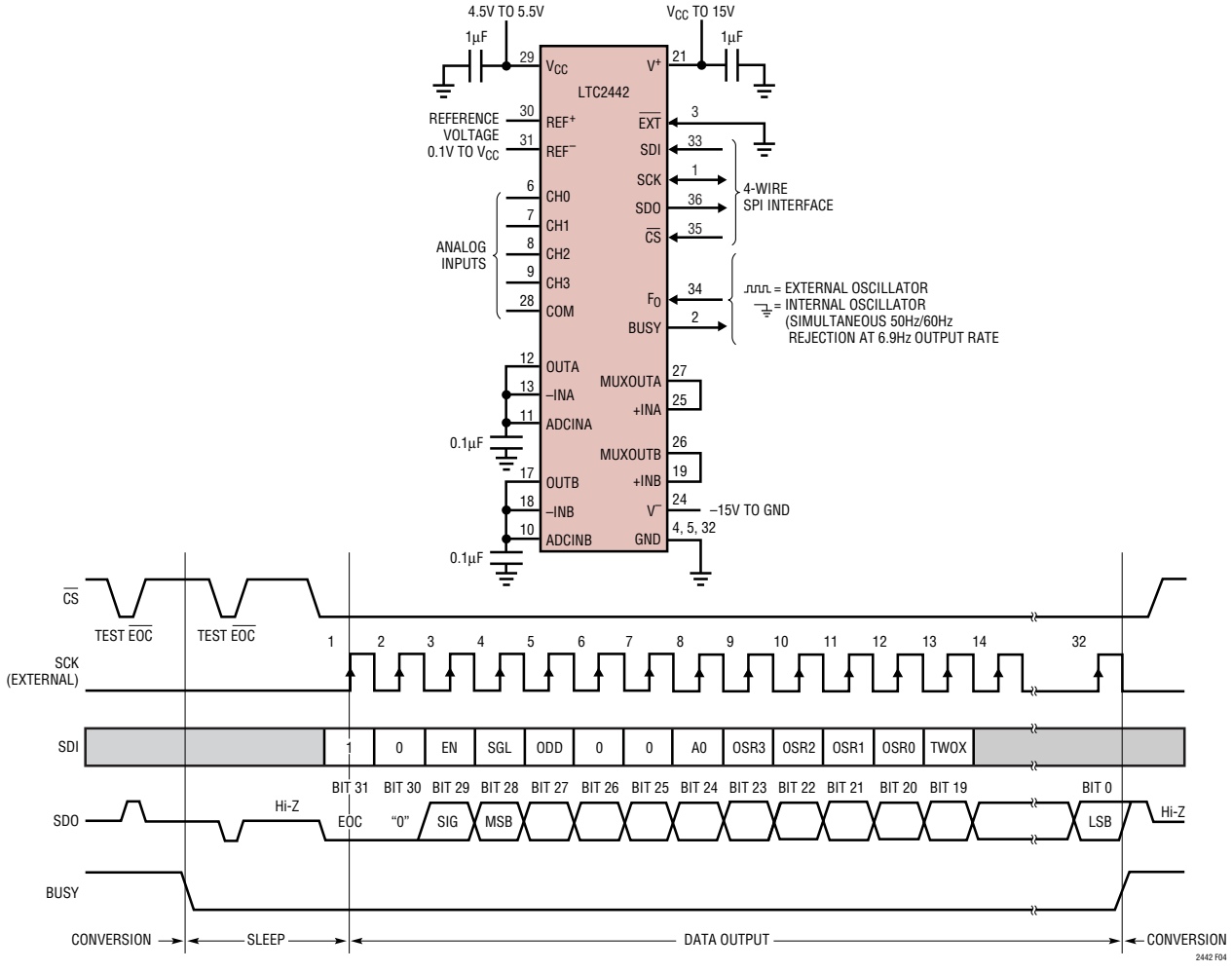


Figure 4. External Serial Clock, Single Cycle Operation

APPLICATIONS INFORMATION

As described above, $\overline{CS}$ may be pulled LOW at any time in order to monitor the conversion status on the SDO pin.

Typically, $\overline{CS}$ remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$ HIGH anytime between the fifth falling edge and the 32nd falling edge of SCK, see Figure 5. On the rising edge of $\overline{CS}$, the device aborts the data output state and immediately initiates a new conversion. Thirteen serial input data bits are required in order to properly program the speed/resolution and input channel. If the data output sequence is aborted prior to the 13th rising edge of SCK, the new input data is ignored, and the previously selected speed/resolution and channel are used for the next conversion cycle. This is useful for systems not requiring all 32 bits of output data, aborting an invalid conversion cycle or synchronizing the start of a conversion. If a new channel is being programmed, the rising edge of $\overline{CS}$ must come after the 14th falling edge of SCK in order to store the data input sequence.

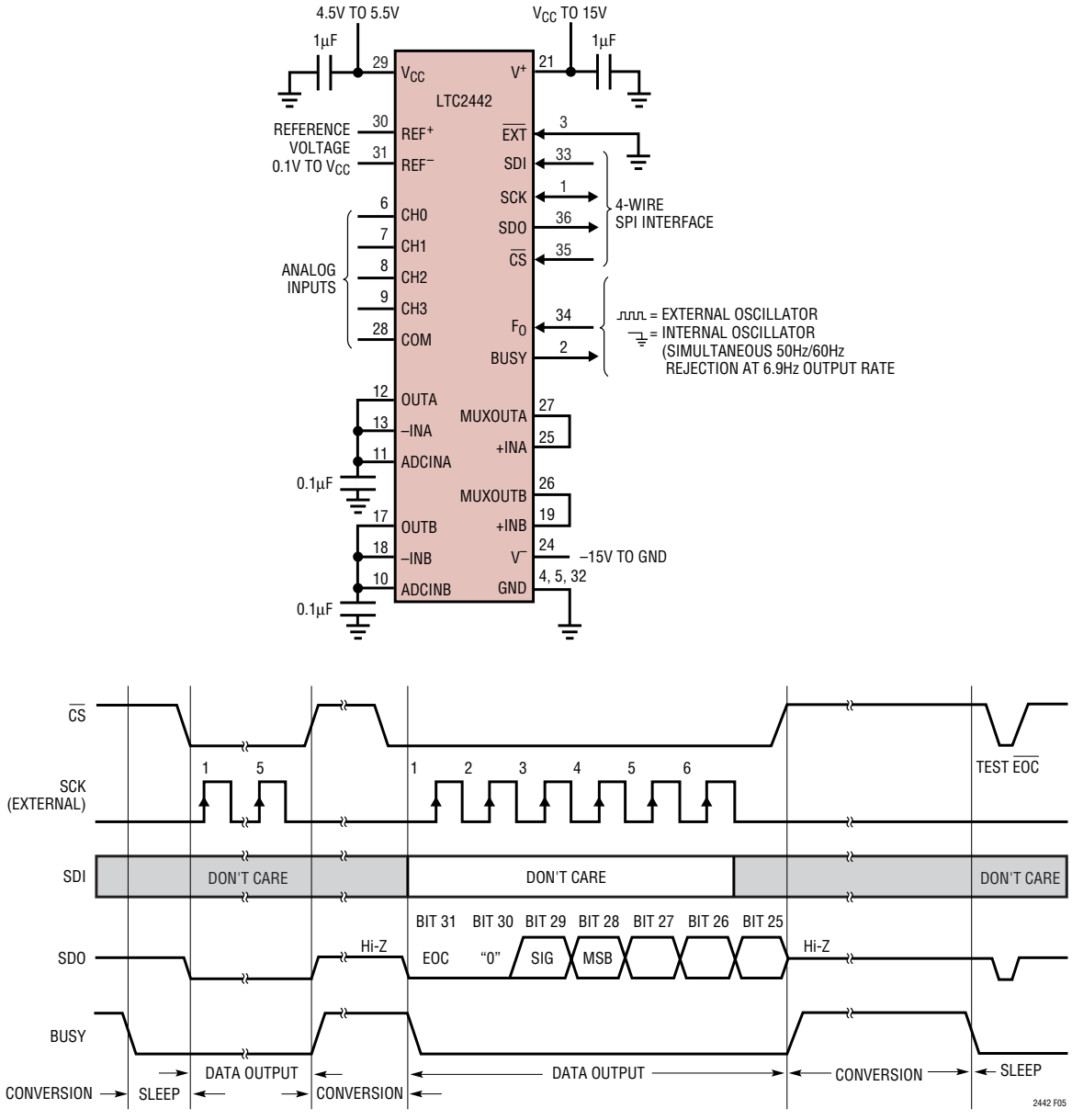


Figure 5. External Serial Clock, Reduced Output Data Length

APPLICATIONS INFORMATION

External Serial Clock, 2-Wire I/O

This timing mode utilizes a 2-wire serial I/O interface. The conversion result is shifted out of the device by an externally generated serial clock (SCK) signal, see Figure 6. $\overline{CS}$ may be permanently tied to ground, simplifying the user interface or isolation barrier. The external serial clock mode is selected by tying $\overline{EXT}$ LOW.

Since $\overline{CS}$ is tied LOW, the end-of-conversion ($\overline{EOC}$) can be continuously monitored at the SDO pin during the convert and sleep states. Conversely, BUSY (Pin 2) may be used to monitor the status of the conversion cycle. $\overline{EOC}$ or BUSY may be used as an interrupt to an external controller indicating the conversion result is ready. $\overline{EOC}$ = 1 (BUSY = 1) while the conversion is in progress and $\overline{EOC}$ = 0 (BUSY = 0) once the conversion enters the sleep state. On the falling edge of $\overline{EOC}$/BUSY, the conversion result is loaded into an internal static shift register. The device remains in the sleep state until the first rising edge of SCK. Data is shifted out the SDO pin on each falling edge of SCK enabling external circuitry to latch data on the rising edge of SCK. $\overline{EOC}$ can be latched on the first rising edge of SCK. On the 32nd falling edge of SCK, SDO and BUSY go HIGH ($\overline{EOC}$ = 1) indicating a new conversion has begun.

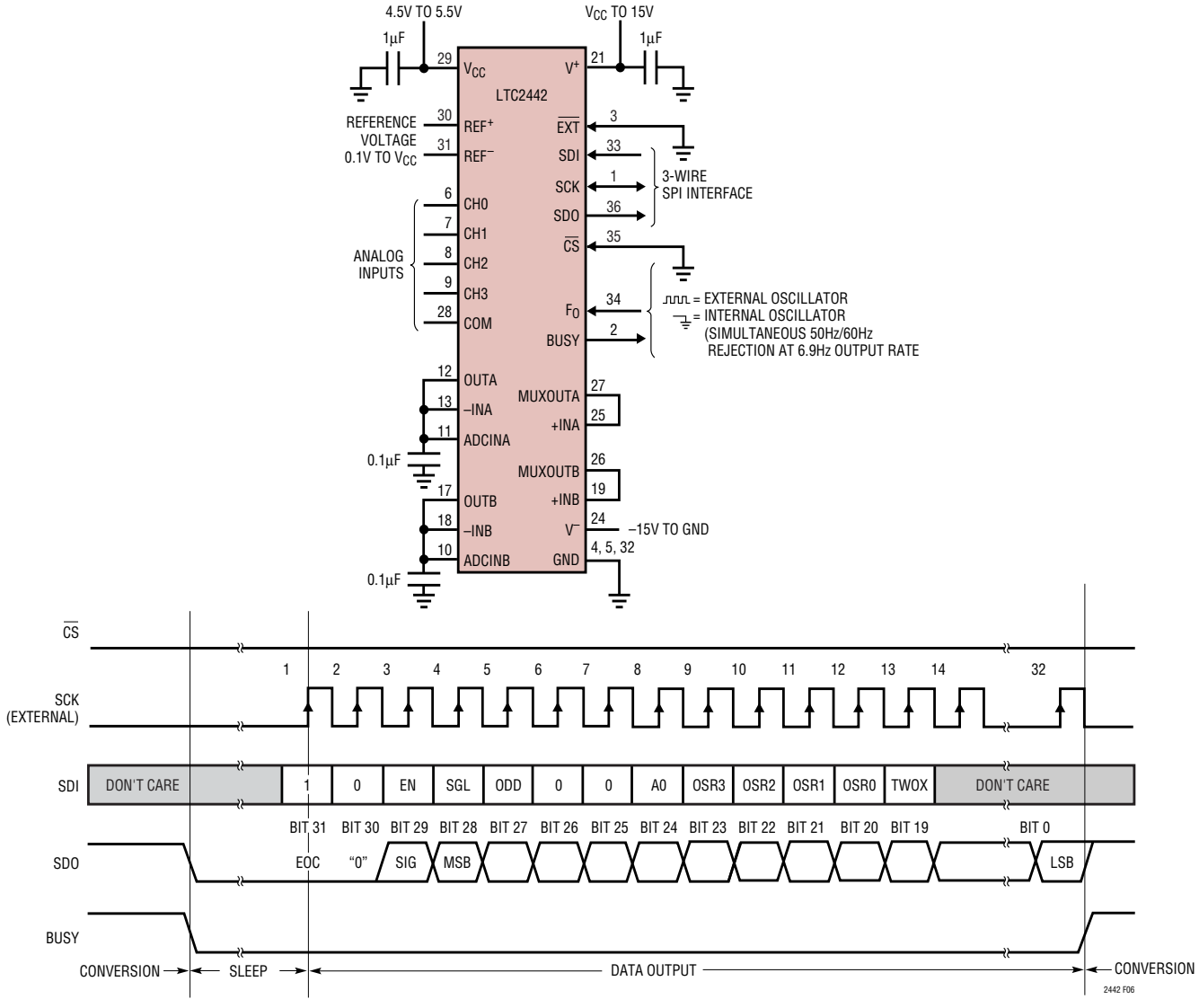


Figure 6. External Serial Clock, CS = 0 Operation (2-Wire)

APPLICATIONS INFORMATION

Internal Serial Clock, Single Cycle Operation

This timing mode uses an internal serial clock to shift out the conversion result and a $\overline{CS}$ signal to monitor and control the state of the conversion cycle, see Figure 7.

In order to select the internal serial clock timing mode, the $\overline{EXT}$ pin must be tied HIGH.

The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$ is HIGH. At any time during the conversion cycle, $\overline{CS}$ may be pulled LOW in order to monitor the state of the converter. Once $\overline{CS}$ is pulled LOW, SCK goes LOW and $\overline{EOC}$ is output to the SDO pin. EOC = 1 while a conversion is in progress and $\overline{EOC}$ = 0 if the device is in the sleep state. Alternatively, BUSY (Pin 2) may be used to monitor the status of the conversion in progress. BUSY is HIGH during the conversion and goes LOW at the conclusion. It remains LOW until the result is read from the device.

When testing $\overline{EOC}$, if the conversion is complete ($\overline{EOC}$ = 0), the device will exit the sleep state and enter the data output state if $\overline{CS}$ remains LOW. In order to prevent the device from exiting the sleep state, $\overline{CS}$ must be pulled HIGH before the first rising edge of SCK. In the internal SCK timing mode, SCK goes HIGH and the device begins outputting data at time $t_{EOCtest}$ after the falling edge of $\overline{CS}$ (if $\overline{EOC}$ = 0) or $t_{EOCtest}$ after $\overline{EOC}$ goes LOW (if $\overline{CS}$ is LOW during the falling edge of $\overline{EOC}$). The value of $t_{EOCtest}$ is 500ns. If $\overline{CS}$ is pulled HIGH before time $t_{EOCtest}$, the device remains in the sleep state. The conversion result is held in the internal static shift register.

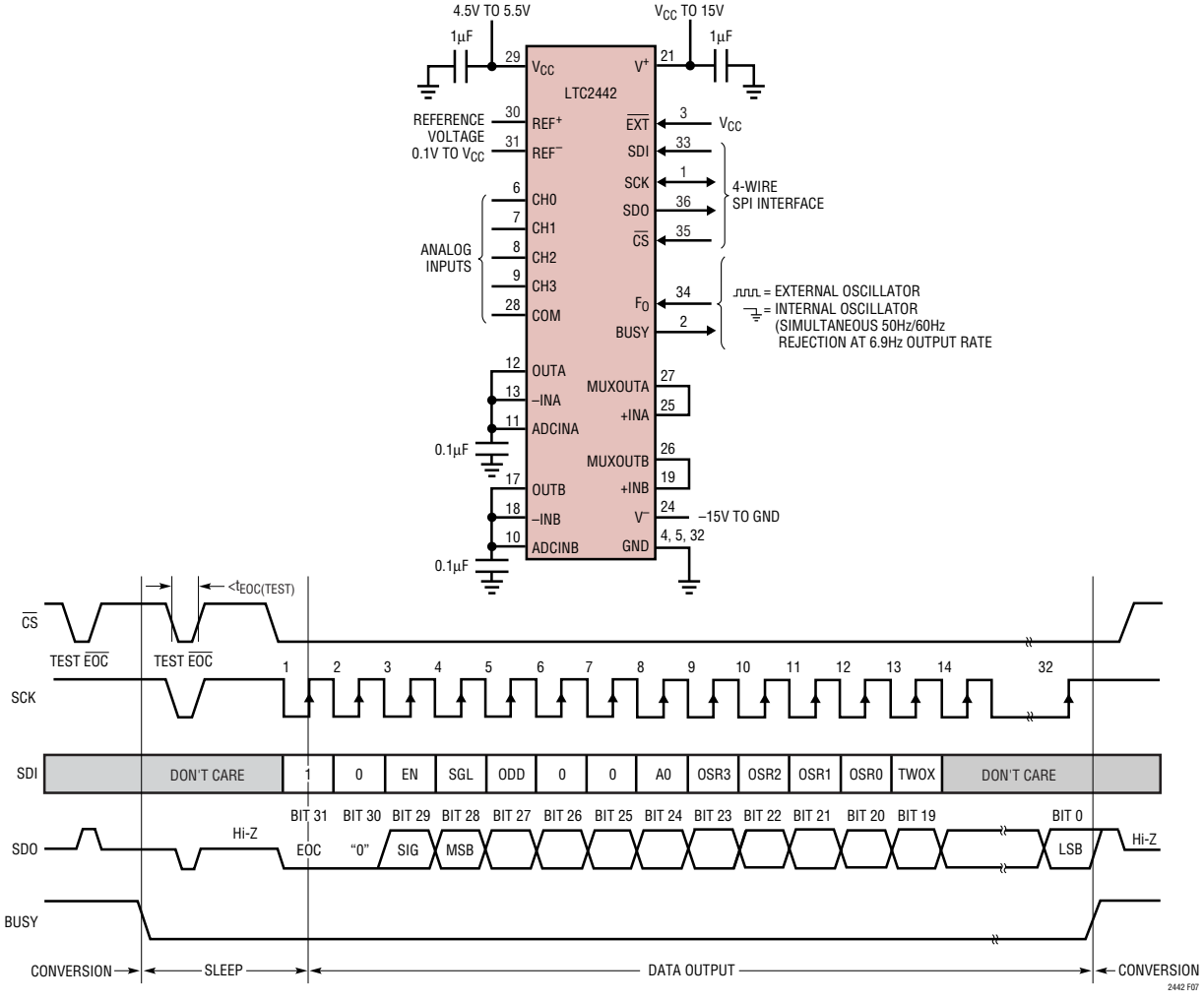


Figure 7. Internal Serial Clock, Single Cycle Operation

APPLICATIONS INFORMATION

If $\overline{CS}$ remains LOW longer than $t_{EOCtest}$, the first rising edge of SCK will occur and the conversion result is serially shifted out of the SDO pin. The data output cycle begins on this first rising edge of SCK and concludes after the 32nd rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result on the 32nd rising edge of SCK. After the 32nd rising edge, SDO goes HIGH ($\overline{EOC}$ = 1), SCK stays HIGH and a new conversion starts.

Typically, $\overline{CS}$ remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$ HIGH anytime between the first and 32nd rising edge of SCK, see Figure 8. On the rising edge of $\overline{CS}$, the device aborts the data output state and immediately initiates a new conversion. This is useful for systems not requiring all 32 bits of output data, aborting an invalid conversion cycle, or synchronizing the start of a conversion. Thirteen serial input data bits are required in order to properly program the speed/resolution and input channel. If the data output sequence is aborted prior to the 13th rising edge of SCK, the new input data is ignored, and the previously selected speed/resolution and channel are used for the next conversion cycle. If a new channel is being programmed, the rising edge of $\overline{CS}$ must come after the 14th falling edge of SCK in order to store the data input sequence.

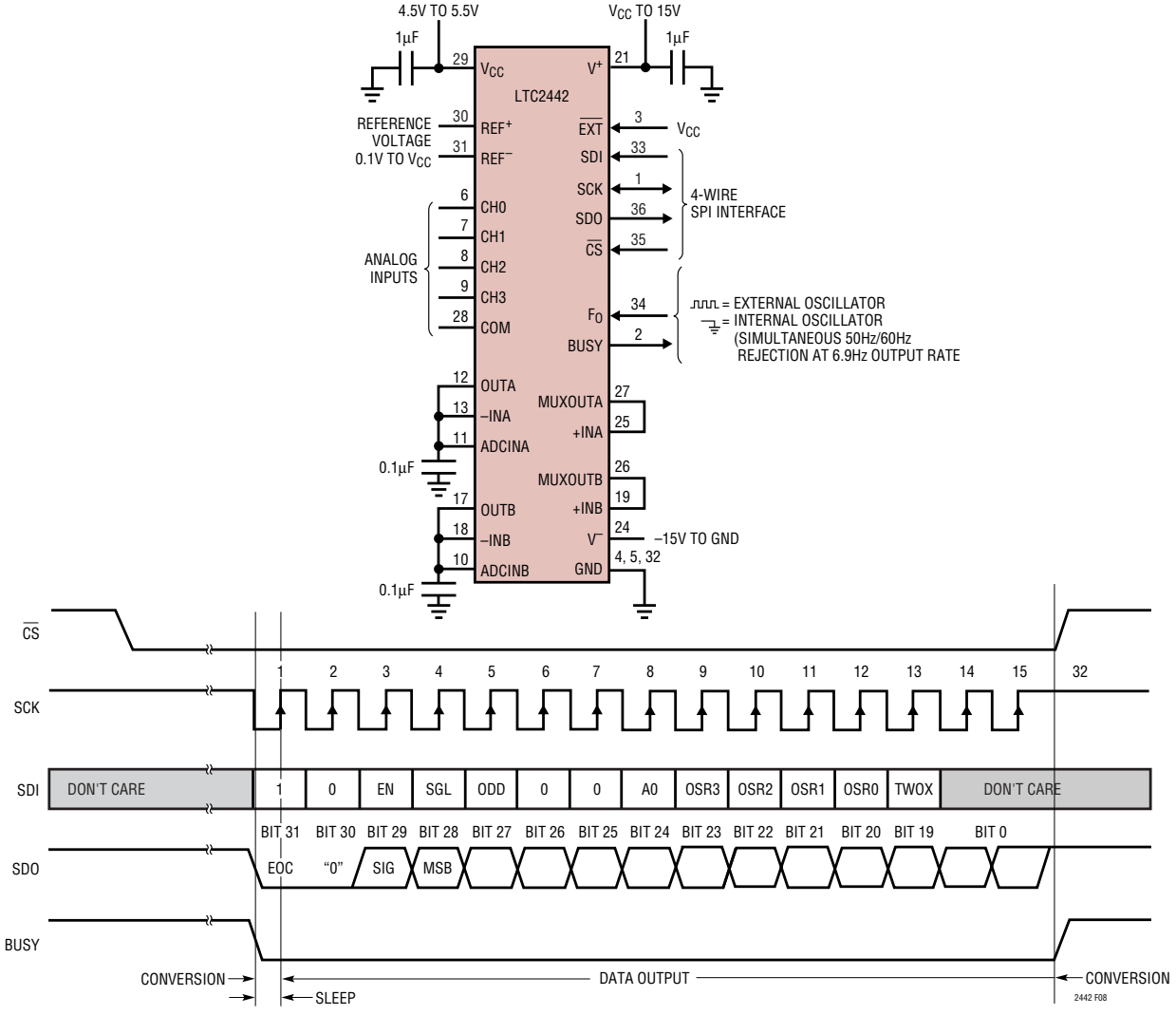


Figure 8. Internal Serial Clock, Reduced Data Output Length

APPLICATIONS INFORMATION

Internal Serial Clock, 3-Wire I/O, Continuous Conversion

This timing mode uses a 3-wire, all output (SCK and SDO) interface. The conversion result is shifted out of the device by an internally generated serial clock (SCK) signal, see Figure 9. $\overline{CS}$ may be permanently tied to ground, simplifying the user interface or isolation barrier. The internal serial clock mode is selected by tying $\overline{EXT}$ HIGH.

During the conversion, the SCK and the serial data output pin (SDO) are HIGH ($\overline{EOC}$ = 1) and BUSY = 1. Once the conversion is complete, SCK, BUSY and SDO go LOW ($\overline{EOC}$ = 0) indicating the conversion has finished and the device has entered the sleep state. The part remains in the sleep state a minimum amount of time (≈500ns) then immediately begins outputting data. The data output cycle begins on the first rising edge of SCK and ends after the 32nd rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 32nd rising edge of SCK. After the 32nd rising edge, SDO goes HIGH ($\overline{EOC}$ = 1) indicating a new conversion is in progress. SCK remains HIGH during the conversion.

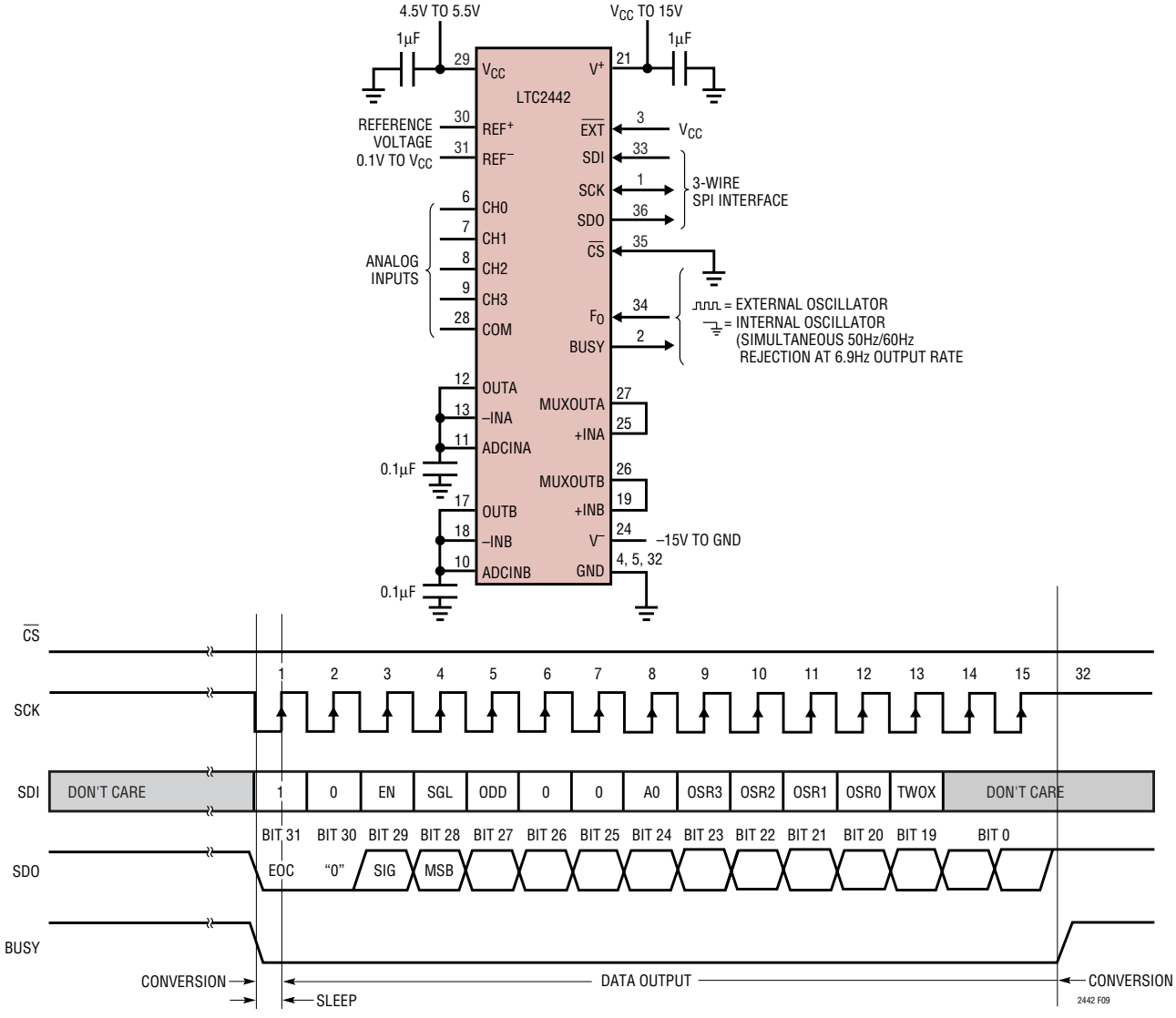


Figure 9. Internal Serial Clock, Continuous Operation

APPLICATIONS INFORMATION

Normal Mode Rejection and Antialiasing

One of the advantages delta-sigma ADCs offer over conventional ADCs is on-chip digital filtering. Combined with a large oversampling ratio, the LTC2442 significantly simplifies antialiasing filter requirements.

The LTC2442's speed/resolution is determined by the oversample ratio (OSR) of the on-chip digital filter. The OSR ranges from 64 for 3.5kHz output rate to 32,768 for 6.9Hz (in No Latency mode) output rate. The value of OSR and the sample rate f_S determine the filter characteristics of the device. The first NULL of the digital filter is at f_N and multiples of f_N where $f_N = f_S/OSR$, see Figure 10 and Table 6. The rejection at the frequency f_N ±14% is better than 80dB, see Figure 11.

Table 6. OSR vs Notch Frequency (f_N) (with Internal Oscillator Running at 9MHz)

OSR	NOTCH (f_N)
64	28.13kHz
128	14.06kHz
256	7.03kHz
512	3.52kHz
1024	1.76kHz
2048	879Hz
4096	439Hz
8192	220Hz
16384	110Hz
32768*	55Hz

* Simultaneous 50/60Hz rejection

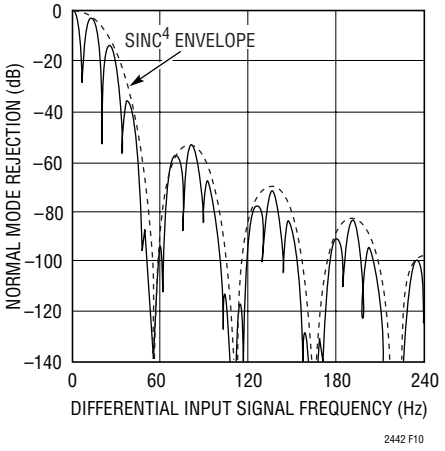


Figure 10. Normal Mode Rejection (Internal Oscillator)

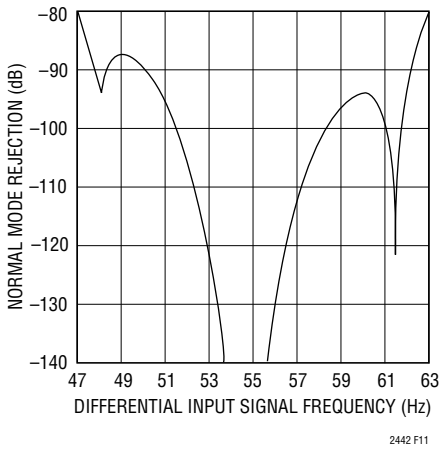


Figure 11. Normal Mode Rejection (Internal Oscillator)

APPLICATIONS INFORMATION

If F_O is grounded, f_S is set by the on-chip oscillator at 1.8MHz ±5% (over supply and temperature variations). At an OSR of 32,768, the first NULL is at f_N = 55Hz and the no latency output rate is $f_N/8$ = 6.9Hz. At the maximum OSR, the noise performance of the device is 220nV$_{RMS}$ with better than 80dB rejection of 50Hz ±2% and 60Hz ±2%. Since the OSR is large (32,768) the wide band rejection is extremely large and the antialiasing requirements are simple. The first multiple of f_S occurs at 55Hz • 32,768 = 1.8MHz, see Figure 12.

The first NULL becomes f_N = 7.03kHz with an OSR of 256 (an output rate of 879Hz) and F_O grounded. While the NULL has shifted, the sample rate remains constant. As a result of constant modulator sampling rate, the linearity, offset and full-scale performance remains unchanged as does the first multiple of f_S.

The sample rate f_S and NULL f_N, may also be adjusted by driving the F_O pin with an external oscillator. The sample rate is $f_S = f_{EOSC}/5$, where f_{EOSC} is the frequency of the clock applied to F_O. Combining a large OSR with a reduced sample rate leads to notch frequencies f_N near DC while maintaining simple antialiasing requirements. A 100kHz clock applied to F_O results in a NULL at 0.6Hz plus all harmonics up to 20kHz, see Figure 13. This is useful in applications requiring digitalization of the DC component of a noisy input signal and eliminates the need of placing a 0.6Hz filter in front of the ADC.

An external oscillator operating from 100kHz to 20MHz can be implemented using the LTC1799 (resistor set SOT-23 oscillator), see Figure 14. By floating pin 4 (DIV) of the LTC1799, the output oscillator frequency is:

$$f_{OSC} = 10MHz \bullet \left(\frac{10k}{10 \bullet R_{SET}} \right)$$

The normal mode rejection characteristic shown in Figure 13 is achieved by applying the output of the LTC1799 (with R_{SET} = 100k) to the F_O pin on the LTC2442 with OSR = 32,768.

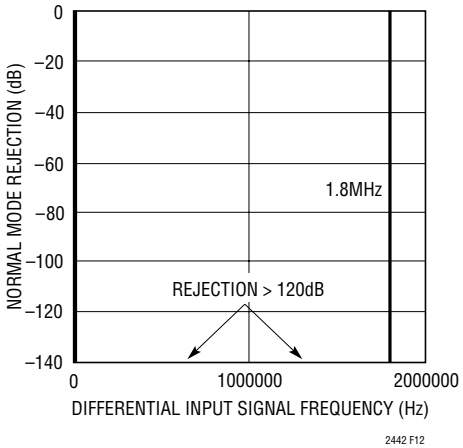


Figure 12. Normal Mode Rejection (Internal Oscillator)

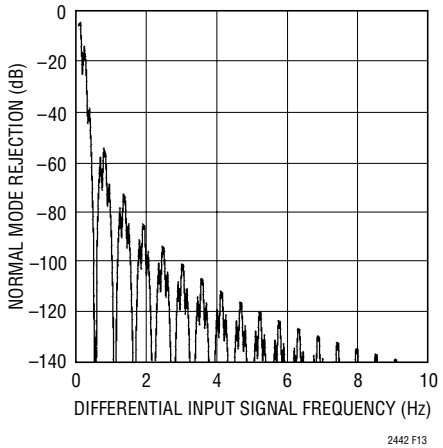


Figure 13. Normal Mode Rejection (Internal Oscillator at 90kHz)

APPLICATIONS INFORMATION

Input Bandwidth and Frequency Rejection

The combined effect of the internal SINC^4 digital filter and the digital and analog autocalibration circuits determines the LTC2442 input bandwidth and rejection characteristics. The digital filter's response can be adjusted by setting the oversample ratio (OSR) through the SPI interface or by supplying an external conversion clock to the f_O pin.

Table 7 lists the properties of the LTC2442 with various combinations of oversample ratio and clock frequency. Understanding these properties is the key to fine tuning the characteristics of the LTC2442 to the application.

Maximum Conversion Rate

The maximum conversion rate is the fastest possible rate at which conversions can be performed.

First Notch Frequency

This is the first notch in the SINC^4 portion of the digital filter and depends on the fo clock frequency and the oversample ratio. Rejection at this frequency and its multiples (up to the modulator sample rate of 1.8MHz) exceeds 120dB. This is 8 times the maximum conversion rate.

Effective Noise Bandwidth

The LTC2442 has extremely good input noise rejection from the first notch frequency all the way out to the modulator sample rate (typically 1.8MHz). Effective noise bandwidth is a measure of how the ADC will reject wideband input noise up to the modulator sample rate

Table 7

Over-sample Ratio (OSR)	*RMS Noise	ENOB (V_{REF} = 5V)	Maximum Conversion Rate		First Notch Frequency		Effective Noise BW		–3dB point (Hz)	
			Internal 9MHz clock	External f_0	Internal 9MHz clock	External f_0	Internal 9MHz clock	External f_0	Internal 9MHz clock	External f_0
64	23µV	17.7	3515.6	f_0/2560	28125	f_0/320	3148	f_0/5710	1696	f_0/5310
128	3.6µV	20.4	1757.8	f_0/5120	14062.5	f_0/640	1574	f_0/2860	848	f_0/10600
256	2.1µV	21.2	878.9	f_0/10240	7031.3	f_0/1280	787	f_0/1140	424	f_0/21200
512	1.5µV	21.6	439.5	f_0/20480	3515.6	f_0/2560	394	f_0/2280	212	f_0/42500
1024	1.2µV	22	219.7	f_0/40960	1757.8	f_0/5120	197	f_0/4570	106	f_0/84900
2048	840nV	22.5	109.9	f_0/81920	878.9	f_0/1020	98.4	f_0/9140	53	f_0/170000
4096	630nV	22.4	54.9	f_0/163840	439.5	f_0/2050	49.2	f_0/18300	26.5	f_0/340000
8192	430nV	23.5	27.5	f_0/327680	219.7	f_0/4100	24.6	f_0/36600	13.2	f_0/679000
16384	305nV	24	13.7	f_0/655360	109.9	f_0/8190	12.4	f_0/73100	6.6	f_0/1358000
32768	220nV	24.4	6.9	f_0/1310720	54.9	f_0/16380	6.2	f_0/146300	3.3	f_0/2717000

*ADC noise increases by approximately $\sqrt{2}$ when OSR is decreased by a factor of 2 for OSR 32768 to OSR 256. The ADC noise at OSR 64 include effects from internal modulator quantization noise.

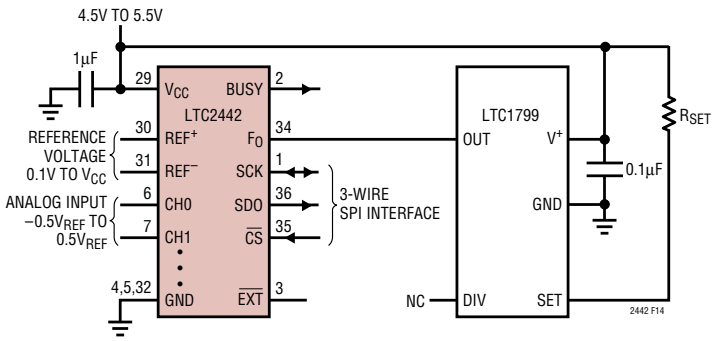


Figure 14. Simple External Clock Source

APPLICATIONS INFORMATION

Optimizing Linearity

While the integrated op-amp has rail-to-rail input range, in order to achieve parts-per-million linearity performance, the input range and op-amp supply voltages must be considered. Input levels within 1.25V of the upper op-amp rail (V^+) begin to degrade the performance. For example (see Figure 15) while operating with $V^+ = 5.1V$ and absolute input voltages ($V_{IN}CM + V_{IN}DIFF$) up to 3.75V ($V_{IN}CM = 2.5V$ and $-2.5V < V_{IN}DIFF < 2.5V$), the linearity is degraded to about 17-bits. Once V^+ is increased to 5.25V or greater the linearity improves to 19-Bits (2ppm). If the reference is reduced to 4.096V and the input common mode is $V_{REF}/2$ (2.048V) the linearity performance improves to better than 1ppm with V^+ tied to V_{CC} and V^- tied to ground, see Figure 16. Input signals near ground require about 100mV headroom on the op-amp power supply in order to achieve 1ppm INL, see Figure 17. Optimal linearity is achieved by driving the input differentially. As seen in Figure 18, a single ended input (the negative input is tied to ground) yields 18-bits (±4ppm) linearity performance. In this case V^- is 100mV below ground.

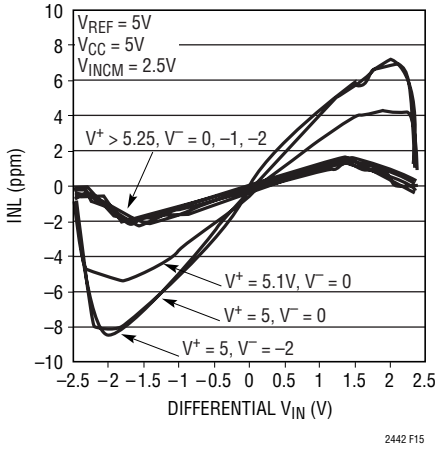


Figure 15. INL vs Op-Amp Supply Voltage

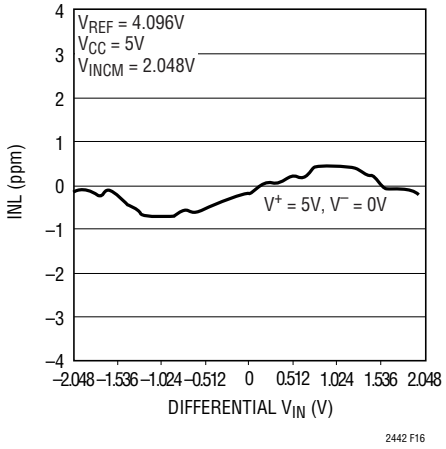


Figure 16. Linearity vs V_{IN}

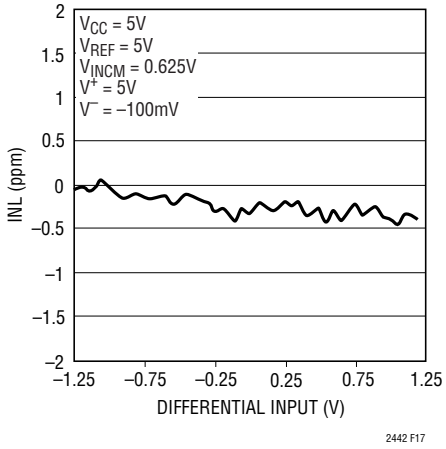


Figure 17. Linearity Near Ground

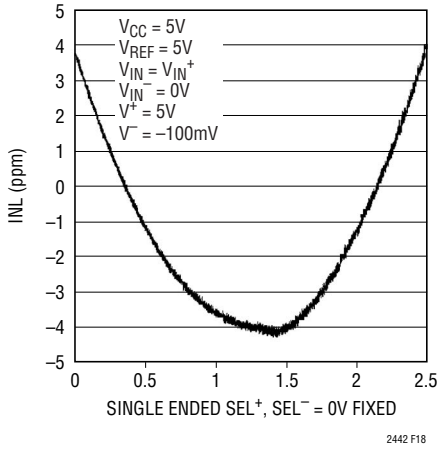


Figure 18. Single-Ended Linearity

APPLICATIONS INFORMATION

The LTC2442 breaks new ground in high impedance input ΔΣ ADCs. The input buffer is optimized to make driving the ADC as easy as possible, while overcoming many of the limitations typical of integrated buffers.

Convenient +5V to –5V/+9V DC-DC Converter

If either of the signal inputs must include ground and V_{CC}, then the amplifier will require both a positive supply greater than the maximum input voltage and a negative supply. Figure 19 shows how to derive both –5V and +9V from a single 5V supply using an LTC1983, allowing the ADC inputs to extend as much as 300mV below ground and above V_{CC}. For inputs that include ground but do not go within 1.5V of V_{CC}, then C4, C5, C6 and D1 can be eliminated and the amplifier positive supply can be connected to V_{CC}.

Input Bias Current

The 10nA typical bias current of the buffers results in less than 1ppm (5μV) error for source resistance imbalances of less than 500Ω. Matching the resistance at the inputs cancels much of the error due to amplifier bias current. For source resistances up to 50k, 1% resistors are adequate. Figure 20 shows proper input resistance matching for a precision voltage divider on the CH2-3 inputs. The resistance seen by CH2 is the parallel combination of 30k and 10k or 7.5k. A 1%, 7.5k resistor at CH3 balances the resistance of the divider output.

While the two input buffers will have slightly different bias currents, the autozero process applies the bias current from each buffer to both of the inputs for half of the conversion time, so the offset is equal to the average of the two bias currents multiplied by the mismatch in source resistance.

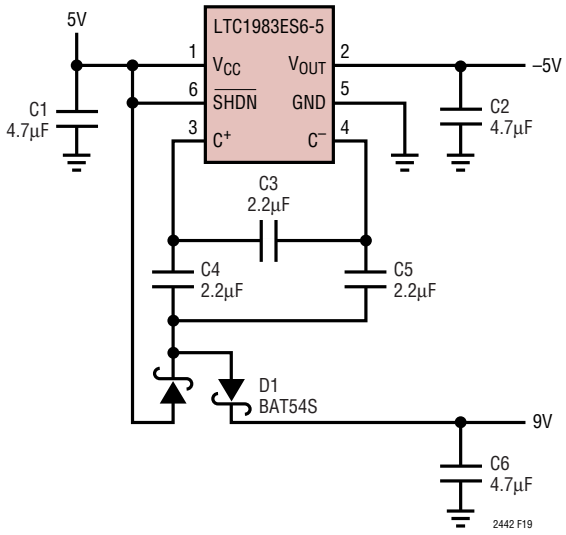


Figure 19. LTC1983 with Another Charge Pump Stacked onto V_{CC} to Give 9V

APPLICATIONS INFORMATION

Low Power Operation

The integrated buffers have a supply current of 1mA total, greatly reducing the total power consumption when the ADC is operated at a low duty cycle. The typical approach to driving a ΔΣ ADC is to use a high bandwidth amplifier that settles very quickly in response to the sampling process at the ADC input. The LTC2442 approach is to use an accurate, low bandwidth amplifier that requires a load capacitor for compensation. This capacitor also serves as a charge reservoir during the sampling process, so the disturbance at the ADC input is minimal. The amplifier only supplies the average sampling current that the ADC draws, which is on the order of 50µA.

Scaling for Higher Input Voltages

The LTC2442 is ideally suited for applications with low-level, differential signal with a common mode approximately equal to mid-supply, such as strain gages and silicon micromachined sensors. Other applications require scaling a high voltage signal to the range of the ADC.

Figure 20 shows how to properly scale a bipolar, ground-referred input voltage to drive the LTC2442. First, the input must be level shifted so that it never exceeds the LTC2442 supply rails. This is commonly done with an instrumentation amplifier or simple op-amp level shift circuit. Rather than shift the analog input, the LTC2442 can run on ±2.5V supplies so that ground is centered in the input range. This is equivalent to a perfect analog level shift with no degradation in accuracy. The digital signals are shifted from 0 to 5V logic to ±2.5V logic by a very inexpensive 74HC4053 analog switch and the data from the LTC2442 is shifted back to 0 to 5V logic by a MMBT3904 transistor.

On both inputs, precision resistor networks scale the input signal from ±10V to ±2.5V. CH0-1 is driven truly differentially for maximum linearity, typically better than 3ppm, however 3 resistors and an LTC2050HV autozero amplifier are required. The 8.88kΩ output resistor balances the offset associated with the LTC2442's bias current. The resistance seen by CH0 is 4.44k and the offset at CH0 is also inverted and appears at the output of the LTC2050HV.

CH2 to CH3 is driven single-ended, with CH3 tied to ground. This degrades linearity slightly, but it is easier to implement than a true differential drive. In this case the resistance at CH3 should be equal to the resistance at CH2 or 7.5k. This circuit is also suitable for signals that are always positive, with the LTC2442 operating on a single 5V supply.

APPLICATIONS INFORMATION

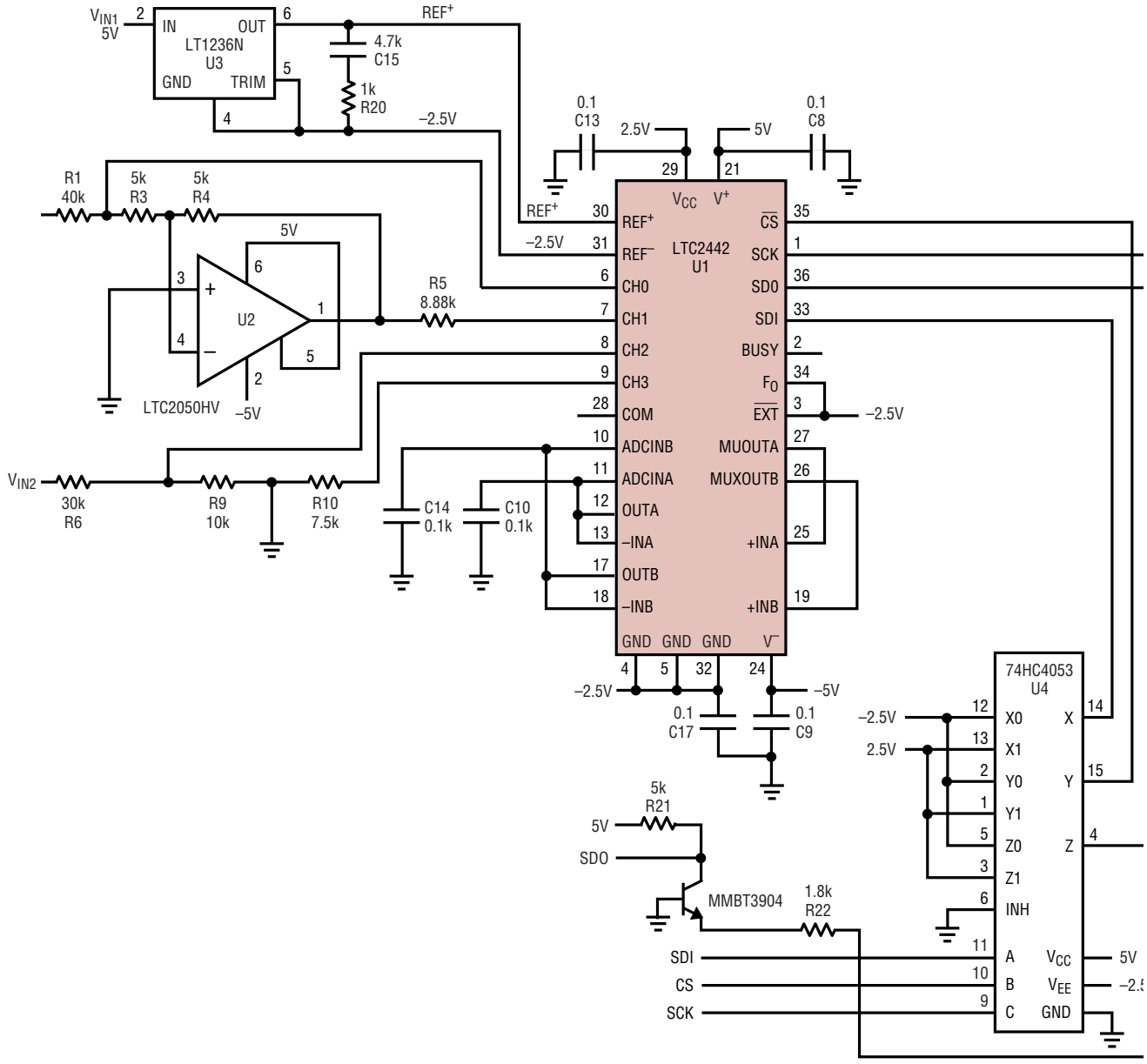


Figure 20. Scaling Inputs for ±10V Range

APPLICATIONS INFORMATION

Details of the Conversion and Autozero Process

The LTC2442 performs automatic offset cancellation for each conversion. This is accomplished by taking the average of two "half-conversions" with the inputs applied in opposite polarity. Figure 21 shows a conversion on CH0 to CH1 differential at OSR of 32768, in 1x mode. This channel is selected by sending the appropriate configuration word to the LTC2442 through the SPI interface. On the 13th falling clock edge, the CH0 input is applied to +INA through the multiplexer and CH1 is connected to +INB. The outputs of the amplifiers slew during the remainder of the data I/O state and the conversion begins on the 32nd falling clock edge. Halfway through the conversion (approximately 73ms later) the multiplexer switches the CH0 input to +INB and the CH1 input to +INA. The digital filter subtracts the two half-conversions, which removes the offset of the amplifiers and converter.

At the end of a conversion, the multiplexer assumes that the next conversion will be on the same channel and switches back to the opposite polarity on the channel just converted. This gives extra settling time when converting on one channel continuously. If a different channel is programmed, the multiplexer will switch again on the 13th falling clock edge.

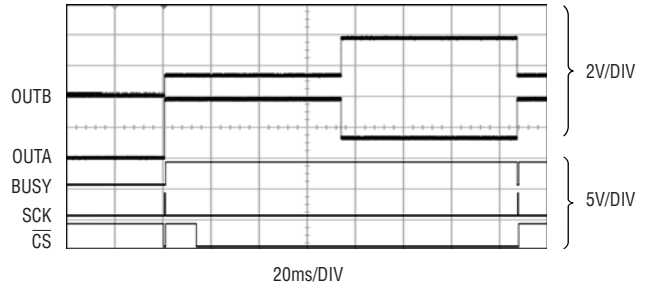


Figure 21. Amplifier Outputs and $\overline{CS}$, SCK, BUSY During a Conversion on CH0-1, OSR32768. V_{INDIFF} = 2.5V, V_{CM} = 2.5V

APPLICATIONS INFORMATION

The amplifiers take approximately 50µs to settle for a full-scale input voltage. This does not affect accuracy in either 2x mode or 1x mode for OSR values between 256 to 32768. However, the amplifier settling time will cause a gain error in 1x mode for OSR values between 64 to 256. This is because the mid-conversion slew time is a significant portion of the total conversion time. Figure 22 shows the details of a conversion in 1x mode, OSR128, with a full-scale input voltage applied (V_{IN} = 2.5V, V_{CM} = 2.5V). The previously selected channel had both inputs grounded. On the 13th falling clock edge, the amplifiers begin slewing and have reached the correct voltage before the conversion begins. Midway through the conversion, the multiplexer reverses the inputs. Figure 23 shows operation in 2x mode. After the first half-conversion is done, the multiplexer reverses. Waiting 50µs before beginning the next half-conversion allows the amplifiers to settle fully. 2x mode is recommended for OSR values between 64 and 128 because the amplifiers have time to settle between half conversions. If only the 1x data rate is required, ignore every other sample.

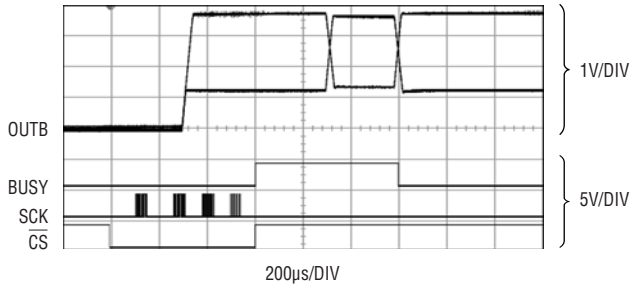


Figure 22. Details of Conversion in 1x Mode, OSR128 (OUTA and OUTB Superimposed)

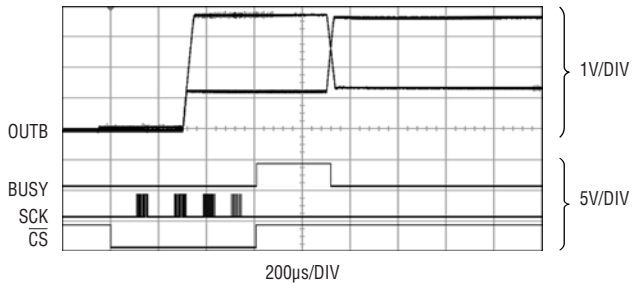
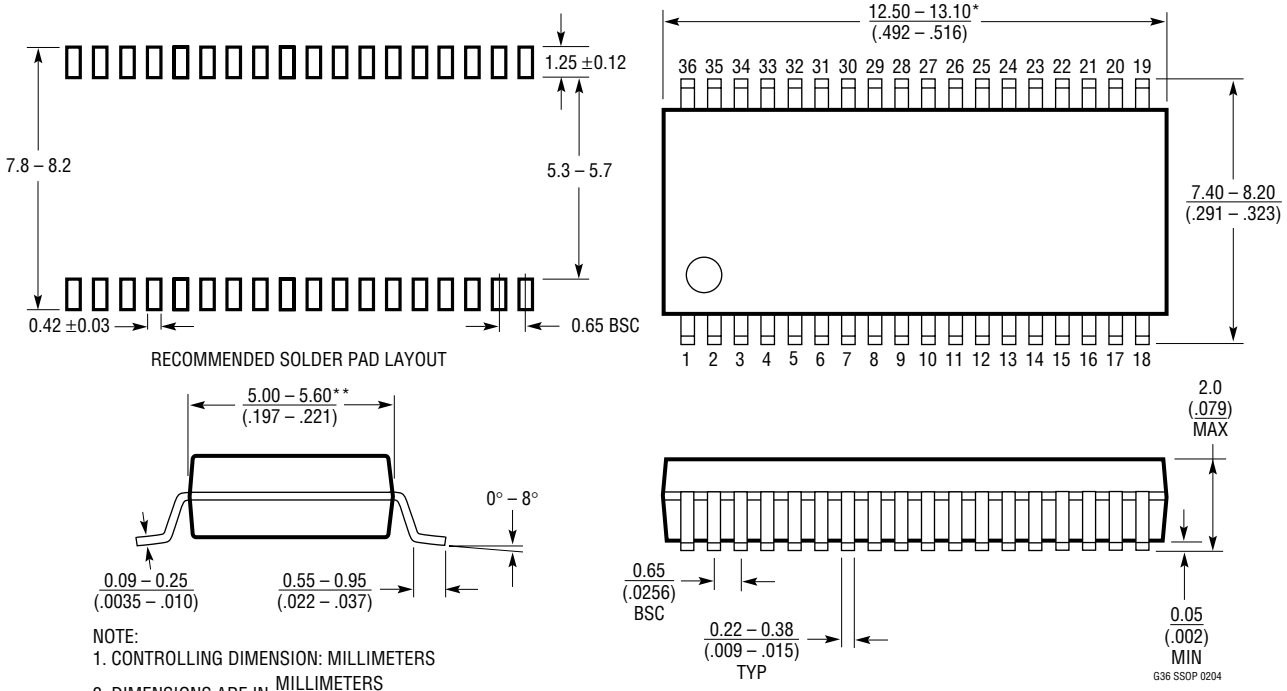


Figure 23. Details of Conversion in 2x Mode, OSR128 (OUTA and OUTB Superimposed)

PACKAGE DESCRIPTION

G Package
36-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



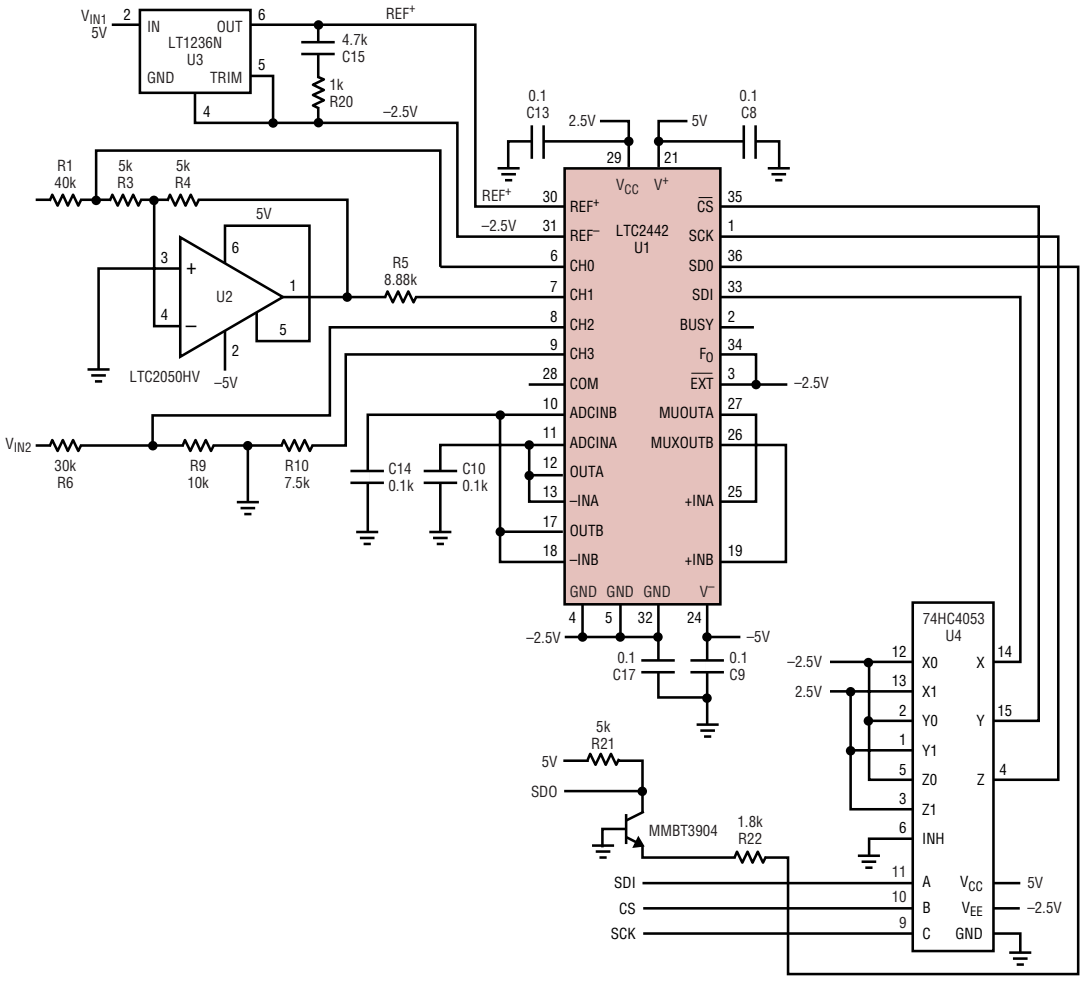
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

TYPICAL APPLICATION

Scaling Inputs for ±10V Range



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1025	Micropower Thermocouple Cold Junction Compensator	80µA Supply Current, 0.5°C Initial Accuracy
LTC1043	Dual Precision Instrumentation Switched Capacitor Building Block	Precise Charge, Balanced Switching, Low Power
LTC2050	Precision Chopper Stabilized Op Amp	No External Components 3µV Offset, 1.5µV_{P-P} Noise
LT1236A-5	Precision Bandgap Reference, 5V	0.05% Max, 5ppm/°C Drift
LT1461	Micropower Series Reference, 2.5V	0.04% Max, 3ppm/°C Max Drift
LT1592	Ultraprecise 16-Bit SoftSpan™ DAC	Six Programmable Output Ranges
LTC1799	Resistor Set SOT-23 Oscillator	Single Resistor Frequency Set
LTC1983	100mA Charge Pump	5V to Regulated –5V Conversion
LTC2053	Rail-to-Rail Instrumentation Amplifier	10µV Offset with 50nV/°C Drift, 2.5µV_{P-P} Noise 0.01Hz to 10Hz
LTC2440	1-Channel, Differential Input, High Speed/Low Noise, 24-Bit, No Latency ΔΣ ADC	2µV_{RMS} Noise at 880Hz, 200nV_{RMS} Noise at 6.9Hz, 0.0005% INL, Up to 3.5kHz Output Rate