LT1028/LT1128

Ultra Low Noise Precision High Speed Op Amps

LINEAR TECHNOLOGY

FEATURES

- Voltage Noise
  - 1.1nV/√Hz Max. at 1kHz
  - 0.85nV/√Hz Typ. at 1kHz
  - 1.0nV/√Hz Typ. at 10Hz
  - 35nV$_{P-P}$ Typ., 0.1Hz to 10Hz
- Voltage and Current Noise 100% Tested
- Gain-Bandwidth Product
  - LT1028: 50MHz Min.
  - LT1128: 13MHz Min.
- Slew Rate
  - LT1028: 11V/μs Min.
  - LT1128: 5V/μs Min.
- Offset Voltage: 40μV Max.
- Drift with Temperature: 0.8μV/°C Max.
- Voltage Gain: 7 Million Min.
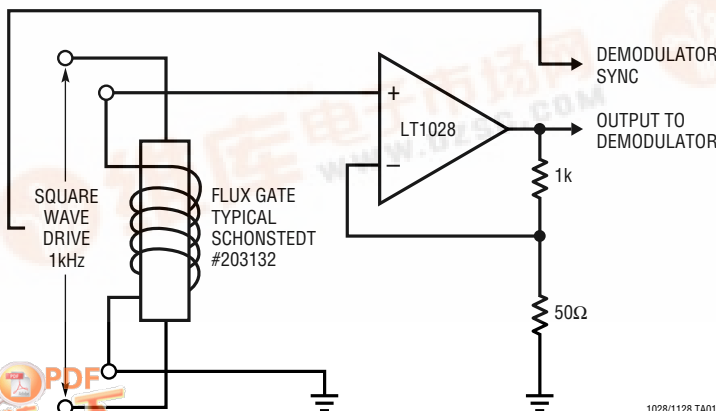- Available in 8-Pin SO Package

APPLICATIONS

- Low Noise Frequency Synthesizers
- High Quality Audio
- Infrared Detectors
- Accelerometer and Gyro Amplifiers
- 350Ω Bridge Signal Conditioning
- Magnetic Search Coil Amplifiers
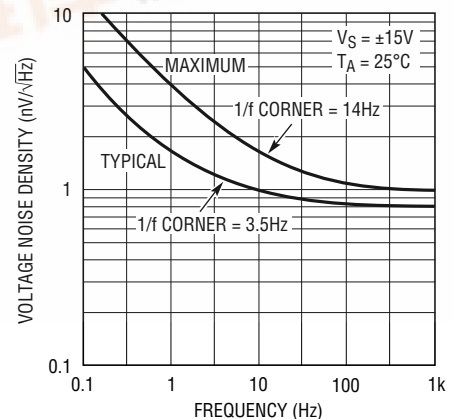- Hydrophone Amplfiers

DESCRIPTION

The LT1028(gain of –1 stable)/LT1128(gain of +1 stable) achieve a new standard of excellence in noise performance with 0.85nV/√Hz 1kHz noise, 1.0nV/√Hz 10Hz noise. This ultra low noise is combined with excellent high speed specifications (gain-bandwidth product is 75MHz for LT1028, 20MHz for LT1128), distortion-free output, and true precision parameters (0.1μV/°C drift, 10μV offset voltage, 30 million voltage gain). Although the LT1028/LT1128 input stage operates at nearly 1mA of collector current to achieve low voltage noise, input bias current is only 25nA.

The LT1028/LT1128's voltage noise is less than the noise of a 50Ω resistor. Therefore, even in very low source impedance transducer or audio amplifier applications, the LT1028/LT1128's contribution to total system noise will be negligible.
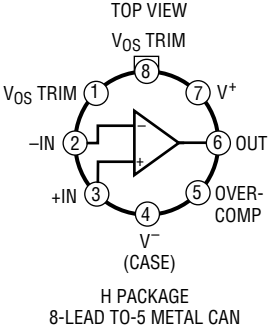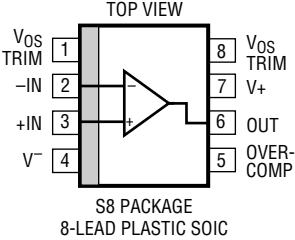
Flux Gate Amplifier

LT1028

SQUARE WAVE DRIVE 1kHz

FLUX GATE TYPICAL SCHONSTEDT #203132

DEMODULATOR SYNC

OUTPUT TO DEMODULATOR

1k

50Ω

1028/1128 TA01

Voltage Noise vs Frequency

VOLTAGE NOISE DENSITY (nV/√Hz)

V$_S$ = ±15V
T$_A$ = 25°C

MAXIMUM

1/f CORNER = 14Hz

TYPICAL

1/f CORNER = 3.5Hz

FREQUENCY (Hz)

1028/1128 TA02
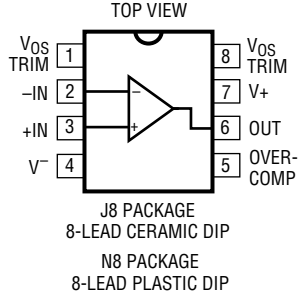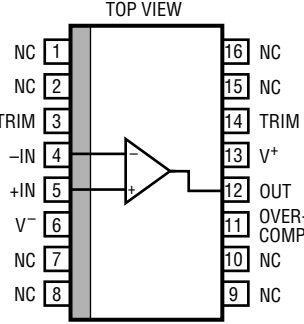
ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- −55°C to 105°C .... ±22V
- 105°C to 125°C .... ±16V

Differential Input Current (Note 8) .... ±25mA
Input Voltage .... Equal to Supply Voltage
Output Short Circuit Duration .... Indefinite

Operating Temperature Range
- LT1028/LT1128AM, M .... −55°C to 125°C
- LT1028/LT1128AC, C .... −40°C to 85°C

Storage Temperature Range
- All Devices .... −65°C to 150°C

Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
TOP VIEW H PACKAGE 8-LEAD TO-5 METAL CAN	LT1028AMH LT1028MH LT1028ACH LT1028CH

V_OS TRIM (8)
V_OS TRIM (1) — V+ (7)
−IN (2) — OUT (6)
+IN (3) — OVER-COMP (5)
V− (4) (CASE)

	ORDER PART NUMBER
TOP VIEW S8 PACKAGE 8-LEAD PLASTIC SOIC	LT1028CS8 LT1128CS8
	S8 PART MARKING
	1028 1128

V_OS TRIM [1] — [8] V_OS TRIM
−IN [2] — [7] V+
+IN [3] — [6] OUT
V− [4] — [5] OVER-COMP

	ORDER PART NUMBER
TOP VIEW J8 PACKAGE 8-LEAD CERAMIC DIP N8 PACKAGE 8-LEAD PLASTIC DIP	LT1028AMJ8 LT1028MJ8 LT1028ACJ8 LT1028CJ8 LT1028ACN8 LT1028CN8 LT1128AMJ8 LT1128MJ8 LT1128CJ8 LT1128ACN8 LT1128CN8

V_OS TRIM [1] — [8] V_OS TRIM
−IN [2] — [7] V+
+IN [3] — [6] OUT
V− [4] — [5] OVER-COMP

	ORDER PART NUMBER
TOP VIEW S PACKAGE 16-LEAD PLASTIC SOL	LT1028CS16

NC [1] — [16] NC
NC [2] — [15] NC
TRIM [3] — [14] TRIM
−IN [4] — [13] V+
+IN [5] — [12] OUT
V− [6] — [11] OVER-COMP
NC [7] — [10] NC
NC [8] — [9] NC

NOTE: THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGNS

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1028AM/AC LT1128AM/AC			LT1028M/C LT1128M/C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)		10	40		20	80	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Note 2)		0.3			0.3		μV/Mo
I_{OS}	Input Offset Current	$V_{CM} = 0V$		12	50		18	100	nA
I_B	Input Bias Current	$V_{CM} = 0V$		±25	±90		±30	±180	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 3)		35	75		35	90	nV_P-P

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1028AM/AC LT1128AM/AC			LT1028M/C LT1128M/C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
	Input Noise Voltage Density	$f_O = 10Hz$ (Note 4)			1.00	1.7		1.0	1.9	$nV/\sqrt{Hz}$
		$f_O = 1000Hz$, 100% tested			0.85	1.1		0.9	1.2	$nV/\sqrt{Hz}$
I_n	Input Noise Current Density	$f_O = 10Hz$ (Note 3 and 5)			4.7	10.0		4.7	12.0	$pA/\sqrt{Hz}$
		$f_O = 1000Hz$, 100% tested			1.0	1.6		1.0	1.8	$pA/\sqrt{Hz}$
	Input Resistance Common Mode				300			300		$M\Omega$
	Differential Mode				20			20		$k\Omega$
	Input Capacitance				5			5		pF
	Input Voltage Range			±11.0	±12.2		±11.0	±12.2		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm11V$		114	126		110	126		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4V$ to $\pm18V$		117	133		110	132		dB
A_{VOL}	Large-Signal Voltage Gain	$R_L \geq 2k$, $V_O = \pm12V$		7.0	30.0		5.0	30.0		$V/\mu V$
		$R_L \geq 1k$, $V_O = \pm10V$		5.0	20.0		3.5	20.0		$V/\mu V$
		$R_L \geq 600\Omega$, $V_O = \pm10V$		3.0	15.0		2.0	15.0		$V/\mu V$
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k$		±12.3	±13.0		±12.0	±13.0		V
		$R_L \geq 600\Omega$		±11.0	±12.2		±10.5	±12.2		V
SR	Slew Rate	$A_{VCL} = -1$ LT1028		11.0	15.0		11.0	15.0		$V/\mu s$
		$A_{VCL} = -1$ LT1128		5.0	6.0		4.5	6.0		$V/\mu s$
GBW	Gain-Bandwidth Product	$f_O = 20kHz$ (Note 6) LT1028		50	75		50	75		MHz
		$f_O = 200kHz$ (Note 6) LT1128		13	20		11	20		MHz
Z_O	Open-Loop Output Impedance	$V_O = 0$, $I_O = 0$			80			80		Ω
I_S	Supply Current				7.4	9.5		7.6	10.5	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1028AM LT1128AM			LT1028M LT1128M			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)	●		30	120		45	180	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 7)	●		0.2	0.8		0.25	1.0	$\mu V/°C$
I_{OS}	Input Offset Current	$V_{CM} = 0V$	●		25	90		30	180	nA
I_B	Input Bias Current	$V_{CM} = 0V$	●		±40	±150		±50	±300	nA
	Input Voltage Range		●	±10.3	±11.7		±10.3	±11.7		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm10.3V$	●	106	122		100	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4.5V$ to $\pm16V$	●	110	130		104	130		dB
A_{VOL}	Large-Signal Voltage Gain	$R_L \geq 2k$, $V_O = \pm10V$	●	3.0	14.0		2.0	14.0		$V/\mu V$
		$R_L \geq 1k$, $V_O = \pm10V$		2.0	10.0		1.5	10.0		$V/\mu V$
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k$	●	±10.3	±11.6		±10.3	±11.6		V
I_S	Supply Current		●		8.7	11.5		9.0	13.0	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1028AC LT1128AC			LT1028C LT1128C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)	●		15	80		30	125	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note7)	●		0.1	0.8		0.2	1.0	μV/°C
I_{OS}	Input Offset Current	$V_{CM} = 0V$	●		15	65		22	130	nA
I_B	Input Bias Current	$V_{CM} = 0V$	●		±30	±120		±40	±240	nA
	Input Voltage Range		●	±10.5	±12.0		±10.5	±12.0		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm10.5V$	●	110	124		106	124		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4.5V$ to $\pm18V$	●	114	132		107	132		dB
A_{VOL}	Large-Signal Voltage Gain	$R_L \ge 2k$, $V_O = \pm10V$	●	5.0	25.0		3.0	25.0		V/μV
		$R_L \ge 1k$, $V_O = \pm10V$		4.0	18.0		2.5	18.0		V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \ge 2k$	●	±11.5	±12.7		±11.5	±12.7		V
		$R_L \ge 600\Omega$ (Note 9)		±9.5	±11.0		±9.0	±10.5		V
I_S	Supply Current		●		8.0	10.5		8.2	11.5	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $-40°C \le T_A \le 85°C$, unless otherwise noted. (Note 10)

SYMBOL	PARAMETER	CONDITIONS		LT1028AC LT1128AC			LT1028C LT1128C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●		20	95		35	150	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift		●		0.2	0.8		0.25	1.0	μV/°C
I_{OS}	Input Offset Current	$V_{CM} = 0V$	●		20	80		28	160	nA
I_B	Input Bias Current	$V_{CM} = 0V$	●		±35	±140		±45	±280	nA
	Input Voltage Range		●	±10.4	±11.8		±10.4	±11.8		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm10.5V$	●	108	123		102	123		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4.5V$ to $\pm18V$	●	112	131		106	131		dB
A_{VOL}	Large-Signal Voltage Gain	$R_L \ge 2k$, $V_O = \pm10V$	●	4.0	20.0		2.5	20.0		V/μV
		$R_L \ge 1k$, $V_O = \pm10V$		3.0	14.0		2.0	14.0		V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \ge 2k$	●	±11.0	±12.5		±11.0	±12.5		V
I_S	Supply Current		●		8.5	11.0		8.7	12.5	mA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 sec. after application of power. In addition, at $T_A = 25°C$, offset voltage is measured with the chip heated to approximately 55°C to account for the chip temperature rise when the device is fully warmed up.

Note 2: Long Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV.

Note 3: This parameter is tested on a sample basis only.

Note 4: 10Hz noise voltage density is sample tested on every lot with the exception of the S8 and S16 packages. Devices 100% tested at 10Hz are available on request.

Note 5: Current noise is defined and measured with balanced source resistors. The resultant voltage noise (after subtracting the resistor noise on an RMS basis) is divided by the sum of the two source resistors to obtain current noise. Maximum 10Hz current noise can be inferred from 100% testing at 1kHz.

Note 6: Gain-bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

**Note 7:** This parameter is not 100% tested.

Note 8: The inputs are protected by back-to-back diodes. Current-limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±1.8V, the input current should be limited to 25mA.

Note 9: This parameter guaranteed by design, fully warmed up at $T_A = 70°C$. It includes chip temperature increase due to supply and load currents.

Note 10: The LT1028/LT1128 are not tested and are not quality-assurance-sampled at −40°C and at 85°C. These specifications are guaranteed by design, correlation and/or inference from −55°C, 0°C, 25°C, 70°C and /or 125°C tests.

TYPICAL PERFORMANCE CHARACTERISTICS

10Hz Voltage Noise Distribution

$V_S = \pm 15V$
$T_A = 25°C$
500 UNITS
MEASURED
FROM 4 RUNS

NUMBER OF UNITS
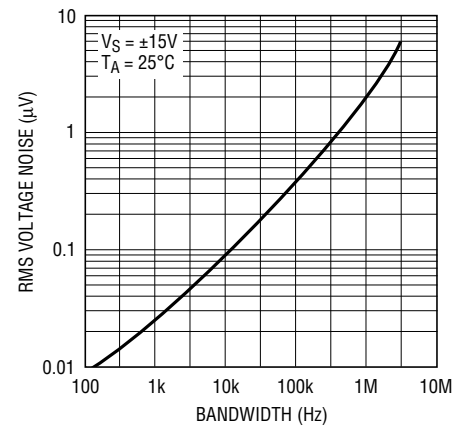
VOLTAGE NOISE DENSITY (nV/√Hz)
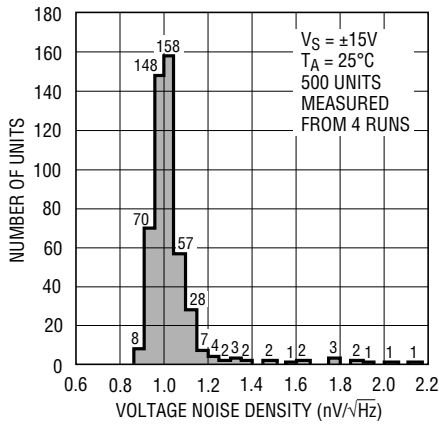
LT1020/1120 • TPC01

Wideband Noise, DC to 20kHz
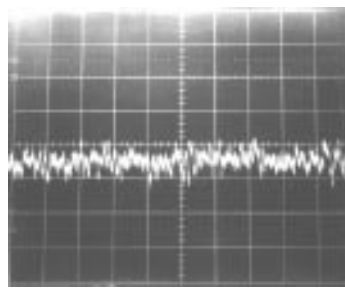
VERTICAL SCALE = 0.5µV/DIV
HORIZONTAL SCALE = 0.5ms/DIV

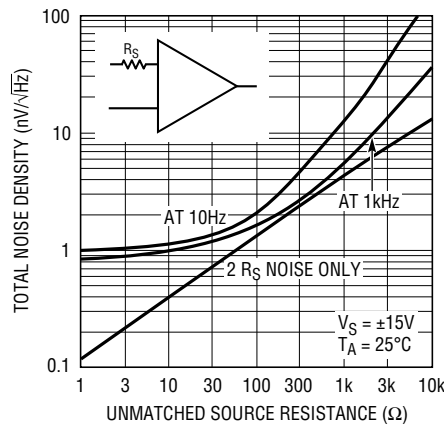**Wideband Voltage Noise
(0.1Hz to Frequency Indicated)**

$V_S = \pm 15V$
$T_A = 25°C$

RMS VOLTAGE NOISE (µV)

BANDWIDTH (Hz)

LT1028/1128 • TPC03

**Total Noise vs Matched Source
Resistance**

R_S
R_S

AT 10Hz   AT 1kHz

2 R_S NOISE ONLY

$V_S = \pm 15V$
$T_A = 25°C$

TOTAL NOISE DENSITY (nV/√Hz)

MATCHED SOURCE RESISTANCE (Ω)
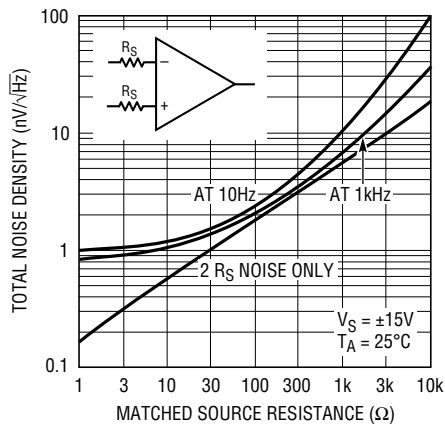
LT1028/1128 • TPC04

**Total Noise vs Unmatched
Source Resistance**

R_S

AT 10Hz   AT 1kHz

2 R_S NOISE ONLY

$V_S = \pm 15V$
$T_A = 25°C$

TOTAL NOISE DENSITY (nV/√Hz)

UNMATCHED SOURCE RESISTANCE (Ω)

LT1028/1128 • TPC05

Current Noise Spectrum

MAXIMUM

1/f CORNER = 800Hz

TYPICAL

1/f CORNER = 250Hz

CURRENT NOISE DENSITY (pA/√Hz)

FREQUENCY (Hz)
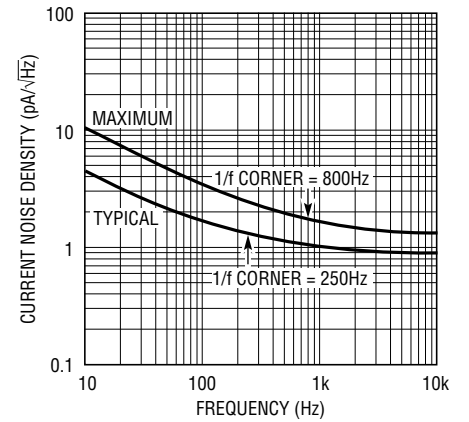
LT1028/1128 • TPC06

0.1Hz to 10Hz Voltage Noise

$V_S = \pm 15V$
$T_A = 25°C$

10nV

TIME (SEC)
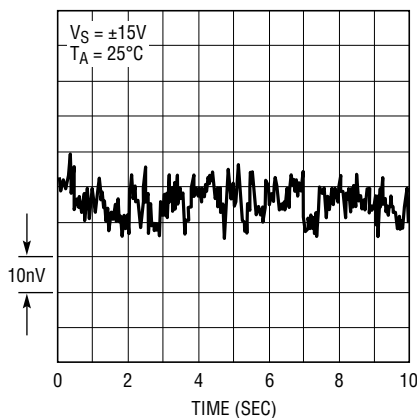
LT1028/1128 • TPC07

0.01Hz to 1Hz Voltage Noise

$V_S = \pm 15V$
$T_A = 25°C$

10nV

TIME (SEC)
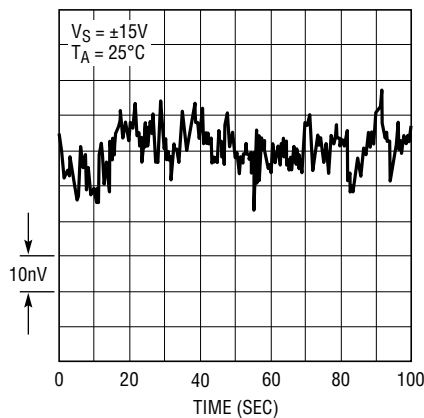
LT1028/1128 • TPC07

Voltage Noise vs Temperature

$V_S = \pm 15V$

AT 10Hz

AT 1kHz

RMS VOLTAGE DENSITY (nV/√Hz)
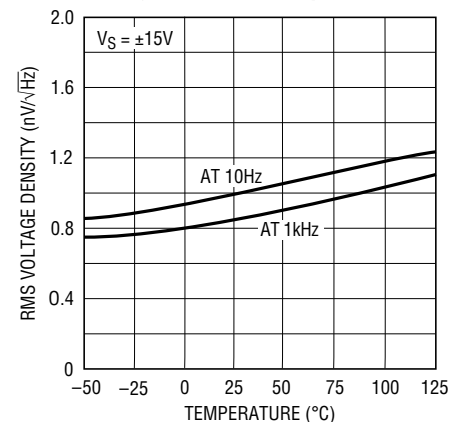
TEMPERATURE (°C)

LT1028/1128 • TPC09

TYPICAL PERFORMANCE CHARACTERISTICS

Distribution of Input Offset Voltage

$V_S = \pm 15V$
$T_A = 25°C$
800 UNITS TESTED FROM FOUR RUNS

UNITS (%) vs OFFSET VOLTAGE (μV)
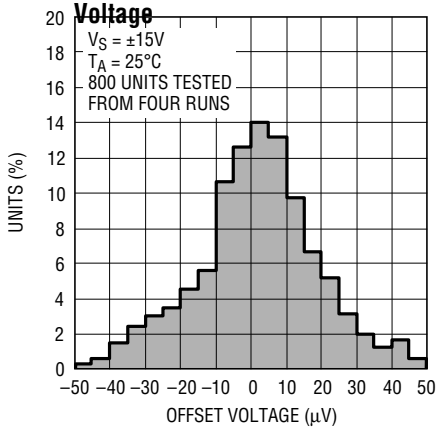
LT1028/1128 • TPC10

Offset Voltage Drift with Temperature of Representative Units

$V_S = \pm 15V$

OFFSET VOLTAGE (μV) vs TEMPERATURE (°C)
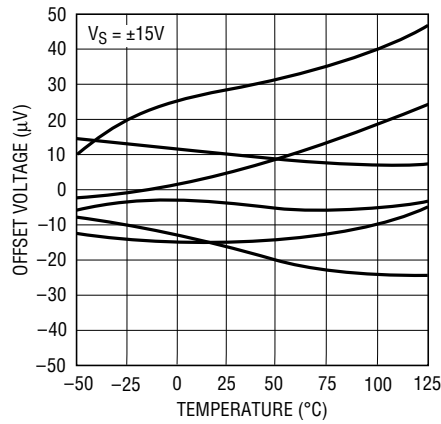
LT1028/1128 • TPC11

Long-Term Stability of Five Representative Units

$V_S = \pm 15V$
$T_A = 25°C$
t = 0 AFTER 1 DAY PRE-WARM UP

OFFSET VOLTAGE CHANGE (μV) vs TIME (MONTHS)
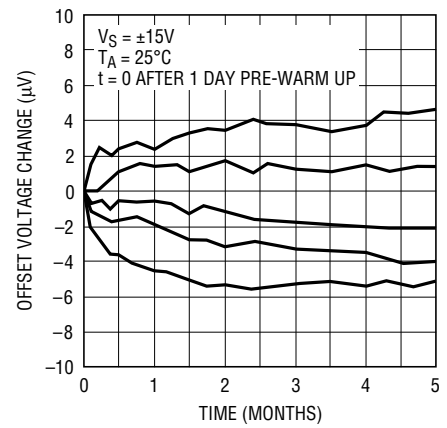
LT1028/1128 • TPC12

Warm-Up Drift

$V_S = \pm 15V$
$T_A = 25°C$

METAL CAN (H) PACKAGE

DUAL-IN-LINE PACKAGE PLASTIC (N) OR CERDIP (J)

CHANGE IN OFFSET VOLTAGE (μV) vs TIME AFTER POWER ON (MINUTES)
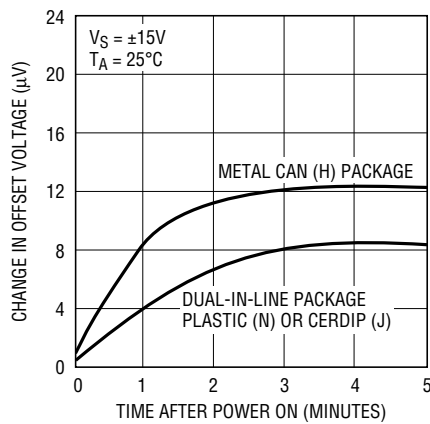
LT1028/1128 • TPC13

Input Bias and Offset Currents Over Temperature

$V_S = \pm 15V$
$V_{CM} = 0V$

BIAS CURRENT

OFFSET CURRENT

INPUT BIAS AND OFFSET CURRENTS (nA) vs TEMPERATURE (°C)
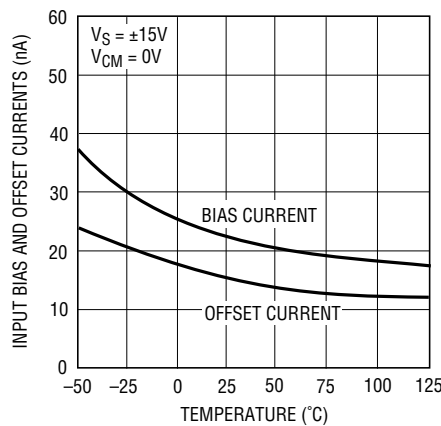
LT1028/1128 • TPC14

Bias Current Over the Common-Mode Range

$R_{CM} = \dfrac{20V}{65nA} \approx 300M\Omega$ $V_S = \pm 15V$ $T_A = 25°C$

POSITIVE INPUT CURRENT (UNDERCANCELLED) DEVICE

NEGATIVE INPUT CURRENT (OVERCANCELLED) DEVICE

INPUT BIAS CURRENT (nA) vs COMMON-MODE INPUT VOLTAGE (V)
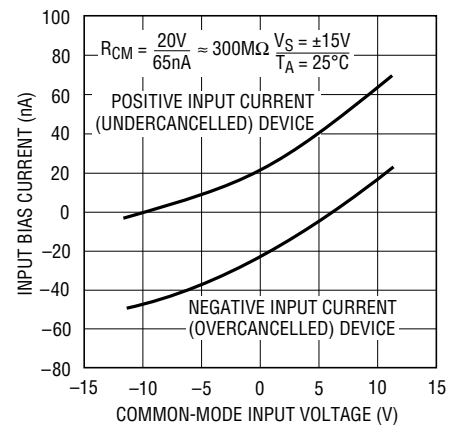
LT1028/1128 • TPC15

Voltage Noise vs Supply Voltage

$T_A = 25°C$

AT 10Hz

AT 1kHz

RMS VOLTAGE NOISE DENSITY (nV/$\sqrt{Hz}$) vs SUPPLY VOLTAGE (V)
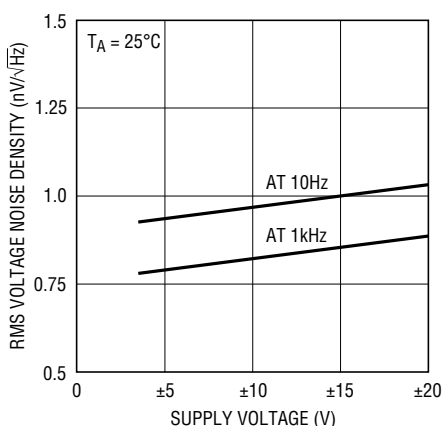
LT1028/1128 • TPC16

Supply Current vs Temperature

$V_S = \pm 15V$

$V_S = \pm 5V$

SUPPLY CURRENT (mA) vs TEMPERATURE (°C)
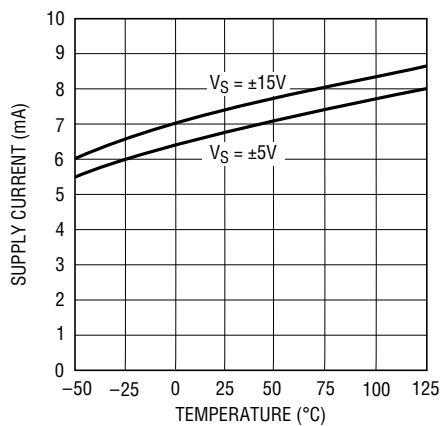
LT1028/1128 • TPC17

Output Short-Circuit Current vs Time

$-50°C$ $V_S = \pm 15V$
$25°C$
$125°C$
SOURCING

$125°C$
$25°C$
SINKING
$-50°C$

SHORT-CIRCUIT CURRENT (mA) vs TIME FROM OUTPUT SHORT TO GROUND (MINUTES)
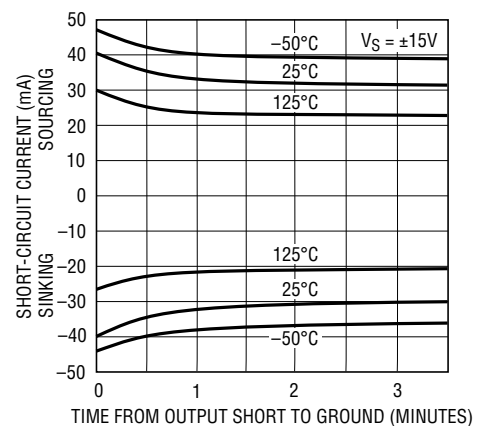
LT1028/1128 • TPC18

TYPICAL PERFORMANCE CHARACTERISTICS

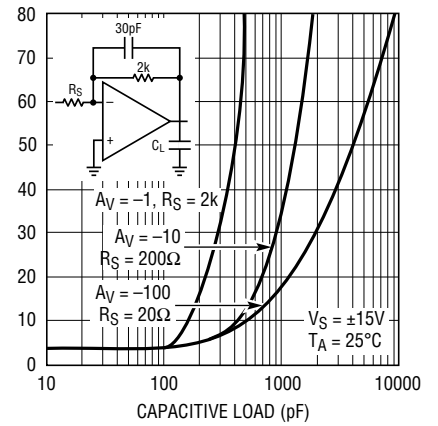### Voltage Gain vs Frequency
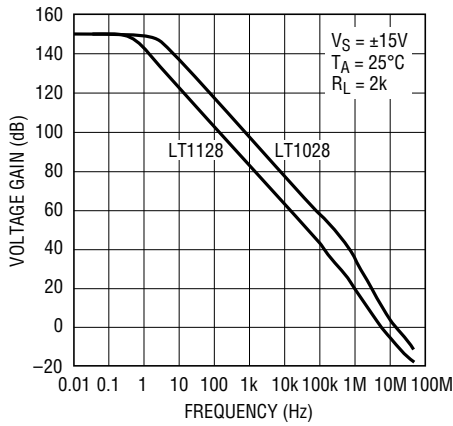
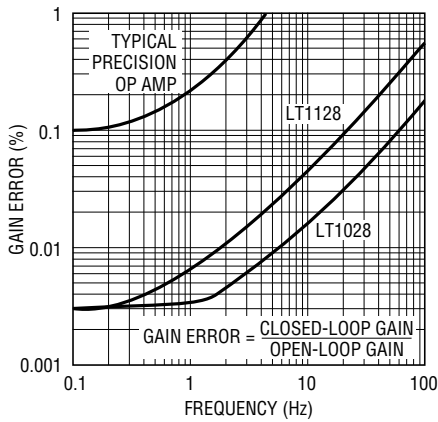LT1028/1128 • TPC19

LT1028
Gain, Phase vs Frequency
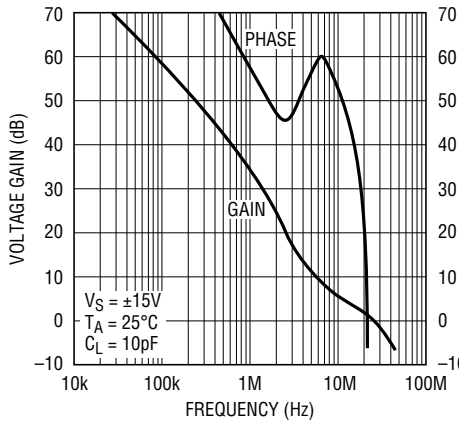
LT1028/1128 • TPC20

LT1028
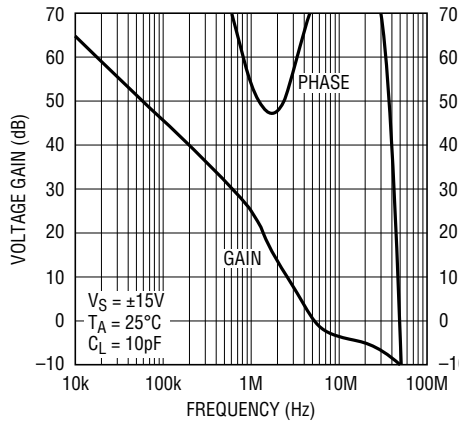### Capacitance Load Handling

LT1028/1128 • TPC21

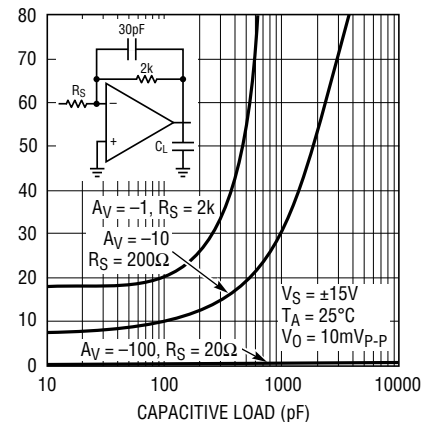### Gain Error vs Frequency
Closed-Loop Gain = 1000

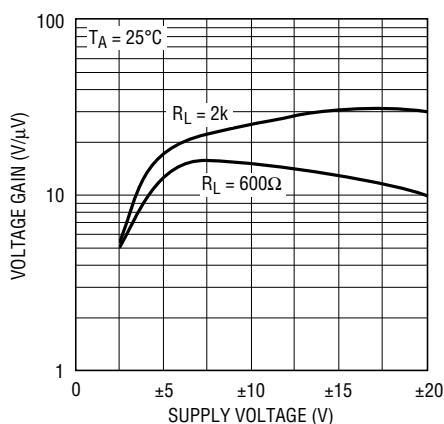LT1028/1128 • TPC22

LT1128
Gain Phase vs Frequency

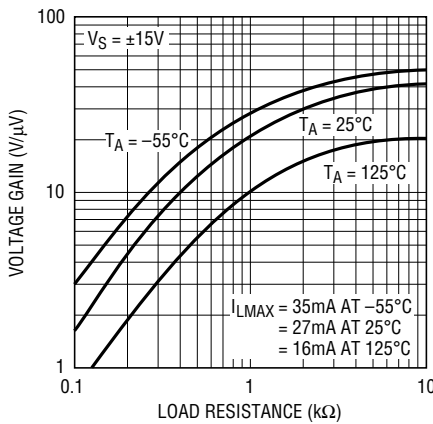LT1028/1128 • TPC23

LT1128
Capacitance Load Handling
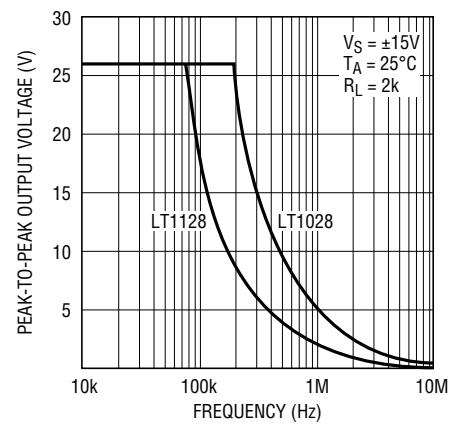

LT1028/1128 • TPC 24

Voltage Gain vs Supply Voltage

LT1028/1128 • TPC25

Voltage Gain vs Load Resistance

LT1028/1128 • TPC26

Maximum Undistorted Output
vs Frequency

LT1028/1128 • TPC27
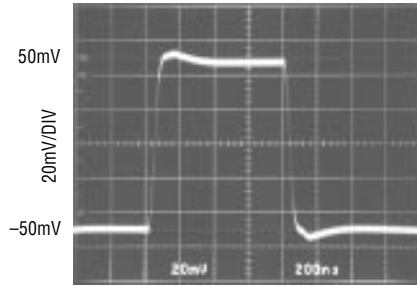
LT1028/LT1128

TYPICAL PERFORMANCE CHARACTERISTICS

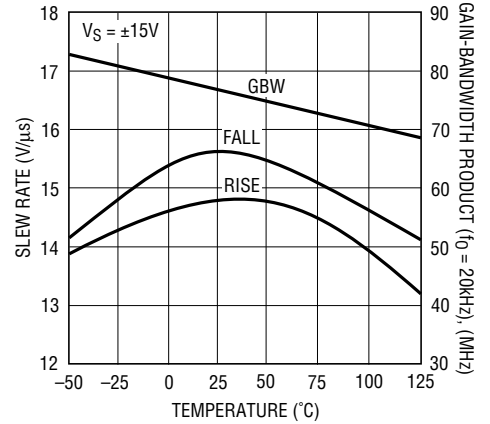**LT1028**
Large-Signal Transient Response
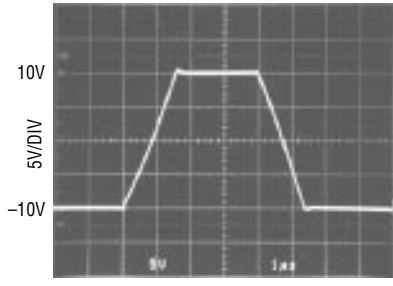
1μs/DIV
$A_V = -1$, $R_S = R_F = 2k$, $C_F = 15pF$
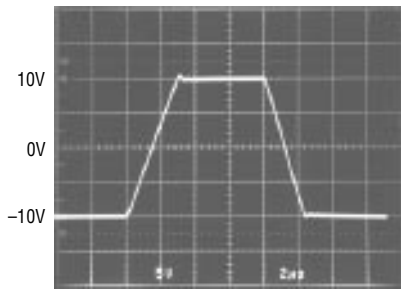
LT1028
Small-Signal Transient Response

0.2μs/DIV
$A_V = -1$, $R_S = R_F = 2k$
$C_F = 15pF$, $C_L = 80pF$

LT1028
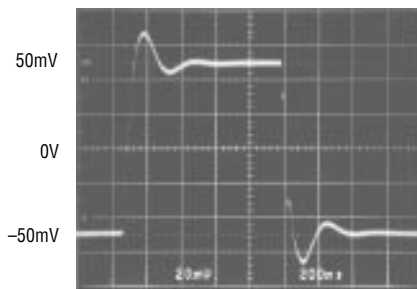**Slew Rate, Gain-Bandwidth Product Over Temperature**

LT1028/1128 • TPC30
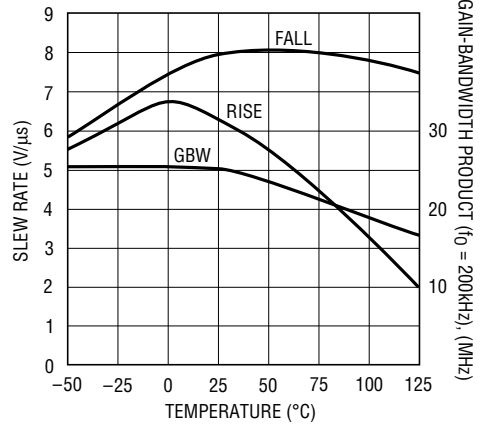
LT1128
Large-Signal Transient Response

2μs/DIV
$A_V = -1$, $R_S = R_F = 2k$, $C_F = 30pF$

LT1128
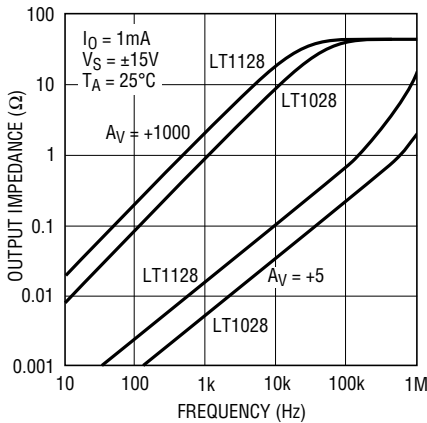**Small-Signal Transient Response**

0.2μs/DIV
$A_V = +1$, $C_L = 10pF$

LT1128
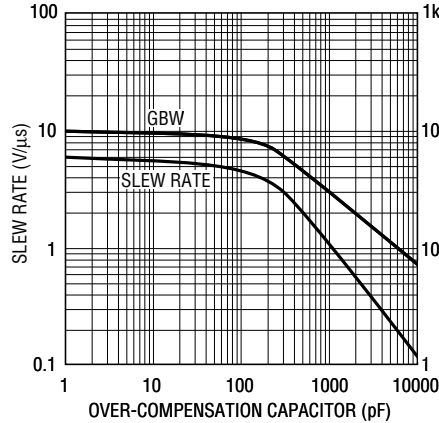**Slew Rate, Gain-Bandwidth Product Over Temperature**

LT1028/1128 • TPC33

Closed-Loop Output Impedance

$I_O = 1mA$
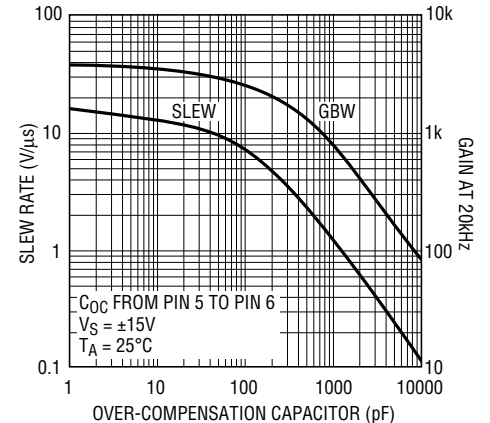$V_S = ±15V$
$T_A = 25°C$

LT1028/1128 • TPC34

LT1128
Slew Rate, Gain-Bandwidth Product vs Over-Compensation Capacitor

LT1028/1128 • TPC35

LT1028
Slew Rate, Gain-Bandwidth Product vs Over-Compensation Capacitor

C_{OC} FROM PIN 5 TO PIN 6
$V_S = ±15V$
$T_A = 25°C$

LT1028/1128 • TPC36

TYPICAL PERFORMANCE CHARACTERISTICS

Common-Mode Limit Over Temperature
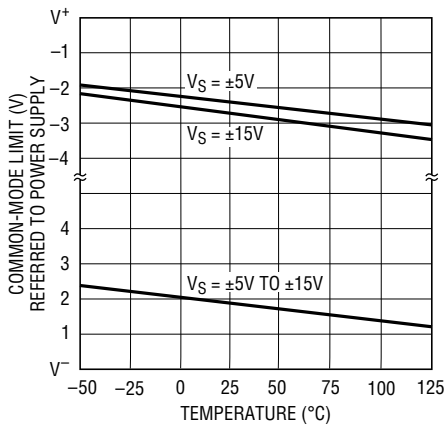
LT1028/1128 • TPC37

Common-Mode Rejection Ratio vs Frequency
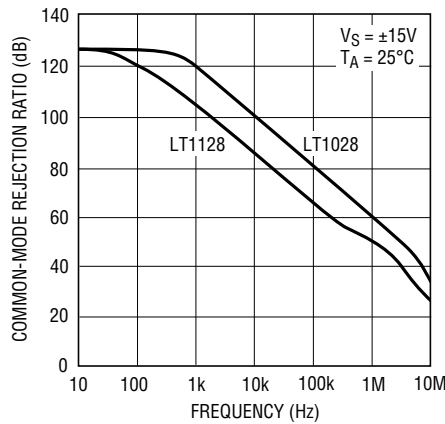
LT1028/1128 • TPC38

Power Supply Rejection Ratio vs Frequency
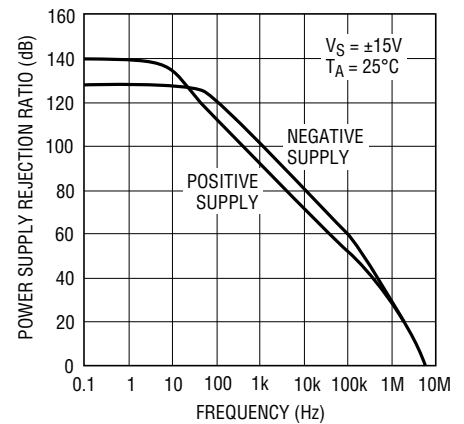
LT1028/1128 • TPC39

**LT1028
Total Harmonic Distortion vs Frequency and Load Resistance**
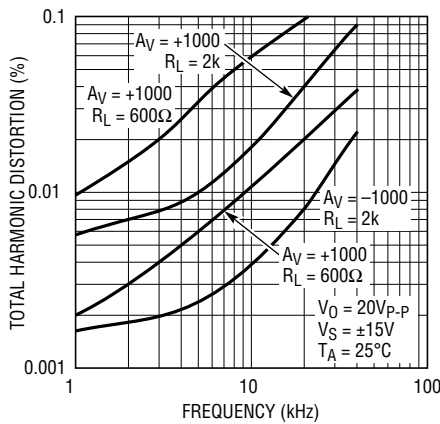
LT1028/1128 • TPC40

**LT1028
Total Harmonic Distortion vs Closed-Loop Gain**

LT1028/1128 • TPC41

High Frequency Voltage Noise vs Frequency

LT1028/1128 • TPC42

**LT1128
Total Harmonic Distortion vs Frequency and Load Resistance**

LT1028/1128 • TPC43

**LT1128
Total Harmonic Distortion vs Closed-Loop Gain**

LT1028/1128 • TPC44

APPLICATIONS INFORMATION–NOISE

Voltage Noise vs Current Noise

The LT1028/LT1128's less than 1nV/$\sqrt{Hz}$ voltage noise is three times better than the lowest voltage noise heretofore available (on the LT1007/1037). A necessary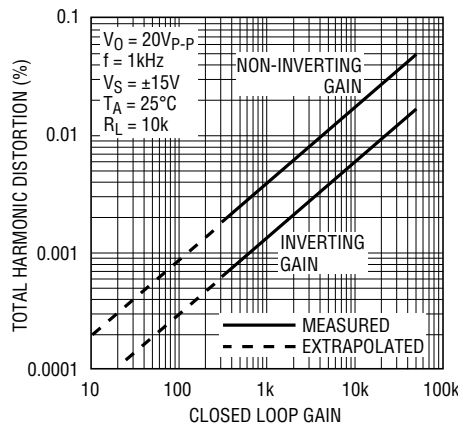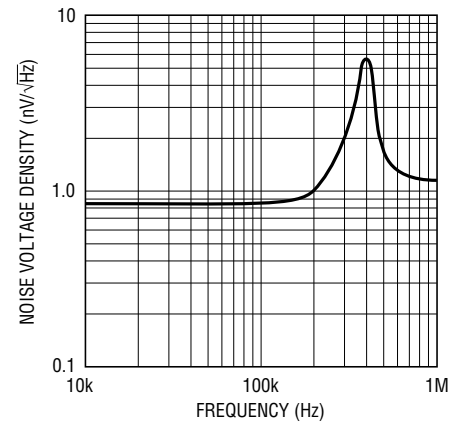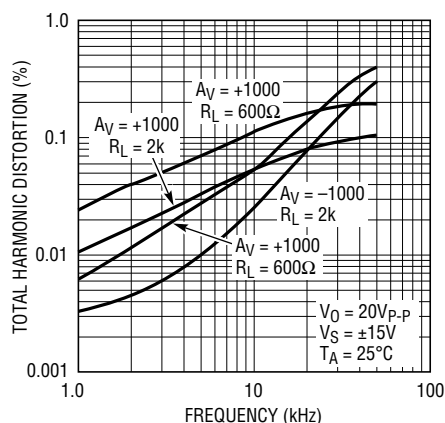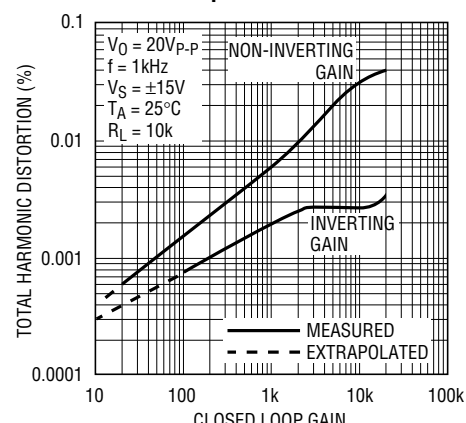 condition for such low voltage noise is operating the input transistors at nearly 1mA of collector currents, because voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. Consequently, the LT1028/LT1128's current noise is significantly higher than on most monolithic op amps.

Therefore, to realize truly low noise performance it is important to understand the interaction between voltage noise (e_n), current noise (I_n) and resistor noise (r_n).
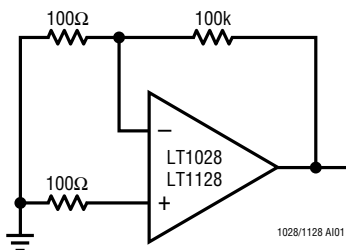
Total Noise vs Source Resistance

The total input referred noise of an op amp is given by

$$e_t = [e_n^2 + r_n^2 + (I_n R_{eq})^2]^{1/2}$$

where R_{eq} is the total equivalent source resistance at the two inputs, and

$$r_n = \sqrt{4kTR_{eq}} = 0.13\sqrt{R_{eq}} \quad \text{in nV}/\sqrt{Hz} \text{ at } 25°C$$

As a numerical example, consider the total noise at 1kHz of the gain 1000 amplifier shown below.

1028/1128 AI01

$$R_{eq} = 100\Omega + 100\Omega \parallel 100k \approx 200\Omega$$
$$r_n = 0.13\sqrt{200} = 1.84\text{nV}\sqrt{Hz}$$
$$e_n = 0.85\text{nV}\sqrt{Hz}$$
$$I_n = 1.0\text{pA}/\sqrt{Hz}$$
$$e_t = [0.85^2 + 1.84^2 + (1.0 \times 0.2)^2]^{1/2} = 2.04\text{nV}/\sqrt{Hz}$$

Output noise = 1000 e_t = 2.04μV/$\sqrt{Hz}$

At very low source resistance ($R_{eq} < 40\Omega$) voltage noise dominates. As R_{eq} is increased resistor noise becomes the largest term, as in the example above, and the LT1028/LT1128's voltage noise becomes negligible. As R_{eq} is further increased, current noise becomes important. At 1kHz, when R_{eq} is in excess of 20k, the current noise component is larger than the resistor noise. The total noise versus matched source resistance plot illustrates the above calculations.

The plot also shows that current noise is more dominant at low frequencies, such as 10Hz. This is because resistor noise is flat with frequency, while the 1/f corner of current noise is typically at 250Hz. At 10Hz when $R_{eq} > 1k$, the current noise term will exceed the resistor noise.

When the source resistance is unmatched, the total noise versus unmatched source resistance plot should be consulted. Note that total noise is lower at source resistances below 1k because the resistor noise contribution is less. When $R_S > 1k$ total noise is not improved, however. This is because bias current cancellation is used to reduce input bias current. The cancellation circuitry injects two correlated current noise components into the two inputs. With matched source resistors the injected current noise creates a common-mode voltage noise and gets rejected by the amplifier. With source resistance in one input only, the cancellation noise is added to the amplifier's inherent noise.

In summary, the LT1028/LT1128 are the optimum amplifiers for noise performance, provided that the source resistance is kept low. The following table depicts which op amp manufactured by Linear Technology should be used to minimize noise, as the source resistance is increased beyond the LT1028/LT1128's level of usefulness.

Best Op Amp for Lowest Total Noise vs Source Resistance

SOURCE RESISTANCE(Ω) (Note 1)	BEST OP AMP	
	AT LOW FREQ(10Hz)	WIDEBAND(1kHz)
0 to 400	LT1028/LT1128	LT1028/LT1128
400 to 4k	LT1007/1037	LT1028/LT1128
4k to 40k	LT1001	LT1007/1037
40k to 500k	LT1012	LT1001
500k to 5M	LT1012 or LT1055	LT1012
>5M	LT1055	LT1055

Note 1: Source resistance is defined as matched or unmatched, e.g., R_S = 1k means: 1k at each input, or 1k at one input and zero at the other.

APPLICATIONS INFORMATION–NOISE

Noise Testing – Voltage Noise

The LT1028/LT1128's RMS voltage noise density can be accurately measured using the Quan Tech Noise Analyzer, Model 5173 or an equivalent noise tester. Care should be taken, however, to subtract the noise of the source resistor used. Prefabricated test cards for the Model 5173 set the device under test in a closed-loop gain of 31 with a 60Ω source resistor and a 1.8k feedback resistor. The noise of this resistor combination is $0.13\sqrt{58}$ = 1.0nV/$\sqrt{\text{Hz}}$. An LT1028/LT1128 with 0.85nV/$\sqrt{\text{Hz}}$ noise will read $(0.85^2 + 1.0^2)^{1/2}$ = 1.31nV/$\sqrt{\text{Hz}}$. For better resolution, the resistors should be replaced with a 10Ω source and 300Ω feedback resistor. Even a 10Ω resistor will show an apparent noise which is 8% to 10% too high.
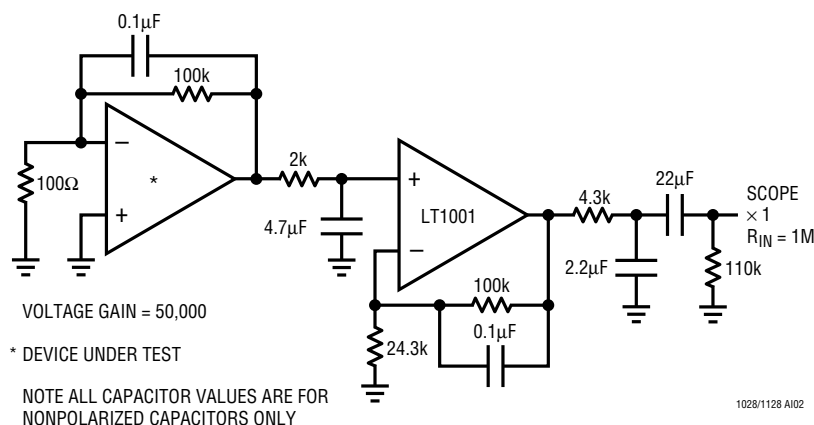
The 0.1Hz to 10Hz peak-to-peak noise of the LT1028/LT1128 is measured in the test circuit shown. The frequency response of this noise tester indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

Measuring the typical 35nV peak-to-peak noise performance of the LT1028/LT1128 requires special test precautions:

(a) The device should be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically 10μV due to its chip temperature increasing 30°C to 40°C from the moment the power supplies are turned on. In the 10 second measurement interval these temperature-induced effects can easily exceed tens of nanovolts.

(b) For similar reasons, the device must be well shielded from air current to eliminate the possibility of thermo-electric effects in excess of a few nanovolts, which would invalidate the measurements.

(c) Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.

A noise-voltage density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage density measurement will correlate well with a 0.1Hz to 10Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

0.1Hz to 10Hz Noise Test Circuit

VOLTAGE GAIN = 50,000

* DEVICE UNDER TEST

NOTE ALL CAPACITOR VALUES ARE FOR NONPOLARIZED CAPACITORS ONLY

1028/1128 AI02

0.1Hz to 10Hz Peak-to-Peak Noise Tester Frequency Response

LT1028/1128 • AI03
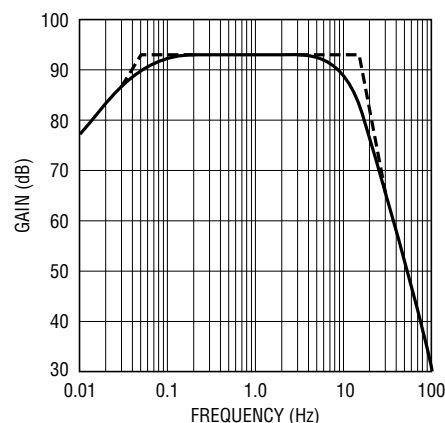
APPLICATIONS INFORMATION – NOISE

Noise Testing – Current Noise

Current noise density (I_n) is defined by the following formula, and can be measured in the circuit shown:

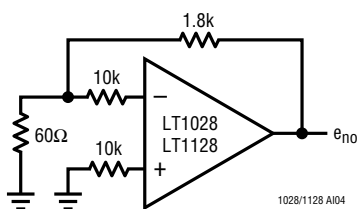$$I_n = \frac{[e_{no}^2 - (31 \times 18.4nV/\sqrt{Hz})^2]^{1/2}}{20k \times 31}$$


1028/1128 AI04

If the Quan Tech Model 5173 is used, the noise reading is input-referred, therefore the result should not be divided by 31; the resistor noise should not be multiplied by 31.

100% Noise Testing

The 1kHz voltage and current noise is 100% tested on the LT1028/LT1128 as part of automated testing; the approximate frequency response of the filters is shown. The limits on the automated testing are established by extensive correlation tests on units measured with the Quan Tech Model 5173.

10Hz voltage noise density is sample tested on every lot. Devices 100% tested at 10Hz are available on request for an additional charge.

10Hz current noise is not tested on every lot but it can be inferred from 100% testing at 1kHz. A look at the current noise spectrum plot will substantiate this statement. The only way 10Hz current noise can exceed the guaranteed limits is if its 1/f corner is higher than 800Hz and/or its white noise is high. If that is the case then the 1kHz test will fail.

Automated Tester Noise Filter

LT1028/1128 • AI05
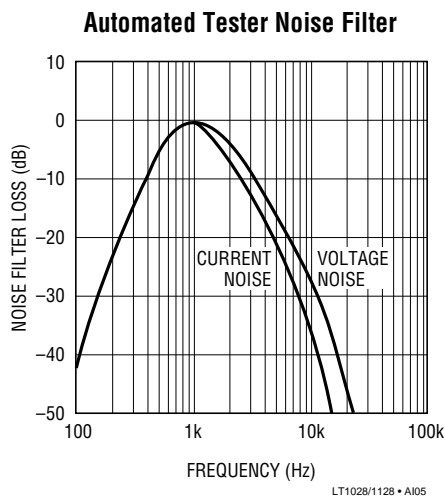
APPLICATIONS INFORMATION

General

The LT1028/LT1128 series devices may be inserted directly into OP-07, OP-27, OP-37, LT1007 and LT1037 sockets with or without removal of external nulling components. In addition, the LT1028/LT1128 may be fitted to 5534 sockets with the removal of external compensation components.

Offset Voltage Adjustment

The input offset voltage of the LT1028/LT1128 and its drift with temperature, are permanently trimmed at wafer testing to a low level. However, if further adjustment of V_{OS} is necessary, the use of a 1k nulling potentiometer will not degrade drift with temperature. Trimming to a value other

1028/1128 AI06
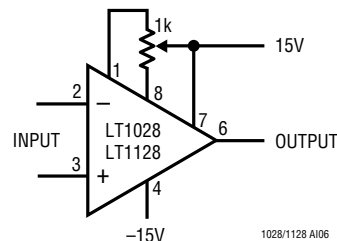
than zero creates a drift of $(V_{OS}/300)\mu V/°C$, e.g., if V_{OS} is adjusted to $300\mu V$, the change in drift will be $1\mu V/°C$.

The adjustment range with a 1k pot is approximately ±1.1mV.

Offset Voltage and Drift

Thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input

APPLICATIONS INFORMATION

terminals, can exceed the inherent drift of the amplifier unless proper care is exercised. Air currents should be minimized, package leads should be short, the two input leads should be close together and maintained at the same temperature.

The circuit shown to measure offset voltage is also used as the burn-in configuration for the LT1028/LT1128.

**Test Circuit for Offset Voltage
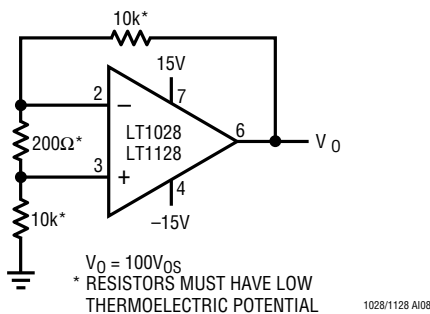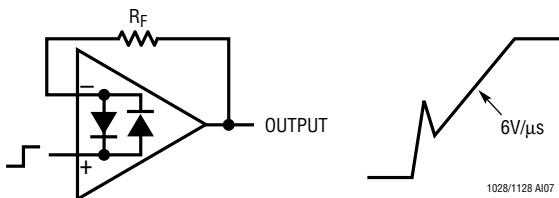and Offset Voltage Drift with Temperature**

$V_O = 100V_{OS}$
* RESISTORS MUST HAVE LOW
  THERMOELECTRIC POTENTIAL

1028/1128 AI08

Unity-Gain Buffer Applications (LT1128 Only)

When $R_F \leq 100\Omega$ and the input is driven with a fast, large-signal pulse (>1V), the output waveform will look as shown in the pulsed operation diagram.


1028/1128 AI07

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_F \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at 10V) and the amplifier stays in its active mode and a smooth transition will occur.

As with all operational amplifiers when $R_F > 2k$, a pole will be created with R_F and the amplifier's input capacitance, creating additional phase shift and reducing the phase margin. A small capacitor (20pF to 50pF) in parallel with R_F will eliminate this problem.

Frequency Response

The LT1028's Gain, Phase vs Frequency plot indicates that the device is stable in closed-loop gains greater than +2 or −1 because phase margin is about 50° at an open-loop gain of 6dB. In the voltage follower configuration phase margin seems inadequate. This is indeed true when the output is shorted to the inverting input and the noninverting input is driven from a 50Ω source impedance. However, when feedback is through a parallel R-C network (provided $C_F < 68pF$), the LT1028 will be stable because of interaction between the input resistance and capacitance and the feedback network. Larger source resistance at the noninverting input has a similar effect. The following voltage follower configurations are stable:

1028/1128 AI09
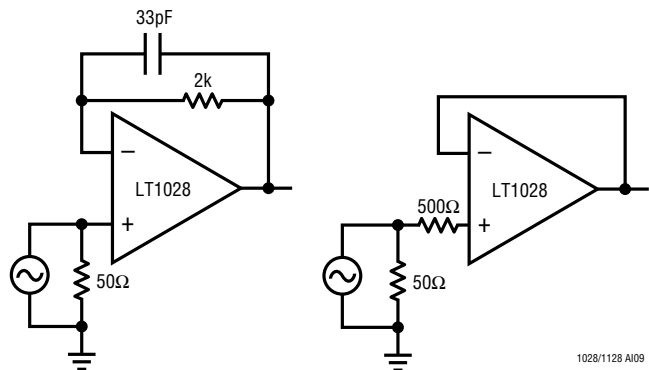
Another configuration which requires unity-gain stability is shown below. When C_F is large enough to effectively short the output to the input at 15MHz, oscillations can occur. The insertion of $R_{S2} \geq 500\Omega$ will prevent the LT1028 from oscillating. When $R_{S1} \geq 500\Omega$, the additional noise contribution due to the presence of R_{S2} will be minimal. When $R_{S1} \leq 100\Omega$, R_{S2} is not necessary, because R_{S1} represents a heavy load on the output through the C_F short. When $100\Omega < R_{S1} < 500\Omega$, R_{S2} should match R_{S1}. For example, $R_{S1} = R_{S2} = 300\Omega$ will be stable. The noise increase due to R_{S2} is 40%.

1028/1128 AI10
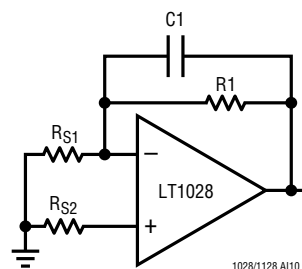
APPLICATIONS INFORMATION

If C_F is only used to cut noise bandwidth, a similar effect can be achieved using the over-compensation terminal.

The Gain, Phase plot also shows that phase margin is about 45° at gain of 10 (20dB). The following configura-

tion has a high (≈70%) overshoot without the 10pF capacitor because of additional phase shift caused by the feedback resistor – input capacitance pole. The presence of the 10pF capacitor cancels this pole and reduces overshoot to 5%.
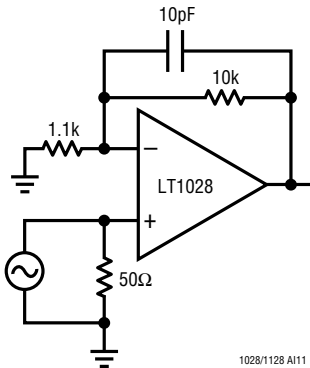
Over-Compensation

The LT1028/LT1128 are equipped with a frequency over-compensation terminal (pin 5). A capacitor connected between pin 5 and the output will reduce noise bandwidth. Details are shown on the Slew Rate, Gain-Bandwidth Product vs Over-Compensation Capacitor plot. An additional benefit is increased capacitive load handling capability.

1028/1128 AI11

TYPICAL APPLICATION

Strain Gauge Signal Conditioner with Bridge Excitation

THE LT1028's NOISE CONTRIBUTION IS NEGLIGIBLE COMPARED TO THE BRIDGE NOISE.
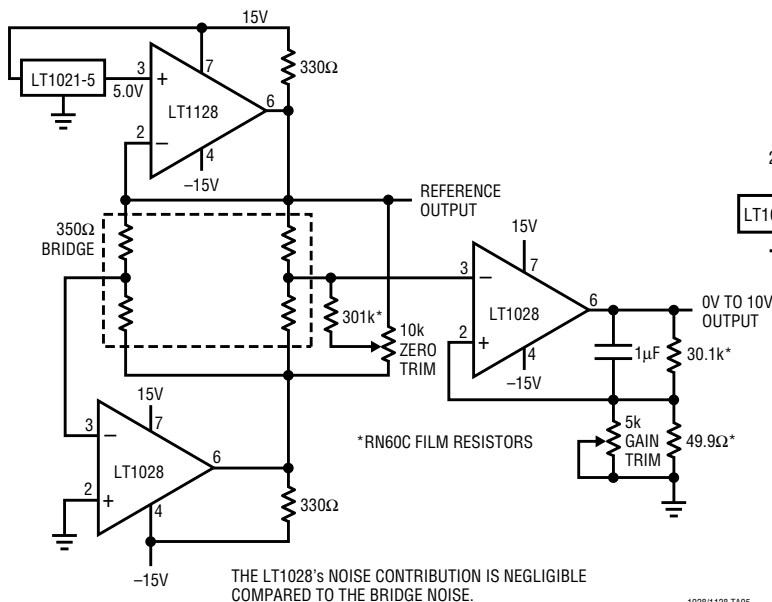
1028/1128 TA05

Low Noise Voltage Regulator
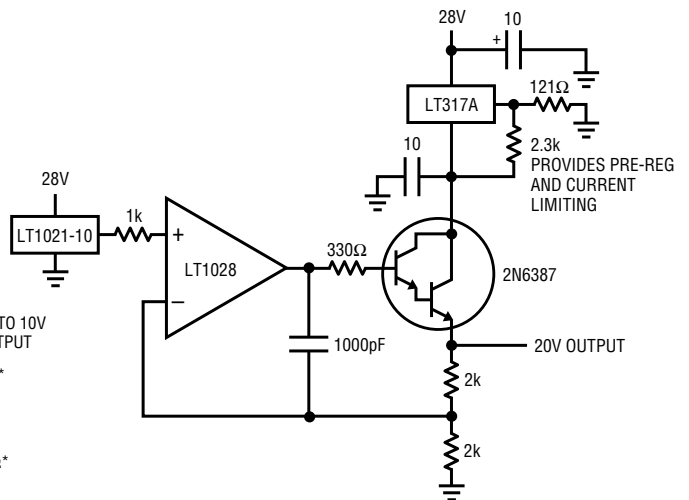
1028/1128 TA04

TYPICAL APPLICATION

Paralleling Amplifiers to Reduce Voltage Noise
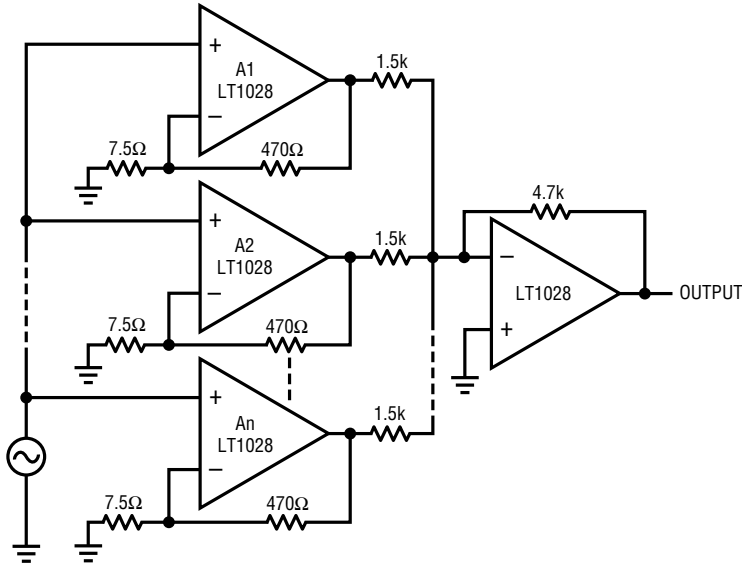
1. ASSUME VOLTAGE NOISE OF LT1028 AND 7.5 Ω SOURCE RESISTOR = 0.9nV/√Hz.
2. GAIN WITH n LT1028s IN PARALLEL = n × 200.
3. OUTPUT NOISE = √n × 200 × 0.9nV/√Hz.
4. INPUT REFERRED NOISE = $\frac{OUTPUT\ NOISE}{n \times 200}$ = $\frac{0.9}{\sqrt{n}}$nV/ √Hz.
5. NOISE CURRENT AT INPUT INCREASES √n TIMES.
6. IF n = 5, GAIN = 1000, BANDWIDTH = 1MHz, RMS NOISE, DC TO 1MHz = $\frac{2\mu V}{\sqrt{5}}$ = 0.9 μV.

1028/1128 TA03

Phono Preamplifier
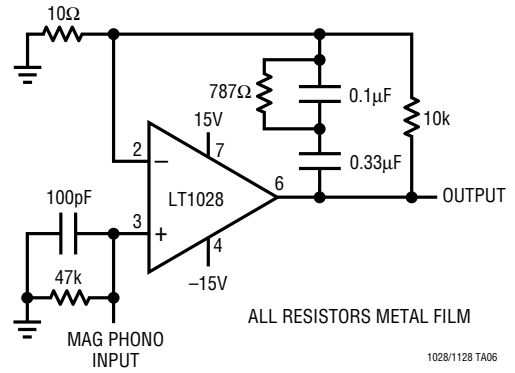
ALL RESISTORS METAL FILM

1028/1128 TA06

Tape Head Amplifier
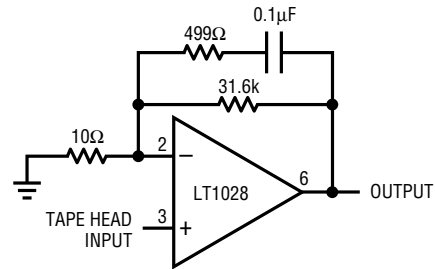
ALL RESISTORS METAL FILM

1028/1128 TA07

Low Noise, Wide Bandwidth Instrumentation Amplifier
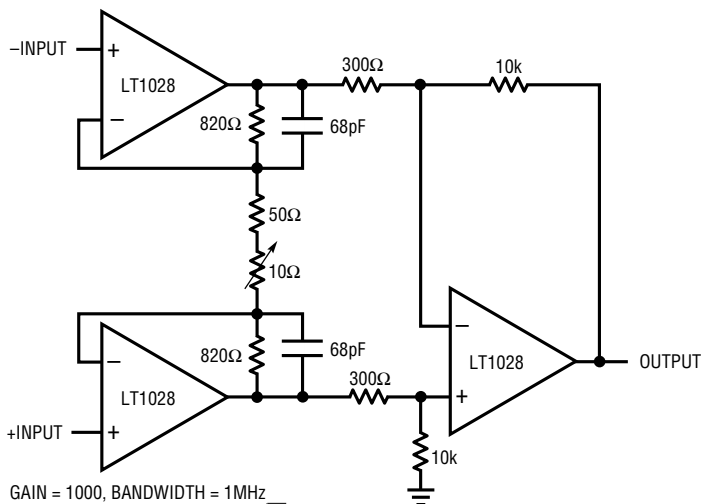
GAIN = 1000, BANDWIDTH = 1MHz
INPUT REFERRED NOISE = 1.5nV/√Hz AT 1kHz
WIDEBAND NOISE –DC to 1MHz = 3μV$_{RMS}$
IF BW LIMITED TO DC TO 100kHz = 0.55μV$_{RMS}$

1028/1128 TA08

Gyro Pick-Off Amplifier
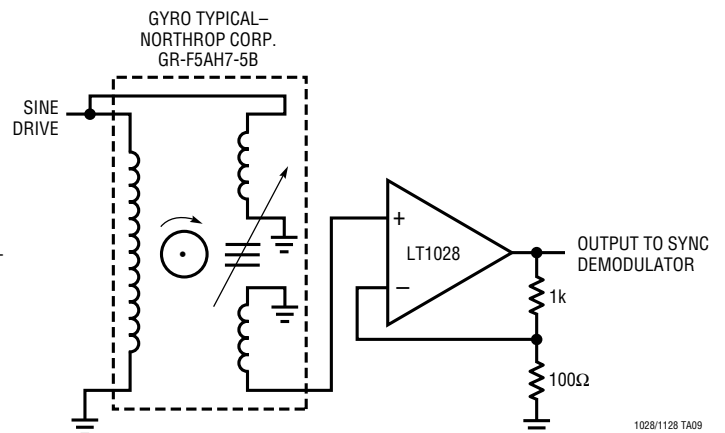
1028/1128 TA09

TYPICAL APPLICATION

Super Low Distortion Variable Sine Wave Oscillator

C1
0.047

R1
20Ω 2k

C2
0.047

20Ω
2k
R2

LT1028

$$1V_{RMS} \text{ OUTPUT}$$
1.5kHz TO 15kHz
$$\left(f = \frac{1}{2\,RC} \right)$$
WHERE R1C1 = R2C2

4.7k
15V
LT1004-1.2V

2.4k   5.6k

10pF

22k

15µF

2N4338   10k

560Ω   100k

20k

TRIM FOR
LOWEST
DISTORTION

LT1055

MOUNT 1N4148s
IN CLOSE PROXIMITY

10k

<0.0018% DISTORTION AND NOISE.
MEASUREMENT LIMITED BY RESOLUTION OF
HP339A DISTORTION ANALYZER

1028/1128 TA10

Chopper-Stabilized Amplifier

15V
1N758

3
2
LT1052
1
4
8
6

0.1   0.1

0.01

1N758
−15V

15V

100k

130Ω   68Ω   30k

INPUT

3
+
2
−
LT1028
1
7
4
8
6

OUTPUT

10k

10Ω

−15V

1028/1128 TA11

Low Noise Infrared Detector

5V

10Ω

1k

33Ω

100µF

100µF

OPTICAL
CHOPPER
WHEEL

267Ω

1000µF

IR
RADIATION

PHOTO-
ELECTRIC
PICK-OFF

INFRA RED ASSOCIATES, INC.
HgCdTe IR DETECTOR
13Ω AT 77°K

39Ω

5V

3
+
2
−
LT1028
7
4
6
8

−5V

10k

10Ω

SYNCHRONOUS
DEMODULATOR

10k*   10k*

1/4 LTC1043

13
14   12
16

5V

2
+
1
−
LM301A
7
4
8
6

−5V

30pF

1M

5V

2
+
3
−
LT1012
7
1
6
8

−5V

DC OUT

1028/1128 TA12
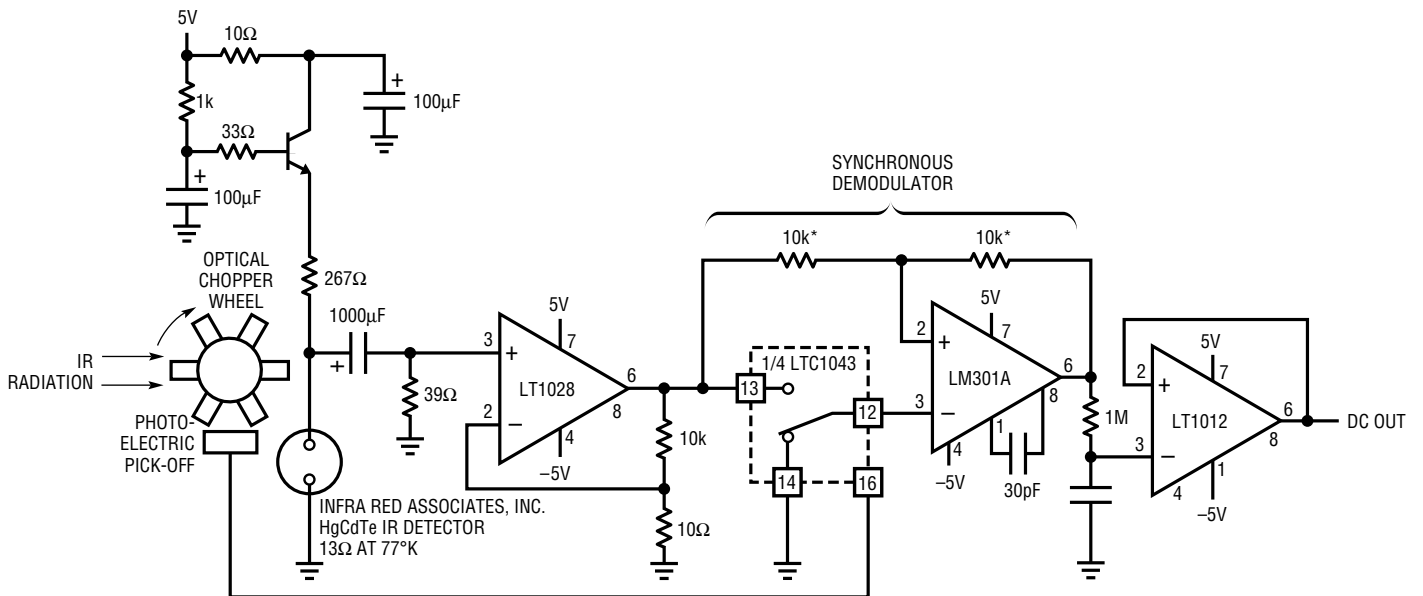
SCHEMATIC DIAGRAM
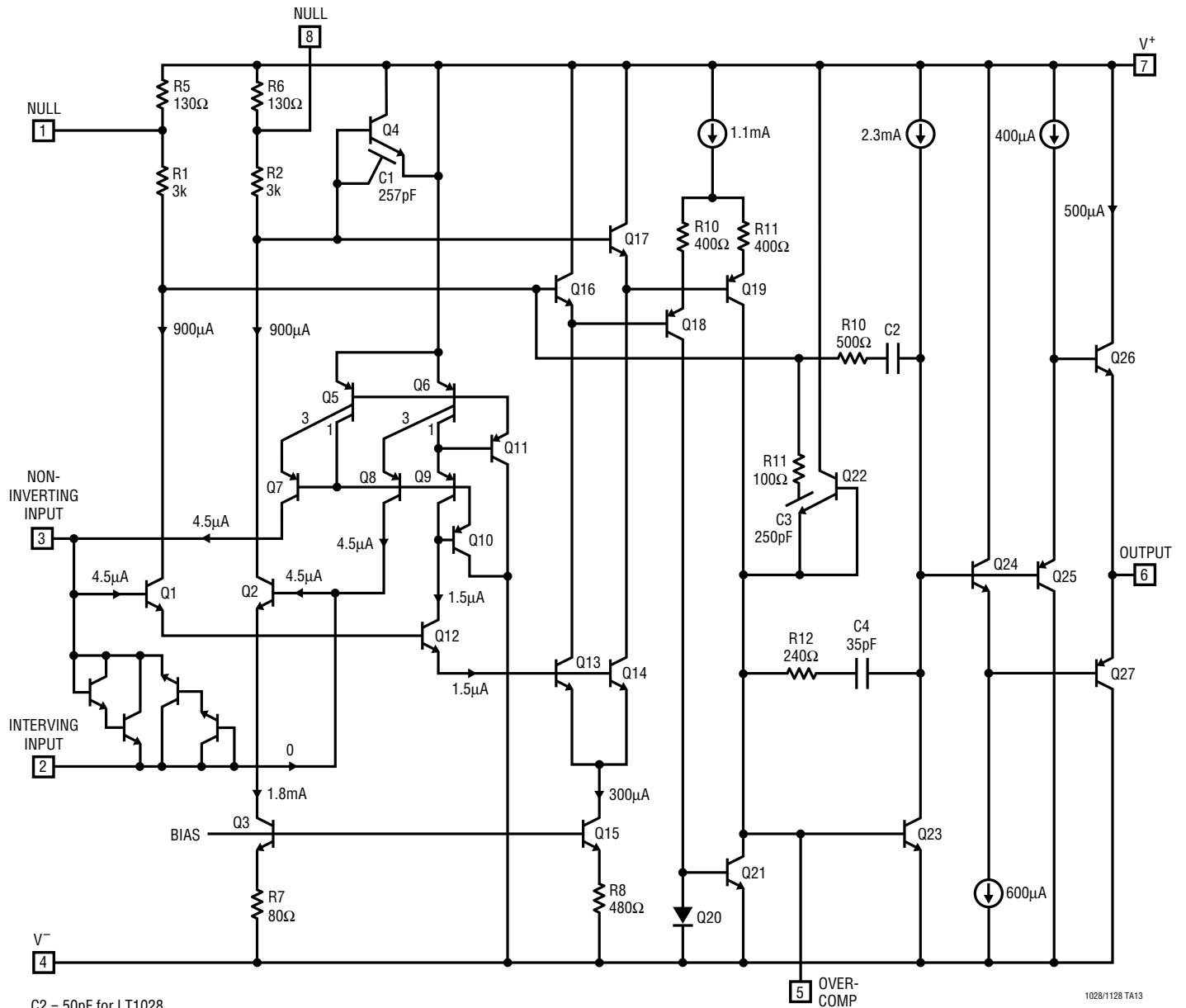
C2 = 50pF for LT1028
C2 = 275pF for LT1128

1028/1128 TA13

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

**J8 Package
8-Lead Ceramic DIP**

0.290 – 0.320
(7.366 – 8.128)

0.008 – 0.018
(0.203 – 0.460)

0° – 15°

0.385 ± 0.025
(9.779 ± 0.635)

0.200
(5.080)
MAX

0.015 – 0.060
(0.381 – 1.524)

0.125
3.175
MIN

0.038 – 0.068
(0.965 – 1.727)

0.014 – 0.026
(0.360 – 0.660)

0.100 ± 0.010
(2.540 ± 0.254)

0.405
(10.287)
MAX

0.005
(0.127)
MIN

0.025
(0.635)
RAD TYP

0.220 – 0.310
(5.588 – 7.874)

0.055
(1.397)
MAX

T_{JMAX}	θ_{JA}
165°C	100°C/W

**N8 Package
8-Lead Plastic DIP**

0.300 – 0.320
(7.620 – 8.128)

0.009 – 0.015
(0.229 – 0.381)

$0.325 \begin{smallmatrix} +0.025 \\ -0.015 \end{smallmatrix}$

$\left(8.255 \begin{smallmatrix} +0.635 \\ -0.381 \end{smallmatrix} \right)$

0.045 – 0.065
(1.143 – 1.651)

0.130 ± 0.005
(3.302 ± 0.127)

0.065
(1.651)
TYP

0.045 ± 0.015
(1.143 ± 0.381)

0.100 ± 0.010
(2.540 ± 0.254)

0.018 ± 0.003
(0.457 ± 0.076)

0.125
(3.175)
MIN

0.020
(0.508)
MIN

0.400
(10.160)
MAX

0.250 ± 0.010
(6.350 ± 0.254)

T_{JMAX}	θ_{JA}
130°C	130°C/W

**S8 Package
8-Lead Plastic SOIC**

0.010 – 0.020
(0.254 – 0.508) × 45°

0.008 – 0.010
(0.203 – 0.254)

0° – 8° TYP

0.016 – 0.050
0.406 – 1.270

0.053 – 0.069
(1.346 – 1.752)

0.004 – 0.010
(0.101 – 0.254)

0.014 – 0.019
(0.355 – 0.483)

0.050
(1.270)
BSC

0.189 – 0.197
(4.801 – 5.004)

0.228 – 0.244
(5.791 – 6.197)

0.150 – 0.157
(3.810 – 3.988)

T_{JMAX}	θ_{JA}
135°C	140°C/W

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

S Package
16-Lead Plastic SOL

0.291 – 0.299
(7.391 – 7.595)

0.005
(0.127)
RAD MIN

0.010 – 0.029
(0.254 – 0.737) × 45°

0° – 8° TYP

0.009 – 0.013
(0.229 – 0.330)

SEE NOTE

0.016 – 0.050
(0.406 – 1.270)

0.093 – 0.104
(2.362 – 2.642)

0.037 – 0.045
(0.940 – 1.143)

0.050
(1.270)
TYP

0.014 – 0.019
(0.356 – 0.482)
TYP

0.004 – 0.012
(0.102 – 0.305)

0.398 – 0.413
(10.109 – 10.490)

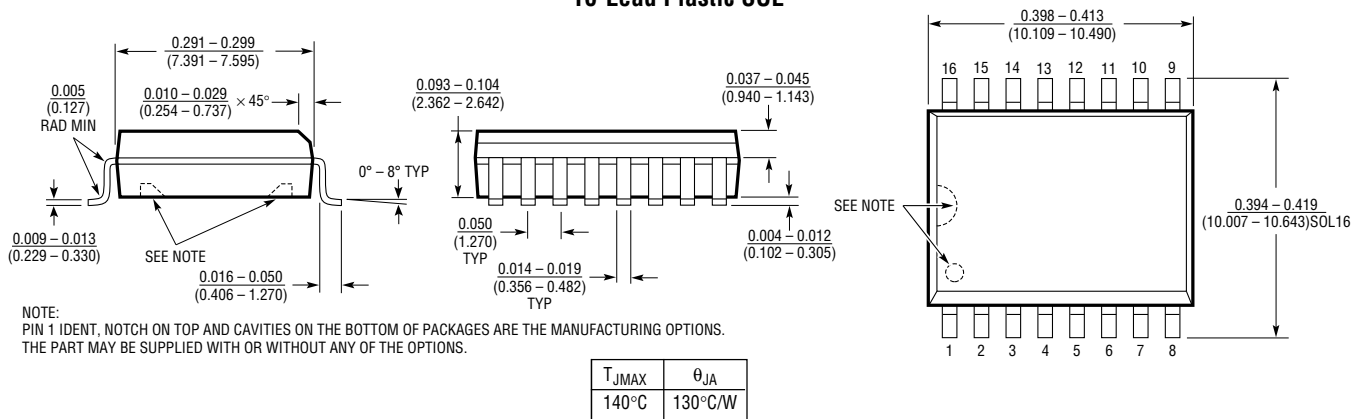16 15 14 13 12 11 10 9

SEE NOTE

0.394 – 0.419
(10.007 – 10.643)SOL16

1   2   3   4   5   6   7   8

NOTE:
PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS.
THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

T_{JMAX}	θ_{JA}
140°C	130°C/W

H Package
8-Lead TO-5 Metal Can

45°TYP

0.027 – 0.045
(0.686 – 1.143)

0.027 – 0.034
(0.686 – 0.864)

8   1
7   2
        3
6   4
    5

0.200 – 0.230
(5.080 – 5.842)
BSC

0.110 – 0.160
(2.794 – 4.064)
INSULATING
STANDOFF

NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN
THE REFERENCE PLANE AND SEATING PLANE.

0.335 – 0.370
(8.509 – 9.398)
DIA

0.305 – 0.335
(7.747 – 8.509)

0.040
(1.016)
MAX

SEATING
PLANE

0.010 – 0.045
(0.254 – 1.143)

0.050
(1.270)
MAX

0.016 – 0.021
(0.406 – 0.533)
TYP

GAUGE
PLANE

0.165 – 0.185
(4.191 – 4.699)

REFERENCE
PLANE

0.500 – 0.750
(12.70 – 19.05)

T_{JMAX}	θ_{JA}	θ_{JC}
175°C	140°C/W	40°C/W

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