Stereo, 24-Bit, 192 kHz Multibit ΣΔ DAC

AD1852*

FEATURES

5 V Stereo Audio DAC System
Accepts 16-Bit/18-Bit/20-Bit/24-Bit Data
Supports 24 Bits, 192 kHz Sample Rate
Accepts a Wide Range of Sample Rates Including: 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, and 192 kHz
Multibit Sigma-Delta Modulator with "Perfect Differential Linearity Restoration" for Reduced Idle Tones and Noise Floor
Data-Directed Scrambling DAC—Least Sensitive to Jitter
Differential Output for Optimum Performance
117 dB Signal-to-Noise (Not Muted) at 48 kHz Sample Rate (A-Weighted Mono)
114 dB Signal-to-Noise (Not Muted) at 48 kHz Sample Rate (A-Weighted Stereo)
117 dB Dynamic Range (Not Muted) at 48 kHz Sample Rate (A-Weighted Mono)
114 dB Dynamic Range (Not Muted) at 48 kHz Sample Rate (A-Weighted Stereo)
–105 dB THD+N (Mono Application Circuit)
–102 dB THD+N (Stereo)
115 dB Stopband Attenuation
On-Chip Clickless Volume Control
Hardware and Software Controllable Clickless Mute
Serial (SPI) Control for: Serial Mode, Number of Bits, Sample Rate, Volume, Mute, De-Emp
Digital De-Emphasis Processing for 32 kHz, 44.1 kHz, 48 kHz Sample Rates
Clock Autodivide Circuit Supports Five Master-Clock Frequencies
Flexible Serial Data Port with Right-Justified, Left-Justified, I²S-Compatible and DSP Serial Port Modes
28-Lead SSOP Plastic Package

APPLICATIONS

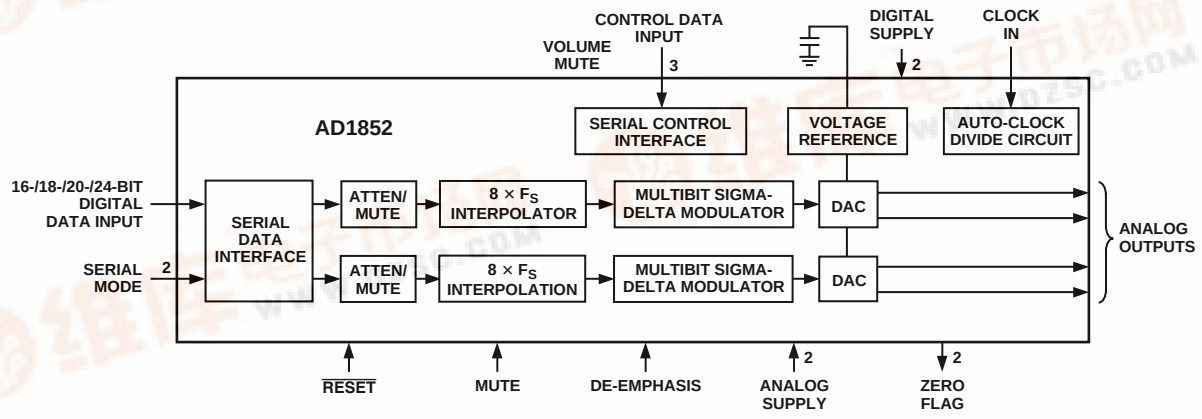
Hi End: DVD, CD, Home Theater Systems, Automotive Audio Systems, Sampling Musical Keyboards, Digital Mixing Consoles, Digital Audio Effects Processors

PRODUCT OVERVIEW

The AD1852 is a complete high performance single-chip stereo digital audio playback system. It is comprised of a multibit sigma-delta modulator, digital interpolation filters, and analog output drive circuitry. Other features include an on-chip stereo attenuator and mute, programmed through an SPI-compatible serial control port. The AD1852 is fully compatible with all known DVD formats including 192 kHz as well as 96 kHz sample frequencies and 24 bits. It also is backwards compatible by supporting 50 µs/15 µs digital de-emphasis intended for "Redbook" compact discs, as well as de-emphasis at 32 kHz and 48 kHz sample rate.

The AD1852 has a very simple but very flexible serial data input port that allows for glueless interconnection to a variety of ADCs, DSP chips, AES/EBU receivers and sample rate converters. The AD1852 can be configured in left-justified, I²S, right-justified, or DSP serial port compatible modes. It can support 16, 18, 20, and 24 bits in all modes. The AD1852 accepts serial audio data in MSB first, twos-complement format. The AD1852 operates from a single 5 V power supply. It is fabricated on a single monolithic integrated circuit and is housed in a 28-lead SSOP package for operation over the temperature range 0°C to 70°C.

FUNCTIONAL BLOCK DIAGRAM



*Patents Pending

REV. 0

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AD1852–SPECIFICATIONS

TEST CONDITIONS UNLESS OTHERWISE NOTED

Supply Voltages (AV_{DD}, DV_{DD})	5.0 V
Ambient Temperature	25°C
Input Clock	24.576 MHz (512 × F_S Mode)
Input Signal	996.11 Hz
	–0.5 dB Full Scale
Input Sample Rate	48 kHz
Measurement Bandwidth	20 Hz to 20 kHz
Word Width	20 Bits
Load Capacitance	100 pF
Load Impedance	47 kΩ
Input Voltage HI	2.4 V
Input Voltage LO	0.8 V

ANALOG PERFORMANCE (See Figures)

	Min	Typ	Max	Unit
Resolution		24		Bits
Signal-to-Noise Ratio (20 Hz to 20 kHz)				
No Filter (Stereo)		112		dB
(Mono—See Figure 29)		115		dB
With A-Weighted Filter (Stereo)		114		dB
(Mono—See Figure 29)		117		dB
Dynamic Range (20 Hz to 20 kHz, –60 dB Input)				
No Filter (Stereo)	107	112		dB
(Mono—See Figure 29)		115		dB
With A-Weighted Filter (Stereo)	110	114		dB
(Mono—See Figure 29)		117		dB
Total Harmonic Distortion + Noise (Stereo)	–94	–102		dB
		0.00079		%
Total Harmonic Distortion + Noise (Mono—See Figure 29)		–105		dB
		0.00056		%
Total Harmonic Distortion + Noise (Stereo) V_O = –20 dB		–92		dB
Total Harmonic Distortion + Noise (Stereo) V_O = –60 dB		–52		dB
Analog Outputs				
Differential Output Range (± Full Scale)		5.6		V p-p
Output Capacitance at Each Output Pin			2	pF
Out-of-Band Energy (0.5 × F_S to 100 kHz)			–90	dB
CMOUT		2.37		V
DC Accuracy				
Gain Error	–10	±2.0	+10	%
Interchannel Gain Mismatch	–0.15	±0.015	+0.15	dB
Gain Drift		150	250	ppm/°C
DC Offset		–50		mV
Interchannel Crosstalk (EIAJ Method)		–120		dB
Interchannel Phase Deviation		±0.1		Degrees
Mute Attenuation		–100		dB
De-Emphasis Gain Error			±0.1	dB

Performance of right and left channels are identical (exclusive of the Interchannel Gain Mismatch and Interchannel Phase Deviation specifications).
Specifications subject to change without notice.

DIGITAL I/O (0°C TO 70°C)

	Min	Typ	Max	Unit
Input Voltage HI (V_{IH})	2.2			V
Input Voltage LO (V_{IL})			0.8	V
Input Leakage (I_{IH} @ V_{IH} = 2.4 V)			10	µA
Input Leakage (I_{IL} @ V_{IL} = 0.8 V)			10	µA
High Level Output Voltage (V_{OH}) I_{OH} = 1 mA	2.0			V
Low Level Output Voltage (V_{OL}) I_{OL} = 1 mA			0.4	V
Input Capacitance			20	pF

Specifications subject to change without notice.

TEMPERATURE RANGE

	Min	Typ	Max	Unit
Specifications Guaranteed		25		°C
Functionality Guaranteed	0		70	°C
Storage	–55		+150	°C

Specifications subject to change without notice.

POWER

	Min	Typ	Max	Unit
Supplies				
Voltage, Analog and Digital	4.50	5	5.50	V
Analog Current		33	40	mA
Analog Current—$\overline{\text{RESET}}$		32	46	mA
Digital Current		20	30	mA
Digital Current—$\overline{\text{RESET}}$		27	37	
Dissipation				
Operation—Both Supplies		265		mW
Operation—Analog Supply		165		mW
Operation—Digital Supply		100		mW
Power Supply Rejection Ratio				
1 kHz 300 mV p-p Signal at Analog Supply Pins		–60		dB
20 kHz 300 mV p-p Signal at Analog Supply Pins		–50		dB

Specifications subject to change without notice.

DIGITAL FILTER CHARACTERISTICS

Sample Rate (kHz)	Passband (kHz)	Stopband (kHz)	Stopband Attenuation (dB)	Passband Ripple (dB)
44.1	DC–20	24.1–328.7	110	±0.0002
48	DC–21.8	26.23–358.28	110	±0.0002
96	DC–39.95	56.9–327.65	115	±0.0005
192	DC–87.2	117–327.65	95	+0/–0.04 (DC–21.8 kHz) +0/–0.5 (DC–65.4 kHz) +0/–1.5 (DC–87.2 kHz)

Specifications subject to change without notice.

GROUP DELAY

Chip Mode	Group Delay Calculation	F_S	Group Delay	Unit
INT8x Mode	$5553/(128 \times F_S)$	48 kHz	903.8	µs
INT4x Mode	$5601/(64 \times F_S)$	96 kHz	911.6	µs
INT2x Mode	$5659/(32 \times F_S)$	192 kHz	921	µs

Specifications subject to change without notice.

DIGITAL TIMING (Guaranteed Over 0°C to 70°C, AVDD = DVDD = +5.0 V ± 10%)

		Min	Unit
t_{DMP}	MCLK Period (FMCLK = 256 × FL/$\overline{\text{R}}$CLK)*	54	ns
t_{DML}	MCLK LO Pulsewidth (All Modes)	$0.4 \times t_{DMP}$	ns
t_{DMH}	MCLK HI Pulsewidth (All Modes)	$0.4 \times t_{DMP}$	ns
t_{DBH}	BCLK HI Pulsewidth	20	ns
t_{DBL}	BCLK LO Pulsewidth	20	ns
t_{DBP}	BCLK Period	60	ns
t_{DLS}	L/$\overline{\text{R}}$CLK Setup	20	ns
t_{DLH}	L/$\overline{\text{R}}$CLK Hold (DSP Serial Port Mode Only)	5	ns
t_{DDS}	SDATA Setup	5	ns
t_{DDH}	SDATA Hold	10	ns
t_{RSTL}	RST LO Pulsewidth	15	ns

*Higher MCLK frequencies are allowable when using the on-chip Master Clock Autodivide Feature.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

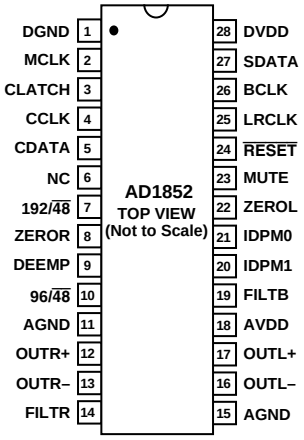
	Min	Max	Unit
DV_{DD} to DGND	–0.3	6	V
AV_{DD} to AGND	–0.3	6	V
Digital Inputs	DGND – 0.3	DV_{DD} + 0.3	V
Analog Outputs	AGND – 0.3	AV_{DD} + 0.3	V
AGND to DGND	–0.3	0.3	V
Reference Voltage		$(AV_{DD} + 0.3)/2$	V
Soldering		300	°C
		10	sec

*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE CHARACTERISTICS

	Min	Typ	Max	Unit
θ_{JA} (Thermal Resistance [Junction-to-Ambient])		109		°C/W
θ_{JC} (Thermal Resistance [Junction-to-Case])		39		°C/W

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature	Package Description	Package Option
AD1852JRS	0°C to 70°C	28-Lead Shrink Small Outline Package (SSOP)	RS-28
AD1852JRSRL	0°C to 70°C	28-Lead Shrink Small Outline Package (SSOP)	RS-28 on 13" Reels

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1852 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin	Input/Output	Pin Name	Description
1	I	DGND	Digital Ground.
2	I	MCLK	Master Clock Input. Connect to an external clock source at either 256 F_S, 384 F_S, 512 F_S, 768 F_S, or 1024 F_S.
3	I	CLATCH	Latch Input for Control Data. This input is rising-edge sensitive.
4	I	CCLK	Control Clock Input for Control Data. Control input data must be valid on the rising edge of CCLK. CCLK may be continuous or gated.
5	I	CDATA	Serial Control Input, MSB first, containing 16 bits of unsigned data per channel. Used for specifying channel-specific attenuation and mute.
6		NC	No Connect.
7	I	192/$\overline{48}$	Selects 48 kHz (LO) or 192 kHz Sample Frequency.
8	O	ZEROR	Right Channel Zero Flag Output. This pin goes HI when Right Channel has no signal input for more than 1024 LR Clock Cycles.
9	I	DEEMP	De-Emphasis. Digital de-emphasis is enabled when this input signal is HI. This is used to impose a 50 µs/15 µs response characteristic on the output audio spectrum at an assumed 44.1 kHz sample rate. Curves for 32 kHz and 48 kHz sample rates may be selected via SPI control register.
10	I	96/$\overline{48}$	Selects 48 kHz (LO) or 96 kHz Sample Frequency.
11, 15	I	AGND	Analog Ground.
12	O	OUTR+	Right Channel Positive Line Level Analog Output.
13	O	OUTR–	Right Channel Negative Line Level Analog Output.
14	O	FILTR	Voltage Reference Filter Capacitor Connection. Bypass and decouple the voltage reference with parallel 10 µF and 0.1 µF capacitors to the AGND.
16	O	OUTL–	Left Channel Negative Line Level Analog Output.
17	O	OUTL+	Left Channel Positive Line Level Analog Output.
18	I	AVDD	Analog Power Supply. Connect to Analog 5 V Supply.
19		FILTB	Filter Capacitor Connection. Connect 10 µF capacitor to AGND (Pin 15).
20	I	IDPM1	Input Serial Data Port Mode Control One. With IDPM0, defines 1 of 4 serial modes.
21	I	IDPM0	Input Serial Data Port Mode Control Zero. With IDPM1, defines 1 of 4 serial modes.
22	O	ZEROL	Left Channel Zero Flag Output. This pin goes HI when Left Channel has no signal input for more than 1024 LR Clock Cycles.
23	I	MUTE	Mute. Assert HI to mute both stereo analog outputs. Deassert LO for normal operation.
24	I	$\overline{\text{RESET}}$	Reset. The AD1852 is reset on the rising edge of this signal. The serial control port registers are reset to the default values. Connect HI for normal operation.
25	I	L/$\overline{\text{R}}$CLK	Left/$\overline{\text{Right}}$ Clock Input for Input Data. Must run continuously.
26	I	BCLK	Bit Clock Input for Input Data. Need not run continuously; may be gated or used in a burst fashion.
27	I	SDATA	Serial Input, MSB first, containing two channels of 16, 18, 20, and 24 bits of twos complement data per channel.
28	I	DVDD	Digital Power Supply Connect to digital 5 V supply.

Table I. Serial Data Input Mode

IDPM1 (Pin 20)	IDPM0 (Pin 21)	Serial Data Input Format
0	0	Right-Justified
0	1	I^2S-Compatible
1	0	Left-Justified
1	1	DSP

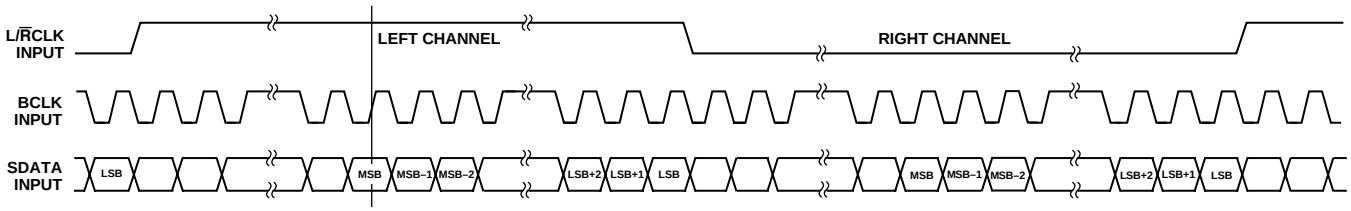


Figure 1. Right-Justified Mode

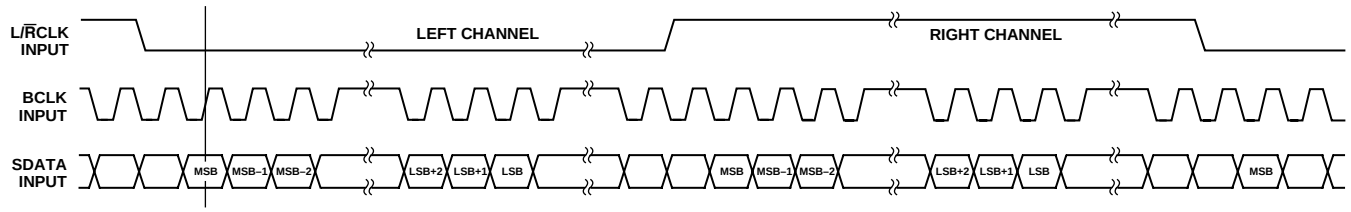


Figure 2. I²S-Justified Mode

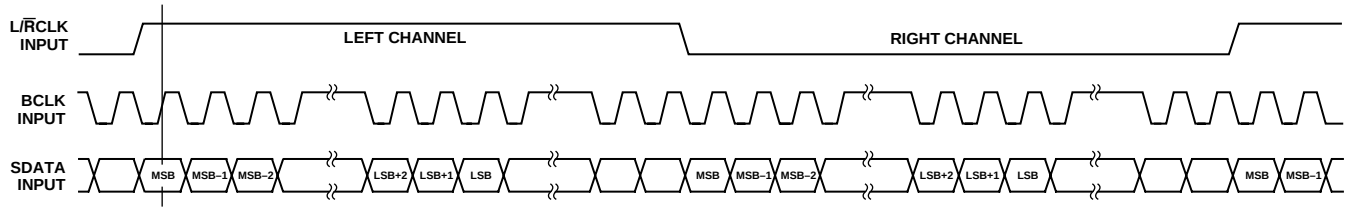


Figure 3. Left-Justified Mode

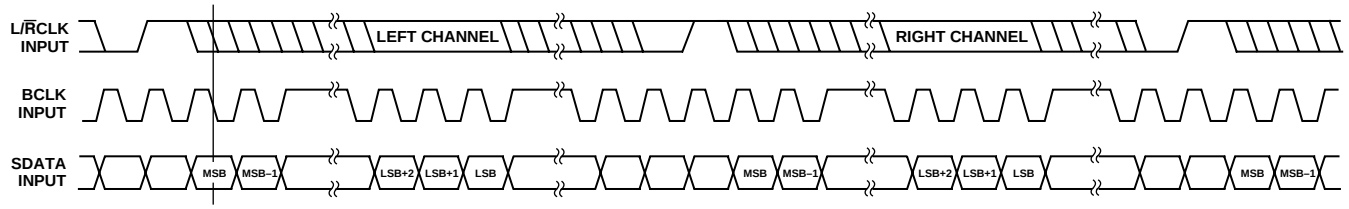


Figure 4. Left-Justified DSP Mode

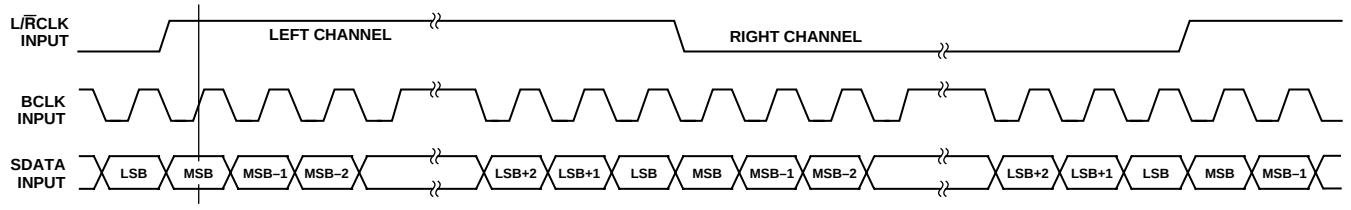


Figure 5. 32 × F_S Packed Mode

OPERATING FEATURES

Serial Data Input Port

The AD1852's flexible serial data input port accepts data in twos-complement, MSB-first format. The left channel data field always precedes the right channel data field. The serial mode is set by using either the external mode pins (IDPM0 Pin 21 and IDPM1 Pin 20) or the mode select bits (Bits 4 and 5) in the SPI control register. To control the serial mode using the external mode pins, the SPI mode select bits should be set to zero (default at power-up). To control the serial mode using the SPI mode select bits, the external mode control pins should be grounded.

In all modes except for the right-justified mode, the serial port will accept an arbitrary number of bits up to a limit of 24. Extra bits will not cause an error, but they will be truncated internally. In the right-justified mode, control register Bits 8 and 9 are used to set the wordlength to 16 bits, 20 bits, or 24 bits. The default on power- up is 24-bit mode. When the SPI Control Port is not being used, the SPI pins (3, 4, and 5) should be tied LO.

Serial Data Input Mode

The AD1852 uses two multiplexed input pins to control the mode configuration of the input data port mode. See Table I.

Figure 1 shows the right-justified mode (16 bits shown). L/$\overline{R}$CLK is HI for the left channel, LO for the right channel. Data is valid on the rising edge of BCLK.

In normal operation, there are 64-bit clocks per frame (or 32 per half-frame). When the SPI wordlength control bits (Bits 8 and 9 in the control register) are set to 24 bits (0:0), the serial port will begin to accept data starting at the eighth bit clock pulse after the L/$\overline{R}$CLK transition. When the wordlength control bits are set to 20-bit mode, data is accepted starting at the twelfth-bit clock position. In 16-bit mode, data is accepted starting at the sixteenth-bit clock position. These delays are independent of the number of bit clocks per frame, and therefore other data formats are possible using the delay values described above. For detailed timing, see Figure 6.

Figure 2 shows the I^{2}S mode. L/$\overline{R}$CLK is LO for the left channel and HI for the right channel. Data is valid on the rising edge of BCLK. The MSB is left-justified to an L/$\overline{R}$CLK transition but with a single BCLK period delay. The I^{2}S mode can be used to accept any number of bits up to 24.

Figure 3 shows the left-justified mode. L/$\overline{R}$CLK is HI for the left channel, and LO for the right channel. Data is valid on the rising edge of BCLK. The MSB is left-justified to an L/$\overline{R}$CLK transition, with no MSB delay. The left-justified mode can accept any wordlength up to 24 bits, and any number of bit clocks from two times the word length to 64 bit clocks per frame.

Figure 4 shows the DSP serial port mode. L/$\overline{R}$CLK must pulse HI for at least one bit clock period before the MSB of the left channel is valid, and L/$\overline{R}$CLK must pulse HI again for at least one bit clock period before the MSB of the right channel is valid. Data is valid on the falling edge of BCLK. The DSP serial port mode can be used with any wordlength up to 24 bits.

In this mode, it is the responsibility of the DSP to ensure that the left data is transmitted with the first L/$\overline{R}$CLK pulse, and that synchronism is maintained from that point forward.

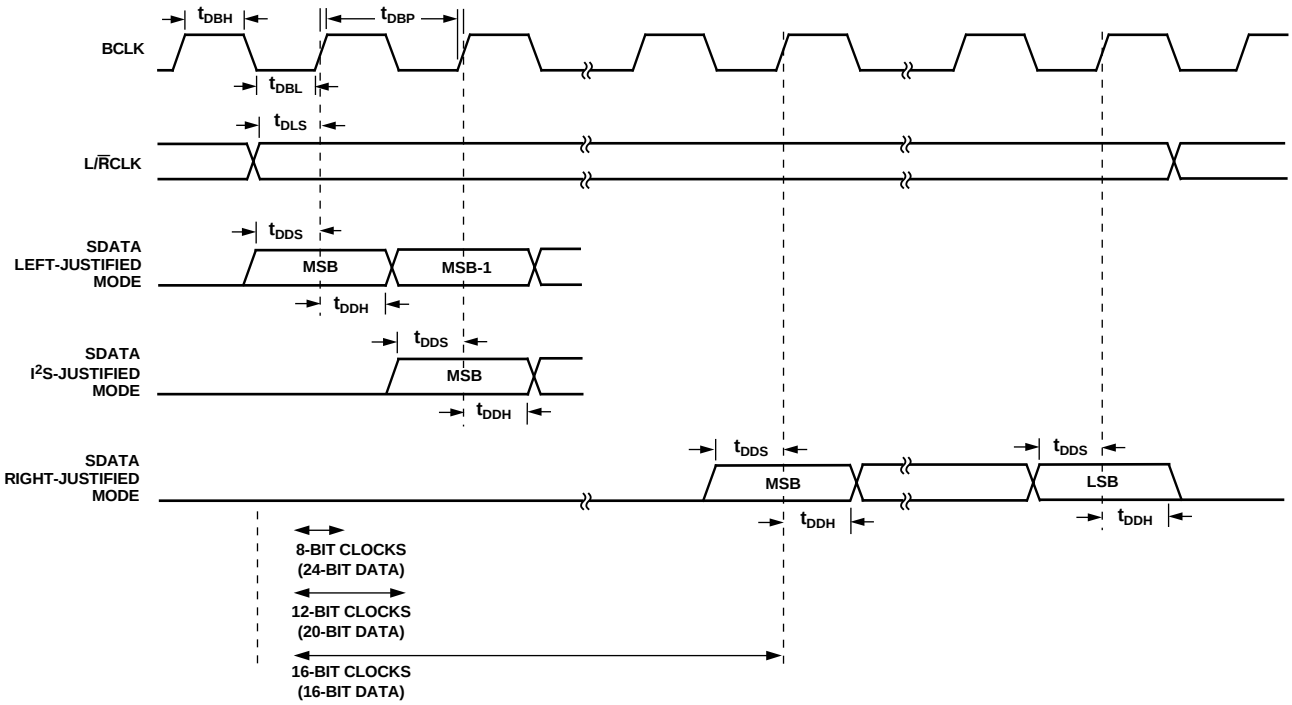


Figure 6. Serial Data Port Timing

Table II.

Chip Mode	Allowable Master Clock Frequencies	Nominal Input Sample Rate	Internal Sigma-Delta Clock Rate
INT8× Mode	$256 \times F_S$, $384 \times F_S$, $512 \times F_S$, $768 \times F_S$, $1024 \times F_S$	48 kHz	$128 \times F_S$
INT4× Mode	$128 \times F_S$, $192 \times F_S$, $256 \times F_S$, $384 \times F_S$, $512 \times F_S$	96 kHz	$64 \times F_S$
INT2× Mode	$64 \times F_S$, $96 \times F_S$, $128 \times F_S$, $192 \times F_S$, $256 \times F_S$	192 kHz	$32 \times F_S$

Note that the AD1852 is capable of a $32 \times F_S$ BCLK frequency "packed mode" where the MSB is left-justified to an L/$\overline{R}$CLK transition, and the LSB is right-justified to the opposite L/$\overline{R}$CLK transition. L/$\overline{R}$CLK is HI for the left channel, and LO for the right channel. Data is valid on the rising edge of BLCK. Packed mode can be used when the AD1852 is programmed in right-justified or left-justified mode. Packed mode is shown is Figure 5.

Master Clock Autodivide Feature

The AD1852 has a circuit that autodetects the relationship between master clock and the incoming serial data, and internally sets the correct divide ratio to run the interpolator and modulator. The allowable frequencies for each mode are shown above. Master clock should be synchronized with L/$\overline{R}$CLK but phase relation between master clock and L/$\overline{R}$CLK is not critical.

SPI REGISTER DEFINITIONS

The SPI port allows flexible control of many chip parameters. It is organized around three registers; a LEFT-CHANNEL VOLUME register, a RIGHT-CHANNEL VOLUME register, and a CONTROL register. Each WRITE operation to the AD1852 SPI control port requires 16 bits of serial data in MSB-first format. The bottom two bits are used to select one of three registers, and the top 14 bits are then written to that register. This allows a write to one of the three registers in a single 16-bit transaction.

The SPI CCLK signal is used to clock in the data. The incoming data should change on the falling edge of this signal. At the end of the 16 CCLK periods, the CLATCH signal should rise to clock the data internally into the AD1852.

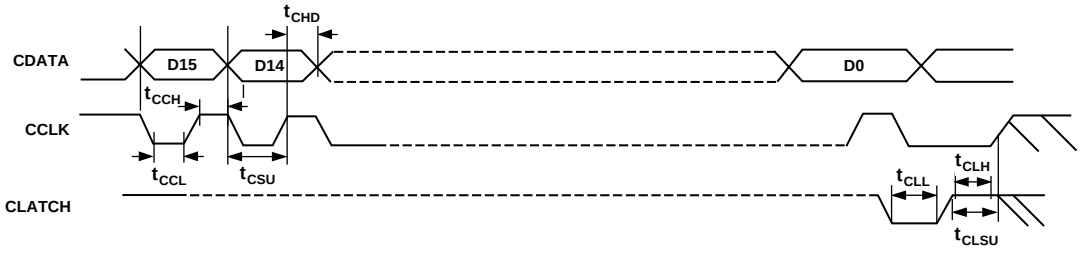


Figure 7. Serial Control Port Timing

Table III. SPI Digital Timing

		Min	Unit
t_{CCH}	CCLK HI Pulsewidth	40	ns
t_{CCL}	CCLK LOW Pulsewidth	40	ns
t_{CSU}	CDATA Setup Time	10	ns
t_{CHD}	CDATA Hold Time	10	ns
t_{CLL}	CLATCH LOW Pulsewidth	10	ns
t_{CLH}	CLATCH HI Pulsewidth	10	ns
t_{CLSU}	CLATCH Setup Time	$4 \times t_{MCLK}$	ns

Register Addresses
The lowest two bits of the 16-bit input word are decoded as follows to set the register that the upper 14 bits will written into.

VOLUME LEFT AND VOLUME RIGHT REGISTERS
A write operation to the left or right volume registers will activate the "autoramp" clickless volume control feature of the AD1852. This feature works as follows. The upper 10 bits of the volume control word will be incremented or decremented by 1 at a rate equal to the input sample rate. The bottom four bits are not fed into the autoramp circuit and thus take effect immediately. This arrangement gives a worst-case ramp time of about 20 ms for step changes of more than 60 dB, which has been determined by listening tests to be optimal in terms of preventing the perception of a "click" sound on large volume changes. See Figure 8 for a graphical description of how the volume changes as a function of time.

The 14-bit volume control word is used to multiply the signal, and therefore the control characteristic is linear, not dB. A constant dB/step characteristic can be obtained by using a lookup table in the microprocessor that is writing to the SPI port. The volume word is unsigned (i.e., 0 dB is 11 1111 1111 1111).

Table IV.

Bit 1	Bit 0	Register
0	0	Volume Left
1	0	Volume Right
0	1	Control Register

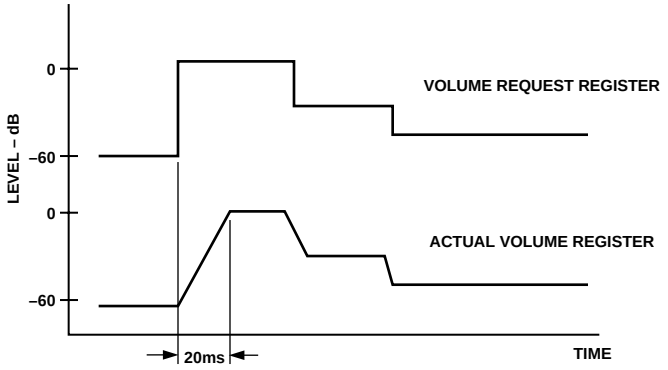


Figure 8. Smooth Volume Control

SPI Timing
The SPI port is a 3-wire interface with serial data (CDATA), serial bit clock (CCLK), and data latch (CLATCH). The data is clocked into an internal shift register on the rising edge of CCLK. The serial data should change on the falling edge of CCLK and be stable on the rising edge of CCLK. The rising edge of CLATCH is used internally to latch the parallel data from the serial-to-parallel converter. This rising edge should be aligned with the falling edge of the last CCLK pulse in the 16-bit frame. The CCLK can run continuously between transactions.

Note that the serial control port timing is asynchronous to the serial data port timing. Changes made to the attenuator level will be updated on the next edge of the L/$\overline{R}$CLK after the CLATCH write pulse as shown in Figure 7.

Mute
The AD1852 offers two methods of muting the analog output. By asserting the MUTE (Pin 23) signal HI, both the left and right channel are muted. As an alternative, the user can assert the mute bit in the serial control register (data11) HI. The AD1852 has been designed to minimize pops and clicks when muting and unmuting the device by automatically "ramping" the gain up or down. When the device is unmuted, the volume returns to the value set in the volume register.

Table V.

Bit 11	Bit 10	Bit 9:8	Bit 7	Bit 6	Bit 5:4	Bit 3:2
INT2× Mode OR'd with Pin 7 (192/$\overline{48}$). Default = 0	INT4× Mode OR'd with Pin 10 (96/$\overline{48}$). Default = 0	Number of Bits in Right-Justified Serial Mode. 0:0 = 24 0:1 = 20 1:0 = 16 Default = 0:0	Reset. Default = 0	Soft Mute OR'd with Pin. Default = 0	Serial Mode OR'd with Mode Pins. IDPM1:IDPM0 0:0 Right-Justified 0:1 I^2S 1:0 Left-Justified 1:1 DSP Mode Default = 0:0	De-Emphasis Filter Select. 0:0 No Filter 0:1 44.1 kHz Filter 1:0 32 kHz Filter 1:1 48 kHz Filter Default = 0:0

Control Register
Table V shows the functions of the control register. The control register is addressed by having an '01' in the bottom two bits of the 16-bit SPI word. The top 14 bits are then used for the control register.

De-Emphasis
The AD1852 has a built-in de-emphasis filter that can be used to decode CDs that have been encoded with the standard "redbook" 50 µs/15 µs emphasis response curve. Three curves are available; one each for 32 kHz, 44.1 kHz, and 48 kHz sampling rates. The external "DEEMP" pin (Pin 9) turns on the 44.1 kHz de-emphasis filter. The other filters may be selected by writing to Control Bits 2 and 3 in the control register. If the SPI port is used to control the de-emphasis filter, the external DEEMP pin should be tied LO.

Output Impedance
The output impedance of the AD1852 is 65 Ω ± 30%.

Reset
The AD1852 may be reset either by a dedicated hardware pin ($\overline{\text{RESET}}$, Pin 24) or by software, via the SPI control port. While reset is active, normal operation of the AD1852 is suspended and the outputs assume midscale values. The AD1852 should always be reset at power up. The $\overline{\text{RESET}}$ function should be active for a minimum of 64 master clock periods. When the $\overline{\text{RESET}}$ function becomes inactive, normal operation will continue after a delay equal to the group delay plus three MCLK periods.

Using the $\overline{\text{RESET}}$ pin, the internal registers will be set to their default values, when the $\overline{\text{RESET}}$ pin is active low. Default operation will then be enabled when the $\overline{\text{RESET}}$ pin is raised. Alternatively, the internal registers can be reset to their default values by setting Bit 7, of the internal control register, high. When Bit 7 is reset low, default operation will continue. The software reset differs from the hardware reset because the soft reset does not affect the values stored in the SPI registers.

Control Signals
The IDPM0 and IDPM1 control inputs are normally connected HI or LO to establish the operating state of the AD1852. They can be changed dynamically (and asynchronously to L/$\overline{\text{R}}$CLK and the master clock), but it is possible that a click or pop sound may result during the transition from one serial mode to another. If possible, the AD1852 should be placed in mute before such a change is made.

Figures 9–14 show the calculated frequency response of the digital interpolation filters. Figures 15–26 show the performance of the AD1852 as measured by an Audio Precision System 2 Cascade. For the wideband plots, the noise floor shown in the plots is higher than the actual noise floor of the AD1852. This is caused by the higher noise floor of the "High Bandwidth" ADC used in the Audio Precision measurement system. The two-tone test shown in Figure 17 is per the SMPTE standard for measuring Intermodulation Distortion.

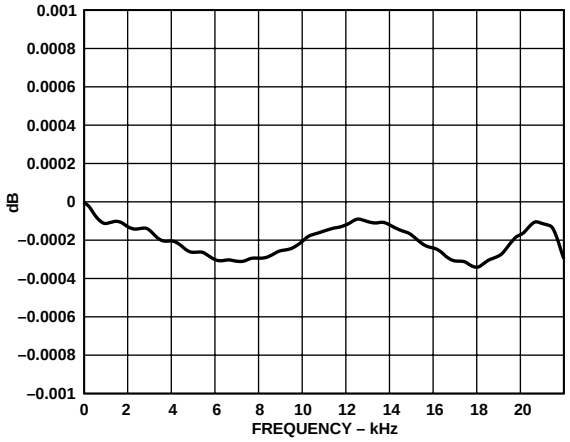


Figure 9. Passband Response 8× Mode, 48 kHz Sample Rate

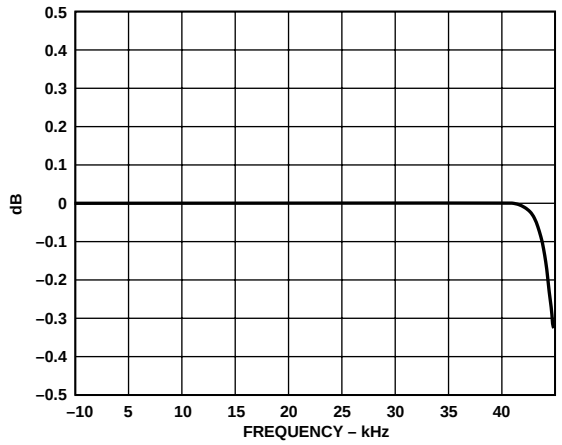


Figure 10. 44 kHz Passband Response 4× Mode, 96 kHz Sample Rate

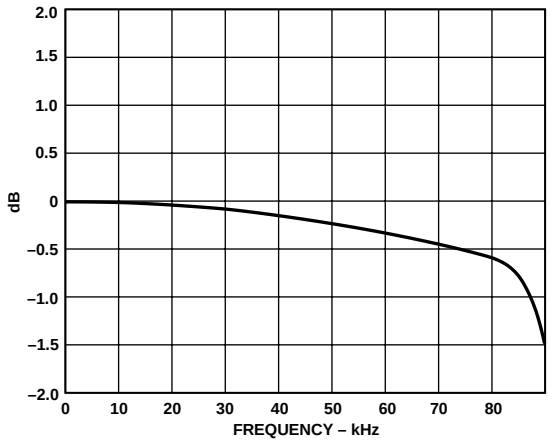


Figure 11. 88 kHz Passband Response 2× Mode, 192 kHz Sample Rate

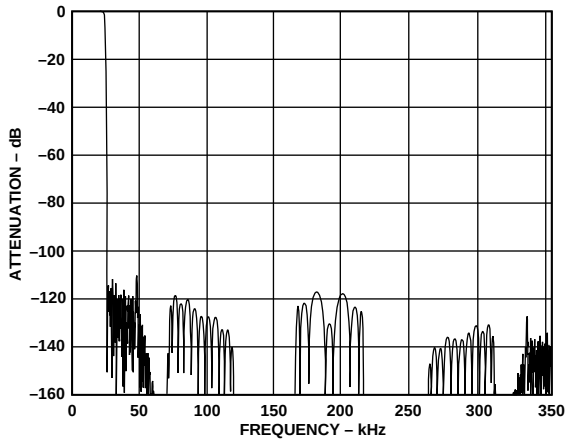


Figure 12. Complete Response, 8× Mode, 48 kHz Sample Rate

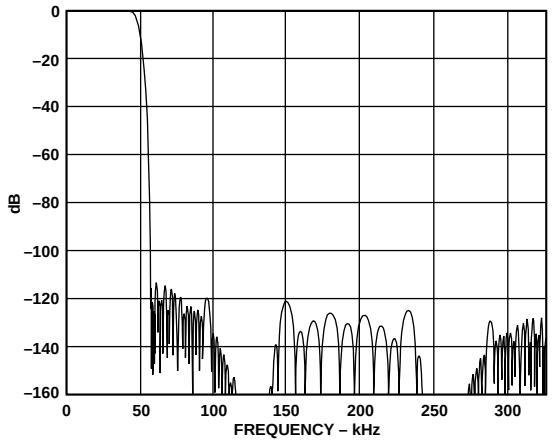


Figure 13. Complete Response, 4× Mode, 96 kHz Sample Rate

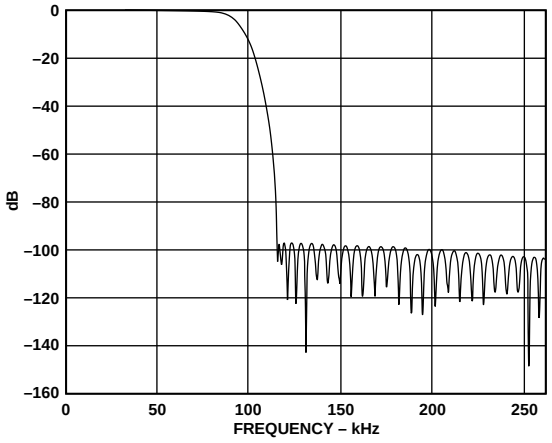


Figure 14. Complete Response, 2× Mode, 192 kHz Sample Rate

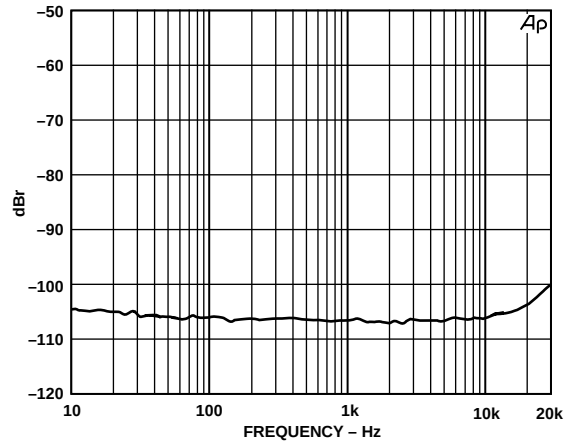


Figure 15. THD vs. Frequency Input @ –3 dBFS, SR 48 kHz

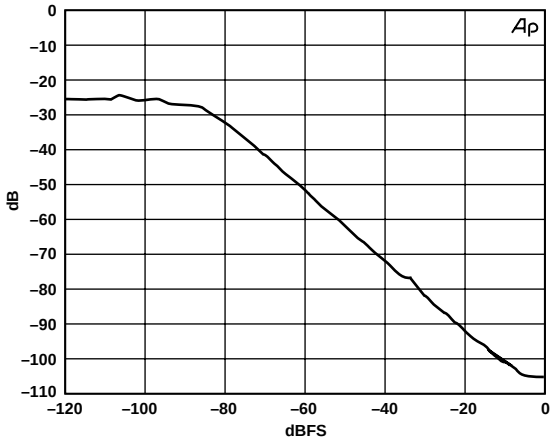


Figure 18. THD + N Ratio vs. Amplitude Input 1 kHz, SR 48 kS/s, 24-Bit

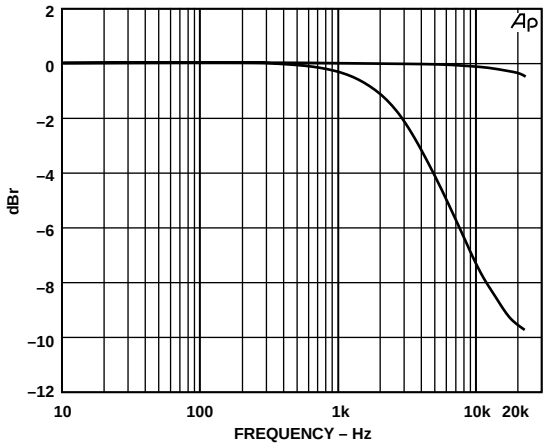


Figure 16. Normal De-Emphasis Frequency Response Input @ –10 dBFS, SR 48 kHz

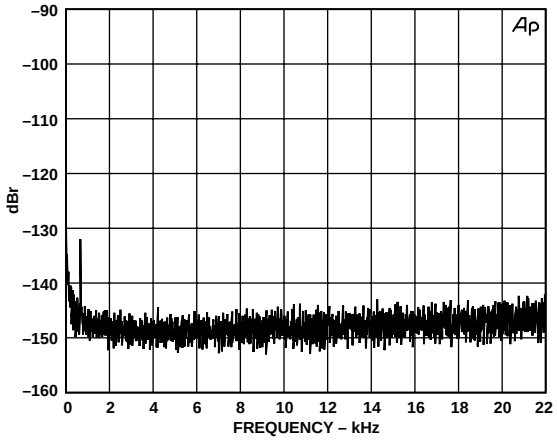


Figure 19. Noise Floor for Zero Input, SR 48 kHz

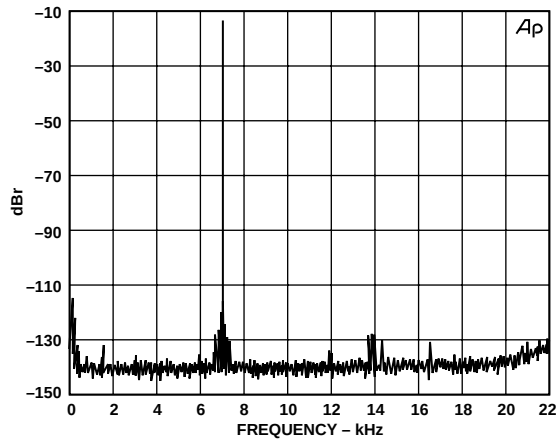


Figure 17. SMPTE/DIN 4:1 IMD 60 Hz/7 kHz @ 0 dBFS

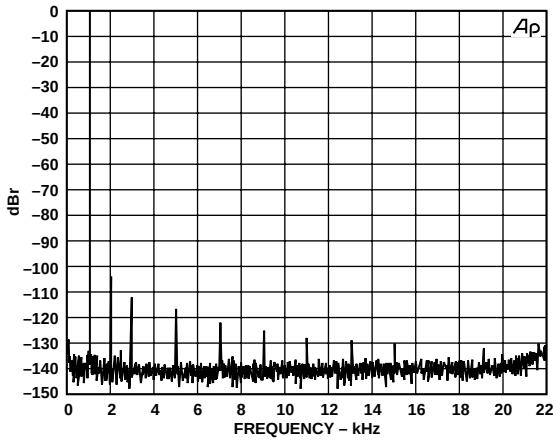


Figure 20. Input 0 dBFS @ 1 kHz, BW 10 Hz to 22 kHz, SR 48 kHz

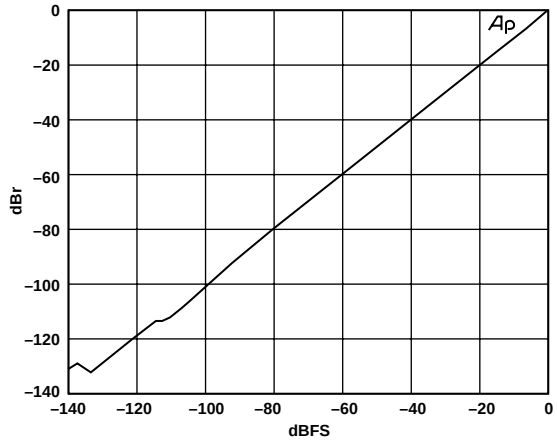


Figure 21. Linearity vs. Amplitude Input 200 Hz, SR 48 kS/s, 24-Bit Word

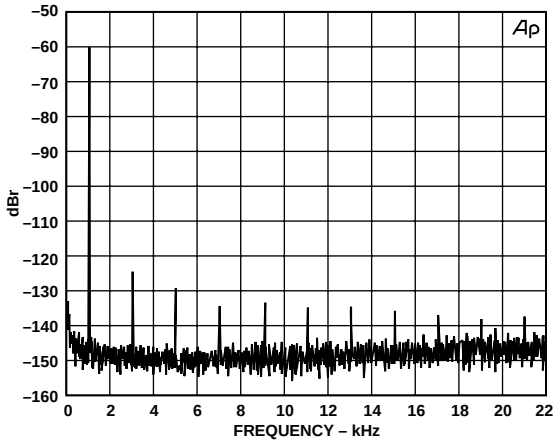


Figure 24. Dynamic Range for 1 kHz @ –60 dBFS, Triangular Dithered Input

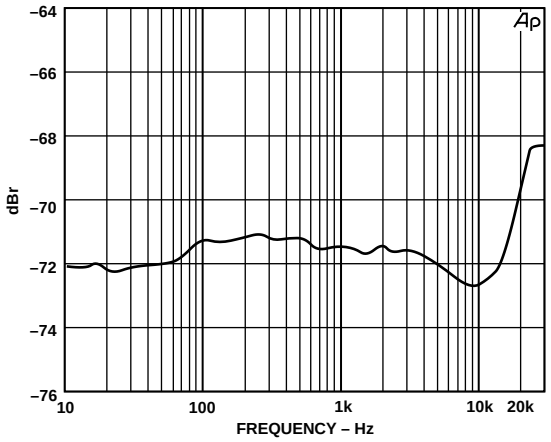


Figure 22. Power Supply Rejection vs. Frequency AV_{DD} 5 V DC + 100 mV p-p AC

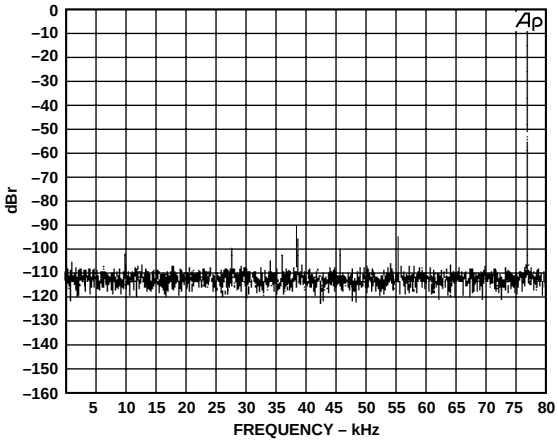


Figure 25. Wideband Plot, 75 kHz Input, 2× Interpolation, SR 192 kHz

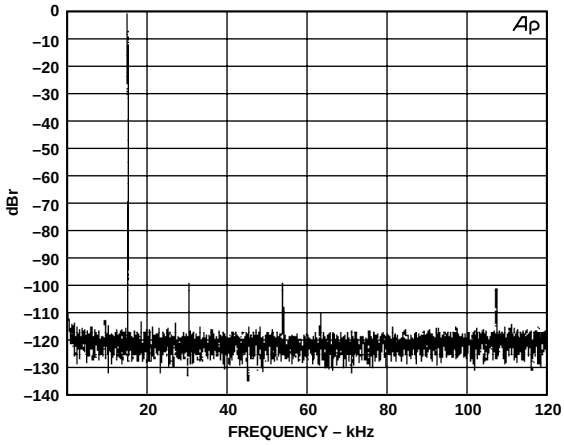


Figure 23. Wideband Plot, 15 kHz Input, 8× Interpolation, SR 48 kHz

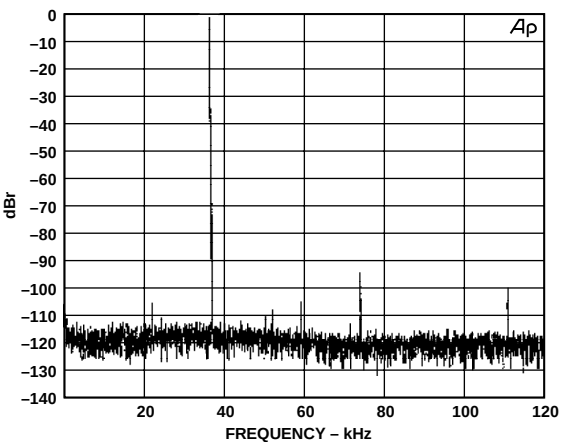


Figure 26. Wideband Plot, 37 kHz Input, 4× Interpolation, SR 96 kHz

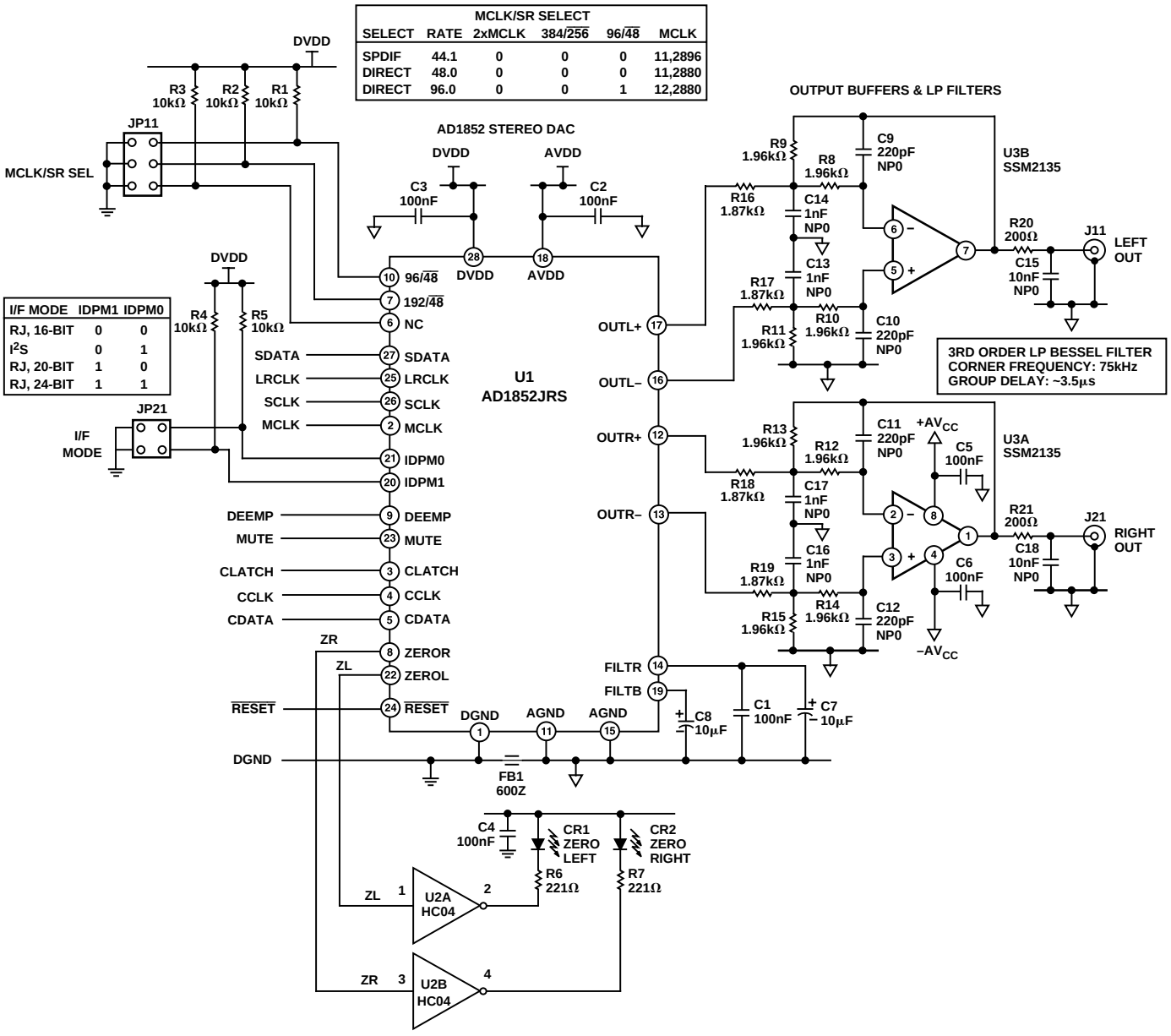


Figure 27. AD1852 DAC, Output Buffers, and LP Filters

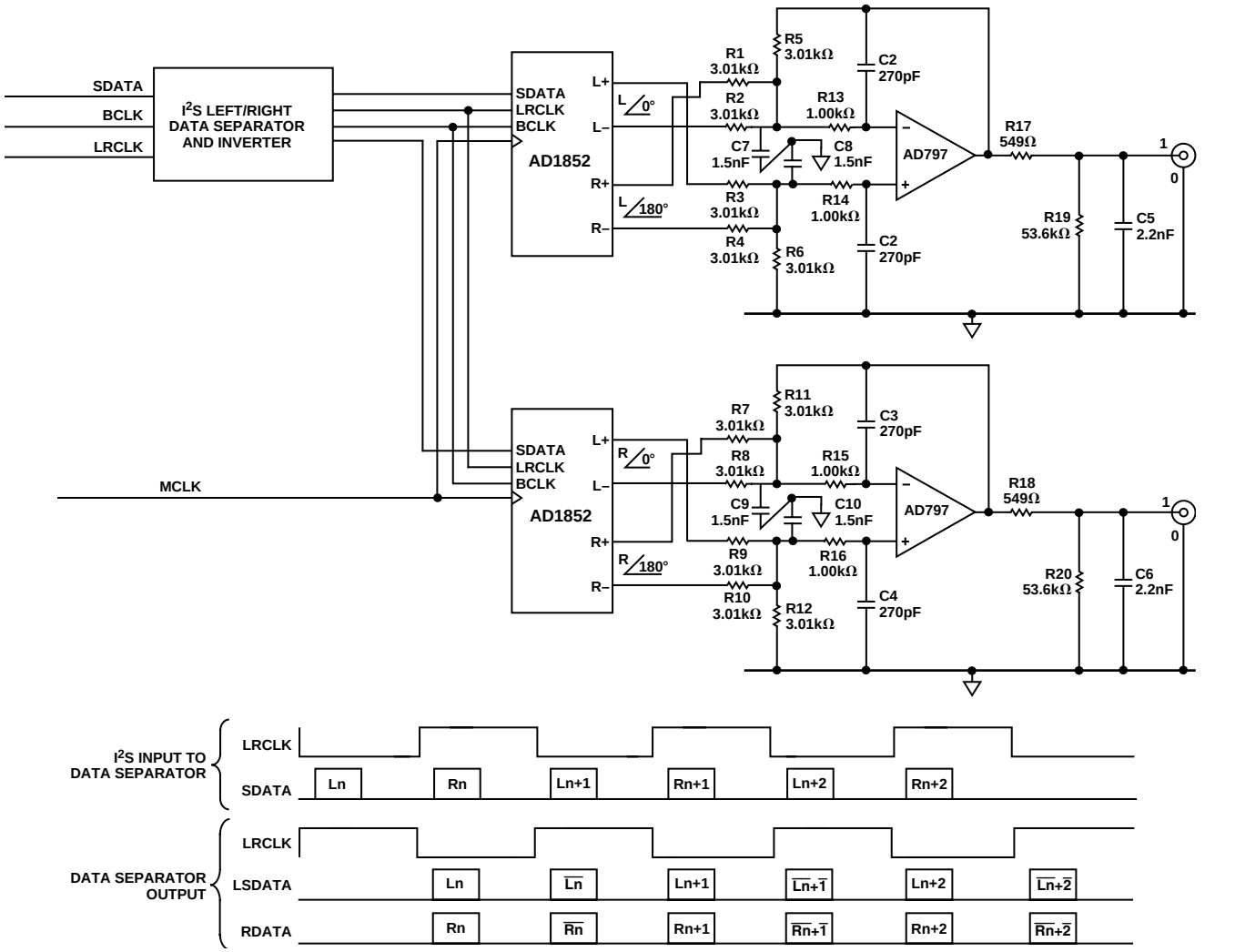
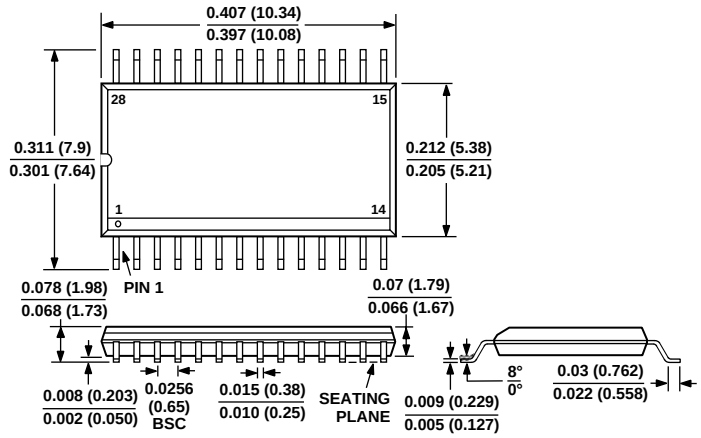


Figure 28. Mono Application Circuit

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead Shrink Small Outline Package (SSOP)
(RS-28)



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