



# Dual 8-Bit, 60 MSPS A/D Converter

## AD9059

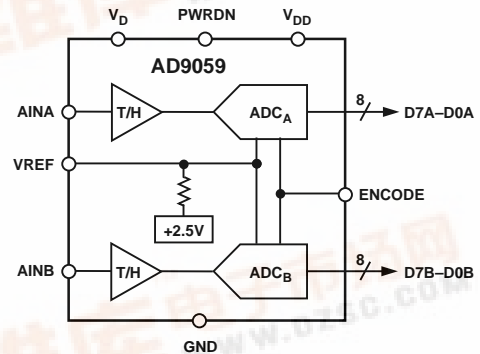
### FEATURES

- Dual 8-Bit ADCs on a Single Chip
- Low Power: 400 mW Typical
- On-Chip +2.5 V Reference and T/Hs
- 1 V p-p Analog Input Range
- Single +5 V Supply Operation
- +5 V or +3 V Logic Interface
- 120 MHz Analog Bandwidth
- Power-Down Mode: < 12 mW

### APPLICATIONS

- Digital Communications (QAM Demodulators)
- RGB & YC/Composite Video Processing
- Digital Data Storage Read Channels
- Medical Imaging
- Digital Instrumentation

### FUNCTIONAL BLOCK DIAGRAM



### PRODUCT DESCRIPTION

The AD9059 is a dual 8-bit monolithic analog-to-digital converter optimized for low cost, low power, small size, and ease of use. With a 60 MSPS encode rate capability and full-power analog bandwidth of 120 MHz typical, the component is ideal for applications requiring multiple ADCs with excellent dynamic performance.

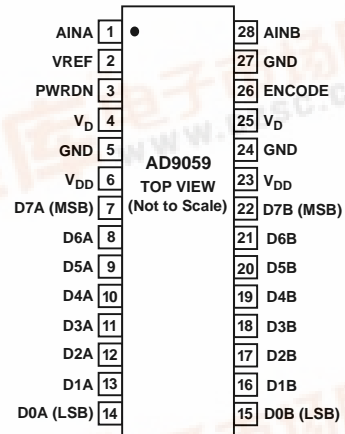
To minimize system cost and power dissipation, the AD9059 includes an internal +2.5 V reference and dual track-and-hold circuits. The ADC requires only a +5 V power supply and an encode clock. No external reference or driver components are required for many applications.

The AD9059's single encode input is TTL/CMOS compatible and simultaneously controls both internal ADC channels. The parallel 8-bit digital outputs can be operated from +5 V or +3 V supplies. A power-down function may be exercised to bring total consumption to < 12 mW when ADC data is not required for lengthy periods of time. In power-down mode the digital outputs are driven to a high impedance state.

Fabricated on an advanced BiCMOS process, the AD9059 is available in a space saving 28-lead surface mount plastic package (28 SSOP) and is specified over the industrial (-40°C to +85°C) temperature range.

Customers desiring single channel digitization may consider the AD9057, a single 8-bit, 60 MSPS monolithic based on the AD9059 ADC core. The AD9057 is available in a 20-lead surface mount plastic package (20 SSOP) and is specified over the industrial temperature range.

### PIN CONFIGURATION



REV. 0

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# AD9059–SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS ( $V_D = +5\text{ V}$ , $V_{DD} = +3\text{ V}$ ; external reference; ENCODE = 60 MSPS unless otherwise noted)

Parameter	Temp	Test Level	AD9059BRS			Units
			Min	Typ	Max	
RESOLUTION			8			Bits
DC ACCURACY						
Differential Nonlinearity	+25°C	I		0.75	2.0	LSB
	Full	VI			2.5	LSB
Integral Nonlinearity	+25°C	I		0.75	2.0	LSB
	Full	VI			2.5	LSB
No Missing Codes	Full	VI	GUARANTEED			
Gain Error <sup>1</sup>	+25°C	I	-6	-2.5	+6	% FS
	Full	VI	-8		+8	% FS
Gain Tempco <sup>1</sup>	Full	V		±70		ppm/°C
ANALOG INPUT						
Input Voltage Range (Centered at +2.5 V)	+25°C	V		1.0		V p-p
Input Offset Voltage	+25°C	I	-15	0	+15	mV
	Full	VI	-25		+25	mV
Input Resistance	+25°C	V		150		kΩ
Input Capacitance	+25°C	V		2		pF
Input Bias Current	+25°C	I		6	16	μA
Analog Bandwidth	+25°C	V		120		MHz
CHANNEL MATCHING (A to B)						
Gain Delta	+25°C	V		±1		% FS
Input Offset Voltage Delta	+25°C	V		±4		mV
BANDGAP REFERENCE						
Output Voltage	Full	VI	2.4	2.5	2.6	V
Temperature Coefficient	Full	V		±10		ppm/°C
SWITCHING PERFORMANCE						
Maximum Conversion Rate	Full	VI	60			MSPS
Minimum Conversion Rate	Full	IV			5	MSPS
Aperture Delay ( $t_A$ )	+25°C	V		2.7		ns
Aperture Uncertainty (Jitter)	+25°C	V		5		ps, rms
Output Valid Time ( $t_V$ ) <sup>2</sup>	Full	IV	4.0	6.6		ns
Output Propagation Delay ( $t_{PD}$ ) <sup>2</sup>	Full	IV		9.5	14.2	ns
DYNAMIC PERFORMANCE <sup>3</sup>						
Transient Response	+25°C	V		9		ns
Overshoot Recovery Time	+25°C	V		9		ns
Signal-to-Noise Ratio (SINAD) (with Harmonics)						
$f_{IN} = 10.3\text{ MHz}$	+25°C	I	40	44.5		dB
$f_{IN} = 76\text{ MHz}$	+25°C	V		43.5		dB
Effective Number of Bits						
$f_{IN} = 10.3\text{ MHz}$	+25°C	I	6.35	7.1		Bits
$f_{IN} = 76\text{ MHz}$	+25°C	V		6.9		Bits
Signal-to-Noise Ratio (SNR) (Without Harmonics)						
$f_{IN} = 10.3\text{ MHz}$	+25°C	I	42	46		dB
$f_{IN} = 76\text{ MHz}$	+25°C	V		45		dB
2nd Harmonic Distortion						
$f_{IN} = 10.3\text{ MHz}$	+25°C	I	-50	-62		dBc
$f_{IN} = 76\text{ MHz}$	+25°C	V		-54		dBc
3rd Harmonic Distortion						
$f_{IN} = 10.3\text{ MHz}$	+25°C	I	-46	-60		dBc
$f_{IN} = 76\text{ MHz}$	+25°C	V		-54		dBc
Two-Tone Intermodulation Distortion (IMD)	+25°C	V		-52		dBc
Channel Crosstalk Rejection	+25°C	V		-50		dBc
Differential Phase	+25°C	V		0.8		Degrees
Differential Gain	+25°C	V		1.0		%

Parameter	Temp	Test Level	AD9059BRS			Units
			Min	Typ	Max	
<b>DIGITAL INPUTS</b>						
Logic "1" Voltage	Full	VI	2.0			V
Logic "0" Voltage	Full	VI			0.8	V
Logic "1" Current	Full	VI			±1	µA
Logic "0" Current	Full	VI			±1	µA
Input Capacitance	+25°C	V		4.5		pF
Encode Pulse Width High ( $t_{EH}$ )	+25°C	IV	6.7		166	ns
Encode Pulse Width Low ( $t_{EL}$ )	+25°C	IV	6.7		166	ns
<b>DIGITAL OUTPUTS</b>						
Logic "1" Voltage ( $V_{DD} = +3$ V)	Full	VI	2.95			V
Logic "1" Voltage ( $V_{DD} = +5$ V)	Full	IV	4.95			V
Logic "0" Voltage ( $V_{DD} = +3$ V or +5 V)	Full	VI			0.05	V
Output Coding			Offset Binary Code			
<b>POWER SUPPLY</b>						
$V_D$ Supply Current ( $V_D = +5$ V)	Full	VI		72	92	mA
$V_{DD}$ Supply Current ( $V_{DD} = +3$ V) <sup>4</sup>	Full	VI		13	15	mA
Power Dissipation <sup>5,6</sup>	Full	VI		400	505	mW
Power-Down Dissipation	Full	VI		6	12	mW
Power Supply Rejection Ratio (PSRR)	+25°C	I			15	mV/V

## NOTES

<sup>1</sup>Gain error and gain temperature coefficient are based on the ADC only (with a fixed +2.5 V external reference).

<sup>2</sup> $t_V$  and  $t_{PD}$  are measured from the 1.5 V level of the ENCODE to the 10%/90% levels of the digital output swing. The digital output load during test is not to exceed an ac load of 10 pF or a dc current of ±40 µA.

<sup>3</sup>SNR/harmonics based on an analog input voltage of -0.5 dBFS referenced to a 1.0 V full-scale input range.

<sup>4</sup>Digital supply current based on  $V_{DD} = +3$  V output drive with <10 pF loading under dynamic test conditions.

<sup>5</sup>Power dissipation is based on 60 MSPS encode and 10.3 MHz analog input dynamic test conditions ( $V_D = +5$  V ± 5%,  $V_{DD} = +3$  V ± 5%).

<sup>6</sup>Typical thermal impedance for the RS style (SSOP) 28-pin package:  $\theta_{JC} = 39^\circ\text{C}/\text{W}$ ,  $\theta_{CA} = 70^\circ\text{C}/\text{W}$ ,  $\theta_{JA} = 109^\circ\text{C}/\text{W}$ .

Specifications subject to change without notice.

## EXPLANATION OF TEST LEVELS

## Test Level

- I - 100% production tested.
- II - 100% production tested at +25°C and sample tested at specified temperatures.
- III - Sample tested only.
- IV - Parameter is guaranteed by design and characterization testing.
- V - Parameter is a typical value only.
- VI - 100% production tested at +25°C; guaranteed by design and characterization testing for industrial temperature range.

## ABSOLUTE MAXIMUM RATINGS\*

$V_D, V_{DD}$	.....+7 V
Analog Inputs	..... -0.5 V to $V_D + 0.5$ V
Digital Inputs	..... -0.5 V to $V_D + 0.5$ V
$V_{REF}$ Input	..... -0.5 V to $V_D + 0.5$ V
Digital Output Current	..... 20 mA
Operating Temperature	..... -55°C to +125°C
Storage Temperature	..... -65°C to +150°C

\*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## ORDERING GUIDE

Model	Temperature Range	Package Option
AD9059BRS	-40°C to +85°C	RS-28
AD9059/PCB	+25°C	Evaluation Board

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9059 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# AD9059

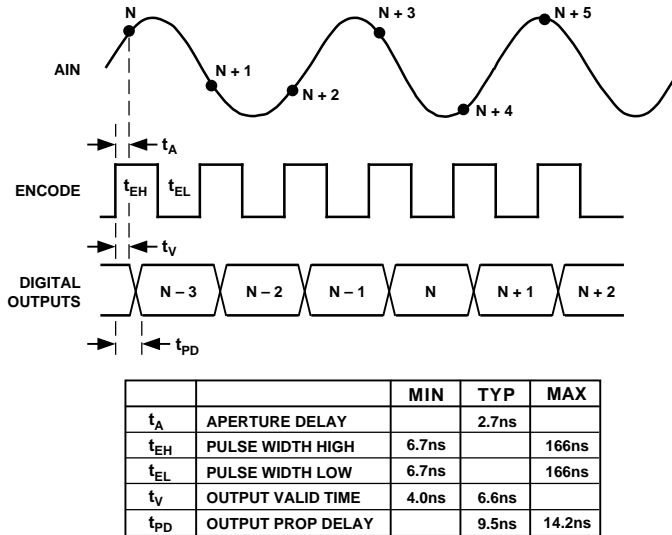
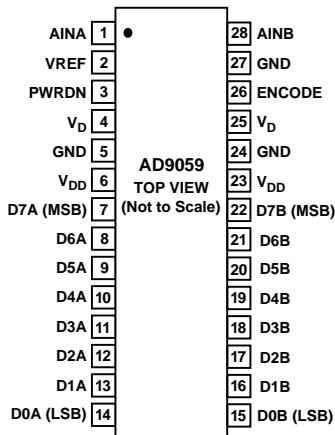


Figure 1. Timing Diagram

## PIN CONFIGURATION



## PIN DESCRIPTIONS

Pin No.	Name	Function
1, 28	AINA, AINB	Analog Inputs for ADC A and B.
2	VREF	Internal Voltage Reference (+2.5 V Typical); Bypass with 0.1 $\mu$ F to Ground or Overdrive with External Voltage Reference.
3	PWRDN	Power-Down Function Select; Logic HIGH for Power-Down Mode (Digital Outputs Go to High-Impedance State).
4, 25	$V_D$	Analog +5 V Power Supply.
5, 24, 27	GND	Ground.
6, 23	$V_{DD}$	Digital Output Power Supply. Nominally +3 V to +5 V.
7-14	D7A-D0A	Digital Outputs of ADCA.
22-15	D7B-D0B	Digital Outputs of ADCB.
26	ENCODE	Encode Clock for ADCs A and B (ADCs Sample Simultaneously On the Rising Edge of ENCODE).

Table I. Digital Coding ( $V_{REF} = +2.5$  V)

Analog Input	Voltage Level	Digital Output
3.0 V	Positive Full Scale	1111 1111
2.502 V	Midscale + 1/2 LSB	1000 0000
2.498 V	Midscale - 1/2 LSB	0111 1111
2.0 V	Negative Full Scale	0000 0000

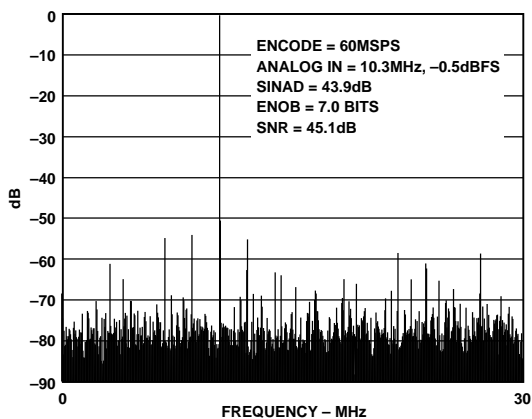


Figure 2. FFT Spectral Plot 60 MSPS, 10.3 MHz

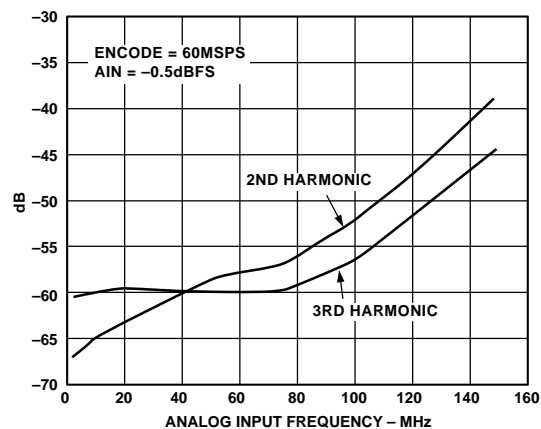


Figure 5. Harmonic Distortion vs. AIN Frequency

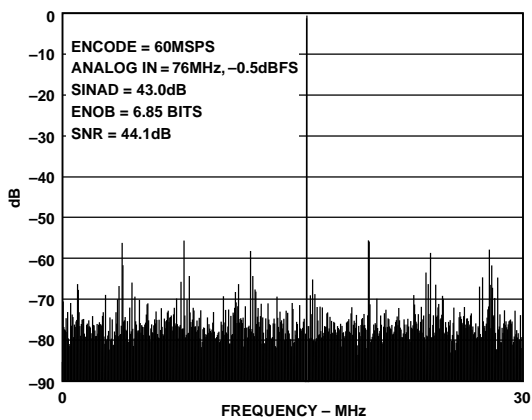


Figure 3. Spectral Plot 60 MSPS, 76 MHz

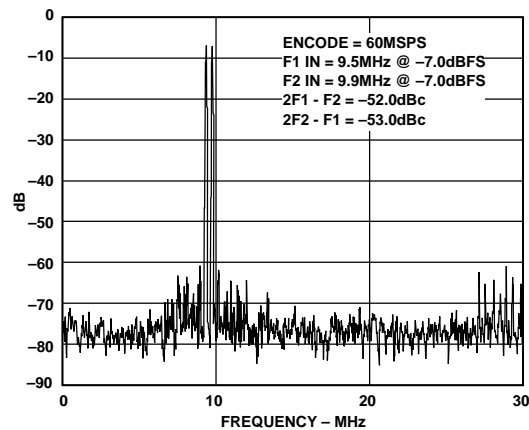


Figure 6. Two-Tone IMD

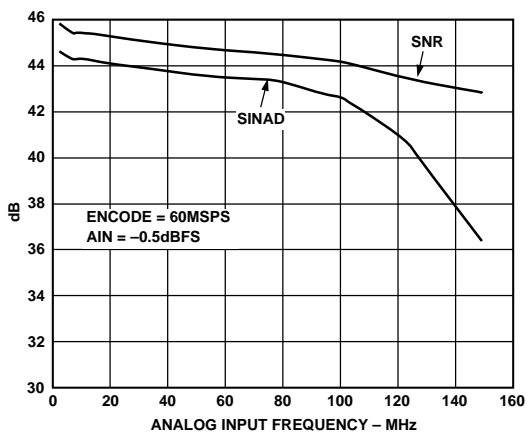


Figure 4. SINAD/SNR vs. AIN Frequency

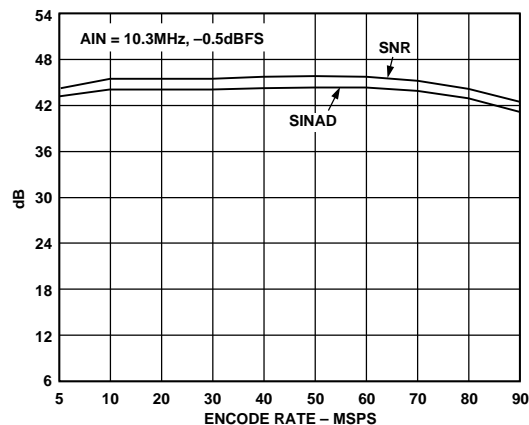


Figure 7. SINAD/SNR vs. Encode Rate

# AD9059

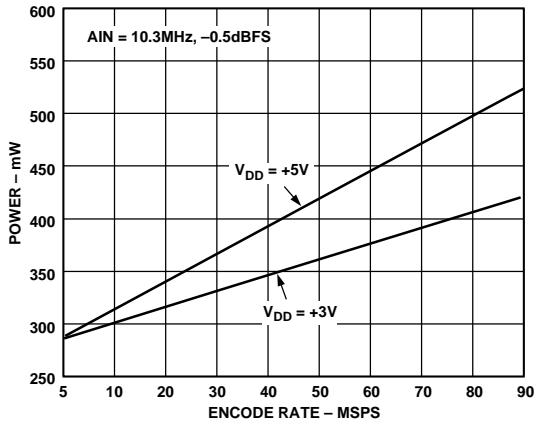


Figure 8. Power Dissipation vs. Encode Rate

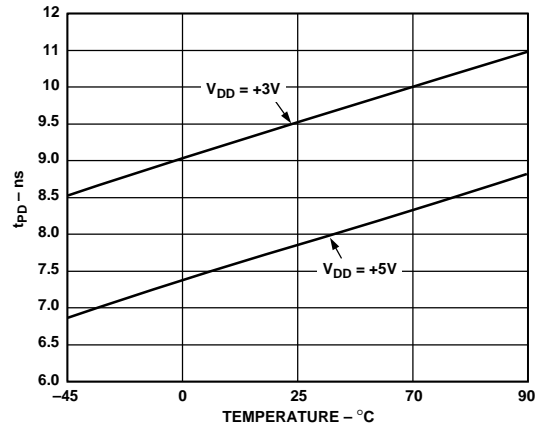


Figure 11.  $t_{PD}$  vs. Temperature/Supply (+3 V/+5 V)

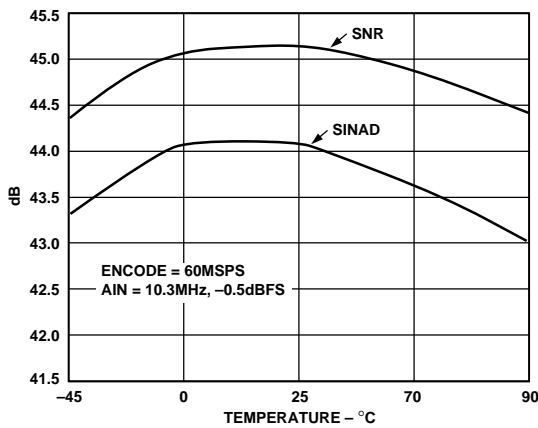


Figure 9. SINAD/SNR vs. Temperature

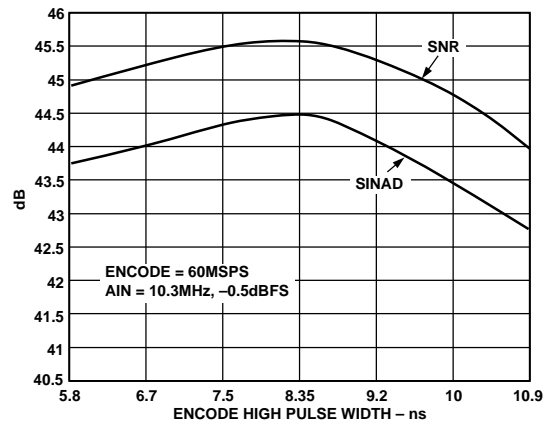


Figure 12. SINAD/SNR vs. Encode Pulse Width

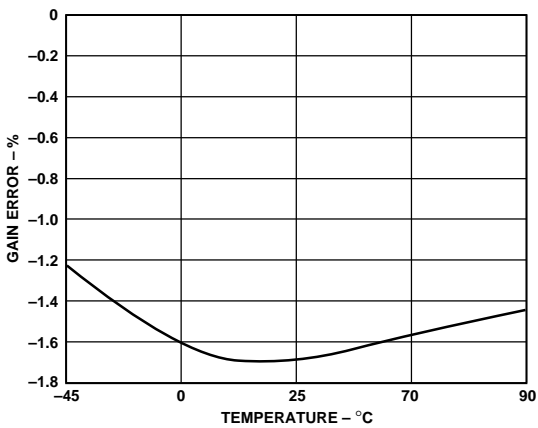


Figure 10. ADC Gain vs. Temperature (With External +2.5 V Reference)

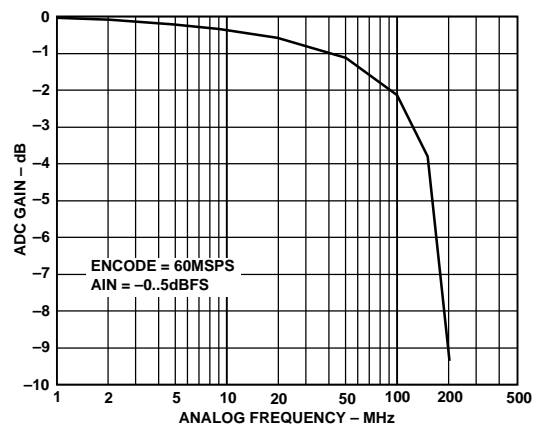


Figure 13. ADC Frequency Response

## THEORY OF OPERATION

The AD9059 combines Analog Devices' proprietary MagAmp gray code conversion circuitry with flash converter technology to provide dual high performance 8-bit ADCs in a single low cost monolithic device. The design architecture ensures low power, high speed, and 8-bit accuracy.

The AD9059 provides two linked ADC channels that are clocked from a single ENCODE input (refer to block diagram). The two ADC channels simultaneously sample the analog inputs (AINA and AINB) and provide non-interleaved parallel digital outputs (D0A–D7A and D0B–D7B). The voltage reference (VREF) is internally connected to both ADCs so channel gains and offsets will track if external reference control is desired.

The analog input signal is buffered at the input of each ADC channel and applied to a high speed track-and-hold. The T/H circuit holds the analog input value during the conversion process (beginning with the rising edge of the ENCODE command). The T/H's output signal passes through the gray code and flash conversion stages to generate coarse and fine digital representations of the held analog input level. Decode logic combines the multistage data and aligns the 8-bit word for strobed outputs on the rising edge of the ENCODE command. The MagAmp/Flash architecture of the AD9059 results in three pipeline delays for the output data.

## USING THE AD9059

### Analog Inputs

The AD9059 provides independent single-ended high impedance (150 k $\Omega$ ) analog inputs for the dual ADCs. Each input requires a dc bias current of 6  $\mu$ A (typical) centered near +2.5 V ( $\pm 10\%$ ). The dc bias may be provided by the user or may be derived from the ADC's internal voltage reference. Figure 14 shows a low cost dc bias implementation allowing the user to capacitively couple ac signals directly into the ADC without additional active circuitry. For best dynamic performance the VREF pin should be decoupled to ground with a 0.1  $\mu$ F capacitor (to minimize modulation of the reference voltage), and the bias resistor should approximately 1 k $\Omega$ .

Figure 15 shows typical connections for high performance dc biasing using the ADC's internal voltage reference. All components may be powered from a single +5 V supply (example analog input signals are referenced to ground).

### Voltage Reference

A stable and accurate +2.5 V voltage reference is built into the AD9059 (VREF). The reference output is used to set the ADC gain/offset and can provide dc bias for the analog input signals. The internal reference is tied to the ADC circuitry through a 800  $\Omega$  internal impedance and is capable of providing 300  $\mu$ A external drive current (for dc biasing the analog input or other user circuitry).

Some applications may require greater accuracy, improved temperature performance, or gain adjustments which cannot be obtained using the internal reference. An external voltage may be

applied to the VREF pin to overdrive the internal voltage reference for gain adjustment of up to  $\pm 10\%$  (the VREF pin is internally tied directly to the ADC circuitry). ADC gain and offset will vary simultaneously with external reference adjustment with a 1:1 ratio (a 2% or 50 mV adjustment to the +2.5 V reference varies ADC gain by 2% and ADC offset by 50 mV).

Theoretical input voltage range versus reference input voltage may be calculated from the following equations:

$$V_{RANGE} (p-p) = VREF/2.5$$

$$V_{MIDSCALE} = VREF$$

$$V_{TOP-OF-RANGE} = VREF + V_{RANGE}/2$$

$$V_{BOTTOM-OF-RANGE} = VREF - V_{RANGE}/2$$

The external reference should have a 1 mA minimum sink/source current capability to ensure complete overdrive of the internal voltage reference.

### Digital Logic (+5 V/+3 V Systems)

The digital inputs and outputs of the AD9059 can easily be configured to interface directly with +3 V or +5 V logic systems. The encode and power-down (PWRDN) inputs are CMOS stages with TTL thresholds of 1.5 V, making the inputs compatible with TTL, +5 V CMOS, and +3 V CMOS logic families. As with all high speed data converters, the encode signal should be clean and jitter free to prevent degradation of ADC dynamic performance.

The AD9059's digital outputs will also interface directly with +5 V or +3 V CMOS logic systems. The voltage supply pins ( $V_{DD}$ ) for these CMOS stages are isolated from the analog  $V_D$  voltage supply. By varying the voltage on these supply pins the digital output HIGH levels will change for +5 V or +3 V systems. The  $V_{DD}$  pins are internally connected on the AD9059 die. Care should be taken to isolate the  $V_{DD}$  supply voltages from the +5 V analog supply to minimize noise coupling into the ADCs.

The AD9059 provides high impedance digital output operation when the ADC is driven into power-down mode (PWRDN, logic HIGH). A 200 ns (minimum) power-down time should be provided before a high impedance characteristic is required. A 200 ns power-up period should be provided to ensure accurate ADC output data after reactivation (valid output data is available three clock cycles after the 200 ns delay).

### Timing

The AD9059 is guaranteed to operate with conversion rates from 5 MSPS to 60 MSPS. At 60 MSPS the ADC is designed to operate with an encode duty cycle of 50%, but performance is insensitive to moderate variations. Pulse width variations of up to  $\pm 10\%$  (allowing the encode signal to meet the minimum/maximum HIGH/LOW specifications) will cause no degradation in ADC performance (refer to Figure 1 Timing Diagram).

Due to the linked ENCODE architecture of the ADCs, the AD9059 cannot be operated in a two-channel ping-pong mode.

# AD9059

## Power Dissipation

The power dissipation of the AD9059 is specified to reflect a typical application setup under the following conditions: encode is 60 MSPS, analog input is  $-0.5$  dBFS at 10.3 MHz,  $V_D$  is +5 V,  $V_{DD}$  is +3 V, and digital outputs are loaded with 7 pF typical (10 pF maximum). The actual dissipation will vary as these conditions are modified in user applications. Figure 8 shows typical power consumption for the AD9059 versus ADC encode frequency and  $V_{DD}$  supply voltage.

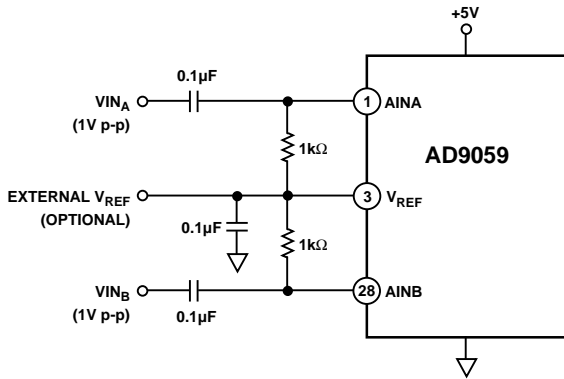


Figure 14. Capacitively Coupled AD9059

A power-down function allows users to reduce power dissipation when ADC data is not required. A TTL/CMOS HIGH signal (PWRDN) shuts down portions of the dual ADC and brings total power dissipation to less than 10 mW. The internal bandgap voltage reference remains active during power-down mode to minimize ADC reactivation time. If the power-down function is not desired, Pin 3 should be tied to ground. Both ADC channels are controlled simultaneously by the PWRDN pin; they cannot be shut down or turned on independently.

## Applications

The wide analog bandwidth of the AD9059 makes it attractive for a variety of high performance receiver and encoder applications. Figure 16 shows the dual ADC in a typical low cost I & Q demodulator implementation for cable, satellite, or wireless LAN modem receivers. The excellent dynamic performance of the ADC at higher analog input frequencies and encode rates empowers users to employ direct IF sampling techniques (refer to Figure 3, *Spectral Plot*). IF sampling eliminates or simplifies analog mixer and filter stages to reduce total system cost and power.

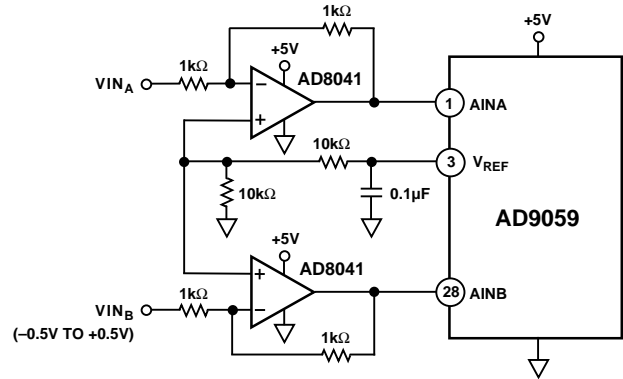


Figure 15. DC Coupled AD9059 (VIN Inverted)

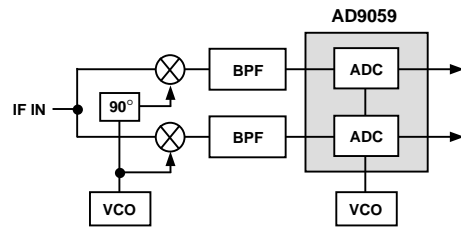


Figure 16. I and Q Digital Receiver

The high sampling rate and analog bandwidth of the AD9059 are ideal for computer RGB video digitizer applications. With a full-power analog bandwidth of  $2\times$  the maximum sampling rate, the ADC provides sufficient pixel-to-pixel transient settling time to ensure accurate 60 MSPS video digitization. Figure 17 shows a typical RGB video digitizer implementation for the AD9059.

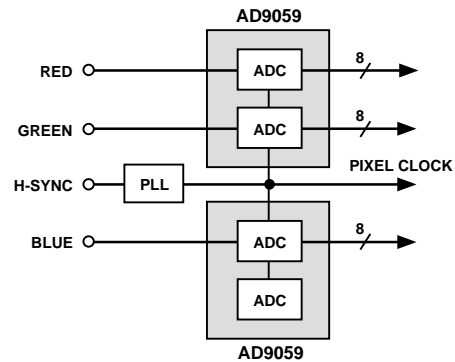


Figure 17. RGB Video Encoder



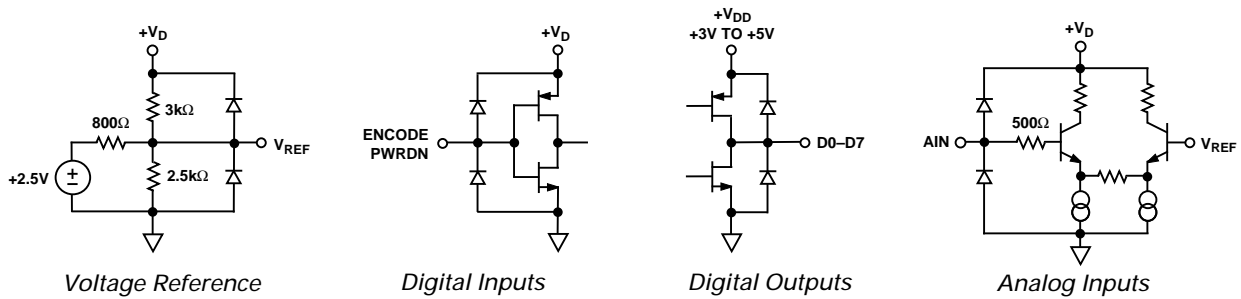


Figure 18. Equivalent Circuits

### Evaluation Board

The AD9059/PCB evaluation board provides an easy-to-use analog/digital interface for the dual 8-bit, 60 MSPS ADC. The board includes typical hardware configurations for a variety of high speed digitization evaluations. On-board components include the AD9059 (in the 28-pin SSOP package), optional analog input buffer amplifiers, digital output latches, board timing drivers, and configurable jumpers for ac coupling, dc coupling, and power-down function testing. The board is configured at shipment for dc coupling using the AD9059's internal reference.

For dc coupled analog input applications, amplifiers U3 and U4 are configured to operate as unity gain inverters with adjustable offset for the analog input signals. For full-scale ADC drive each analog input signal should be 1 V p-p into 50  $\Omega$  referenced to ground. Each amplifier offsets its analog signal by +VREF (+2.5 V typical) to center the voltage for proper ADC input drive. For dc coupled operation, connect E7 to E9 (analog input A to R11), E14 to E13 (amplifier output to analog input A of AD9059), E4 to E5 (analog input B to R10), and E11 to E10 (amplifier output to analog input B of AD9059) using the board jumper connectors.

For ac coupled analog input applications, amplifiers U3 and U4 are removed from the analog signal paths. The analog signals are coupled through capacitors C11 and C12, each terminated to the VREF voltage through separate 1 k $\Omega$  resistors (providing bias current for the AD9059 analog inputs, AINA and AINB).

Analog input signals to the board should be 1 V p-p into 50  $\Omega$  for full-scale ADC drive. For ac coupled operation, connect E7 to E8 (analog input A to C12 feedthrough capacitor), E13 to E15 (C12 to R15 termination resistor for channel A), E4 to E6 (analog input B to C11 feedthrough capacitor), and E10 to E12 (C11 to R14 termination resistor for channel B) using the board jumper connectors.

The on-board reference voltage may be used to drive the ADC or an external reference may be applied. The standard configuration employs the internal voltage reference without any external connection requirements. An external voltage reference may be applied at board connector input REF to overdrive the limited current output of the AD9059's internal voltage reference. The external voltage reference should be +2.5 V typical.

The power-down function of the AD9059 can be exercised through a board jumper connection. Connect E2 to E1 (+5 V to PWRDN) for power-down mode operation. For normal operation, connect E3 to E1 (ground to PWRDN).

The encode signal source should be TTL/CMOS compatible and capable of driving a 50  $\Omega$  termination. The digital outputs of the AD9059 are buffered through latches on the evaluation board (U5 and U6) and are available for the user at connector Pins 30-37 and Pins 22-29. Latch timing is derived from the ADC ENCODE clock and a digital clocking signal is provided for the board user at connector Pins 2 and 21.

# AD9059

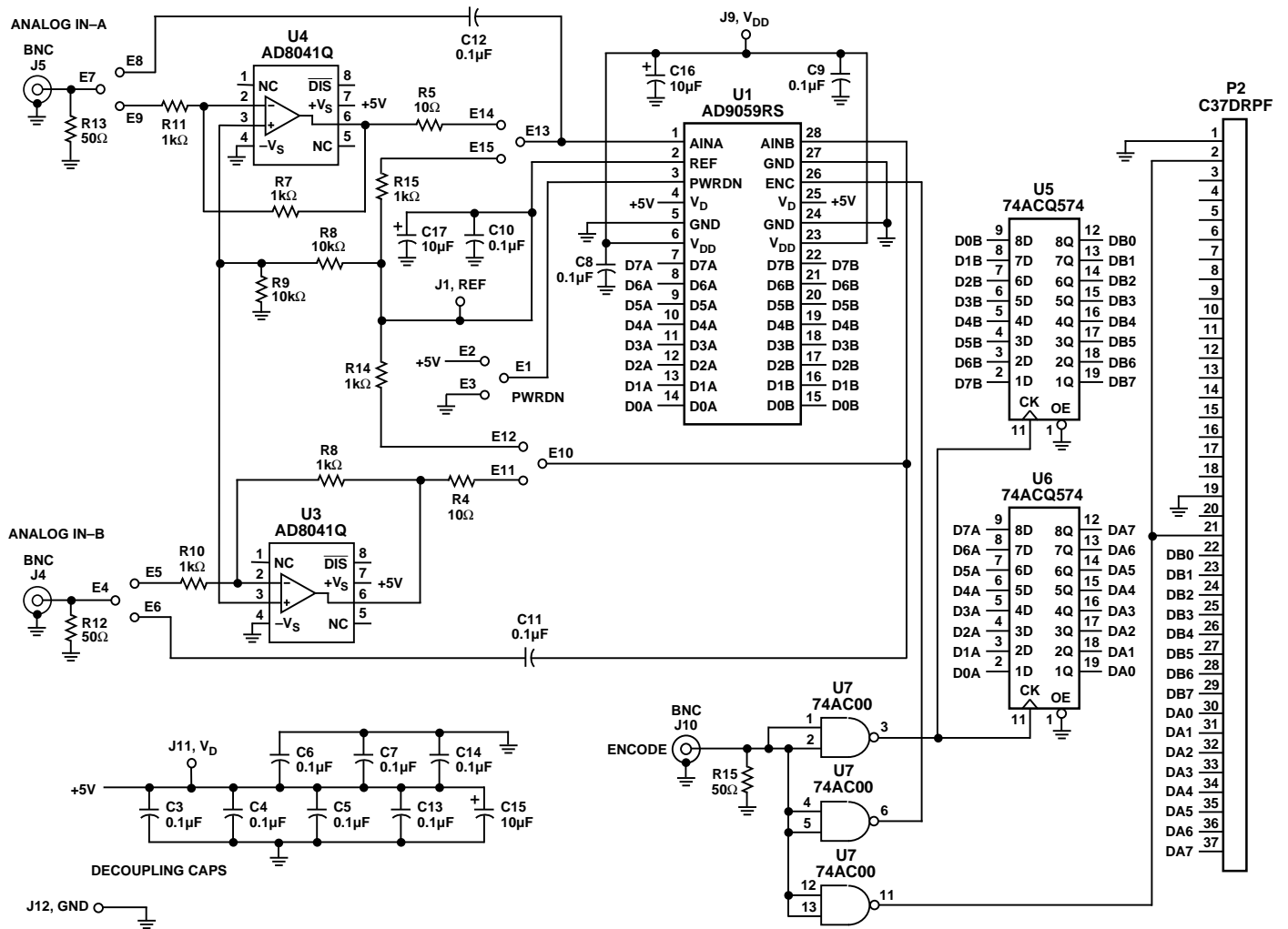


Figure 19. AD9059 Dual Evaluation Board Schematic

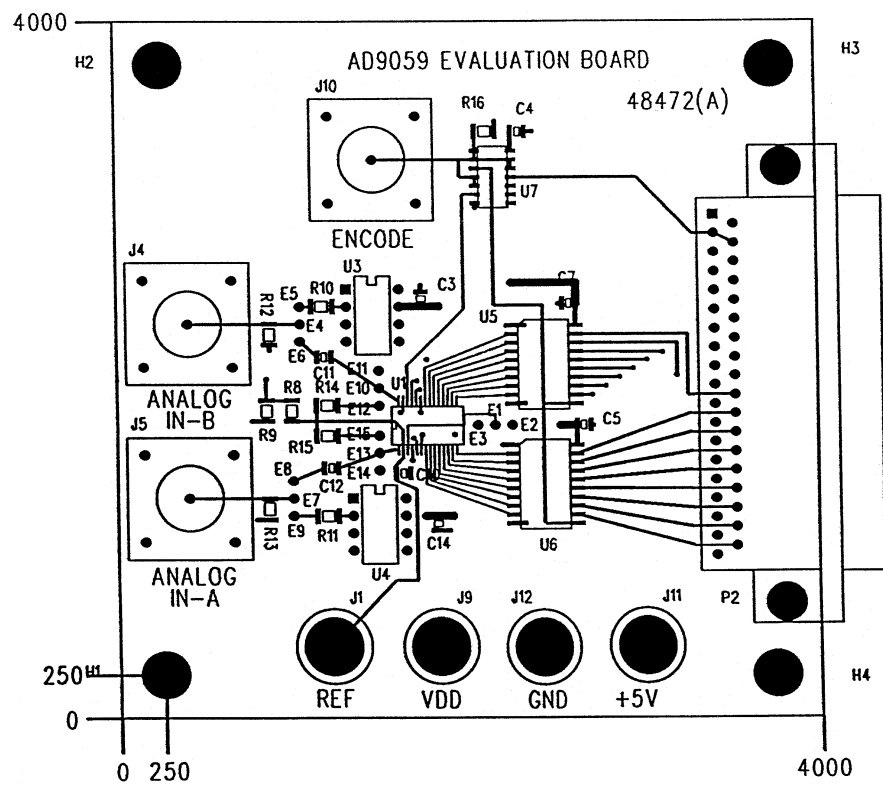


Figure 20. Evaluation Board Layout (Top)

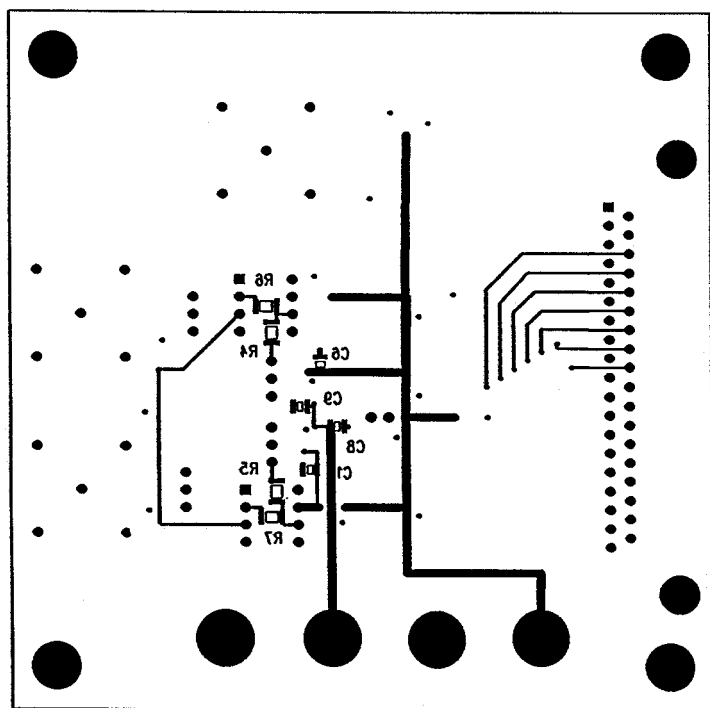


Figure 21. Evaluation Board Layout (Bottom)

AD9059

**OUTLINE DIMENSIONS**  
Dimensions shown in inches and (mm).

**28-Lead SSOP  
(RS-28)**

