10-Bit, 40/65/80/105 MSPS 3 V Dual A/D Converter

AD9218

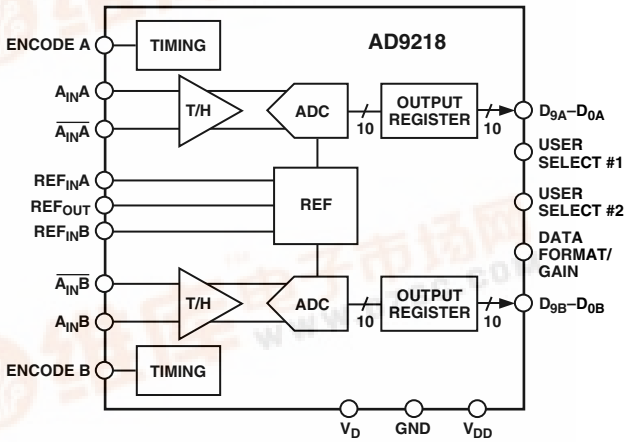
FEATURES

Dual 10-Bit, 40 MSPS, 65 MSPS, 80 MSPS, and 105 MSPS ADC
Low Power: 275 mW at 105 MSPS per Channel
On-Chip Reference and Track/Holds
300 MHz Analog Bandwidth Each Channel
SNR = 57 dB @ 41 MHz, Encode = 80 MSPS
1 V p-p or 2 V p-p Analog Input Range Each Channel
Single 3.0 V Supply Operation (2.7 V–3.6 V)
Power-Down Mode for Single Channel Operation
Two's Complement or Offset Binary Output Mode
Output Data Alignment Mode
Pin-Compatible with 8-Bit AD9288
–75 dBc Crosstalk between Channels

APPLICATIONS

Battery-Powered Instruments
Hand-Held Scopemeters
Low Cost Digital Oscilloscopes
I and Q Communications
Ultrasound Equipment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9218 is a dual 10-bit monolithic sampling analog-to-digital converter with on-chip track-and-hold circuits and is optimized for low cost, low power, small size and ease of use. The product operates at a 105 MSPS conversion rate with outstanding dynamic performance over its full operating range. Each channel can be operated independently.

The ADC requires only a single 3.0 V (2.7 V to 3.6 V) power supply and an encode clock for full operation. No external reference or driver components are required for many applications. The digital outputs are TTL/CMOS-compatible and a separate output power supply pin supports interfacing with 3.3 V or 2.5 V logic.

The clock input is TTL/CMOS-compatible and the 10-bit digital outputs can be operated from 3.0 V (2.5 V to 3.6 V) supplies. User-selectable options are available to offer a combination of power-down modes, digital data formats and digital data timing schemes. In power-down mode, the digital outputs are driven to a high-impedance state.

Fabricated on an advanced CMOS process, the AD9218 is available in a 48-lead surface-mount plastic package (7 × 7 mm LQFP) specified over the industrial temperature range (–40°C to +85°C).

PRODUCT HIGHLIGHTS

Low Power—Just 275 mW power dissipation per channel at 105 MSPS. Other speed grade proportionally scaled down while maintaining high ac performance.

Pin Compatibility Upgrade—Allows easy migration from 8-bit to 10-bit. Pin-compatible with the 8-bit AD9288 dual ADC.

Ease of Use—On-chip reference and user controls provide flexibility in system design.

High Performance—Maintain 54 dB SNR at 105 MSPS with a Nyquist input.

Channel Crosstalk—Very low at –75 dBc.

REV. 0

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AD9218–SPECIFICATIONS

DC SPECIFICATIONS (V_{DD} = 3.0 V, V_D = 3.0 V; external reference, unless otherwise noted.)

Parameter	Temp	Test Level	AD9218BST-40/-65 Min	Typ	Max	AD9218BST-80/-105 Min	Typ	Max	Unit
RESOLUTION				10			10		Bits
ACCURACY									
No Missing Codes[1]	Full	VI		GNT			GNT		
Offset Error[2]	25°C	I	–18	2	18	–18	2	18	LSB
Gain Error[2]	25°C	I	–2	3	8	–2	3.5	8	% FS
Differential Nonlinearity (DNL)	25°C	I	–1	±0.3/±0.6	1/1.3	–1	±0.5/±0.8	1.2/1.7	LSB
	Full	VI		±0.8			±0.6/±0.9		LSB
Integral Nonlinearity (INL)	25°C	I	–1/–1.6	±0.3/±1	1/1.6	–1.35/–2.7	±0.75/±2	1.35/2.7	LSB
	Full	VI		±1			±1/±2.3		LSB
TEMPERATURE DRIFT									
Offset Error	Full	V		10			4		ppm/°C
Gain Error[2]	Full	V		80			100		ppm/°C
Reference	Full	V		40			40		ppm/°C
REFERENCE									
Internal Reference Voltage (REFOUT)	25°C	I	1.18	1.24	1.28	1.18	1.24	1.28	V
Input Resistance (REFIN A, B)	Full	V	9	11	13	9	11	13	kΩ
ANALOG INPUTS									
Differential Input Voltage Range (AIN, $\overline{AIN}$)[3]	Full	V		1 or 2			1		V
Common-Mode Voltage	Full	V		V_D/3			V_D/3		V
Input Resistance	Full	VI	8	10	14	8	10	14	kΩ
Input Capacitance	25°C	V		3			3		pF
POWER SUPPLY									
V_D	Full	IV	2.7	3	3.6	2.7	3	3.6	V
V_{DD}	Full	IV	2.7	3	3.6	2.7	3	3.6	V
Supply Currents									
IV_D (V_D = 3.0 V)[4]	Full	VI		108/117	113/122		172/183	175/188	mA
IV_{DD} (V_{DD} = 3.0 V)[4]	25°C	V		7/11			13/17		mA
Power Dissipation DC[5]	Full	VI		325/350	340/365		515/550	525/565	mW
IV_D Power-Down Current[6]	Full	VI		20			22		mA
Power Supply Rejection Ratio	25°C	I		±1			±1		mV/V

NOTES

[1]No Missing Codes across industrial temperature range guaranteed for -40 MSPS, -65 MSPS, and -80 MSPS grades. No missing codes at room temperature guaranteed for -105 grade.

[2]Gain error and gain temperature coefficients are based on the ADC only (with a fixed 1.25 V external reference) -65 Grade in 2 V p-p range, -40, -85, -105 Grades in 1 V p-p range.

[3](AIN – $\overline{AIN}$) = ±0.5 V in 1 V range (full scale), (AIN – $\overline{AIN}$) = ±1 V in 2 V range (full scale).

[4]AC Power Dissipation measured with rated encode and a 10.3 MHz analog input @ 0.5 dBFS, C_{LOAD} = 5 pF.

[5]DC Power Dissipation measured with rated encode and a dc analog input (Outputs Static, IV_{DD} = 0)

[6]In power-down state IV_{DD} = ±10 µA typical (all grades).

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (V_{DD} = 3.0 V, V_D = 3.0 V; external reference, unless otherwise noted.)

Parameter	Temp	Test Level	AD9218BST-40/-65 Min	Typ	Max	AD9218BST-80/-105 Min	Typ	Max	Unit
DIGITAL INPUTS									
Encode Input Common Mode	Full	V		$V_D/2$			$V_D/2$		V
Encode "1" Voltage	Full	VI	2			2			V
Encode "0" Voltage	Full	VI			0.8			0.8	V
Encode Input Resistance	Full	VI	1.8	2.0	2.3	1.8	2.0	2.3	kΩ
Logic "1" Voltage—S1, S2, DFS	Full	VI	2			2			V
Logic "0" Voltage—S1, S2, DFS	Full	VI			0.8			0.8	V
Logic "1" Current—S1	Full	VI	–50	±10	+50	–50	±10	+50	µA
Logic "0" Current—S1	Full	VI	–400	–230	–50	–400	–230	–50	µA
Logic "1" Current—S2	Full	VI	50	230	400	50	230	400	µA
Logic "0" Current—S2	Full	VI	–50	±10	+50	–50	±10	+50	µA
Logic "1" Current—DFS	Full	VI	30	100	200	30	100	200	µA
Logic "0" Current—DFS	Full	VI	–400	–230	–50	–400	–230	–50	µA
Input Capacitance—S1, S2, Encode Inputs	25°C	V		2			2		pF
Input Capacitance DFS	25°C	V		4.5			4.5		pF
DIGITAL OUTPUTS									
Logic "1" Voltage	Full	VI	2.45			2.45			V
Logic "0" Voltage	Full	VI			0.05			0.05	V
Output Coding			Two's Comp. or Offset Binary			Two's Comp. or Offset Binary			

Specifications subject to change without notice.

AC SPECIFICATIONS (V_{DD} = 3.0 V, V_D = 3.0 V; external reference, unless otherwise noted.)

Parameter	Temp	Test Level	AD9218BST-40/-65 Min	Typ	Max	AD9218BST-80/-105 Min	Typ	Max	Unit
DYNAMIC PERFORMANCE[1]									
Signal-to-Noise Ratio (SNR)									
(Without Harmonics)									
f_{IN} = 10.3 MHz	25°C	I	58/55	59/57		57/53	58/55		dB
f_{IN} = Nyquist[2]	25°C	I	-/54	59/56		55/52	57/54		dB
Signal-to-Noise Ratio (SINAD)									
(With Harmonics)									
f_{IN} = 10.3 MHz	25°C	I	58/54	59/56		56/52	58/53		dB
f_{IN} = Nyquist[2]	25°C	I	-/53	59/55		55/51	57/53		dB
Effective Number of Bits									
f_{IN} = 10.3 MHz	25°C	I	9.4/8.8	9.6/9.1		9.1/8.4	9.4/8.6		Bits
f_{IN} = Nyquist[2]	25°C	I	-/8.6	9.6/8.9		9/8.3	9.3/8.6		Bits
Second Harmonic Distortion									
f_{IN} = 10.3 MHz	25°C	I	–72/–66	–89/–77		–69/–60	–77/–68		dBc
f_{IN} = Nyquist[2]	25°C	I	-/–63	–89/–72		–65/–57	–76/–66		dBc
Third Harmonic Distortion									
f_{IN} = 10.3 MHz	25°C	I	–68/–62	–79/–68		–62/–57	–71/–63		dBc
f_{IN} = Nyquist[2]	25°C	I	-/–60	–78/–64		–63/–57	–73/–69		dBc
Spurious Free Dynamic Range SFDR									
f_{IN} = 10.3 MHz	25°C	I	–68/–62	–79/–67		–62/–57	–69/–62		dBc
f_{IN} = Nyquist[2]	25°C	I	-/–60	–78/–64		–63/–57	–70/–63		dBc
Two-Tone Intermod Distortion (IMD)									
f_{IN1} = 10 MHz, f_{IN2} = 11 MHz at –7 dBFS	25°C	V		–74/–73					dBc
f_{IN1} = 30 MHz, f_{IN2} = 31 MHz at –7 dBFS	25°C	V		–73/–73			–77/–67		dBc
Analog Bandwidth, Full Power	25°C	V		300			300		MHz
Crosstalk	25°C	V		–75			–75		dBc

NOTES
[1]AC specs based on an analog input voltage of –0.5 dBFS at 10.3 MHz unless otherwise noted. AC specs for -40, -80, -105 grades are tested in 1 V p-p range and driven differentially. AC specs for -65 grade are tested in 2 V p-p range and driven differentially.
[2]The -65, -80, and -105 grades are tested close to Nyquist for that grade: 31 MHz, 39 MHz, and 51 MHz for the -65, -80, and -105 grades respectively.

AD9218–SPECIFICATIONS

SWITCHING SPECIFICATIONS (V_{DD} = 3.0 V, V_D = 3.0 V; external reference, unless otherwise noted.)

Parameter	Temp	Test Level	AD9218BST-40/-65 Min	Typ	Max	AD9218BST-80/-105 Min	Typ	Max	Unit
ENCODE INPUT PARAMETERS									
Maximum Encode Rate	Full	VI	40/65			80/105			MSPS
Minimum Encode Rate	Full	IV			20/20			20/20	MSPS
Encode Pulsewidth High (t_{EH})	Full	IV	7/6			5/3.8			ns
Encode Pulsewidth Low (t_{EL})	Full	IV	7/6			5/3.8			ns
Aperture Delay (t_A)	25°C	V		2			2		ns
Aperture Uncertainty (Jitter)	25°C	V		3			3		ps rms
DIGITAL OUTPUT PARAMETERS									
Output Valid Time (t_V)*	Full	VI	3			3			ns
Output Propagation Delay (t_{PD})*	Full	VI		4.5	7		4.5	6	ns
Output Rise Time (t_R)	25°C	V		1			1.0		ns
Output Fall Time (t_F)	25°C	V		1.2			1.2		ns
Out of Range Recovery Time	25°C	V		5			5		ns
Transient Response Time	25°C	V		5			5		ns
Recovery Time from Power-Down	25°C	V		10			10		Cycles
Pipeline Delay	Full	IV		5			5		Cycles

NOTES

*t_V and t_{PD} are measured from the 1.5 level of the ENCODE input to the 50%/50% levels of the digital outputs swing. The digital output load during test is not to exceed an ac load of 5 pF or a dc current of ±40 µA. Rise and fall times measured from 10% to 90%.

Specifications subject to change without notice.

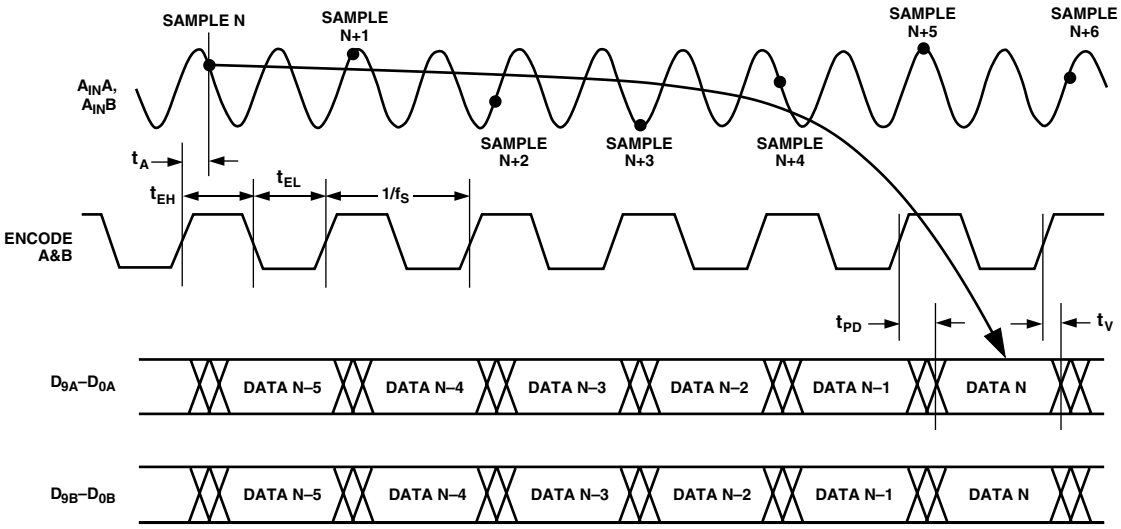


Figure 1. Normal Operation, Same Clock (S1 = 1, S2 = 0) Channel Timing

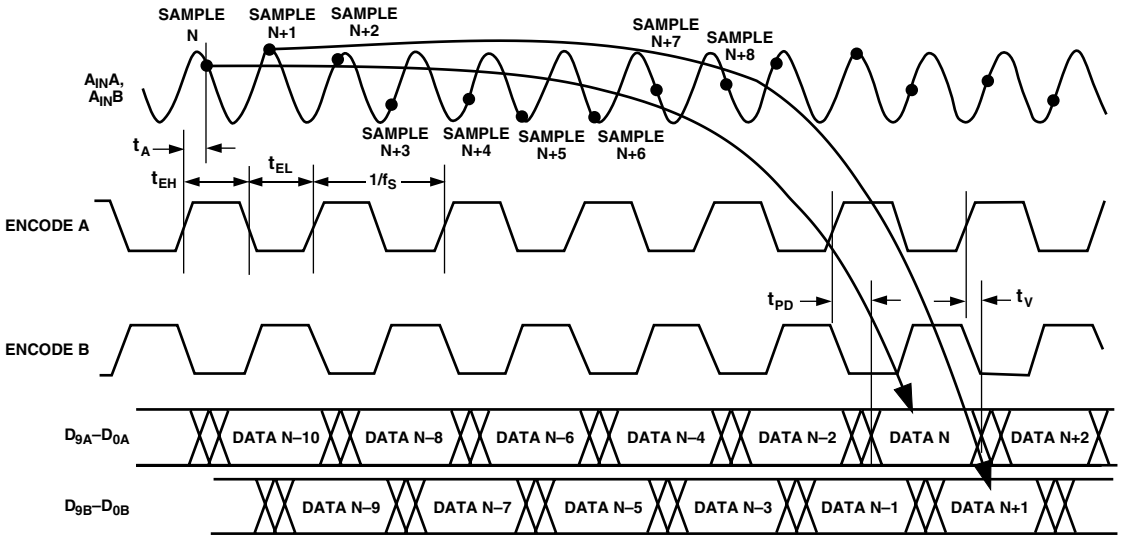


Figure 2. Normal Operation with Two Clock Sources (S1 = 1, S2 = 0) Channel Timing

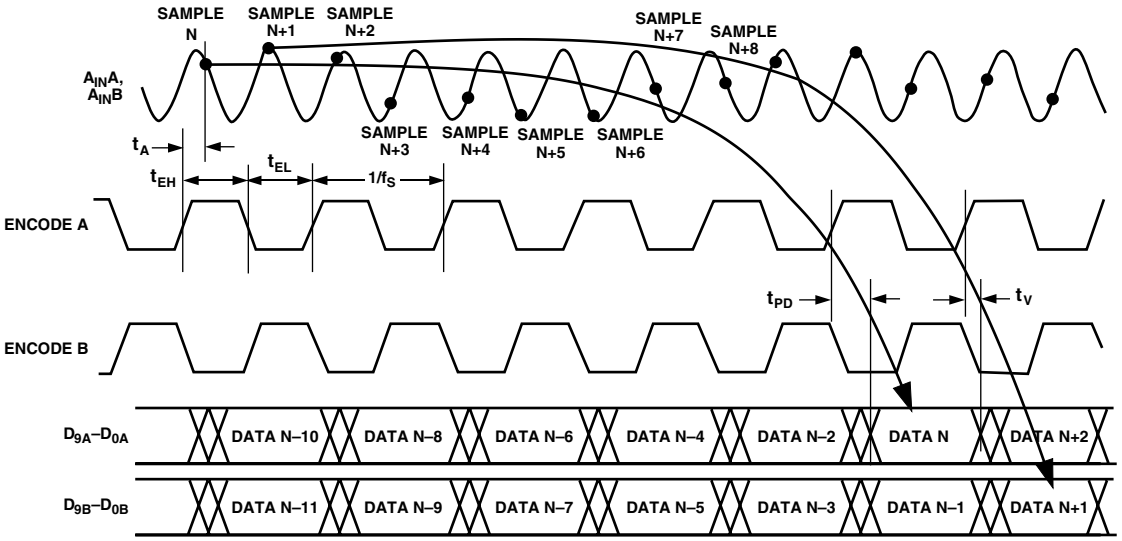


Figure 3. Data Align with Two Clock Sources (S1 = 1, S2 = 1) Channel Timing

ABSOLUTE MAXIMUM RATINGS[1]

V_D, V_{DD}	4 V
Analog Inputs	–0.5 V to V_D + 0.5 V
Digital Inputs	–0.5 V to V_{DD} + 0.5 V
REF_{IN} Inputs	–0.5 V to V_D + 0.5 V
Digital Output Current	20 mA
Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C
θ_{JA}[2]	57°C/W

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

[2] Measured on a four-layer board with solid ground plane.

EXPLANATION OF TEST LEVELS

Test Level

I 100% production tested.

II 100% production tested at 25°C and sample tested at specified temperatures.

III Sample tested only.

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9218 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9218BST-40, -65, -80, -105	–40°C to +85°C	Metric Quad Flat Pack (1.4 mm thick: LQFP)	ST-48
AD9218-65PCB	25°C	Evaluation Board (Supports -40/-65 Grade)	
AD9218-105PCB	25°C	Evaluation Board (Supports -80/-105 Grade)	

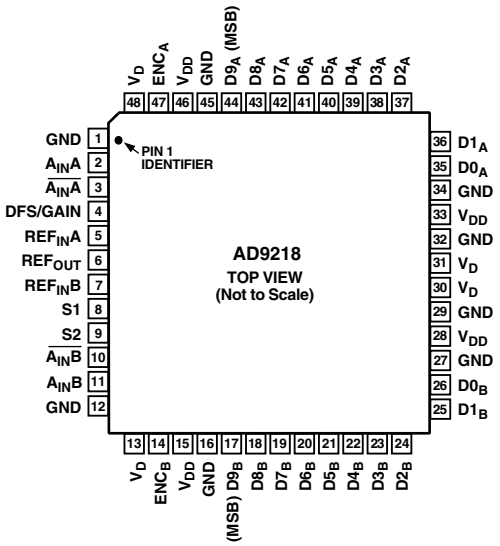
Table I. User Select Modes

S1	S2	User Select Options
0	0	Power-Down Both Channel A and B.
0	1	Power-Down Channel B Only.
1	0	Normal Operation (Data Align Disabled).
1	1	Data Align Enabled (data from both channels available on rising edge of Clock A. Channel B data is delayed by a 1/2 clock cycle.)

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1, 12, 16, 27, 29, 32, 34, 45	GND	Ground
2	$A_{IN}A$	Analog Input for Channel A
3	$\overline{A_{IN}A}$	Analog Input for Channel A (Complementary)
4	DFS/GAIN	Data Format Select and Analog Input Gain Mode. (Low = offset binary output available, 1 V p-p supported; high = two's complement output available, 1 V p-p supported; floating = offset binary output available, 2 V p-p supported; Set to V_{REF} = two's complement output available, 2 V p-p supported.)
5	$REF_{IN}A$	Reference Voltage Input for Channel A
6	REF_{OUT}	Internal Reference Voltage
7	$REF_{IN}B$	Reference Voltage Input for Channel B
8	S1	User Select #1 (Refer to Table I)
9	S2	User Select #2 (Refer to Table I)
10	$\overline{A_{IN}B}$	Analog Input for Channel B (Complementary)
11	$A_{IN}B$	Analog Input for Channel B
13, 30, 31, 48	V_D	Analog Supply (3 V)
14	ENC_B	Clock Input for Channel B
15, 28, 33, 46	V_{DD}	Digital Supply (2.5 V to 3.6 V)
17–26	$D9_B$–$D0_B$	Digital Output for Channel B ($D9_B$ = MSB)
35–44	$D0_A$–$D9_A$	Digital Output for Channel A ($D9_A$ = MSB)
47	ENC_A	Clock Input for Channel A

PIN CONFIGURATION



TERMINOLOGY

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the 50% point of the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Crosstalk
Coupling onto one channel being driven by a low level (–40 dBFS) signal when the adjacent interfering channel is driven by a full-scale signal.

Differential Analog Input Resistance, Differential Analog Input Capacitance and Differential Analog Input Impedance
The real and complex impedances measured at each analog input port. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range
The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180 degrees out of phase. Peak-to-peak differential is computed by rotating the inputs phase 180 degrees and again taking the peak measurement. The difference is then computed between both peak measurements.

Differential Nonlinearity
The deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits
The effective number of bits (ENOB) is calculated from the measured SNR based on the equation:

$$ENOB = \frac{SNR_{MEASURED} - 1.76\ dB}{6.02}$$

ENCODE Pulsewidth/Duty Cycle
Pulsewidth high is the minimum amount of time that the ENCODE pulse should be left in Logic 1 state to achieve rated performance; pulsewidth low is the minimum time ENCODE pulse should be left in low state. See timing implications of changing t_{ENCH} in text. At a given clock rate, these specifications define an acceptable ENCODE duty cycle.

Full-Scale Input Power
Expressed in dBm. Computed using the following equation:

$$Power_{Full-Scale} = 10 \log \left(\frac{\frac{V^2{}_{Full-Scale\ rms}}{Z_{INPUT}}}{0.001} \right)$$

Gain Error
Gain error is the difference between the measured and ideal full scale input voltage range of the ADC.

Harmonic Distortion, Second
The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

Harmonic Distortion, Third
The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Output Propagation Delay
The delay between a differential crossing of ENCODE and ENCODE and the time when all output data bits are within valid logic levels.

Noise (for Any Range within the ADC)

$$V_{NOISE} = \sqrt{Z \times 0.001 \times 10^{\left(\frac{FS_{dBm} - SNR_{dBc} - Signal_{dBFS}}{10}\right)}}$$

Where Z is the input impedance, FS is the full scale of the device for the frequency in question, SNR is the value for the particular input level, and $Signal$ is the signal level within the ADC reported in dB below full scale. This value includes both thermal and quantization noise.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)
The ratio of the rms signal amplitude (set 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (without Harmonics)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as signal level is lowered), or dBFS (always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBc.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal level is lowered), or in dBFS (always related back to converter full scale).

Worst Other Spur
The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second and third harmonic) reported in dBc.

Transient Response Time
Transient response is defined as the time it takes for the ADC to reacquire the analog input after a transient from 10% above negative full scale to 10% below positive full scale.

Out-of-Range Recovery Time
Out of range recovery time is the time it takes for the ADC to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

EQUIVALENT CIRCUITS

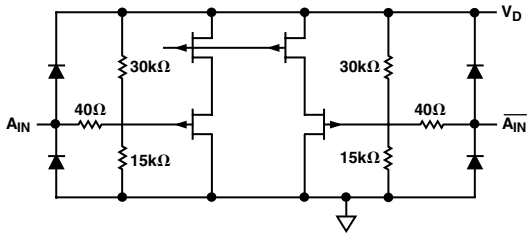


Figure 4. Analog Input Stage

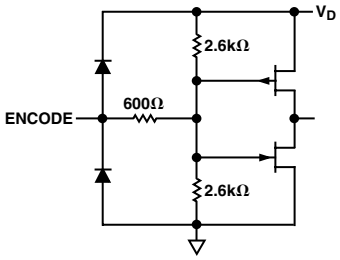


Figure 5. Encode Inputs

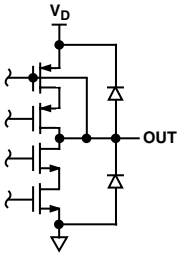


Figure 6. Reference Output Stage

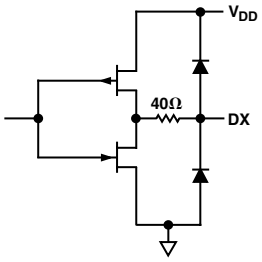


Figure 7. Digital Output Stage

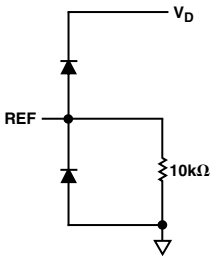


Figure 8. Reference Inputs

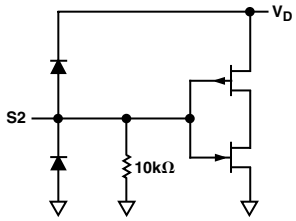


Figure 9. S2 Input

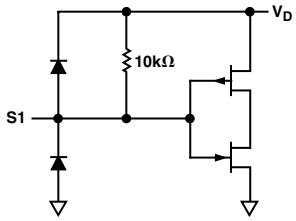


Figure 10. S1 Input

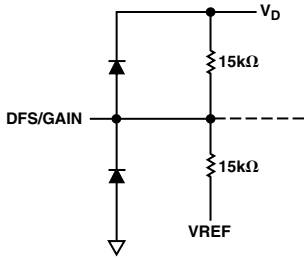
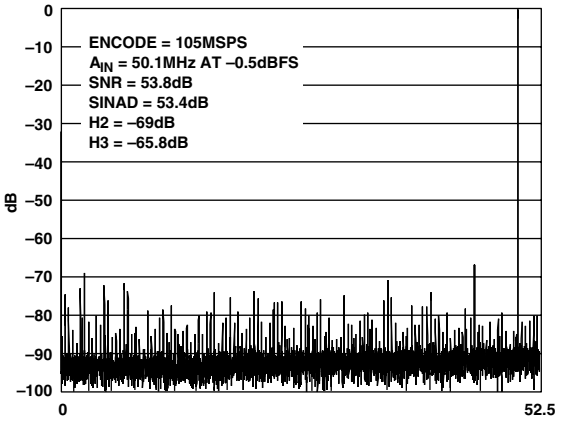
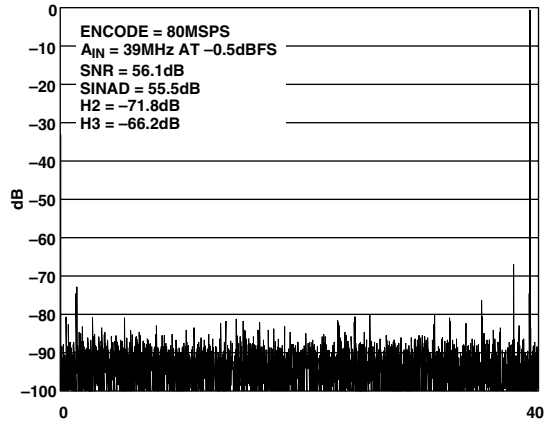


Figure 11. DFS/Gain Input

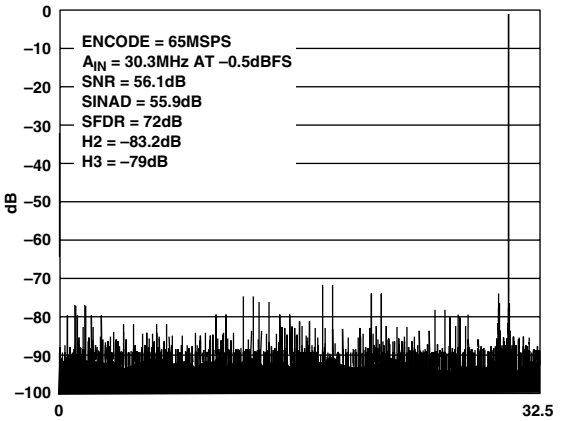
AD9218–Typical Performance Characteristics



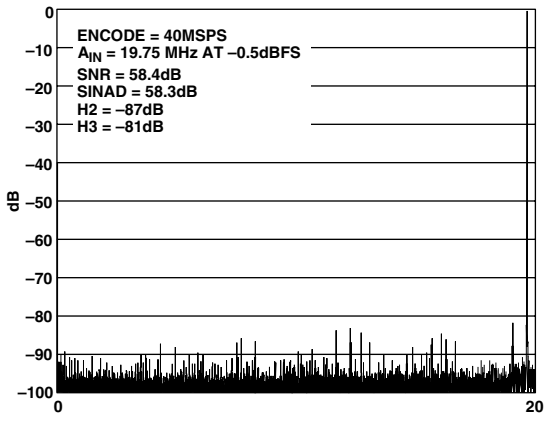
TPC 1. FFT: FS = 105 MSPS, A_{IN} = 50.1 MHz @ –0.5 dBFS, Differential, 1 V p-p Input Range



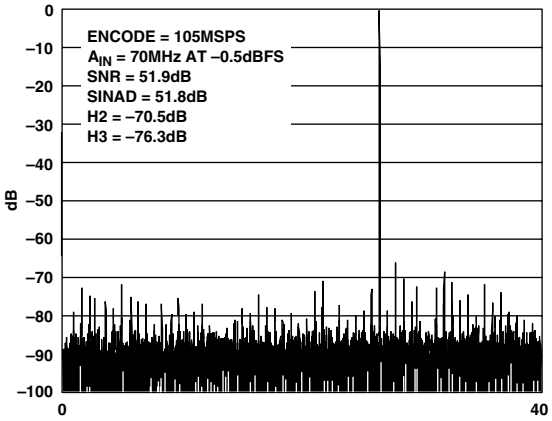
TPC 2. FFT: FS = 80 MSPS, A_{IN} = 39 MHz @ –0.5 dBFS, Differential, 1 V p-p Input Range



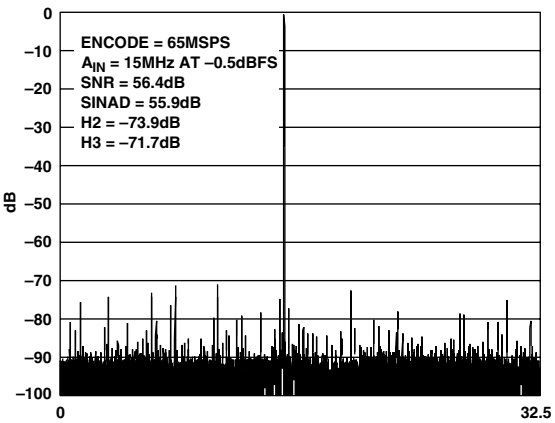
TPC 3. FFT: FS = 65 MSPS, A_{IN} = 30.3 MHz @ –0.5 dBFS, Differential, 2 V p-p Input Range



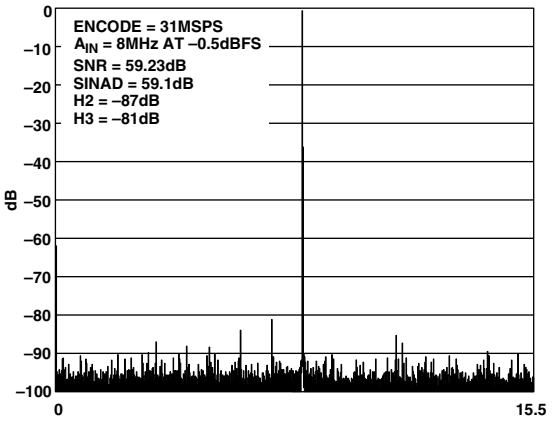
TPC 4. FFT: FS = 40 MSPS, A_{IN} = 19.7 MHz @ –0.5 dBFS, Differential, 1 V p-p Input Range



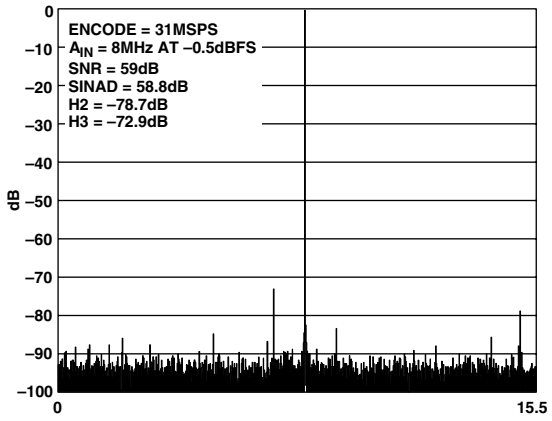
TPC 5. FFT: FS = 105 MSPS, A_{IN} = 70 MHz @ –0.5 dBFS, Differential, 1 V p-p Input Range



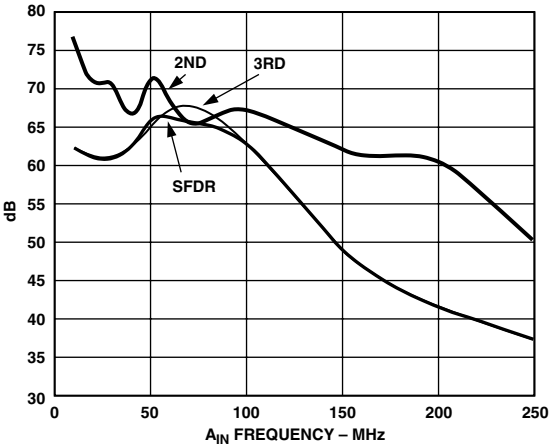
TPC 6. FFT: FS = 65 MSPS, A_{IN} = 15 MHz @ –0.5 dBFS; with AD8138 Driving ADC Inputs, 1 V p-p Input Range



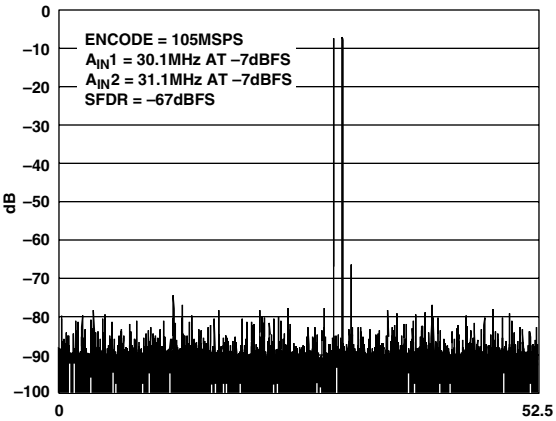
TPC 7. FFT: FS = 31 MSPS, A_{IN} = 8 MHz @ –0.5 dBFS, Differential, 1 V p-p Input Range



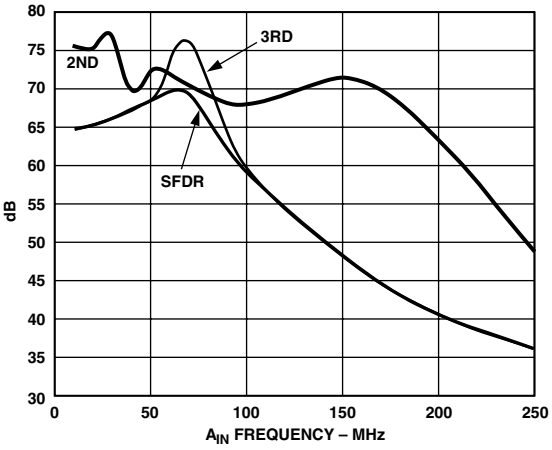
TPC 10. FFT: FS = 31 MSPS, A_{IN} = 8 MHz @ –0.5 dBFS; with AD8138 Driving ADC Inputs, 1 V p-p Input Range



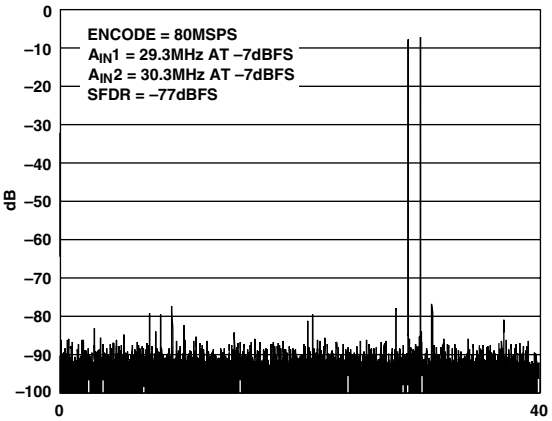
TPC 8. Harmonic Distortion (Second and Third) and SFDR vs. A_{IN} Frequency (1 V p-p, FS = 105 MSPS)



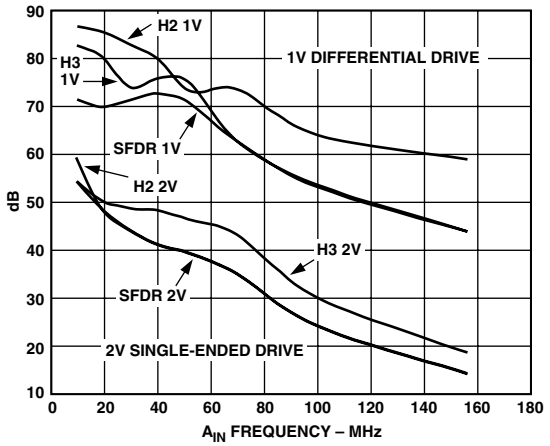
TPC 11. Two–Tone Intermodulation Distortion (30 MHz and 31 MHz; 1 V p-p, FS = 105 MSPS)



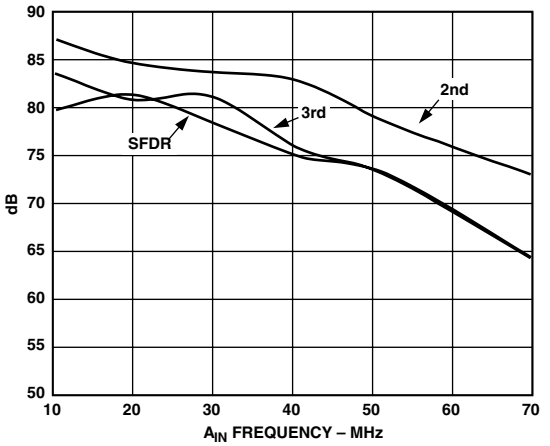
TPC 9. Harmonic Distortion (Second and Third) and SFDR vs. A_{IN} Frequency (1 V p-p, FS = 80 MSPS)



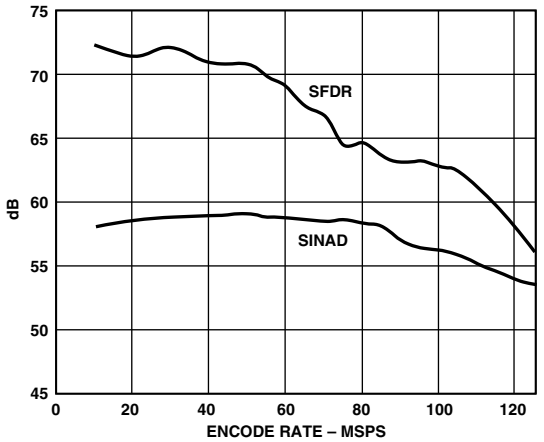
TPC 12. Two–Tone Intermodulation Distortion (29.3 MHz, 30.3 MHz; 1 V p-p, FS = 80 MSPS)



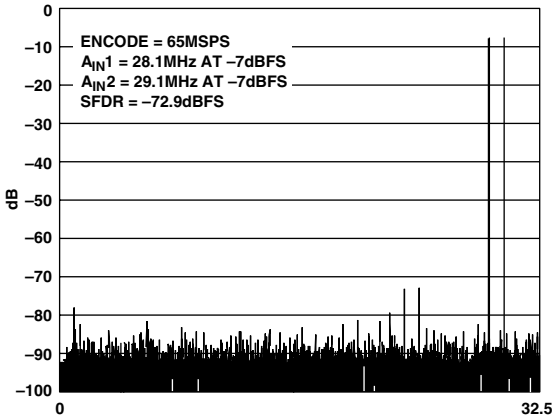
TPC 13. Harmonic Distortion (Second and Third) and SFDR vs. A_{IN} Frequency (FS = 65 MSPS)



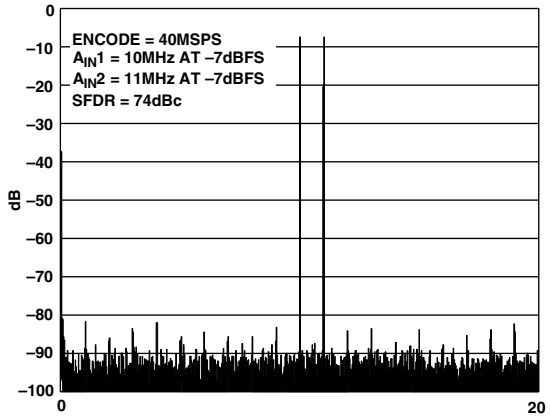
TPC 14. Harmonic Distortion (Second and Third) and SFDR vs. A_{IN} Frequency (1 V p-p, FS = 40 MSPS)



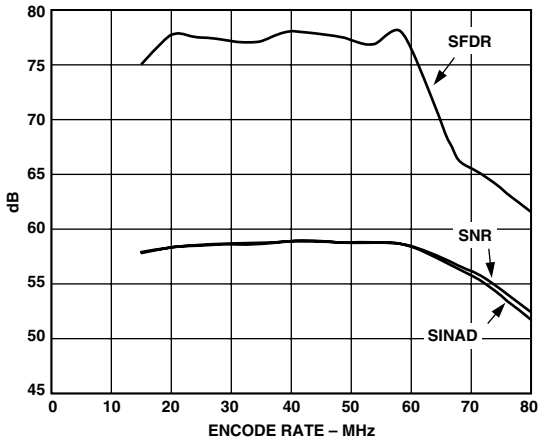
TPC 15. SINAD and SFDR vs. Encode Rate (f_{IN} = 10.3 MHz, 105 MSPS Grade) A_{IN} = –0.5 dBFS Differential, 1 V p-p Analog Input Range



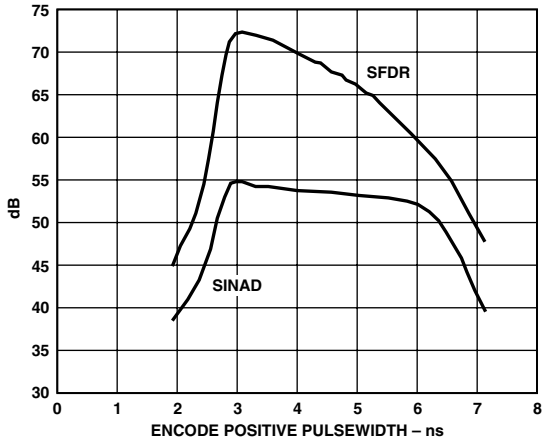
TPC 16. Two-Tone Intermodulation Distortion (28 MHz, 29 MHz; 1 V p-p, FS = 65 MSPS)



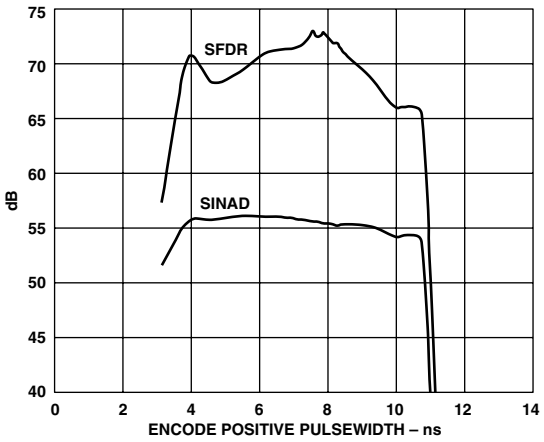
TPC 17. Two–Tone Intermodulation Distortion (10 MHz, 11 MHz; 1 V p-p, FS = 40 MSPS)



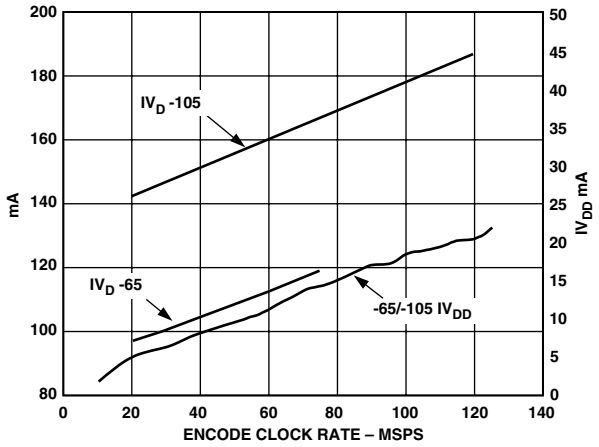
TPC 18. SINAD and SFDR vs. Encode Rate (A_{IN} = 10.3 MHz, 65 MSPS Grade) A_{IN} = –0.5 dBFS Differential, 1 V p-p Analog Input Range



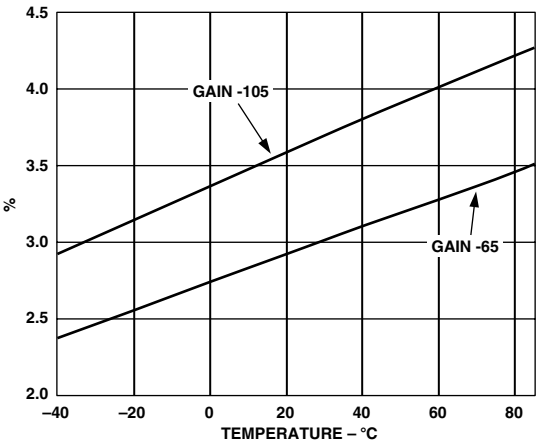
TPC 19. SINAD and SFDR vs. Encode Pulsewidth High. A_{IN} = –0.5 dBFS Single-Ended, 1 V p-p Analog Input Range 105 MSPS



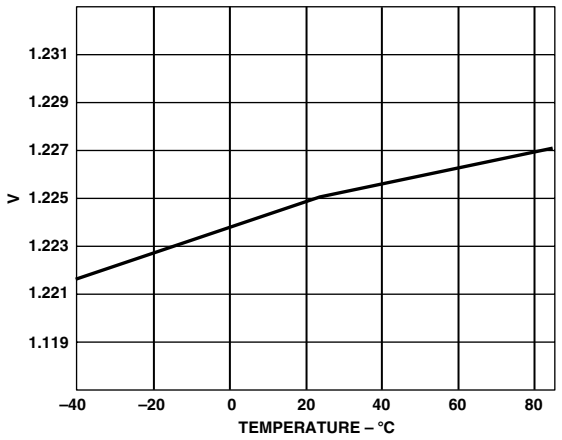
TPC 22. SINAD and SFDR vs. Encode Pulsewidth High. A_{IN} = –0.5 dBFS Single Ended, 1 V p-p Analog Input Range 65 MSPS



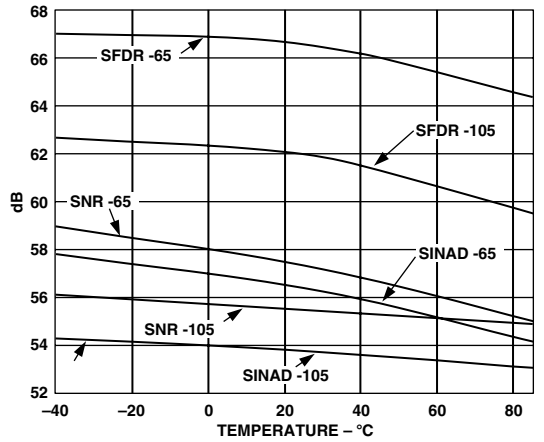
TPC 20. I_{VD} and I_{VDD} vs. Encode Rate (A_{IN} = 10.3 MHz, @ –0.5 dBFS). -65/-105 MSPS Grade Cl = 5 pF



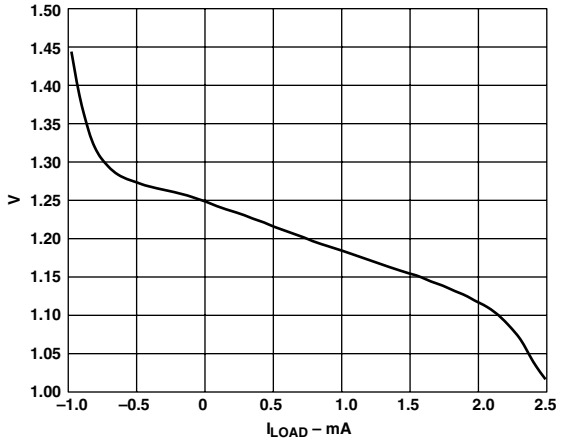
TPC 23. Gain Error vs. Temperature. A_{IN} = 10.3 MHz, -65 MSPS Grade, -105 MSPS Grade, 1 V p-p



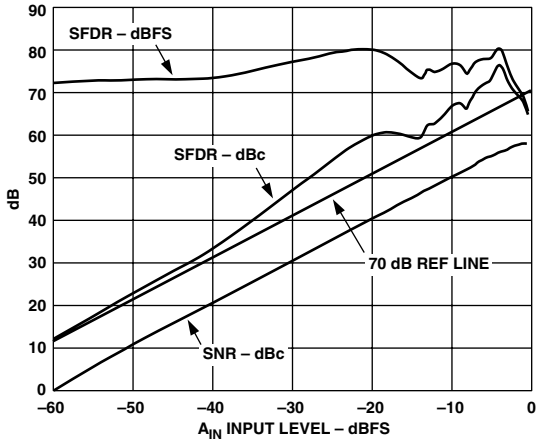
TPC 21. V_{REF} Output Voltage vs. Temperature (I_{LOAD} = 300 μA)



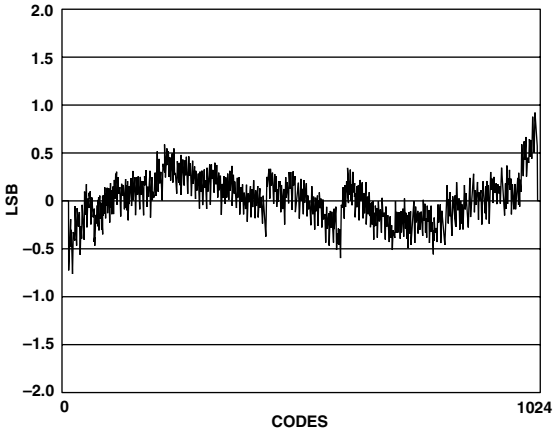
TPC 24. SNR, SINAD, SFDR vs. Temperature. A_{IN} = 10.3 MHz , -65 MSPS Grade, -105 MSPS Grade, 1 V p-p



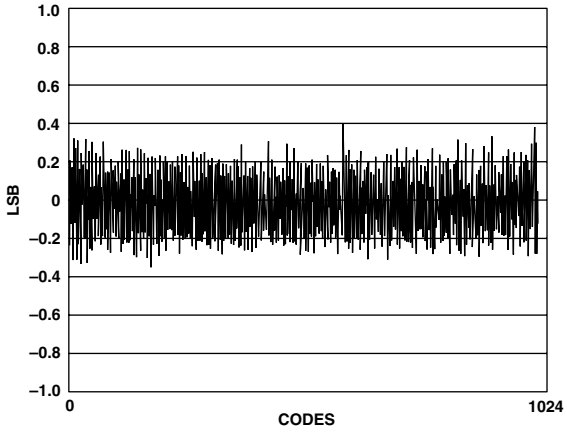
TPC 25. V_{REF} vs. I_{LOAD}



TPC 27. SFDR vs. A_{IN} Input Level. 10.3 MHz A_{IN} @ 80 MSPS



TPC 26. Typical INL Plot. 10.3 MHz A_{IN} @ 80 MSPS



TPC 28. Typical DNL Plot. 10.3 MHz A_{IN} @ 80 MSPS

THEORY OF OPERATION

The AD9218 ADC architecture is a bit-per-stage pipeline-type converter utilizing switch capacitor techniques. These stages determine the 7 MSBs and drive a 3-bit flash. Each stage provides sufficient overlap and error correction allowing optimization of comparator accuracy. The input buffers are differential, and both sets of inputs are internally biased. This allows the most flexible use of ac-coupled or dc-coupled and differential or single-ended input modes. The output staging block aligns the data, carries out the error correction, and feeds the data to output buffers. The set of output buffers are powered from a separate supply, allowing adjustment of the output voltage swing. There is no discernible difference in performance between the two channels.

USING THE AD9218

ENCODE Input

Any high-speed A/D converter is extremely sensitive to the quality of the sampling clock provided by the user. A Track/Hold circuit is essentially a mixer. Any noise, distortion, or timing jitter on the clock will be combined with the desired signal at the A/D output. For that reason, considerable care has been taken in the design of the ENCODE input of the AD9218, and the user is advised to give commensurate thought to the clock source. The ENCODE input is fully TTL/CMOS-compatible.

Digital Outputs

The digital outputs are TTL/CMOS-compatible for lower power consumption. During power-down, the output buffers transition to a high impedance state. A data format selection option supports either two's complement (set high) or offset binary output (set low) formats.

Analog Input

The analog input to the AD9218 is a differential buffer. For best dynamic performance, impedance at AIN and $\overline{AIN}$ should match. Special care was taken in the design of the analog input section of the AD9218 to prevent damage and corruption of data when the input is overdriven. The nominal input range is 1.024 V p-p. Optimum performance is obtained when the part is driven differentially where common mode noise is minimized and even order harmonics are reduced. An example of driving the AD9218 differentially via a wideband RF transformer for ac-coupled applications is shown in Figure 12. Applications that require dc-coupled differential drive can be accommodated using the AD8138 differential output op amp, shown in Figure 13.

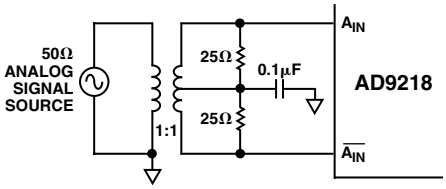


Figure 12. Using a Wideband Transformer to Drive the AD9218

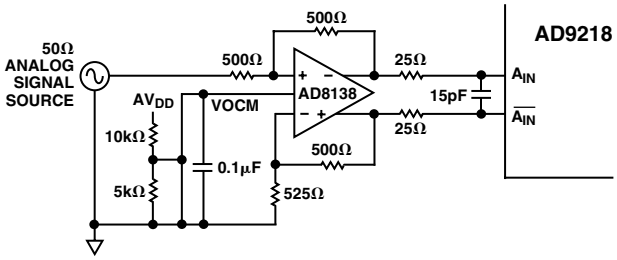


Figure 13. Using the AD8138 to Drive the AD9218

Voltage Reference

A stable and accurate 1.25 V voltage reference is built into the AD9218 (VREF OUT). In normal operation, the internal reference is used by strapping Pin 5 ($REF_{IN}A$) and Pin 7 ($REF_{IN}B$) to Pin 6 (REF_{OUT}). The input range for each channel can be adjusted independently by varying the reference voltage inputs applied to the AD9218. No appreciable degradation in performance occurs when the reference is adjusted ±5%. The full-scale range of the ADC tracks reference voltage, which changes linearly.

Timing

The AD9218 provides latched data outputs, with five pipeline delays. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the encode command (see Timing Diagram). The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9218. These transients can detract from the converter's dynamic performance.

The minimum guaranteed conversion rate of the AD9218 is 20 MSPS. At clock rates below 20 MSPS, dynamic performance will degrade.

User Select Options

Two pins are available for a combination of operational modes. These options allow the user to power-down both channels, excluding the reference, or just the B channel. Both modes place the output buffers in a high impedance state. Recovery from a power-down state is accomplished in 10 clock cycles following power-on.

The other option allows the user to skew the B Channel output data by one-half a clock cycle. In other words, if two clocks are fed to the AD9218 and are 180 degrees out of phase, enabling the data align will allow Channel B output data to be available at the rising edge of Clock A. If the same encode clock is provided to both channels and the data align pin is enabled, output data from Channel B will be 180 degrees out of phase with respect to Channel A. If the same encode clock is provided to both channels and the data align pin is disabled, both outputs are delivered on the same rising edge of the clock.

APPLICATIONS

The wide analog bandwidth of the AD9218 makes it attractive for a variety of high-performance receiver and encoder applications. Figure 14 shows the dual ADC in a typical low cost I and Q demodulator implementation for cable, satellite, or wireless LAN modem receivers. The excellent dynamic performance of the ADC at higher analog input frequencies and encode rates empowers users to employ direct IF sampling techniques. IF sampling eliminates or simplifies analog mixer and filter stages to reduce total system cost and power.

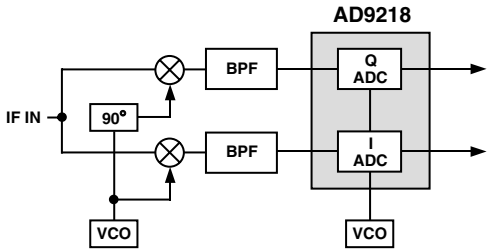


Figure 14. Typical I/Q Demodulation Scheme

EVALUATION BOARD

The AD9218 evaluation board offers an easy way to test the AD9218. It provides a means to drive the analog inputs single-endedly or differentially. Differential drive can be tested through a wideband RF transformer or a differential output operational amplifier, the AD8138. The two encode clocks are accessible via on-board SMB connectors J2, J7. These clocks are buffered on board to provide the clocks for an on-board DAC and latches. The digital outputs and output clocks are available at two 40-pin connectors, P3 and P4. The board has several different modes of operation, and is shipped in the following configuration:

- Differential Analog Input (RF Transformer Mode)
- Normal Operation Timing Mode
- Internal Voltage Reference

Power Connector

Power is supplied to the board via a detachable 12-pin power strip.

+5 V – Optional Supply for Operational Amplifier
–5 V – Optional Supply for Operational Amplifier
$V_{REF}A$ – Optional External Reference Input
$V_{REF}B$ – Optional External Reference Input
V_{DL} – Supply for Support Logic and DAC
V_{DD} – Supply for ADC Outputs
V_D – Supply for ADC Analog

Analog Inputs

The evaluation board accepts a 1 V analog input signal centered at ground at each analog input. SMB connectors J4 and J6 are used for A_{IN} and B_{IN} respectively. These signals each drive a wideband RF transformer T1, T2, allowing the ADC performance for differential inputs to be measured using a single-ended source. In this mode resistors R35, R33, R39, and R32 should not be in place. Each analog input is terminated on the board with 50 Ω to ground. Each input is ac-coupled on the board through a 0.1 µF capacitor to an on-chip resistor divider that provides dc bias. Single-ended performance can be measured by bypassing the transformers using connectors SMB J5 (Channel A) and J1 (Channel B). In this mode, place a 0 Ω resistor at R35 and R33 (A Channel) and place R39 and R32 (B Channel). Note that the inverting analog inputs are terminated on the board with 25 Ω (optimized for differential operation). When driving the board single-ended these resistors (R1, R3) can be changed to 50 Ω to provide balanced inputs. The operational amplifier can be used by connecting to J5 (Channel A) and J1 (Channel B). The ac-coupling capacitors on the top level should be removed from the board to use the operational amplifier. The components to use the op amp should be placed on the bottom of the board. See PCB Bill of Materials list for values.

Encode

The encode clock for Channel A uses SMB connector J7. Channel B encode uses SMB connector J2. Each clock input is terminated on the board with 50 Ω to ground. The input clocks are fed directly to the ADC and to buffers U5, U6, which drive the DAC and latches. The clock inputs are TTL-compatible.

Voltage Reference

The AD9218 has an internal 1.25 V voltage reference. An external reference for each channel may be employed instead. The evaluation board is configured for the internal reference (use jumpers E18–E1 and E17–E19). To use external references, connect to $V_{REF}A$ and $V_{REF}B$ pins on the power connector P1 and use jumpers E20–E18 and E19–E21.

Normal Operation Mode

In this mode both converters are clocked by the same encode clock, latency is five clock cycles (see Timing Diagram). Signal S1 (Pin 8) is held high and signal S2 (Pin 9) is held low. This is set with the jumpers labeled S1 and S2 (near the analog input).

Data Align Mode

In this mode channel B output is delayed an additional one-half cycle. Signals S1 (Pin 8) and signal S2 (Pin 9) are both held high. This is set with the jumpers labeled S1 and S2 (near the analog input).

Data Format Select

Data Format Select sets the output data format and the gain of the ADC. Setting DFS (Pin 4) low sets the output format to be offset binary and gain of 1; setting DFS high sets the output to be two's complement and gain of 1. Removing the jumper for DFS sets the output data format to offset binary and a gain of 2; setting DFS to the middle selection sets the output data format to two's complement and a gain of 2.

PCB Bill of Materials

#	Qty	REFDES	Device	Package	Value
1	29	C1, C3–C15, C20–C25, C27–C35	Capacitor	0603	0.1 µF
2	2	C2, C36	Capacitor	0603	15 pF
3	7	C16, C17, C18, C19, C26, C37, C38	Capacitor	TAJD	10 µF
6	8	J1, J2, J3, J4, J5, J6, J7, J8	Connector	SMB	
7	3	P1, P4, P11	4-Pin Power Connector	TB4	Wieland 25.531.3425.0 Z5.602.5453.0
8	2	P2, P3	HEADER40		
10	8	R1–R4, R22–R24, R30	Resistor	0603	25 Ω
11	10	R5–R12, R34, R37	Resistor	0603	50 Ω
12	2	R13, R14	Resistor	0603	2 kΩ
13	6	R15, R17, R18, R26, R29, R31	Resistor	0603	500 Ω
14	2	R16, R25	Resistor	0603	525 Ω
15	2	R19, R27	Resistor	0603	4 kΩ
16	8	R20, R32, R33, R35, R36, R38–R40	Resistor	0603	0 Ω
17	2	R21, R28	Resistor	0603	1 kΩ
18	2	T1, T2	Transformer	ADT-1-1WT	Minicircuits
19	1	U1	AD9218	LQFP48	
20	2	U2, U3	74LCX821	SO24M3	
21	1	U4	AD9763	LQFP48	
22	2	U5, U6	74LCX86	SO14	
23	4	U7, U8, U9, U10	Resistor Array	CTS20	22 Ω
24	2	U11, U12	AD8138	SO8NB	

NOTE
R22, R23, R24, R30, R32, R33, R35, R36, R38, R39, R40, C2, C36 not placed on board.

Data Outputs

The ADC digital outputs are latched on the board by two LCX821s, the latch outputs are available at the two 40-pin connectors at Pins 23–33 on P3 (Channel A) and Pins 23–33 on P4 (Channel B). The latch output clocks (data ready) are available at Pin 4 on P3 (Channel A) and Pin 4 on P4 (Channel B). The data ready signal on Channel B can be aligned with Clock A input by connecting E43–E42 or aligned with Clock B input by connecting E42–E33.

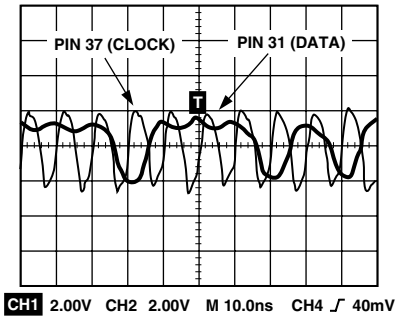


Figure 15. Data Output and Clock at 80-Pin Connector

DAC Outputs

Each channel is reconstructed by an on-board dual channel DAC, an AD9763. This DAC is intended to assist in debug only. It should not be used to measure the performance of the ADC. It is a current output DAC with on-board 50 Ω termination resistors. Figure 16 is representative of the DAC output with a full-scale analog input. The scope setting was low bandwidth, 50 Ω termination.

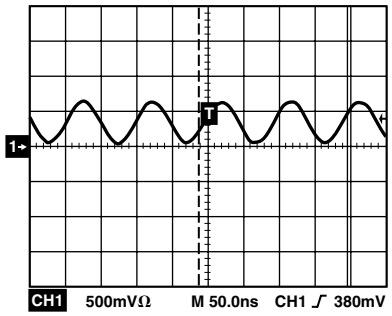


Figure 16. DAC Output

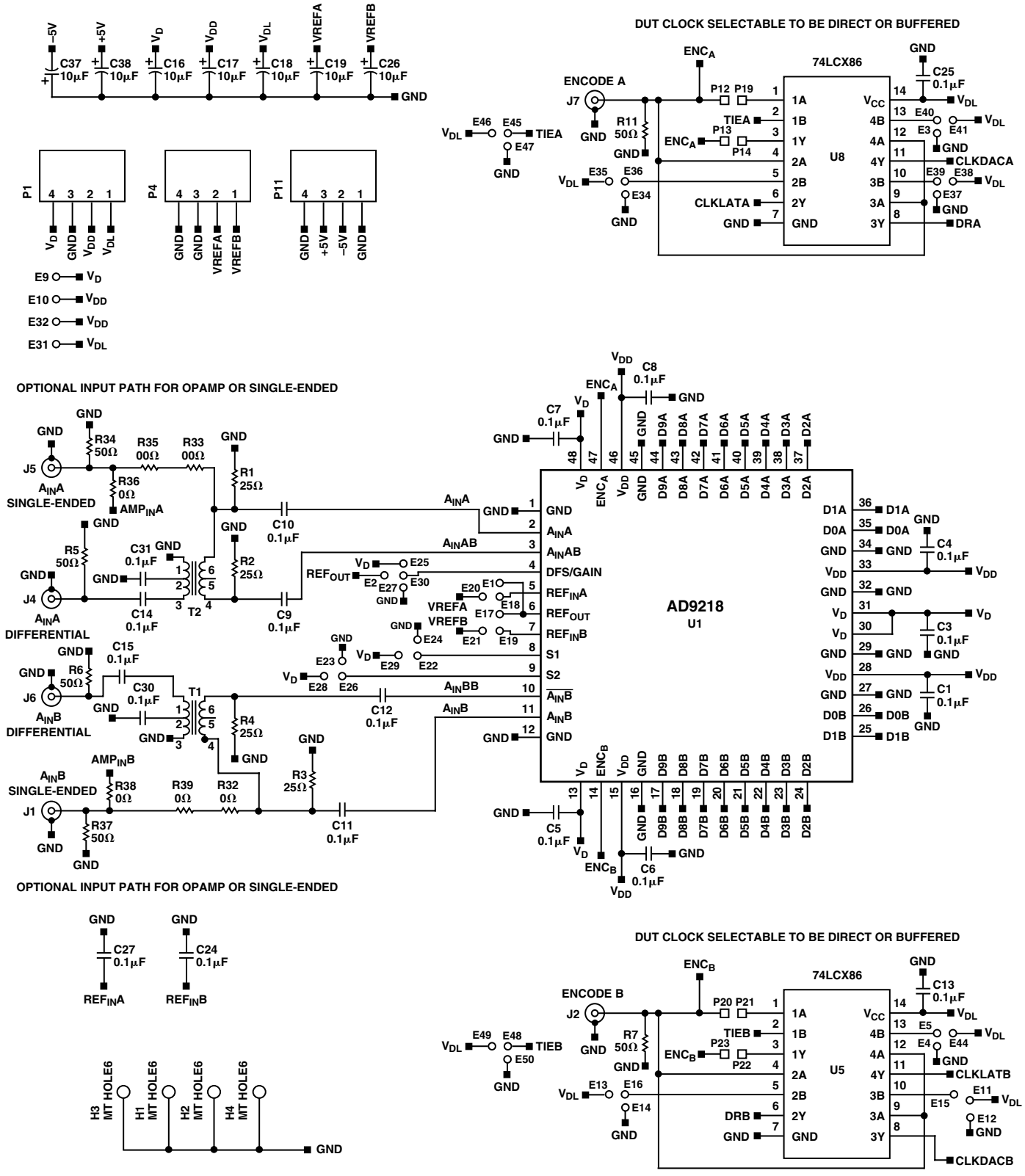


Figure 17a. PCB Schematic

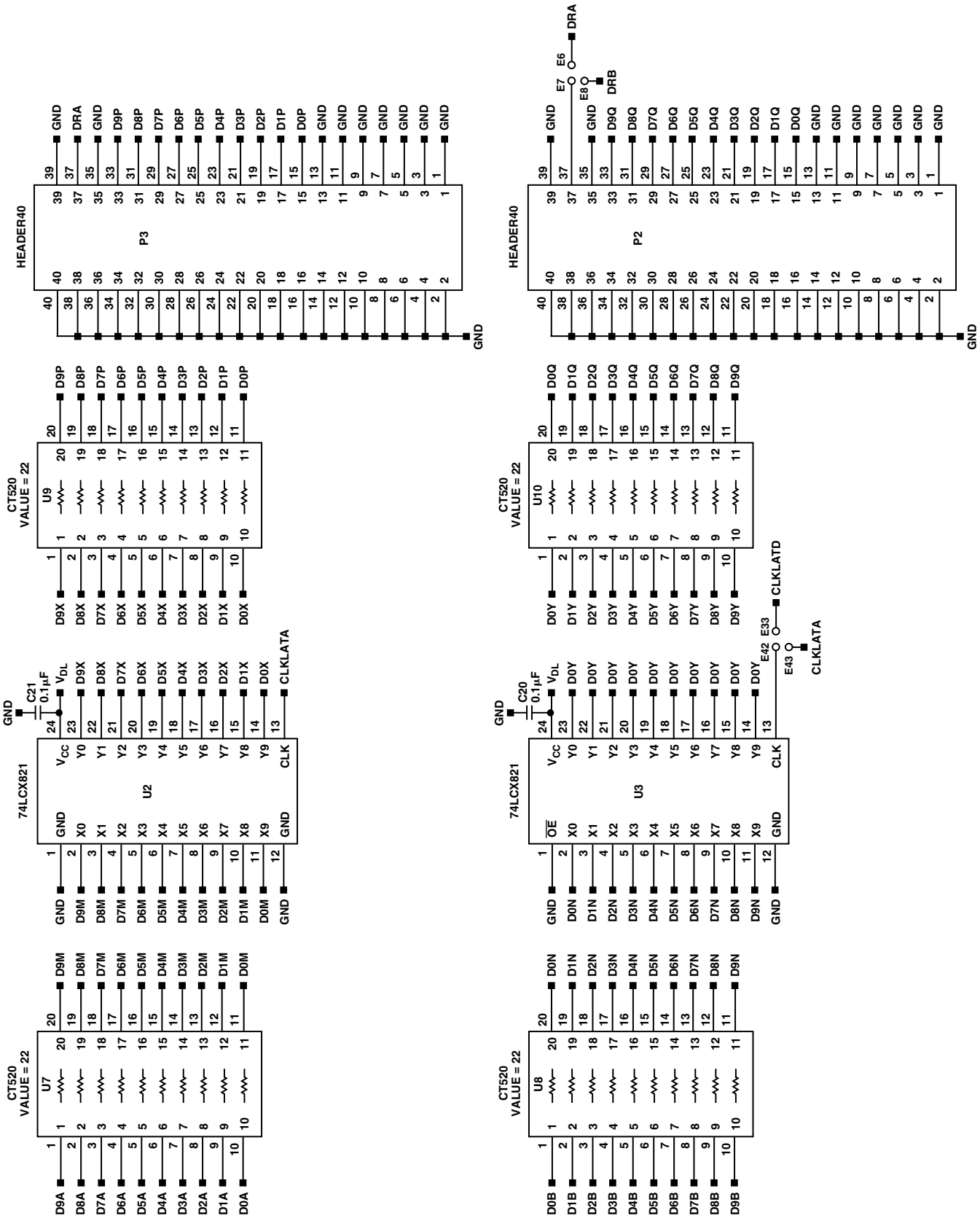


Figure 17b. PCB Schematic

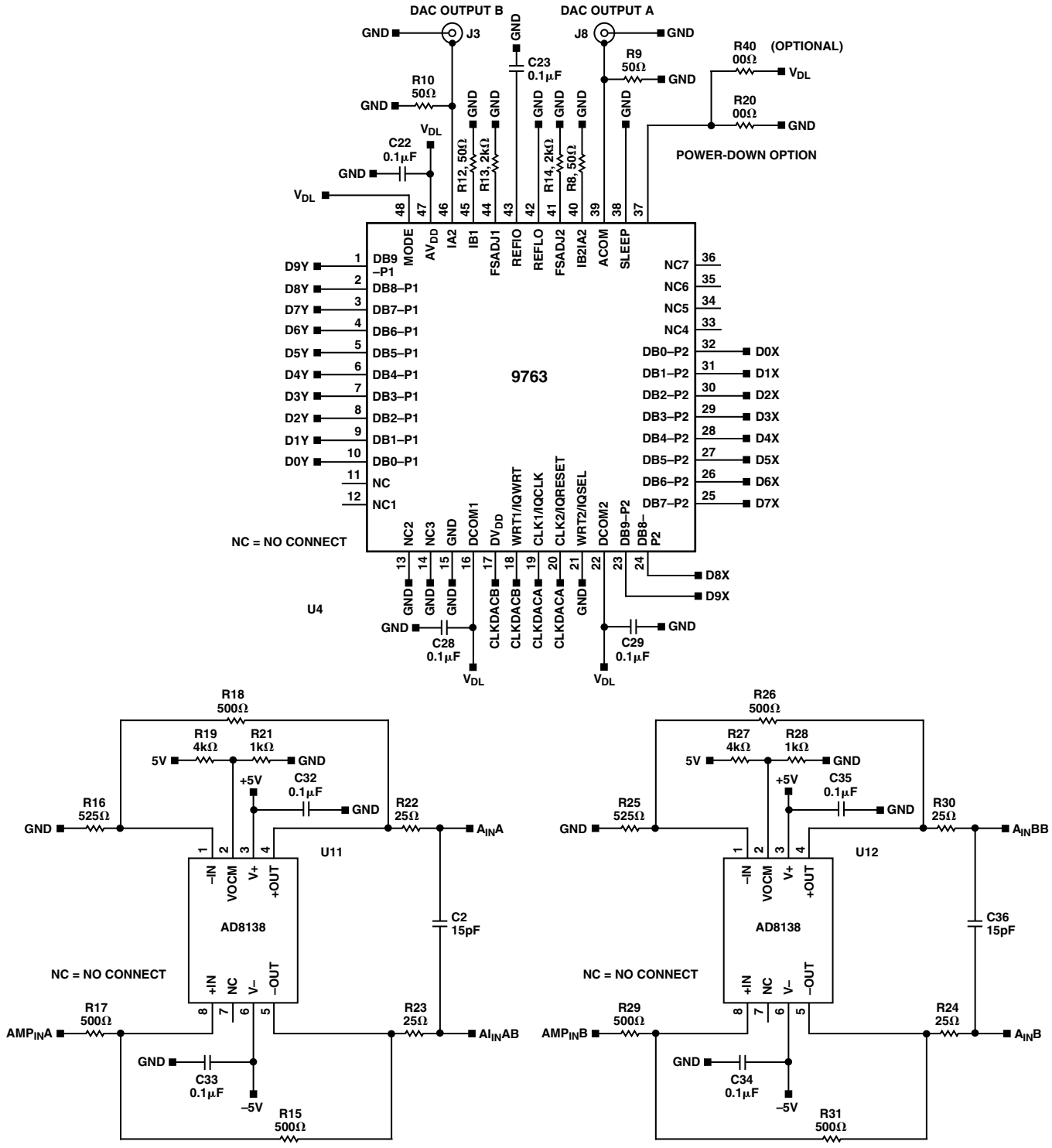


Figure 17c. PCB Schematic

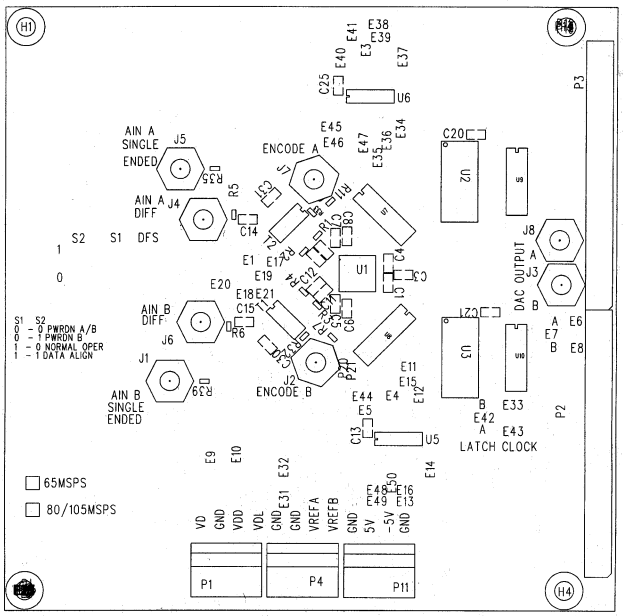


Figure 18. PCB Top Side Silkscreen

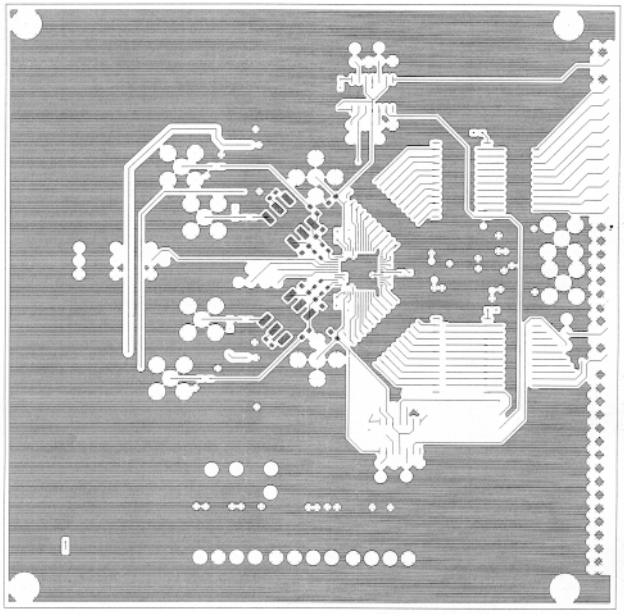


Figure 19. PCB Top Side Copper

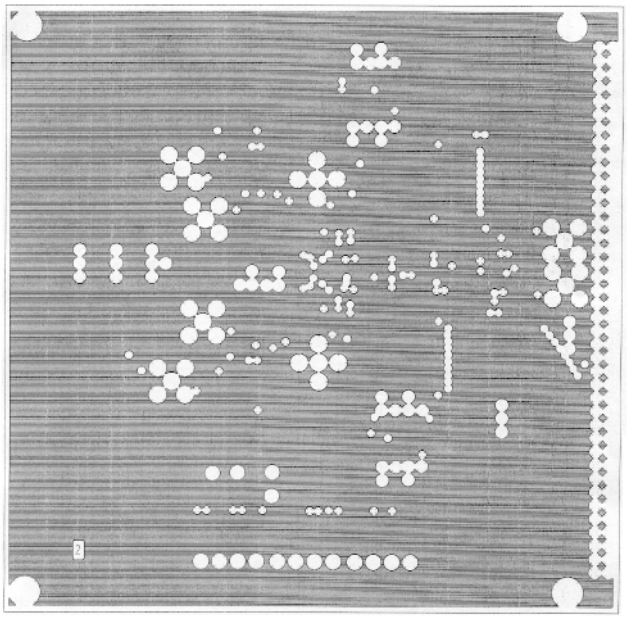


Figure 20. PCB Ground Layer

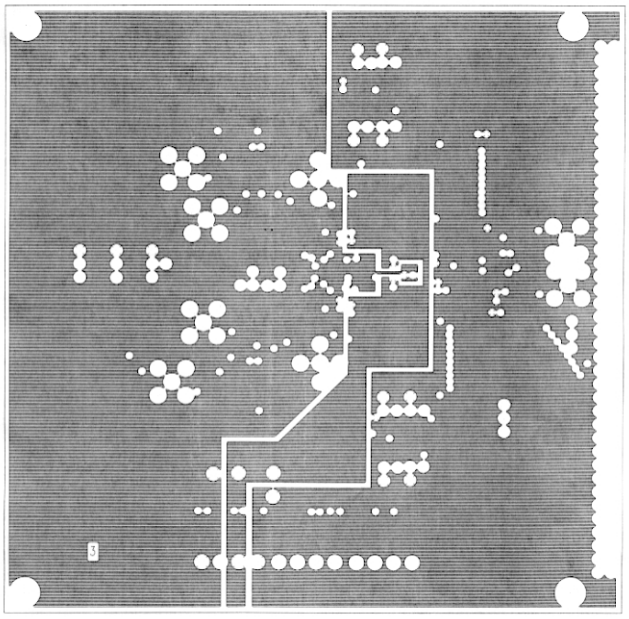


Figure 21. PCB Split Power Plane

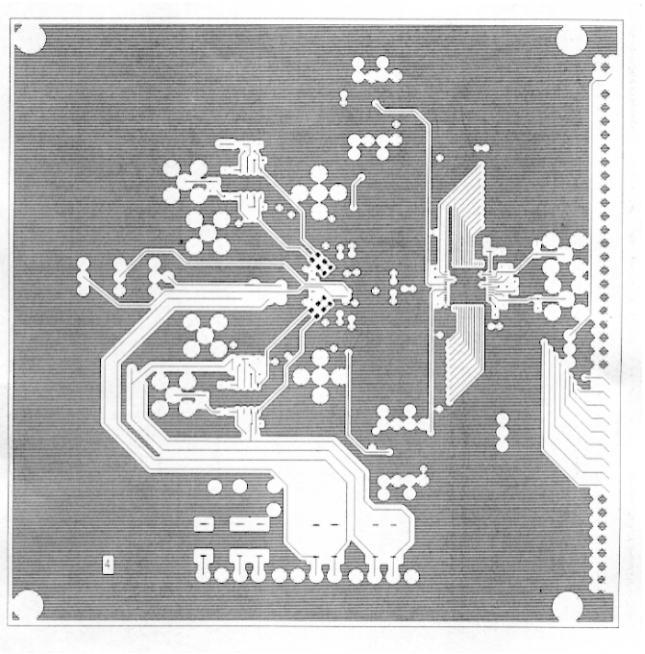


Figure 22. PCB Bottom Side Copper

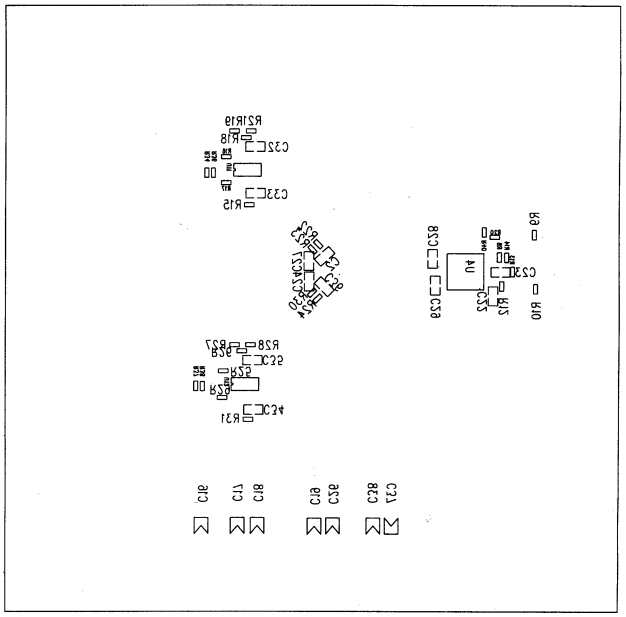


Figure 23. Bottom Side Silkscreen

Troubleshooting

If the board does not seem to be working correctly, try the following:

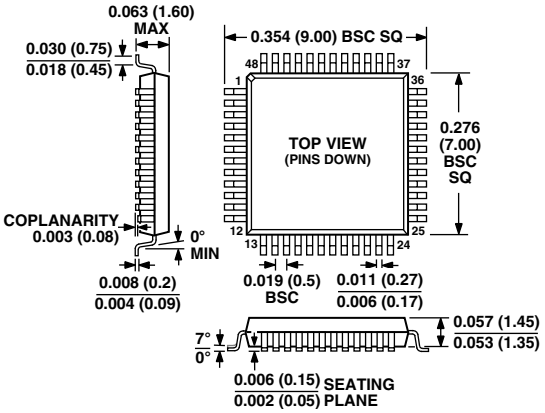
- Verify power at IC pins.
- Check that all jumpers are in the correct position for the desired mode of operation.
- Verify V_{REF} is at 1.23 V.
- Try running encode clock and analog inputs at low speeds (20 MSPS/1 MHz) and monitor LCX821 outputs, DAC outputs, and ADC outputs for toggling.

The AD9218 Evaluation Board is provided as a design example for customers of Analog Devices, Inc. ADI makes no warranties, express, statutory, or implied, regarding merchantability or fitness for a particular purpose.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Lead LQFP (ST-48)



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