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AT91RM9200 Development Kit

User Guide





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Section 1

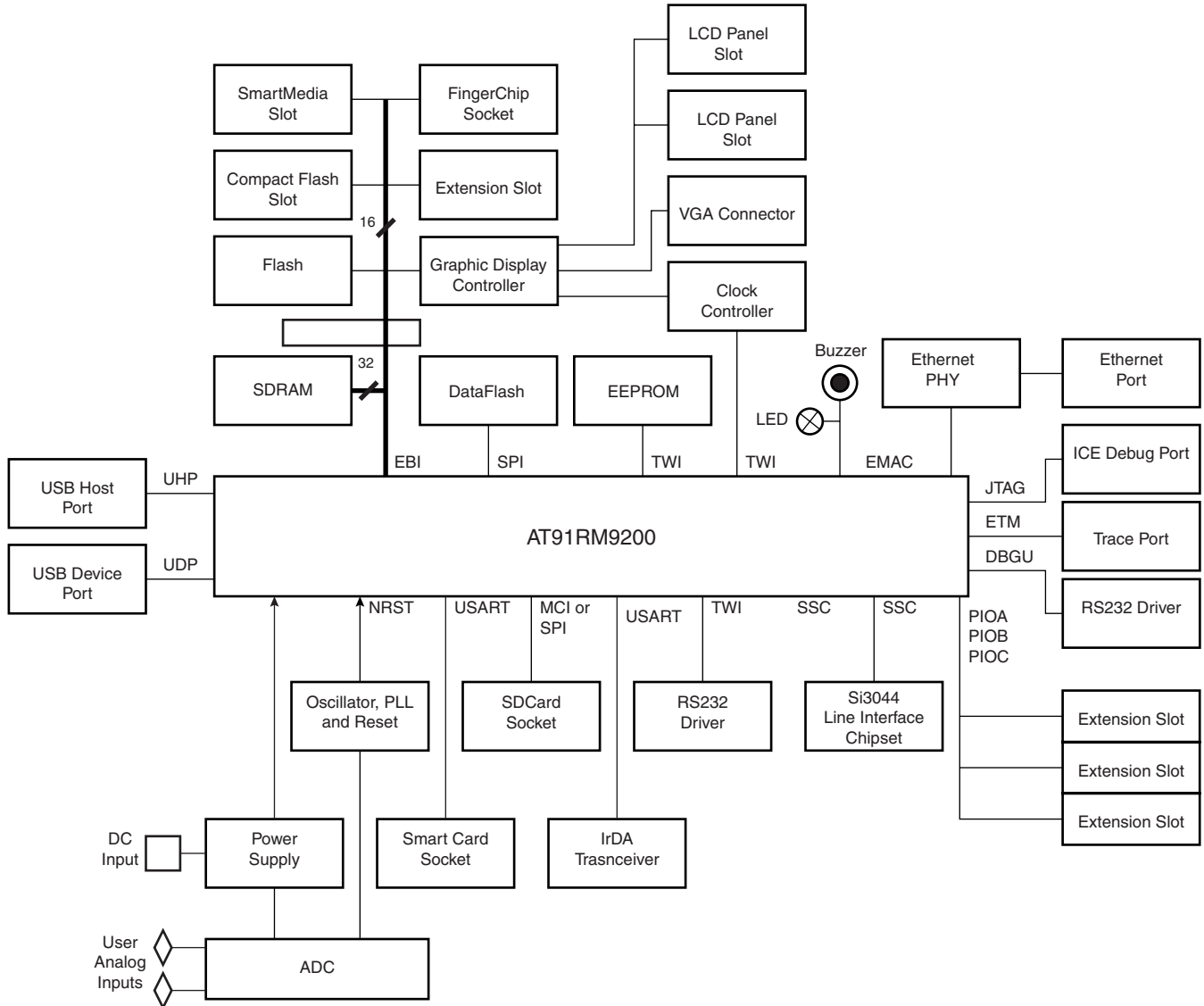
Overview

-
- 1.1 Scope** The AT91RM9200 Development Board enables real-time code development and evaluation. It supports the AT91RM9200 ARM9-based 32-bit RISC microcontroller.
- This guide focuses on the AT91RM9200 Development Board as an evaluation and demonstration platform:
- Section 1 is this overview.
 - Section 2 gives information on setting up the installation.
 - Section 3 contains a description of the development board.
 - Section 4 details the configuration straps.
 - Section 5 shows board schematics.
-
- 1.2 Deliverables** The development kit is delivered with:
- One AC adapter 100 - 240V ~ 1.0A, 50 - 60 Hz
 - One modem RS232 cable
 - One RJ45 Ethernet crossed cable
 - One A/B-type USB cable
 - Two power supply cables, one US format, one French format
 - One CD-ROM containing summary and full datasheets, datasheets with electrical and mechanical characteristics, application notes and getting started documents for all development boards and AT91 microcontrollers. An AT91 software package with C and assembly listings is also provided. This allows the user to begin evaluating the AT91 ARM[®] Thumb[®] 32-bit microcontroller quickly.
-
- 1.3 The AT91RM9200 Development Board** The board consists of an AT91RM9200 together with the following:
- 2M bytes of parallel Flash memory
 - Four banks of 2M x 32-bit SDRAM
 - 128K bytes of EEPROM with two-wire interface access

Overview

- 8M bytes of serial DataFlash®
- Five communication ports (USB host and device, Ethernet, serial and IrDA)
- Graphic controller with output to a standard VGA monitor
- JTAG/ICE, ETM and debug interface
- Expansion connector

Figure 1-1. AT91RM9200 Development Board Block Diagram






Section 2

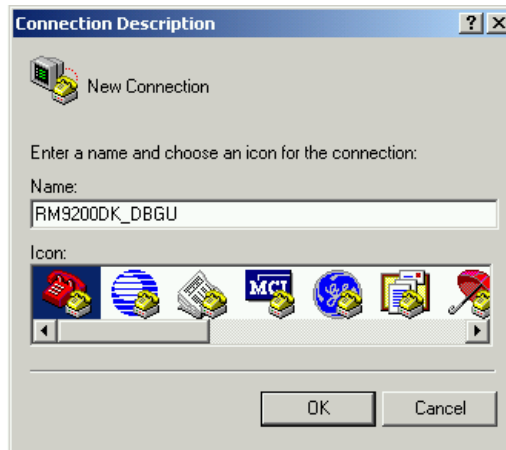
Setting Up the AT91RM9200 Development Board

- | | | |
|------------|------------------------------|--|
| 2.1 | Electrostatic Warning | The AT91RM9200 development board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element. |
| 2.2 | Requirements | In order to connect the AT91RM9200 development board, the following elements are required: <ul style="list-style-type: none">■ The AT91RM9200 development board itself■ Power supply cable capable of supplying 7V to 12V at 1A (not supplied) |
| 2.3 | Powering Up the Board | DC power is supplied to the board via the 2.1 mm socket (J1). The polarity of the power supply is not critical. The minimum voltage required is 7V.

The board has a voltage regulator providing +3.3V. The regulator allows the input voltage range to be from 7V to 12V. |

2.4 Connecting the Board

- Using the RS232 cable supplied in the AT91RM9200-DK kit, connect the board to your PC via the Serial Debug Port (J23).
- Start the HyperTerminal application: 
- In the window *Connection Description*, enter a name for the connection, e.g., “RM9200K_DBGU”.

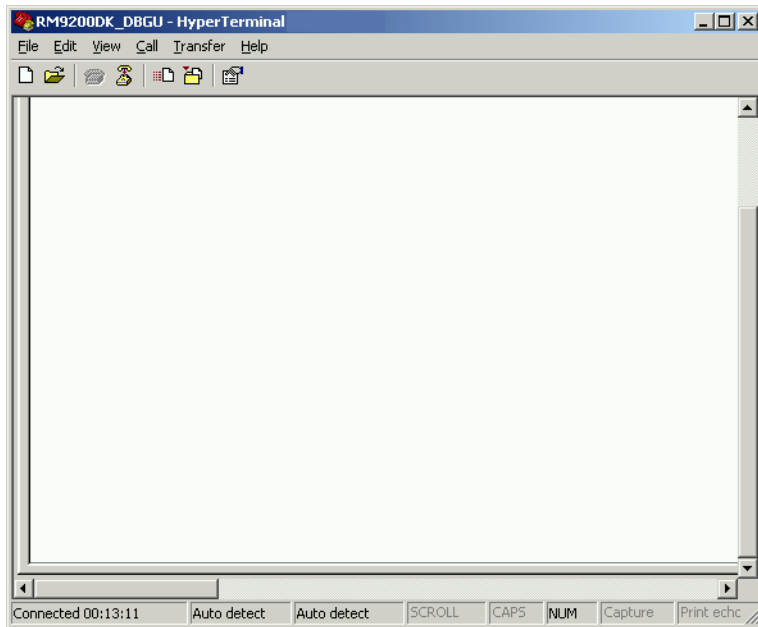


- Click on *OK*.
- In the window *Connect To*, click on the drop-down list arrow at *Connect using:*. Select the COM port used.

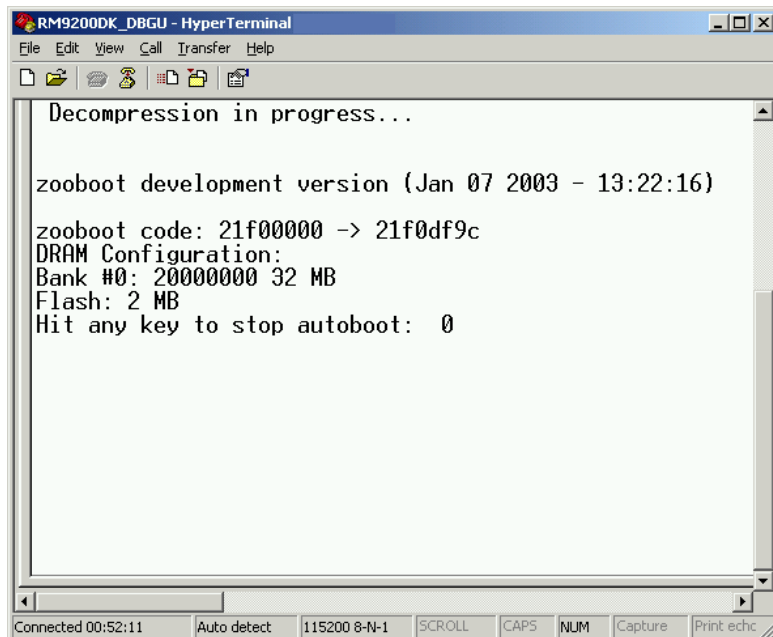


- Click on *OK*.
- Set the serial parameters of the COM port as follows:
 - Bit rate: 115 kbps
 - Data bit: 8
 - Parity: NONE
 - Stop bit: 1
 - Flux control: NONE
- Click on *OK*.

- The AT91RM9200-DK and your PC are connected, as indicated in the lower left-hand corner of the console and by the title bar.



- Press the RESET button on the board.
- A message is sent from the board to the HyperTerminal console. Note that this message can vary depending on the version of Zooboot.



2.5 Getting Started with the AT91RM9200

The AT91RM9200 Development Kit is delivered with a CD-ROM containing all necessary information and step-by-step procedures for working with the most common development toolchains. Please refer to this CD-ROM, or to the AT91 web site, <http://www.atmel.com/products/AT91/>, for the most up-to-date information on getting started with the AT91RM9200.

Setting Up the AT91RM9200 Development Board



Section 3

Board Description

-
- 3.1 AT91RM9200 Processor**
- Incorporates the ARM920T™ ARM® Thumb® Processor
 - 200 MIPS at 180 MHz
 - 16-KByte Data Cache, 16-KByte Instruction Cache, Write Buffer
 - Memory Management Unit
 - In-circuit Emulator including Debug Communication Channel
 - Mid-level Implementation Embedded Trace Macrocell
 - Additional Embedded Memories
 - 16K Bytes of SRAM and 128K Bytes of ROM
 - External Bus Interface (EBI)
 - Supports SDRAM, Static Memory, Burst Flash, Glueless Connection to CompactFlash®, SmartMedia™ and NAND Flash
 - System Peripherals:
 - Enhanced Clock Generator and Power Management Controller
 - Two On-chip Oscillators with Two PLLs
 - Very Slow Clock Operating Mode and Software Power Optimization Capabilities
 - Four Programmable External Clock Signals
 - System Timer Including Periodic Interrupt, Watchdog and Second Counter
 - Real-time Clock with Alarm Interrupt
 - Debug Unit, Two-wire UART and Support for Debug Communication Channel
 - Advanced Interrupt Controller with 8-level Priority, Individually Maskable Vectored Interrupt Sources, Spurious Interrupt Protected
 - Seven External Interrupt Sources and One Fast Interrupt Source
 - Four 32-bit PIO Controllers with Up to 122 Programmable I/O Lines, Input Change Interrupt and Open-drain Capability on Each Line
 - 20-channel Peripheral Data Controller (DMA)
 - Ethernet MAC 10/100 Base-T
 - USB 2.0 Full Speed (12 M-bits per second) Host Double Port and Device Port

Board Description

- Multimedia Card Interface (MCI)
- Three Synchronous Serial Controllers (SSC)
- Four Universal Synchronous/Asynchronous Receiver/Transmitters (USART)
- Master/Slave Serial Peripheral Interface (SPI)
- Two 3-channel, 16-bit Timer/Counters (TC)
- Two-wire Interface (TWI)
- IEEE 1149.1 JTAG Boundary Scan on All Digital Pins

3.2 Memory

- 2-Mbyte parallel Flash memory
- Four banks of 2M x 32-bit SDRAM
- 128-Kbyte EEPROM with 2-wire interface
- 8-Mbyte serial DataFlash

3.3 Memory Card

- SD Card/MMC
 - Supports MultiMedia and SD Card
 - Analog switches provide support for DataFlash Card
- Smart Media[®] Socket
- CompactFlash[®] Socket
- Smart Card Interface

3.4 Clock Circuitry and Analog Functions

- 32.768 kHz standard crystal for the AT91RM9200
- 18.432 MHz standard crystal for the AT91RM9200
- 50 MHz CMOS oscillator for the Display Controller
- Temperature sensor
- Analog-to-digital converter
- FingerChip (Socket only)

3.5 Reset Circuitry

- Reset Controller

3.6 Power Supply Circuitry

- 3.3V DC/DC converter
- 1.8V DC/DC converter

-
- 3.7 Remote Communication**
- Fast Ethernet Physical Layer Single Chip Transceiver
 - IrDA Transceiver
 - Host Interface via RS-232 DB9 male socket
 - Line interface
 - Debug Port via RS-232 DB9 connector
 - Host and Device USB socket

-
- 3.8 User Interface**
- Graphic Display Controller
 - TFT/SNT panel socket
 - 15-pin standard socket for an external VGA monitor
 - On-board buzzer and one LED managed via general PIO lines

-
- 3.9 Expansion Slots**
- Three expansion slots give access to all the microcontroller's signals

-
- 3.10 Debug Interface**
- 38-pin trace Port socket
 - 20-pin JTAG interface connector
 - Serial Debug Unit

Board Description



Section 4

Configuration Straps

4.1 Configuration Straps and Jumper Settings

Table 4-1 gives details on configuration straps and jumper settings on the AT91RM9200 development board and their default settings.

Table 4-1. Configuration Straps and Jumper Settings

Designation	Default Setting	Feature
S1	Closed	The earth plane and the GDN potential are connected.
S3	Closed	The ETM reset (NSRST) and the System Reset (NRST) are connected.
S4	Closed	The PD6/DTXD PIO line is connected to the READY/NBUSY output signal of the SPI DataFlash (MN13).
S5	Opened	The Write Protect feature of the SPI DataFlash (MN13) is disabled.
S6	Closed	The PA26/ TWCK /IRQ1 signal is connected to three remote devices (MN14, MN33, MN34).
S7	Closed	The PA25/ TWD /IRQ2 signal is connected to three remote devices (MN14, MN33, MN34).
S8	Opened	The PA3/ NPCS0 /IRQ5 output signal is not connected to the NCS of the serial DataFlash (MN13).
S9	Closed	The PA5/ NPCS2 /TXD3 signal is connected to the 10-bit SPI ADC (MN15).
S10	Closed	The PC15 I/O line is connected to the 10-bit ADC to read the End Of Conversion event (MN15).
S11	Closed	Not Used: The PS2 Controller is not installed.
S12	Closed	Not Used: The PS2 Controller is not installed.
S13	Closed	The PB12/ TF2 /ETX2 signal is connected to the NRGDT/FSD output signal of the Line Interface (MN23).
S14	Closed	The PB16/ RK2 /ERX2 signal is connected to the NOFHK input signal of the Line Interface (MN23).
S15	Closed	The PB17/ RF2 /ERXDV signal is connected to the NFSYN input signal of the Line Interface (MN23).

Table 4-1. Configuration Straps and Jumper Settings

Designation	Default Setting	Feature
S16	Closed	The PB13/ TK2 /ETX3 signal is connected to the SCLK output signal of the Line Interface (MN23).
S17	Closed	The PB15/ RD2 /ERX2 signal is connected to the SDO output signal of the Line Interface (MN23).
S18	Closed	Not Used: The Front End AC97 is not installed.
S19	Closed	The PA30/ DRXD /CTS2 signal is connected to the receive buffer output of the DBGU transceiver (MN26).
S20	Closed	The AT91RM9200's PC14 PIO line is connected to the NREADY output signal of the Smart Card Interface (MN29).
S21	Closed	The PA17/ TXD0 /TIOA0 is connected to the DATA input/output signal of the Smart Card Interface (MN29).
S22	Closed	The PA22/ RXD2 /TIOB2 is connected to the RX output signal of the IrDA Transceiver (MN30).
S23	Closed	Enables all output signals (DCD1, DSR1, RXD1, CTS1, RI1) of the Transceiver (MN28) used for the RS232 Port COM.
S24	Closed	The PD4 /ETXEN input line is connected to the USB device socket (J28) to detect a host connection.
S25	Closed	The System Reset signal (NRST) is connected to the ICE/JTAG socket (J8, pin 15).
S26	Closed	The NCS2 output signal is connected to the display controller (MN32).
S27	Closed	The NCS0 output signal is connected to the parallel Flash memory (MN21).
S28	Closed	Enables the OE signal from the Atmel FingerChip (MN31). Only the socket is installed.
S29	Closed	The SMCS /NCS3 output signal is connected to the bidirectional buffer used by the Smart Media Connector (MN20B).
S30	Closed	The PA15/ EMDC /TCLK2 output signal is connected to the MDC input signal of the Ethernet Transceiver (MN22).
S31	Closed	The PA16/ EMDIO /IRQ6 input/output signal is connected to the MDIO input/output signal of the Ethernet Transceiver (MN22).
S32	Closed	Disables the power-down mode of the Ethernet Transceiver (MN22).
S33	Closed	Not Used: The Front End AC97 is not installed.
S34	Closed	Not Used: The Front End AC97 is not installed.
S35	Closed	Not Used: The Front End AC97 is not installed.
S36	Closed	Connects the system ground to the Ethernet ground.
S37	Closed	Not Used: The Front End AC97 is not installed.

Table 4-1. Configuration Straps and Jumper Settings

Designation	Default Setting	Feature
S38	Opened	The AT91RM9200 boots up from the parallel Flash Memory.
S39	Closed	Enables the use of the User LED (DS5).
S40	Closed	Not Used: The Buzzer is not installed.

Note: Shaded cells indicate configuration straps/jumpers with open connections.

Note: Signal names in bold indicate that the function is shared between several signals.

Configuration Straps



Section 5

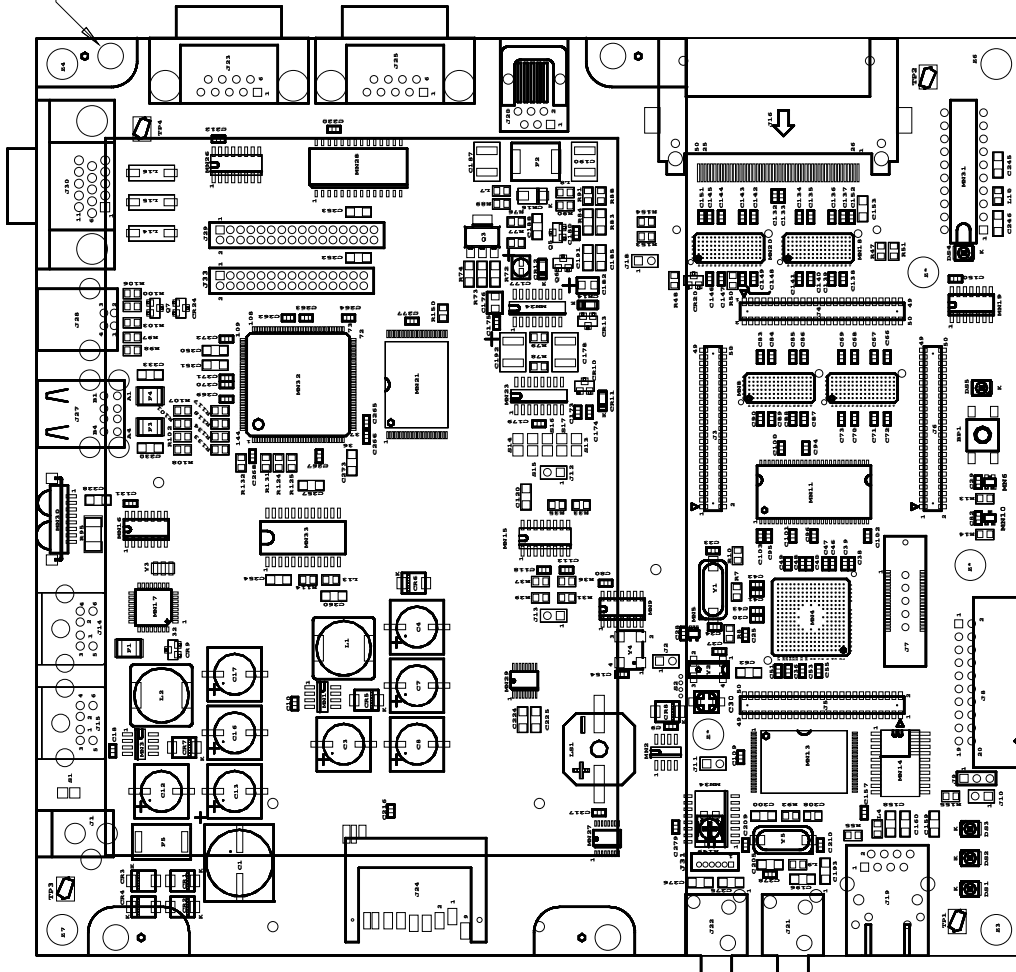
Schematics

5.1 Schematics

This section contains the following schematics:

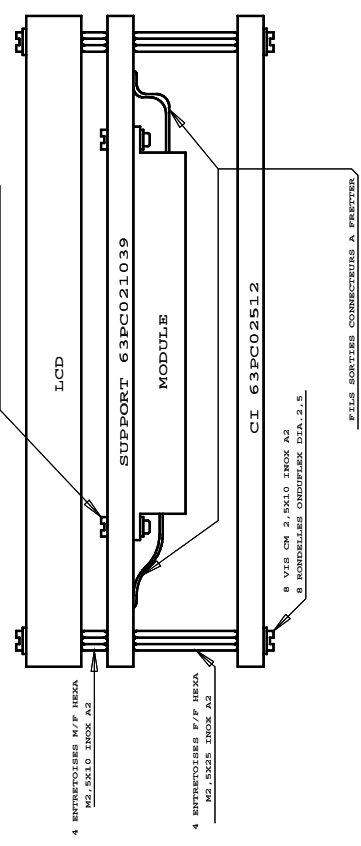
- AT91RM9200 Board Layout - Top View
- AT91RM9200 Board Layout - Bottom View
- Power Supply
- AT91RM9200 Chip
- Buffers
- SDRAM and Flash
- Serial Devices
- PS2 COM Ports
- 3V3 Memory Card
- Ethernet
- DAA
- AC97 Analog Front End
- Serial Interfaces
- Fingerchip
- VGA TFT/CRT Display

VUE FACE ELEMENTS



MONTAGE DU LCD
SUR SUPPORT 63PC021039 VOIR DETAIL

- 2 VIS CM 2,5X6 INOX A2
- 8 RONDELLES OMDUPLEX DIA. 2,5
- 2 BUSHES HMS, 5 INOX A2



- 4 ENTRETOISES M/F HEXA
M2,5X10 INOX A2
- 4 ENTRETOISES F/F HEXA
M2,5X25 INOX A2
- 8 VIS CM 2,5X10 INOX A2
8 RONDELLES OMDUPLEX DIA.2,5
- CI 63PC02512
- FILS SORTIES CONNECTEURS A PRETERRE

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CARTE AT91RM9200-DK

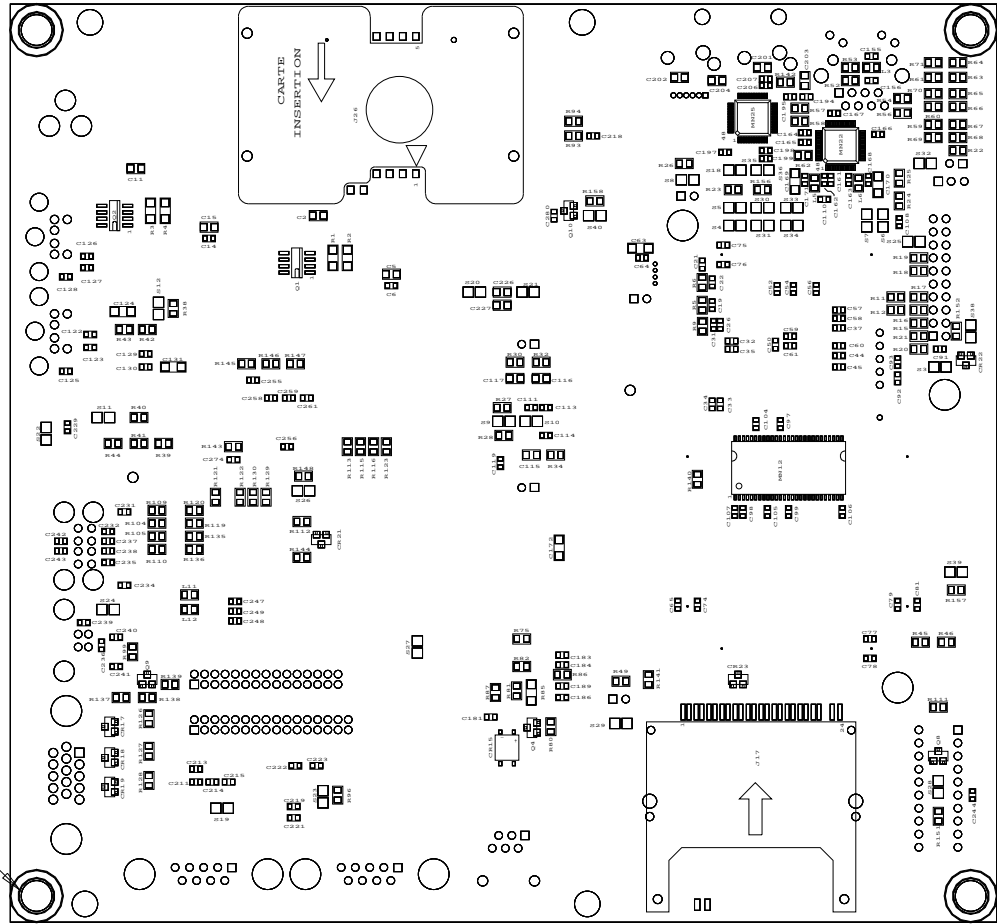
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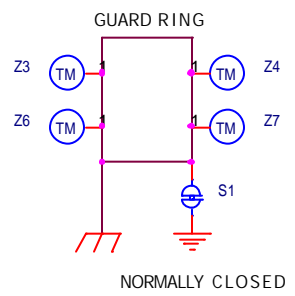
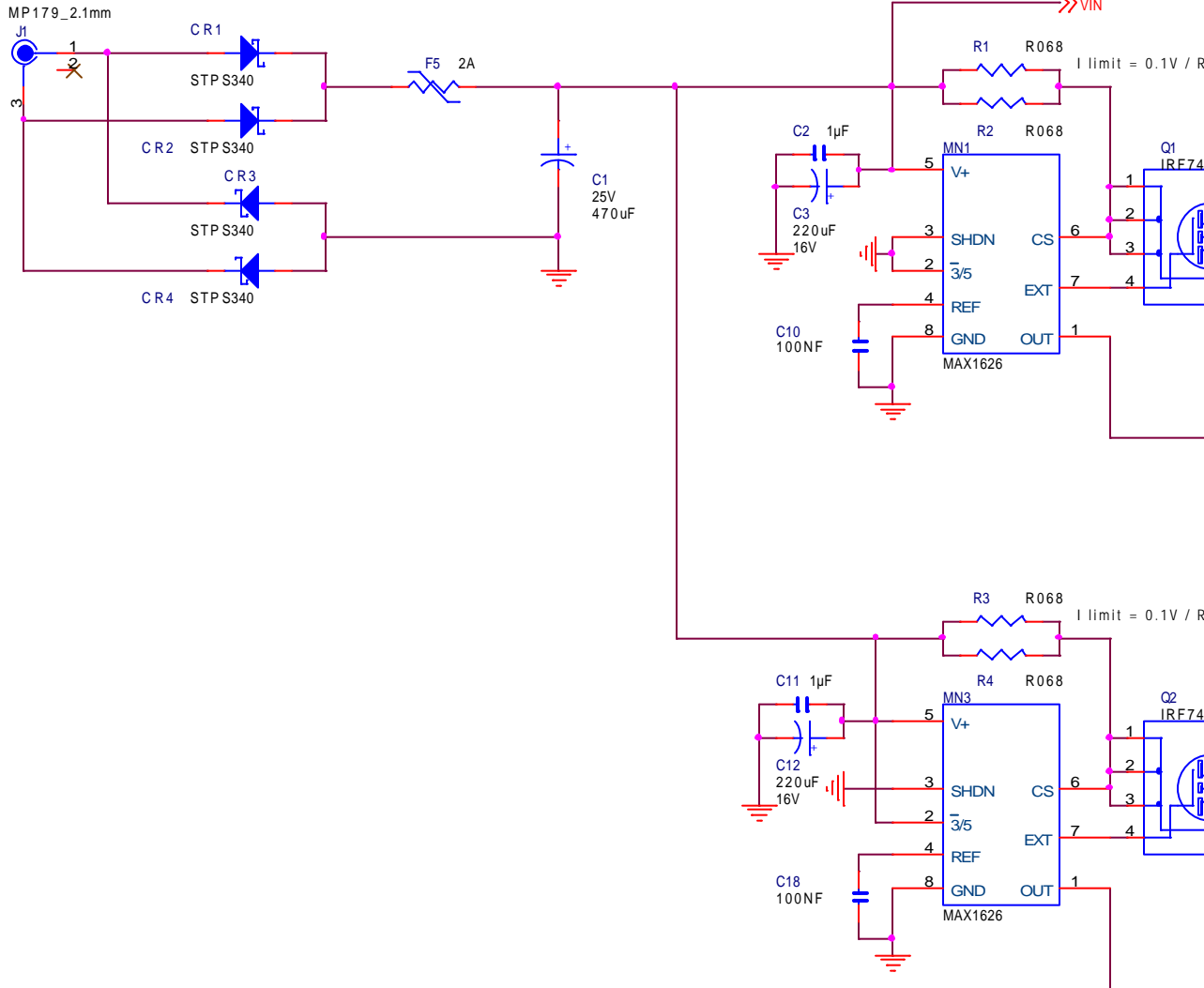
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12V TO 14V DC INPUT



PB[0..29]

PA[0..31]

PD[0..27]

- A10 PA31
- F11 PA30
- E11 PA29
- F12 PA28
- G12 PA27
- E12 PA26
- E13 PA25
- B12 PA24
- A12 PA23
- D12 PA22
- D13 PA21
- C12 PA20
- A13 PA19
- C13 PA18
- B13 PA17
- D14 PA16
- B14 PA15
- A15 PA14
- A17 PA13
- B16 PA12
- B15 PA11
- D15 PA10
- E14 PA9
- C16 PA8
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- E15 PA6
- F16 PA5
- F13 PA4
- G16 PA3
- G15 PA2
- G14 PA1
- G13 PA0

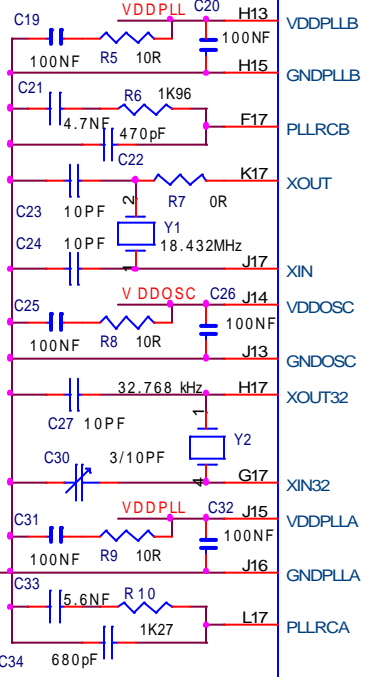
- J6 PB29
- J5 PB28
- G6 PB27
- G4 PB26
- F4 PB25
- F5 PB24
- F3 PB23
- C4 PB22
- B4 PB21
- A3 PB20
- C5 PB19
- B3 PB18
- A4 PB17
- E7 PB16

- PD0 E17 PD0ETX0
- PD1 F15 PD1/ETX1
- PD2 F14 PD2/ETX2
- PD3 E16 PD3/ETX3
- PD4 D17 PD4/ETXEN
- PD5 C17 PD5/ETXER
- PD6 D16 PD6/DTXD
- PD7 D6 PD7/PCK0/TPSYNC
- PD8 A6 PD8/PCK1/TCLK
- PD9 B6 PD9/PCK2/TPS0
- PD10 C6 PD10/PCK3/TPS1
- PD11 A5 PD11/TPS2
- PD12 B5 PD12/TPK0
- PD13 B2 PD13/TPK1
- PD14 C3 PD14/TPK2
- PD15 C2 PD15/TD0/TPK3
- PD16 F1 PD16/TD1/TPK4
- PD17 G2 PD17/TD2/TPK5
- PD18 G5 PD18/NPCS1/TPK6
- PD19 G1 PD19/NPCS2/TPK7
- PD20 H2 PD20/NPCS3/TPK8
- PD21 H4 PD21/RTS0/TPK9
- PD22 H3 PD22/RTS1/TPK10
- PD23 H1 PD23/RTS2/TPK11
- PD24 J3 PD24/RTS3/TPK12
- PD25 J1 PD25/DTR1/TPK13
- PD26 J4 PD26/TPK14
- PD27 J2 PD27/TPK15

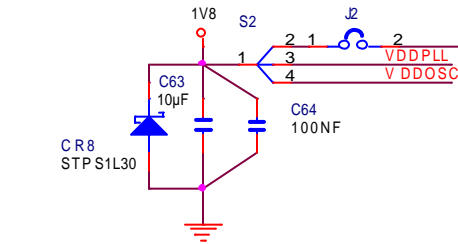
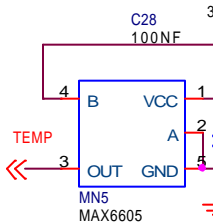
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- DDM K2 DDM
- HDP A K1 HDPA
- HDM A K3 HDMA
- HDP B L2 HDPB
- HDM B L3 HDMB

- TDI A1 TDI
- TMS C1 TMS
- TCK E5 TCK

- TDO B1 TDO
- NTRST E2 NTRST
- JTAGSEL A2 JTAGSEL

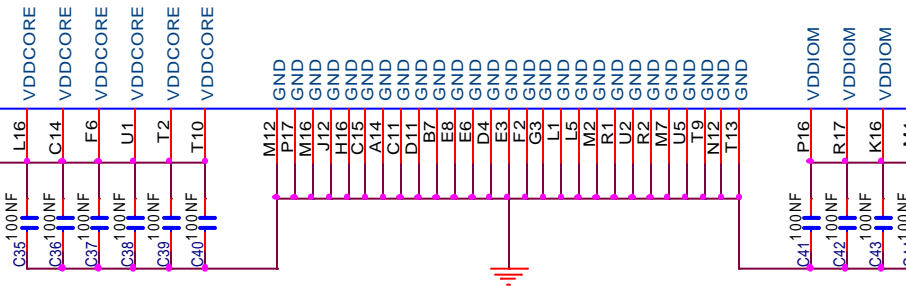


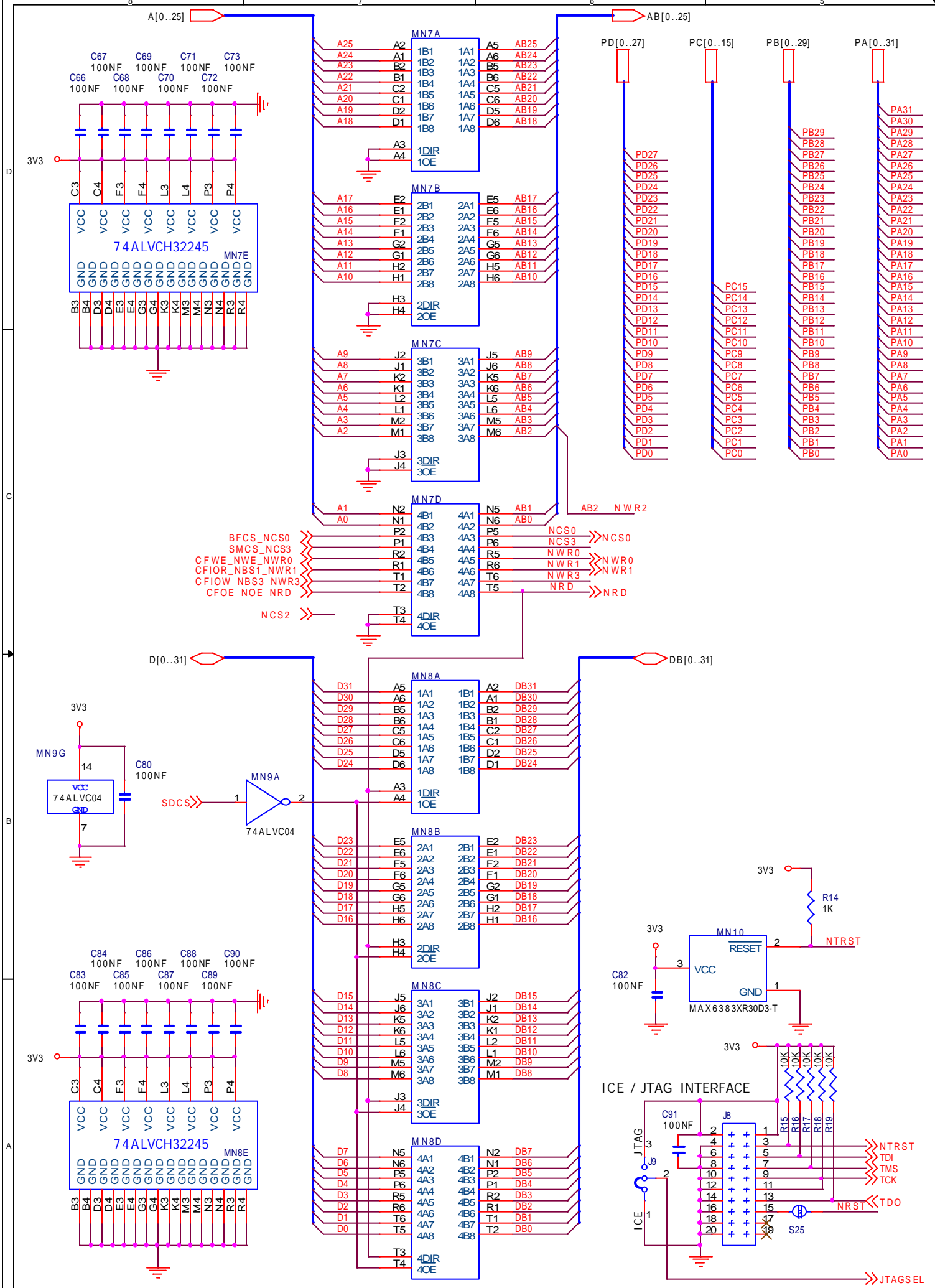
TEMPERATURE SENSOR



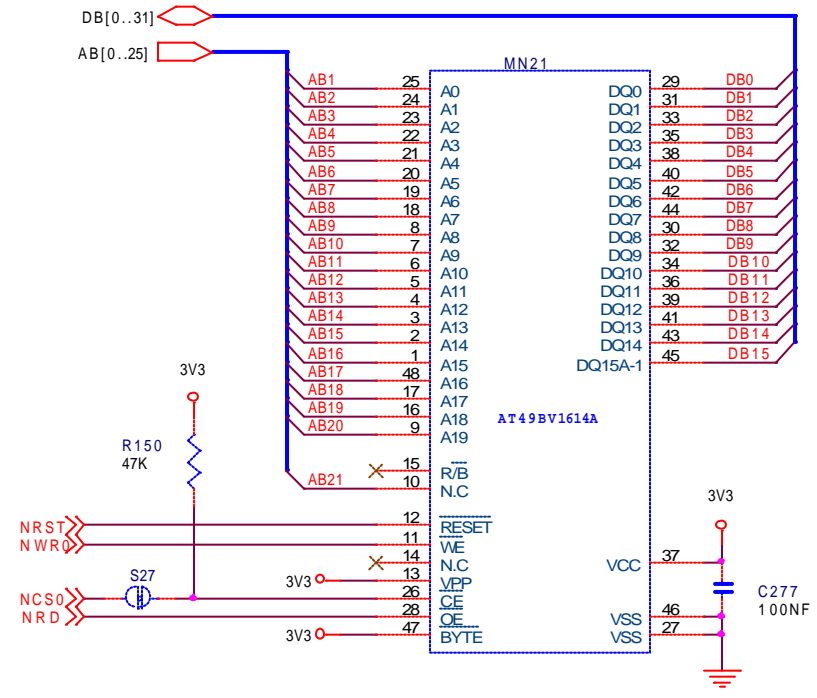
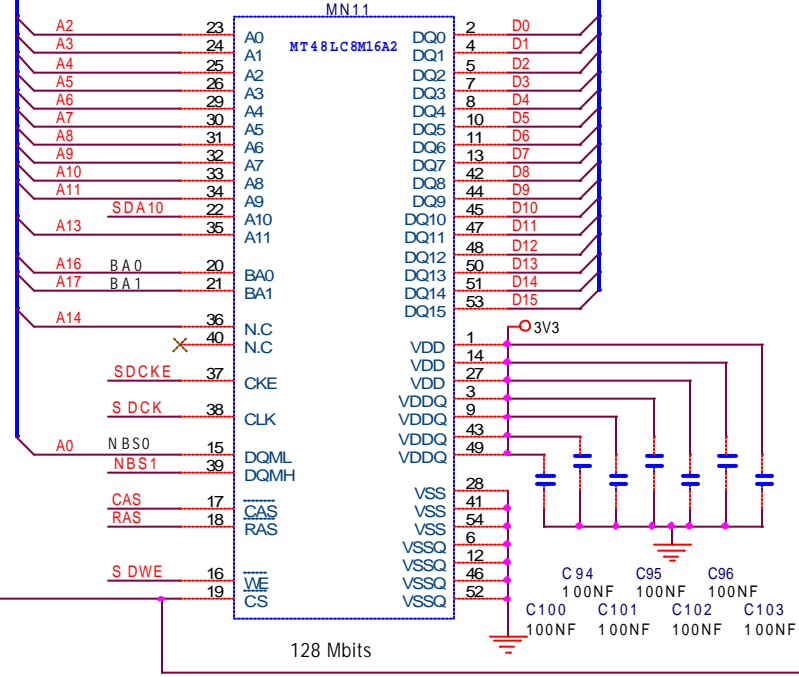
AT91RM9200

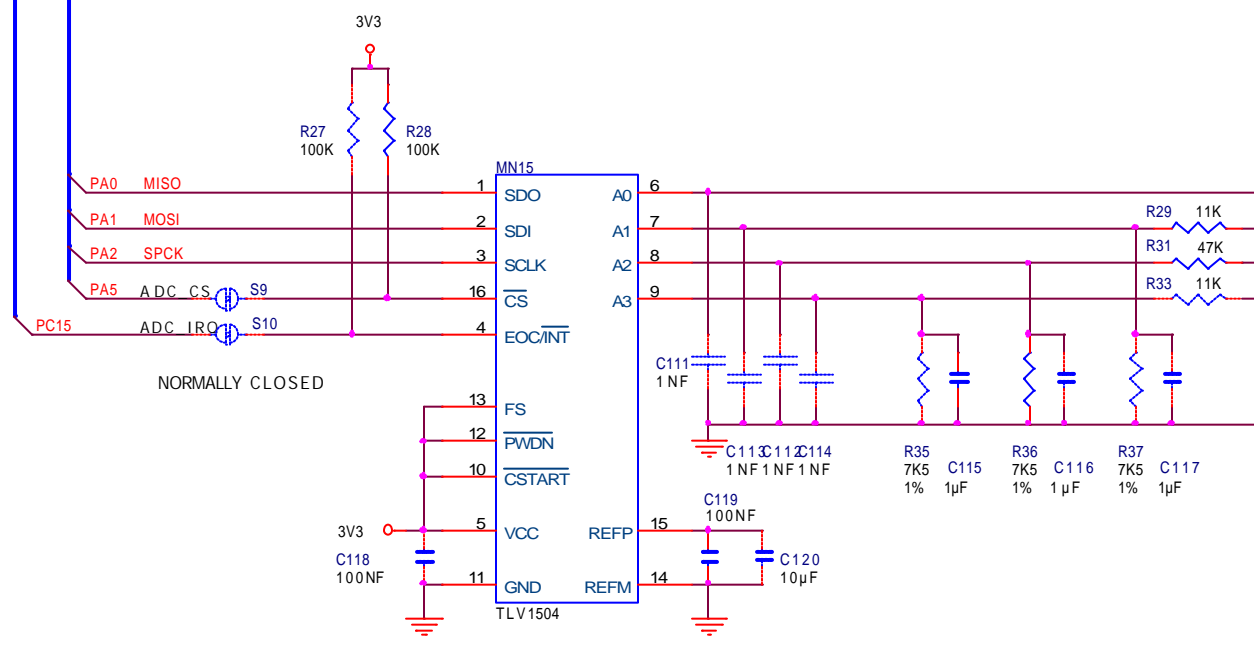
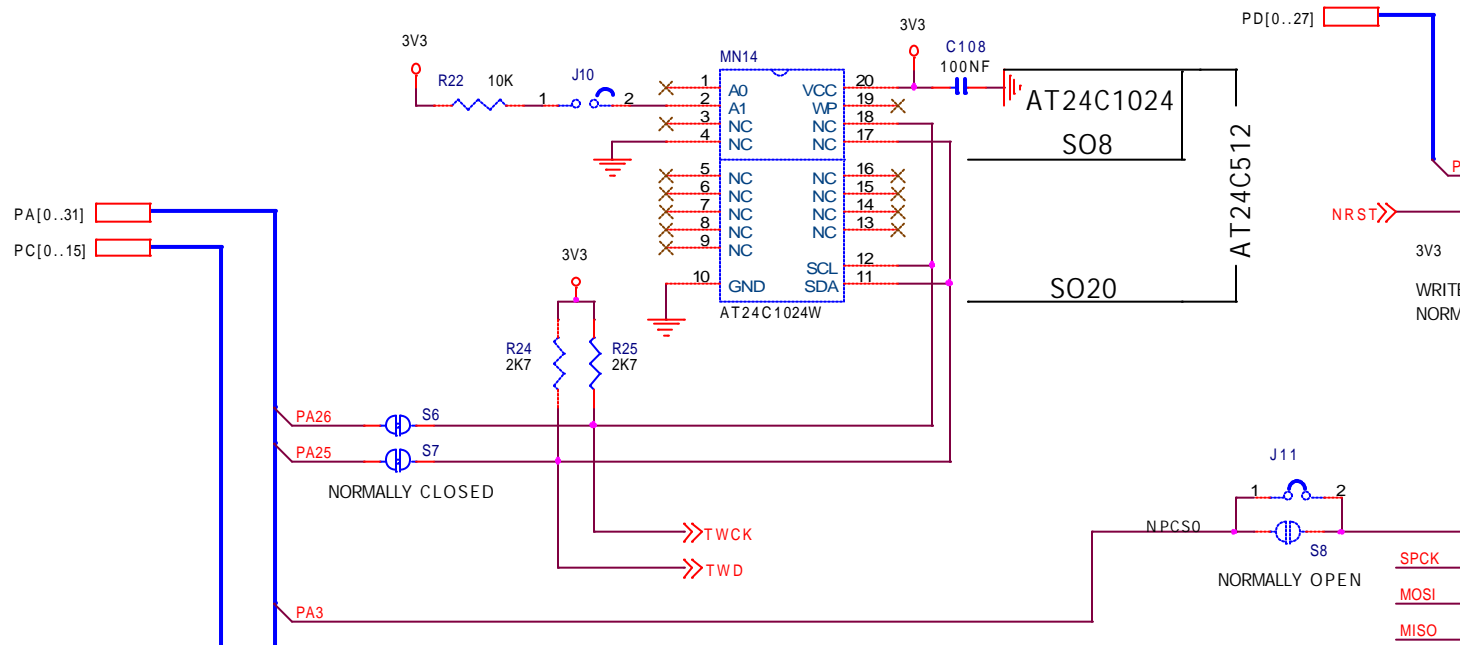
MN4





EBI SDRAM INTERFACE





D
C
B
A

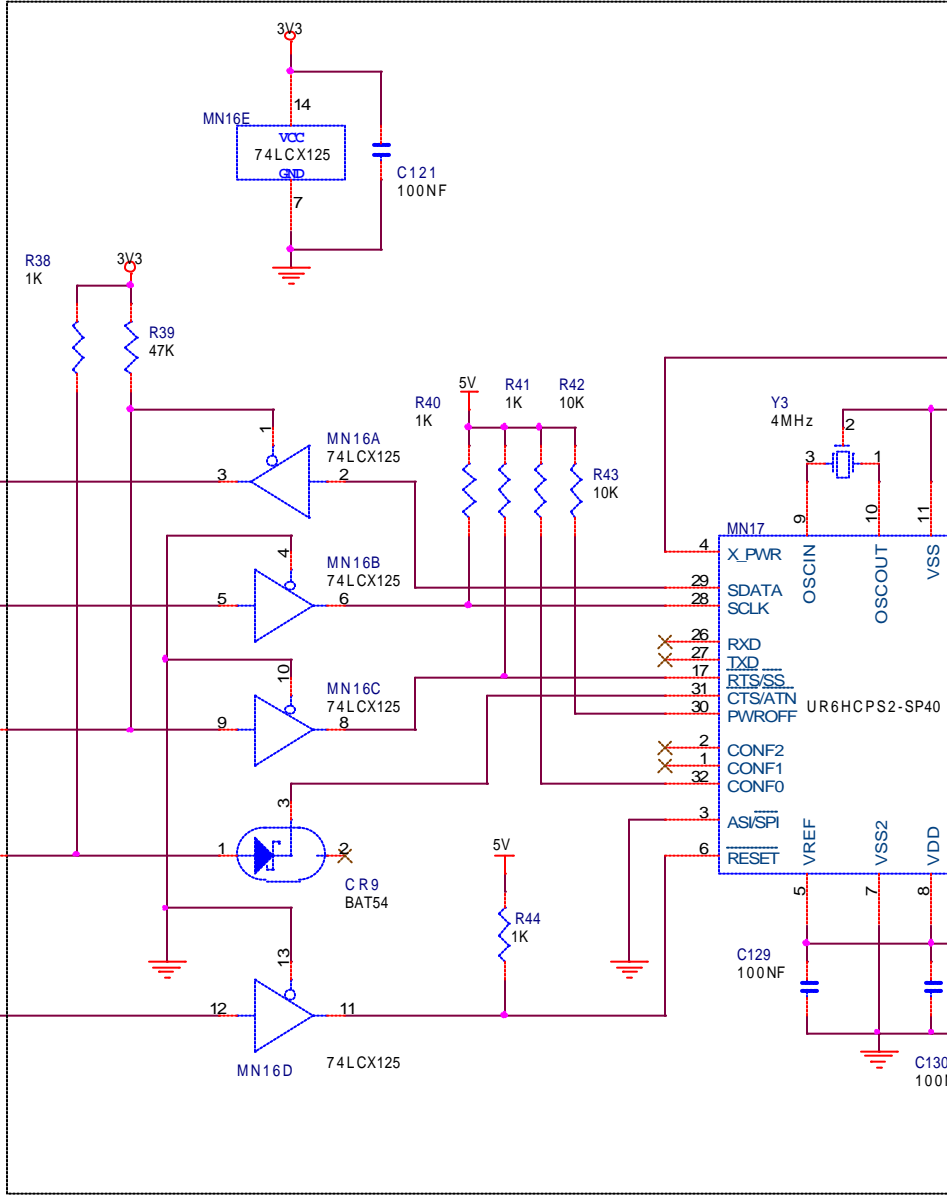
8 7 6 5

PA[0..31]

PB[0..29]

NRST

PA0 MISO
PA2 SPCK
PA4 NPCS1
PB29 IRQ0



MN16E
74LCX125

C121
100NF

R38
1K

R39
47K

5V

R40
1K

R41
1K

R42
10K

R43
10K

MN16A
74LCX125

MN16B
74LCX125

MN16C
74LCX125

CR9
BAT54

MN16D
74LCX125

5V

R44
1K

Y3
4MHz

MN17

UR6HCPS2-SP40

CONF2
CONF1
CONF0

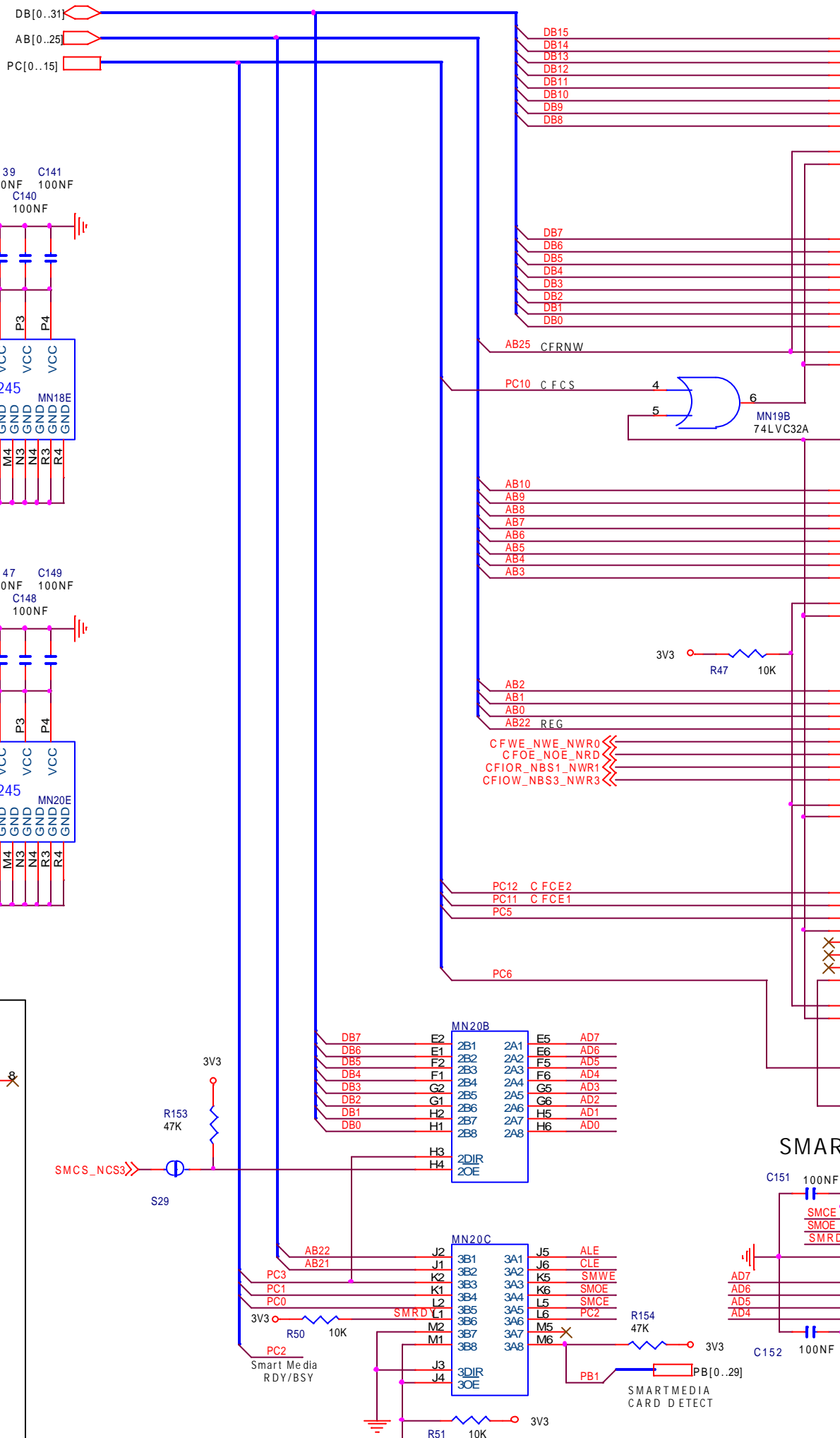
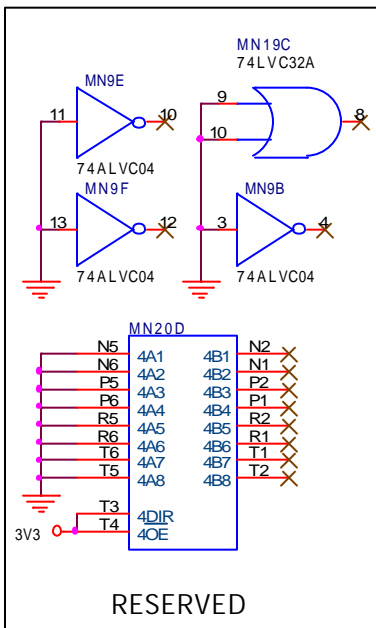
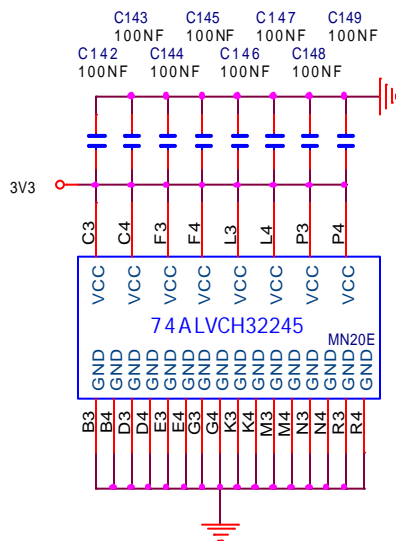
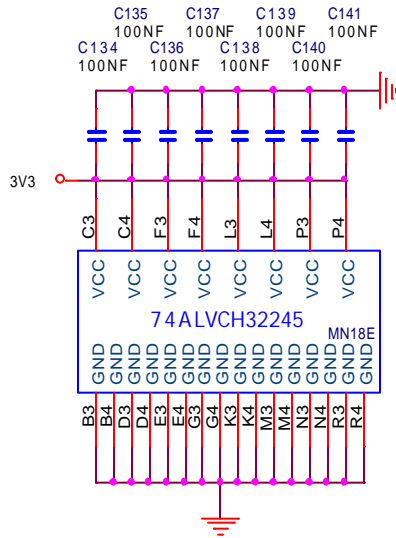
ASI/SPI
RESET

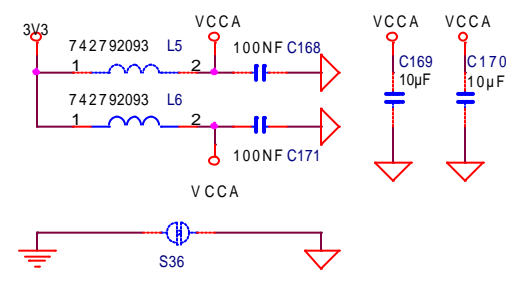
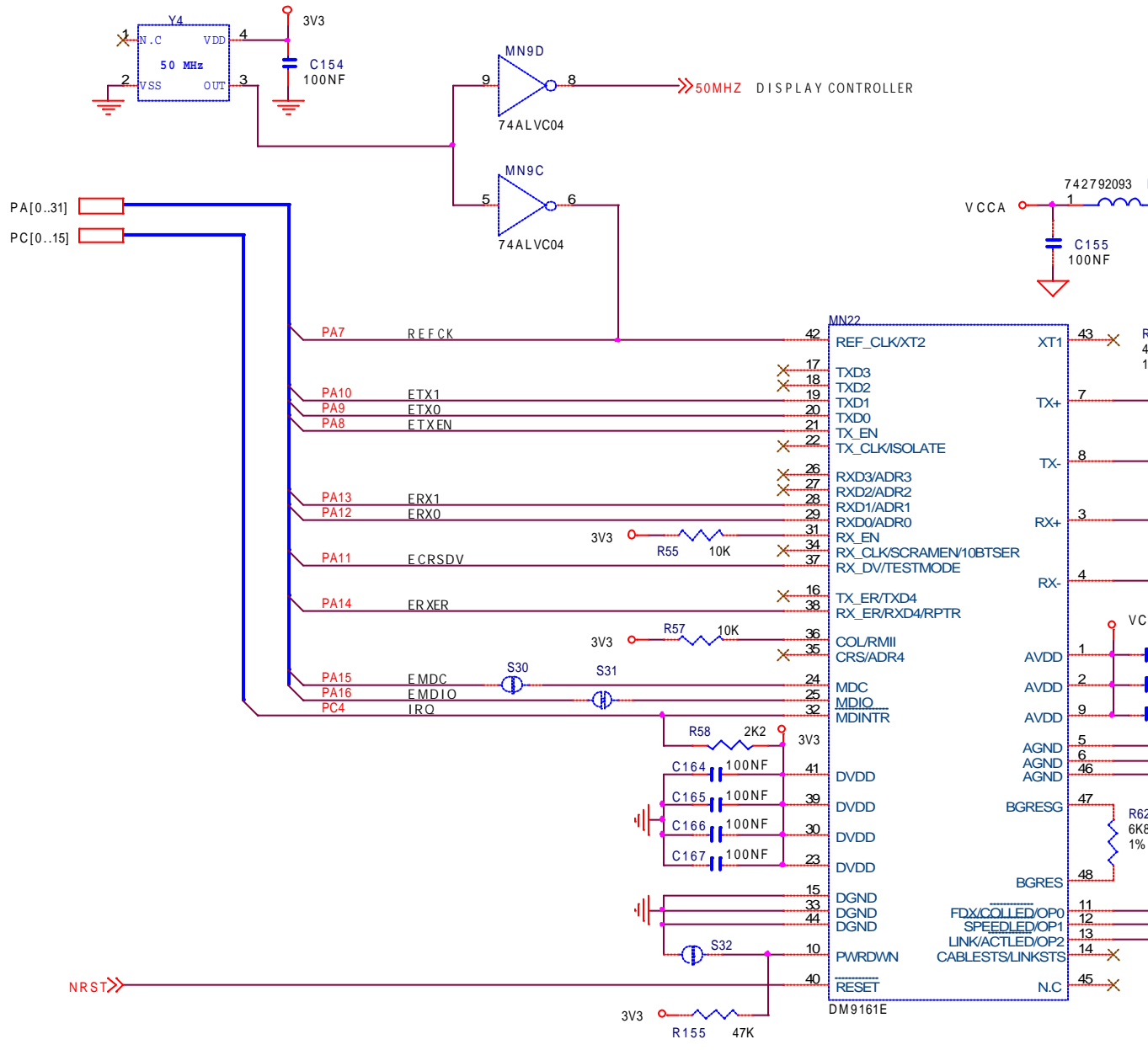
C129
100NF

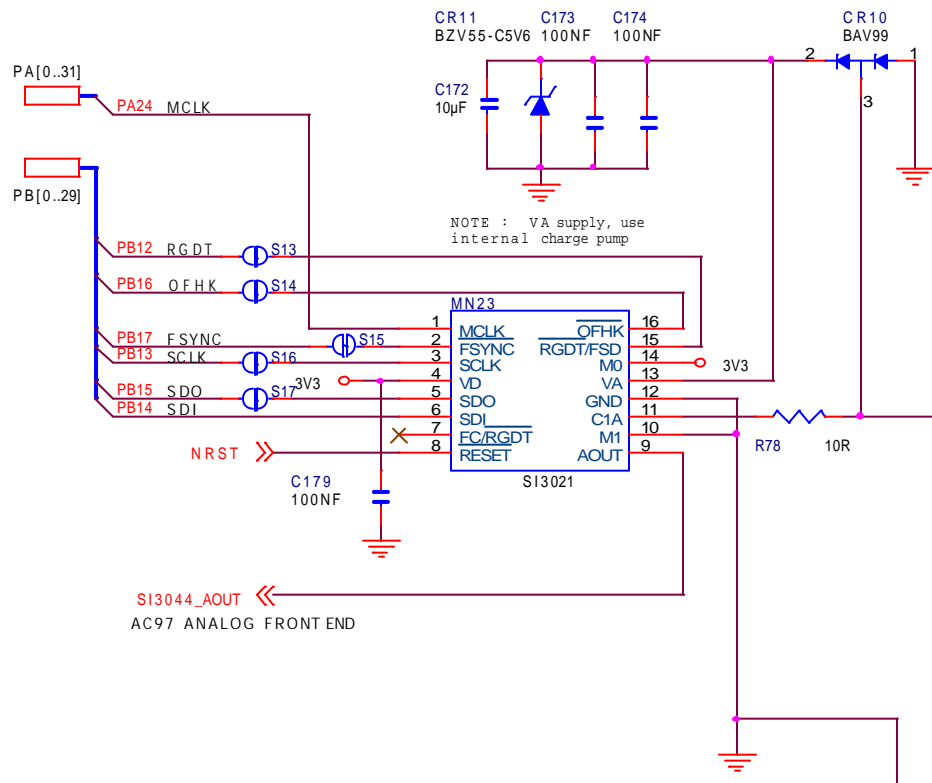
C130
100NF

X_PWR
SDATA
SCLK
RXD
TXD
RTS/SS
CTS/ATN
PWROFF
OSCIN
OSCOUT
VSS

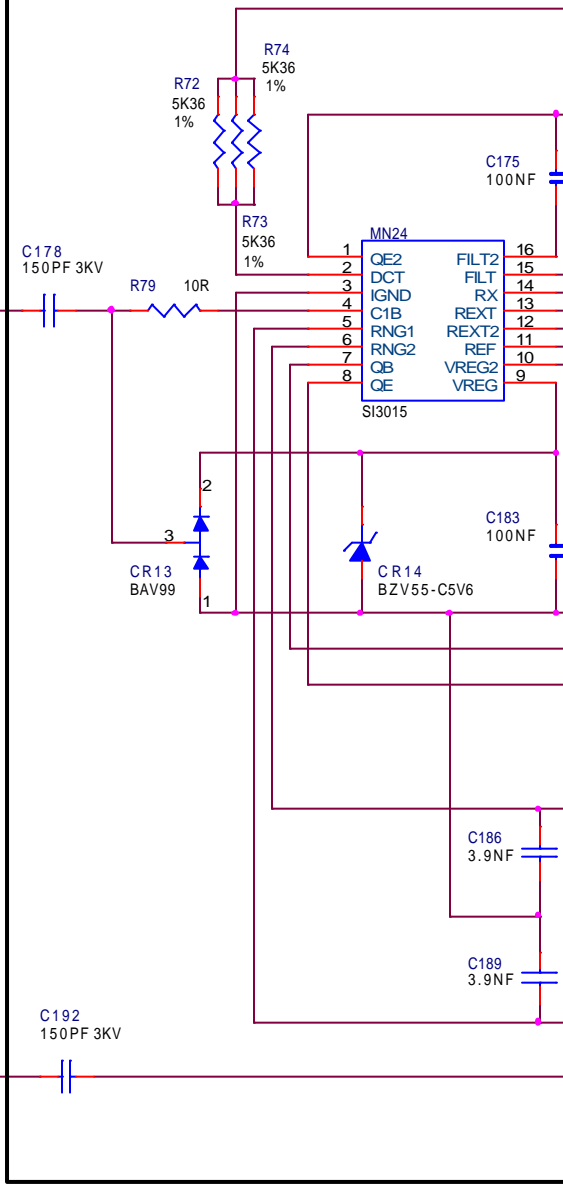
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VDD

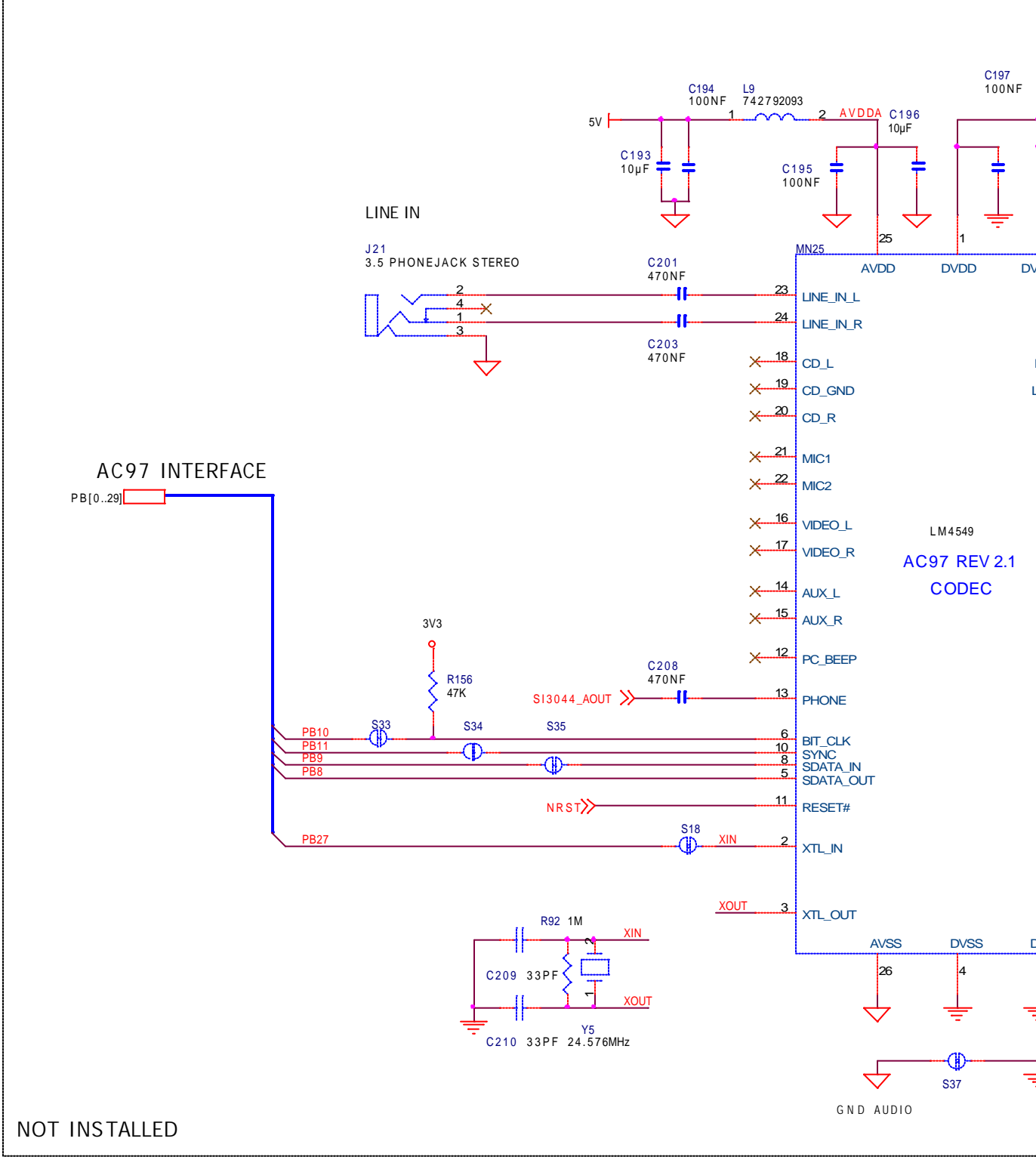






NO GROUND PLANE IN DAA SECTION





NOT INSTALLED

D

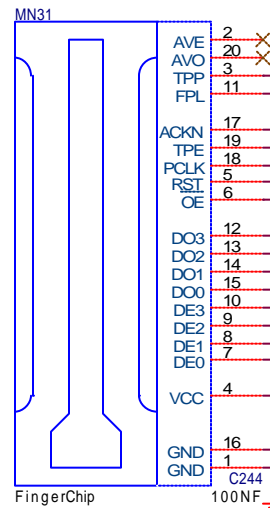
C

B

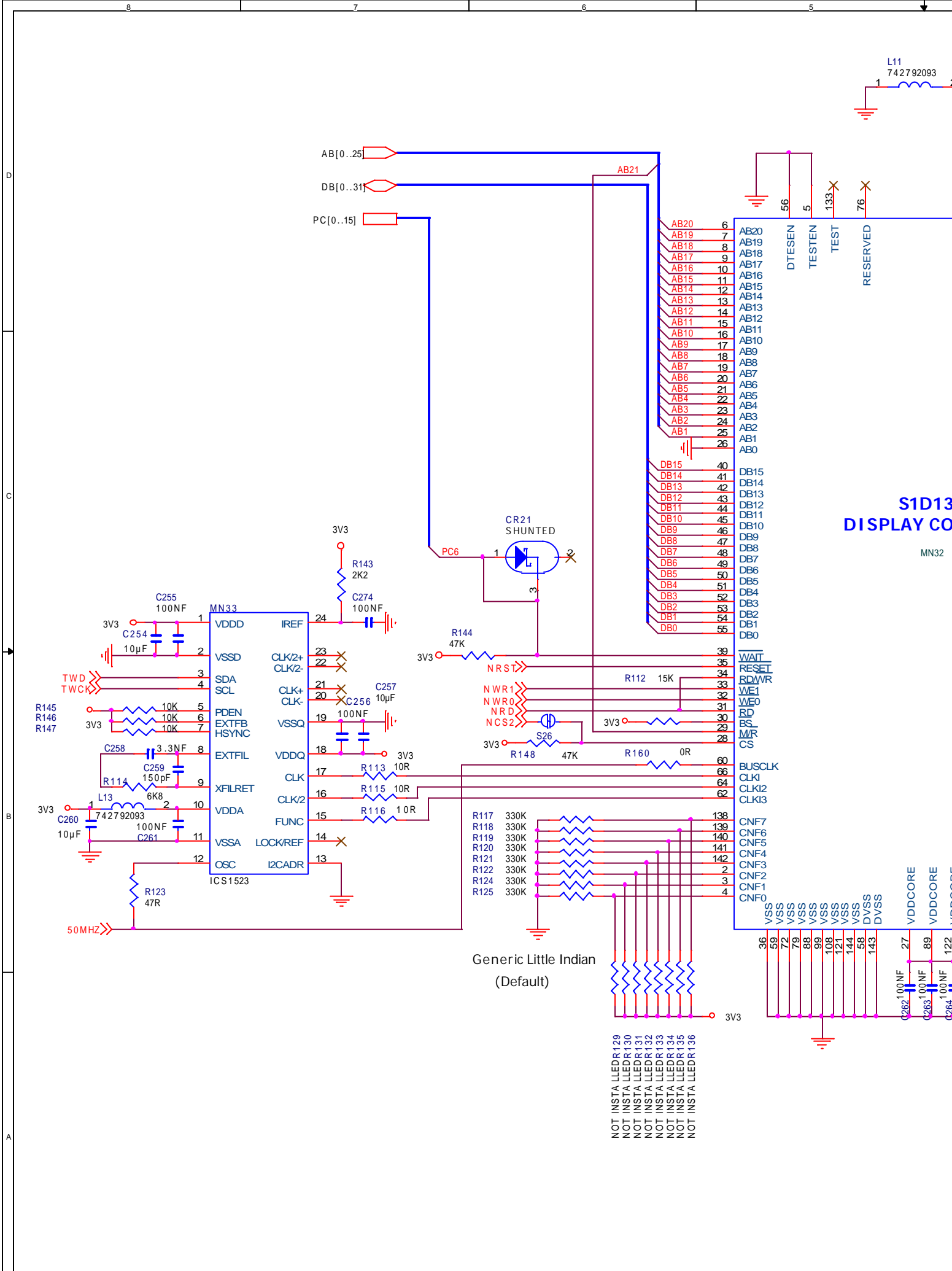
A



Z15
 DIP SOCKET



DO NOT SOLDER



**S1D138010
DISPLAY CONTROLLER**

MN32

- NOT INSTA LLEDR129
- NOT INSTA LLEDR130
- NOT INSTA LLEDR131
- NOT INSTA LLEDR132
- NOT INSTA LLEDR133
- NOT INSTA LLEDR134
- NOT INSTA LLEDR135
- NOT INSTA LLEDR136

- 36 VSS
- 59 VSS
- 72 VSS
- 78 VSS
- 88 VSS
- 99 VSS
- 108 VSS
- 121 VSS
- 144 VSS
- 58 DVSS
- 143 DVSS
- 27 VDDCORE
- 89 VDDCORE
- 122 VDDCORE

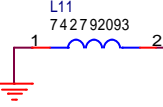
Generic Little Indian
(Default)

- R117 330K
- R118 330K
- R119 330K
- R120 330K
- R121 330K
- R122 330K
- R124 330K
- R125 330K

- AB20
- AB19
- AB18
- AB17
- AB16
- AB15
- AB14
- AB13
- AB12
- AB11
- AB10
- AB9
- AB8
- AB7
- AB6
- AB5
- AB4
- AB3
- AB2
- AB1
- AB0

- DB15
- DB14
- DB13
- DB12
- DB11
- DB10
- DB9
- DB8
- DB7
- DB6
- DB5
- DB4
- DB3
- DB2
- DB1
- DB0

- 56 DTESEN
- 5 TESTEN
- 133 TEST
- 76 RESERVED



D

C

B

A



Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

e-mail

literature@atmel.com

Web Site

<http://www.atmel.com>

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