

**FAIRCHILD**  
SEMICONDUCTOR™

October 1987

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## CD4503BC

### Hex Non-Inverting 3-STATE Buffer

#### General Description

The CD4503BC is a hex non-inverting 3-STATE buffer with high output current sink and source capability. 3-STATE outputs make it useful in bus-oriented applications. Two separate disable inputs are provided. Buffers 1 through 4 are controlled by the disable 4 input. Buffers 5 and 6 are controlled by the disable 2 input. A high level on either disable input will cause those gates on its control line to go into a high impedance state.

#### Features

- Wide supply voltage range:  $3.0 V_{DC}$  to  $18 V_{DC}$
- 3-STATE outputs
- Symmetrical turn on/turn off delays
- Symmetrical output rise and fall times
- Pin-for-pin replacement for MM80C97 and MC14503

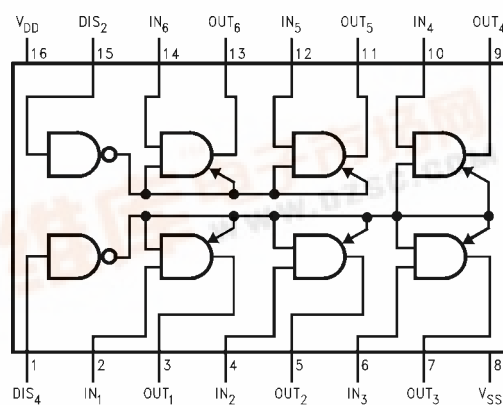
#### Ordering Code:

Order Number	Package Number	Package Description
CD4503BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
CD4503BCSJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4503BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

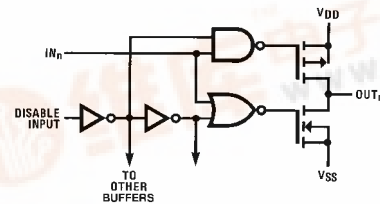
#### Connection Diagram

Pin Assignments for DIP, SOIC and SOP



Top View

#### Schematic Diagram



#### Truth Table

In	Disable Input	Out
0	0	0
1	0	1
X	1	3-STATE

X = Don't Care

CD4503BC Hex Non-Inverting 3-STATE Buffer



**Absolute Maximum Ratings**(Note 1)

(Note 2)

Supply Voltage ( $V_{DD}$ )	–0.5V to +18V
Input Voltage ( $V_{IN}$ )	–0.5V to +0.5V
Storage Temperature Range ( $T_S$ )	–65°C to +150°C
Power Dissipation ( $P_D$ )	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature ( $T_L$ )	
(Soldering, 10 seconds)	260°C

**Recommended Operating Conditions** (Note 2)

Supply Voltage ( $V_{DD}$ )	+3V to +15V
Operating Temperature Range ( $T_A$ )	–40°C to +85°C

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

**Note 2:**  $V_{SS} = 0V$  unless otherwise specified.

**DC Electrical Characteristics** (Note 2)

Symbol	Parameter	Conditions	–40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	$V_{DD} = 5V$ , $V_{IN} = V_{DD}$ or $V_{SS}$		4			4		30	$\mu A$
		$V_{DD} = 10V$ , $V_{IN} = V_{DD}$ or $V_{SS}$		8			8		60	$\mu A$
		$V_{DD} = 15V$ , $V_{IN} = V_{DD}$ or $V_{SS}$		16			16		120	$\mu A$
		$V_{IN} = V_{DD}$ or $V_{SS}$								
$V_{OL}$	LOW Level Output Voltage	$V_{IN} = V_{DD}$ or 0								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
$V_{OH}$	HIGH Level Output Voltage	$V_{IN} = V_{DD}$ or 0								
		$V_{DD} = 5V$	4.95		4.95			4.95		V
		$V_{DD} = 10V$	9.95		9.95			9.95		V
$V_{IL}$	LOW Level Input Voltage	$V_{DD} = 5V$ , $V_O = 4.5V$ or $0.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$ , $V_O = 9.0V$ or $1.0V$		3.0		4.50	3.0		3.0	V
		$V_{DD} = 15V$ , $V_O = 13.5V$ or $1.5V$		4.0		6.75	4.0		4.0	V
$V_{IH}$	HIGH Level Input Voltage	$V_{DD} = 5V$ , $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$ , $V_O = 1.0V$ or $9.0V$	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$ , $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
$I_{OL}$	LOW Level Output Current	$V_{DD} = 4.5V$ , $V_{OL} = 0.4V$	2.30		1.95	2.65		1.60		mA
		$V_{DD} = 5.0V$ , $V_{OL} = 0.4V$	2.5		2.10	2.75		1.75		mA
		$V_{DD} = 10V$ , $V_{OL} = 0.5V$	6.5		5.45	7.0		4.45		mA
		$V_{DD} = 15V$ , $V_{OL} = 1.5V$	16.50		13.80	25.00		11.30		mA
$I_{OH}$	HIGH Level Output Current	$V_{DD} = 5V$ , $V_{OH} = 4.6V$	–1.04		–0.88	–1.76		–0.7		mA
		$V_{DD} = 10V$ , $V_{OH} = 9.5V$	–2.60		–2.2	–4.50		–1.8		mA
		$V_{DD} = 15V$ , $V_{OH} = 13.5V$	–7.2		–6.0	–17.6		–4.8		mA
$I_{TL}$	3-STATE Leakage Current	$V_{DD} = 15V$		$\pm 0.3$		$\pm 10^{-4}$	$\pm 0.3$		$\pm 1.0$	$\mu A$
$I_{IN}$	Input Current	$V_{DD} = 15V$		$\pm 0.3$		$\pm 10^{-5}$	$\pm 0.3$		$\pm 1.0$	$\mu A$

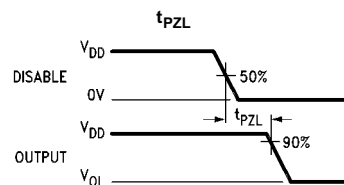
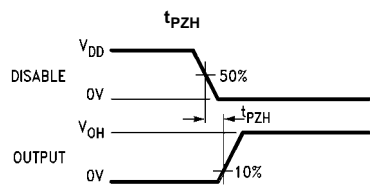
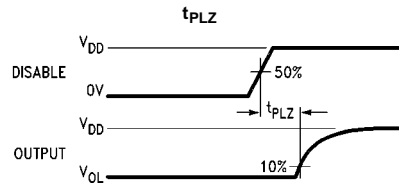
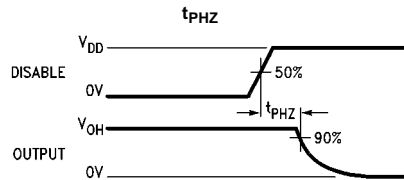
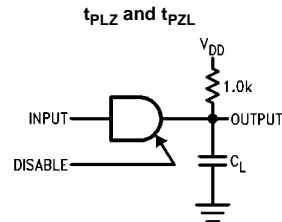
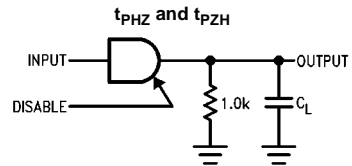
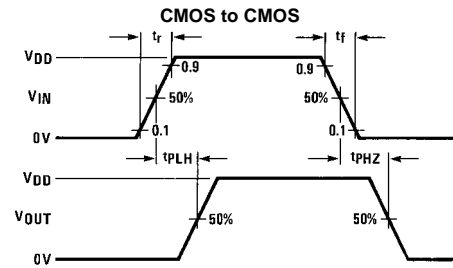
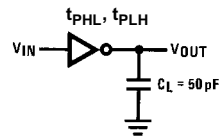
**Note 3:**  $I_{OH}$  and  $I_{OL}$  are tested one output at a time.

**AC Electrical Characteristics** (Note 4) $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$ , Input  $t_r = t_f = 20\text{ ns}$ , unless otherwise specified

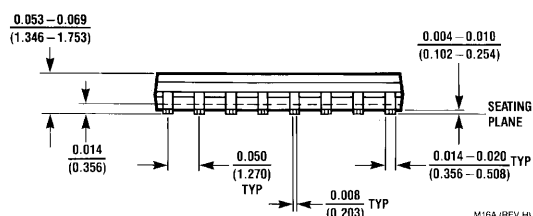
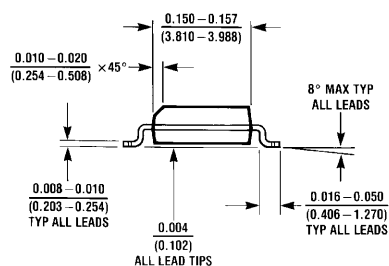
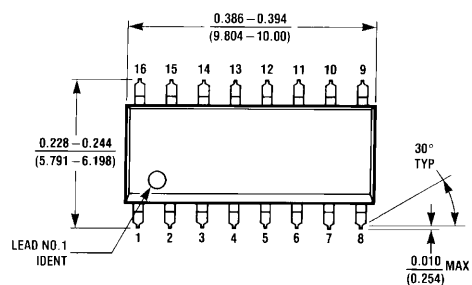
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PHL}$ , $t_{PLH}$	Propagation Delay Time	$V_{DD} = 5V$		75	100	ns
		$V_{DD} = 10V$		35	40	ns
		$V_{DD} = 15V$		25	30	ns
$t_{PLZ}$ , $t_{PHZ}$	Propagation Delay Time, Logical Level to HIGH Impedance State	$V_{DD} = 5V$		80	125	ns
		$V_{DD} = 10V$		40	90	ns
		$V_{DD} = 15V$		35	70	ns
$t_{PZL}$ , $t_{PZH}$	Propagation Delay Time, High Impedance State to Logical Level	$V_{DD} = 5V$		95	175	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		35	70	ns
$t_{TLH}$	Output Rise Time	$V_{DD} = 5V$		45	80	ns
		$V_{DD} = 10V$		23	40	ns
		$V_{DD} = 15V$		18	35	ns
$t_{THL}$	Output Fall Time	$V_{DD} = 5V$		45	80	ns
		$V_{DD} = 10V$		23	40	ns
		$V_{DD} = 15V$		18	35	ns

**Note 4:** AC Parameters are guaranteed by DC correlated testing.

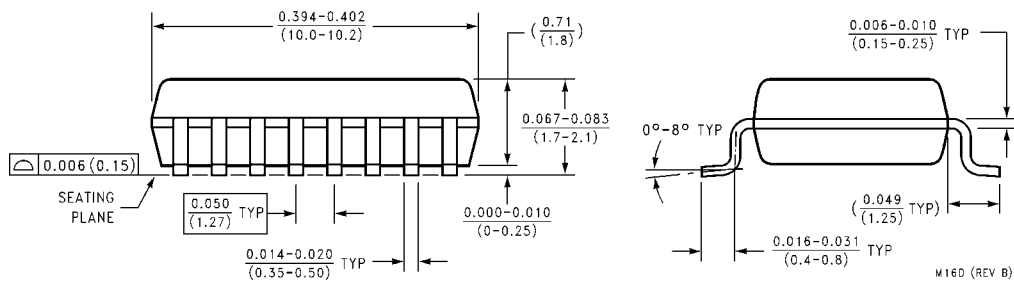
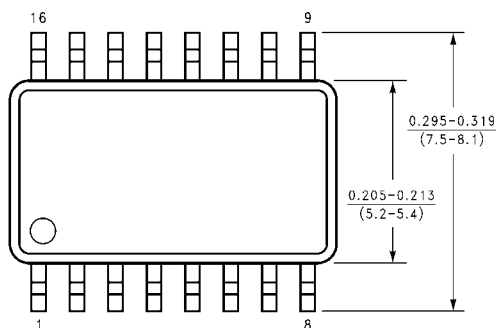
## AC Test Circuits and Switching Time Waveforms



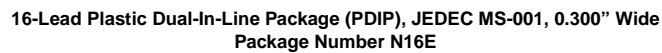
Note: Delays measured with input  $t_r$ ,  $t_f \leq 20\text{ ns}$ .



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M16A**



**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M16D**



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