Benchmarq Products from Texas Instruments

Preliminary **bq2052**

Gas Gauge IC for Lithium Primary Cells

Features

- Accurate measurement of available capacity in Lithium primary batteries such as Lithium Sulphur Dioxide and Lithium Manganese Dioxide
- Provides a low-cost battery monitor solution for pack integration
  - Complete circuit can fit less than 1 square inch of PCB space
  - Low operating current
  - Less than 100nA of data retention current
- Single-wire communication interface (HDQ bus) for critical battery parameters
- Communicates remaining capacity with direct drive of LEDs in 3 selectable modes
- Measurements automatically compensated for discharge rate and temperature
- 16-pin narrow SOIC

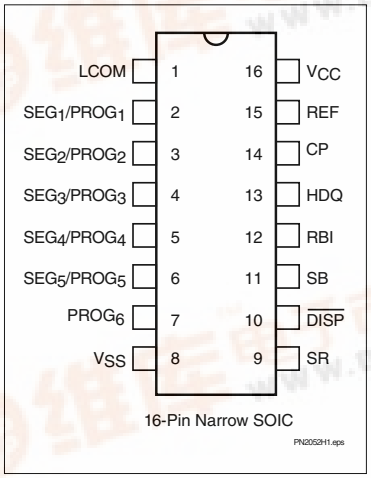
General Description

The bq2052 Lithium Primary Gas Gauge IC is intended for battery-pack or in-system installation to maintain an accurate record of available battery capacity. The IC monitors a voltage drop across a sense resistor connected in series with the cells to determine discharge activity of the battery. The bq2052 applies compensations for battery temperature and discharge rate to the available charge counter to provide available capacity information across a wide range of operating conditions.

Compensated available capacity may be directly indicated using an LED display. The LED display is programmable and can be configured as two, four, or five segments. These segments are used to depict available battery capacity. The bq2052 supports a single-wire serial communications link to an external micro-controller. The link allows the micro-controller to read and write the internal registers of the bq2052. The internal registers include available battery capacity, voltage, temperature, current, and battery status. The controller may also overwrite some of the bq2052 gas gauge data registers.

The bq2052 can operate from the batteries in the pack. The REF output and an external FET provide a simple, inexpensive voltage regulator to supply power to the circuit from the cells.

Pin Connections



Pin Names

LCOM	LED common output
$SEG_1/PROG_1$	LED segment 1/ program 1 input
$SEG_1/PROG_2$	LED segment 2/ program 2 input
$SEG_1/PROG_3$	LED segment 3/ program 3 input
$SEG_1/PROG_4$	LED segment 4/ program 4 input
$SEG_1/PROG_5$	LED segment 5/ program 5 input
CP	Control port
V_{SS}	System ground
SR	Sense resistor input
$\overline{DISP}$	Display control input
SB	Battery sense input
RBI	Register backup input
HDQ	Serial communications input/output
$PROG_6$	Program 6 input
REF	Voltage reference output
V_{CC}	Supply voltage

SLUS019–MAY 1999

Pin Descriptions

LCOM **LED common output**

This open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down program resistors. LCOM is also high impedance when the display is off.

SEG_1–SEG_5 **LED display segment outputs (dual function with $PROG_1$–$PROG_5$)**

Each output may activate an LED to sink the current sourced from LCOM.

$PROG_1$–$PROG_2$ **Programmed full count selections**

These three-level input pins define the programmed full count.

$PROG_3$ **Power gauge scale selection inputs (dual function with SEG_3–SEG_4)**

This three-level input pin defines the scale factor.

$PROG_4$ **Programmed compensation factors**

This three-level input pin defines the battery discharge compensation factors.

$PROG_5$ **Programmed display mode**

This three-level input pin defines the capacity indication display mode.

$PROG_6$ **Programmed initial capacity state**

This input defines the initial battery capacity indication state. When tied to V_{CC}, the bq2052 sets the available capacity to full on reset. When tied to V_{SS}, the bq2052 sets the available capacity to zero on reset.

V_{SS} **Ground**

SR **Sense resistor input**

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret discharge activity. $V_{SR} > V_{SS}$ indicates discharge. The effective voltage drop, V_{SRO}, as seen by the bq2052 is $V_{SR} + V_{OS}$.

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ tied to V_{CC} (no display LEDs in the circuit) allows $PROG_X$ to connect directly to V_{CC} or V_{SS} instead of through a pull-up or pull-down resistor. $\overline{DISP}$ low activates the display.

SB **Secondary battery input**

This input monitors the battery cell voltage potential through a high-impedance resistive divider network for the end-of-discharge voltage (EDV) thresholds.

RBI **Register backup input**

This pin is used to provide backup potential to the bq2052 registers during periods when $V_{CC} \leq 3V$. A storage capacitor or a battery can be connected to RBI.

HDQ **Serial communication input/output**

This is the open-drain bidirectional communications port.

CP **Control port**

This open drain output may be controlled by serial port commands and its state is reflected in the CPIN bit in FLGS1.

REF **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} **Supply voltage input**

Functional Description

General Operation

The bq2052 determines battery capacity by monitoring the amount of charge removed from a primary battery. The bq2052 measures discharge currents and battery voltage, monitors the battery for the low battery-voltage thresholds, and compensates available capacity for temperature and discharge rate. The bq2052 measures capacity by monitoring the voltage across a small-value series sense resistor between the negative battery terminal and ground.

Figure 1 shows a typical battery pack application of the bq2052 using the LED display capability as a charge-state indicator. The bq2052 displays capacity with two, four, or five LEDs using the programmed full count (PFC) as the battery's "full" reference. The bq2052 has a push-button input for momentarily enabling the LED display.

Measurements

The bq2052 uses a voltage-to-frequency converter (VFC) for discharge measurement and an analog-to-digital converter (ADC) for battery voltage measurement.

Discharge Counting

The VFC measures the discharge flow of the battery by monitoring a small value sense resistor between the SR pin and V_{SS} as shown in Figure 1. The bq2052 detects "discharge" activity when the potential at the SR input, V_{SRO}, is positive. The bq2052 integrates the signal over time using an internal counter. The fundamental rate of the counter is 3.125µVh. The VFC measures signals up to 0.5V in magnitude.

Digital Magnitude Filter

The bq2052 has a digital filter to eliminate discharge counting below a set threshold. The minimum discharge threshold, V_{SRD}, for the bq2052 is 250µV.

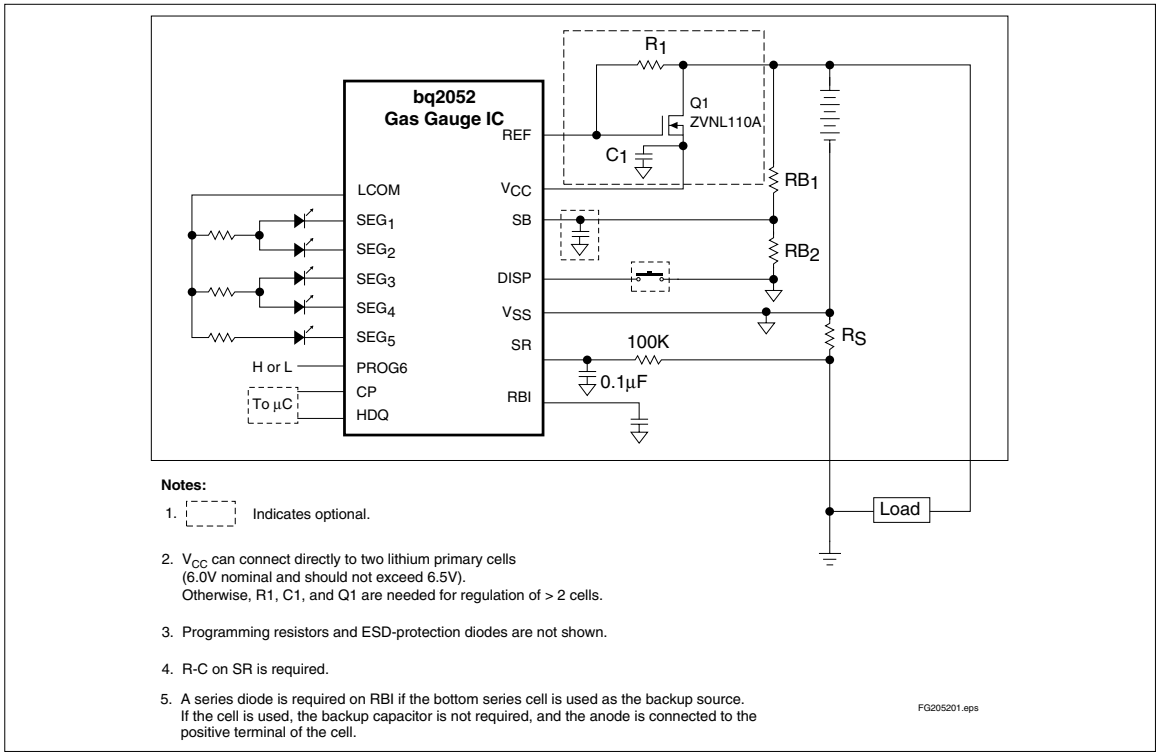


Figure 1. Application Diagram—5-Segment LED Display

Table 1. bq2052 Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

Voltage Monitoring and Thresholds

In conjunction with monitoring the SR input for discharge currents, the bq2052 monitors the battery potential through the SB pin. The voltage at the SB pin, V_{SB}, is developed through a high impedance resistor network connect across the battery. The bq2052 monitors the voltage at the SB pin and reports the voltage in the VSB register (address = 0bh).

The bq2052 compares the V_{SB} reading to two end-of-discharge voltage (EDV) thresholds. The EDV threshold levels are used to determine when the battery has reached an "empty" state. The EDV thresholds for the bq2052 are programmable with the default values fixed at:

EDV1 (first) = 0.76V
EDVF (final) = EDV1 - 0.10V = 0.66V

If V_{SB} is below either of the two EDV thresholds for 8 consecutive samples over a 4 second period, the bq2052 sets the associated flag in the FLGS1 register (address = 01h). Once set, the EDV flags remain set, independent of V_{SB}.

Temperature

The bq2052 has an internal temperature sensor to measure temperature. The bq2052 determines the temperature and stores it in the TEMP register (address = 02h). The bq2052 uses temperature to adapt remaining capacity for the battery's discharge efficiency.

Gas Gauge Operation

General

The operational overview diagram in Figure 2 illustrates the operation of the bq2052. The bq2052 accumulates a measure of discharge currents and calculates available capacity. The bq2052 compensates available capacity for discharge rate and temperature and provides the information in the Compensated Available Capacity (CAC) registers (address = 0eh–0fh). The main counter, Discharge Count Register (DCR) (address = 2eh), represents the cumulative amount of charge removed from the battery. Battery discharging increments the DCR register.

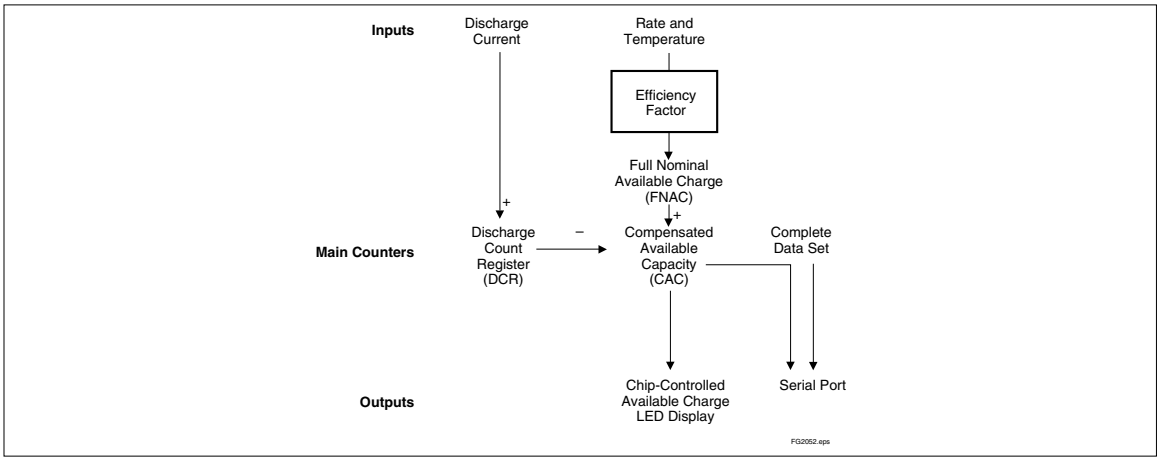


Figure 2. Operational Overview

Table 2. bq2052 Programmed Full Count mVh

$PROG_X$		Programmed Full Count (PFC)	$PROG_3$			Units
1	2		H	Z	L	
-	-	-	SCALE = 1/40	SCALE = 1/80	SCALE = 1/160	mVh/ count
H	H	48128	1203	602	301	mVh
H	Z	46080	1152	576	288	mVh
H	L	43264	1082	541	271	mVh
Z	H	39936	998	499	250	mVh
Z	Z	38400	960	480	240	mVh
Z	L	36096	902	451	226	mVh
L	H	31744	794	397	199	mVh
L	Z	28928	723	362	181	mVh
L	L	26112	653	327	164	mVh

Main Gas-Gauge Registers

Programmed Full Count

The PFC register stores the user-specified battery full capacity. The 8-bit PFC registers stores the full capacity in mVh scaled as shown in Table 2.

Full Nominal Available Capacity

The FNAC register stores the full capacity reference of the battery. It can be programmed to initialize to PFC or zero. The 8-bit FNAC register stores data scaled to the same units as PFC. The bq2052 does not update FNAC during the course of operation; therefore, if it is programmed to 0 on initialization, it must be written to full using the serial port.

Discharge Count Register

The DCR is the main gas gauging register and contains the cumulative amount of discharge counted by the bq2052. The 16-bit register stores data scaled to the same units as PFC.

Compensated Available Capacity

The CAC registers contain the current available capacity of the battery. The data stored in CAC represents the amount of remaining capacity of the battery compensated for rate and temperature use conditions. Tables 3, 4, and, 5 outline the options for typical efficiency compensation factors for lithium primary batteries. The bq2052 applies the efficiency factors to FNAC to derive CAC.

The bq2052 applies the compensation according to the formula:

$$CAC = [F_{CE} * FNAC] - DCR$$

Where F_{CE} is the calculated efficiency compensation factor, FNAC = Full Nominal Available Capacity and DCR = Discharge Count Register.

The bq2052 calculates an F_{CE} based on the battery discharge rate and temperature. The discharge rate portion of the F_{CE} compensation is a "peak hold" function; therefore, the bq2052 latches the highest discharge rate it has measured and uses the highest rate to calculate F_{CE} throughout the complete discharge cycle. The highest discharge rate measured by the bq2052 is stored in MRATE (address = 12h).

The bq2052 does not latch the temperature portion of an F_{CE} calculation. Therefore, CAC may increase or decrease during the course of a complete discharge cycle if a temperature shift causes a change in the calculated F_{CE} value.

Programming the bq2052

The bq2052 is programmed with the $PROG_{1–6}$ pins. During power-up or initialization, the bq2052 reads the state of these six three-level inputs and latches in the programmable configuration settings.

Programmable Configuration Settings

Design Capacity

The battery's rated design capacity or Programmed Full Count (PFC) is programmed with the $PROG_1$–$PROG_3$ pins as shown in Table 2, and represents the battery's full reference.

The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

Battery capacity (mAh) ∗ sense resistor (Ω) = PFC (mVh)

Selecting a PFC slightly less than the rated capacity provides a conservative capacity reference. The bq2052 stores the selected PFC in the PFC register (address = 10h).

Discharge Rate and Temperature Compensation

The discharge rate and temperature compensations are selected using the $PROG_4$ pin. The level of $PROG_4$ on power-up or initialization determines which compensation table the bq2052 uses for the discharge cycle. The following tables illustrate the calculated efficiency compensation factors at selected discharge rates and temperatures.

Table 3. Discharge Efficiency Factor Table PROG4 = Z

	Discharge Rage					
TEMP	0	C/80	C/25	C/10	C/5	C/3
-20	97	99	96	92	85	81
-10	98	98	97	94	89	85
0	98	98	97	94	90	87
21	99	99	98	96	92	89
55	99	99	98	96	93	90
70	99	99	98	96	93	90

Table 4. Discharge Efficiency Factor Table PROG4 = L

	Discharge Rage					
TEMP	0	C/80	C/25	C/10	C/5	C/3
-20	87	85	80	70	53	50
-10	93	91	88	80	68	51
0	96	94	91	85	74	60
21	99	97	95	89	81	68
55	100	99	97	92	85	74
70	101	100	98	93	86	76

Table 5. Discharge Efficiency Factor Table PROG4 = H

	Discharge Rage					
TEMP	0	C/80	C/25	C/10	C/5	C/3
-20	92	93	92	88	83	75
-10	98	98	97	93	89	81
0	100	100	99	96	91	84
21	104	104	102	99	95	88
55	106	106	105	100	97	90
70	107	107	105	101	98	91

Display Mode

The display mode is selected using the $PROG_5$ pin. The three options include a two, four, or five segment display mode as described in Tables 7, 8, and 9.

Initial Capacity Setting

The PFC value is copied to the FNAC register if $PROG_6$ is programmed high, otherwise FNAC defaults to 0. FNAC may be written to the desired full capacity to initialize the pack manually.

Programming Example

Given:

Sense resistor = 0.05mΩ
Number of cells = 5 in series
Capacity = 7000mAh,
Chemistry = $LiSO_2$
Discharge current range = 250mA to 2A
Voltage drop over sense resistor = 12.5mV to 100mV
Display mode = 5 segment bar graph display

Therefore:

7000mAh ∗ 0.05 = 350mVh

Select:

PFC = 26112 counts or 327mVh
$PROG_1$ = low
$PROG_2$ = low
$PROG_3$ = float
$PROG_4$ = float, high, or low depending on desired compensation factors
$PROG_5$ = float selects five segment display
$PROG_6$ = high sets FNAC to PFC

With these selections, the full battery capacity is 327mVh (6540mAh).

Table 6. bq2052 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7	6	5	4	3	2	1	0
CMDWD	Command word	00h	W	CMD7	CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0
FLGS1	Primary status flags	01h	R	INIT	RSVD	RSVD	CPIN	RSVD	RSVD	EDV1	EDVF
TEMP	Temperature (°C)	02h	R	TEMP7	TEMP6	TEMP5	TEMP4	TEMP3	TEMP2	TEMP1	TEMP0
NAC	Nominal available capacity	03h	R/W	NAC7	NAC6	NAC5	NAC4	NAC3	NAC2	NAC1	NAC0
BATID	Battery identification	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
VSRL	Current scale (Low)	05h	R	VSRL7	VSRL6	VSRL5	VSRL4	VSRL3	VSRL2	VSRL1	VSRL0
VSRH	Current scale (High)	06h	R	VSRH7	VSRH6	VSRH5	VSRH4	VSRH3	VSRH2	VSRH1	VSRH0
PPD	Program pin pull-down	07h	R	RSVD	RSVD	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pin pull-up	08h	R	RSVD	RSVD	PPU6	PPU5	PPU4	PPU3	PPU2	PPU1
VSB	Battery voltage register	0bh	R	VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0
VTS	End-of-discharge threshold select register	0ch	R/W	VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0
RCAC	Relative compensated capacity	0dh	R	RSVD	RCAC6	RCAC5	RCAC4	RCAC3	RCAC2	RCAC1	RCAC0
CACL	Compensated available capacity low byte	0eh	R	CACL7	CACL6	CACL5	CACL4	CACL3	CACL2	CACL1	CACL0
CACH	Compensated available capacity high byte	0fh	R	CACH7	CACH6	CACH5	CACH4	CACH3	CACH2	CACH1	CACH0
PFC	Program pin full count	10h	R	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0
FNAC	Full nominal available capacity	11h	R/W	FNAC7	FNAC6	FNAC5	FNAC4	FNAC3	FNAC2	FNAC1	FNAC0
MAX RATE	Maximum discharge rate	12h	R	MAX7	MAX6	MAX5	MAX4	MAX3	MAX2	MAX1	MAX0
RATE	Discharge rate	13h	R	RATE7	RATE6	RATE5	RATE4	RATE3	RATE2	RATE1	RATE0
DCRL	Discharge count register (low byte)	2eh	R/W	DCRL7	DCRL6	DCRL5	DCRL4	DCRL3	DCRL2	DCRL1	DCRL0
DCRH	Discharge count register (high byte)	2fh	R/W	DCRH7	DCRH6	DCRH5	DCRH4	DCRH3	DCRH2	DCRH1	DCRH0

Notes: RSVD = reserved.
All other registers not documented are reserved.

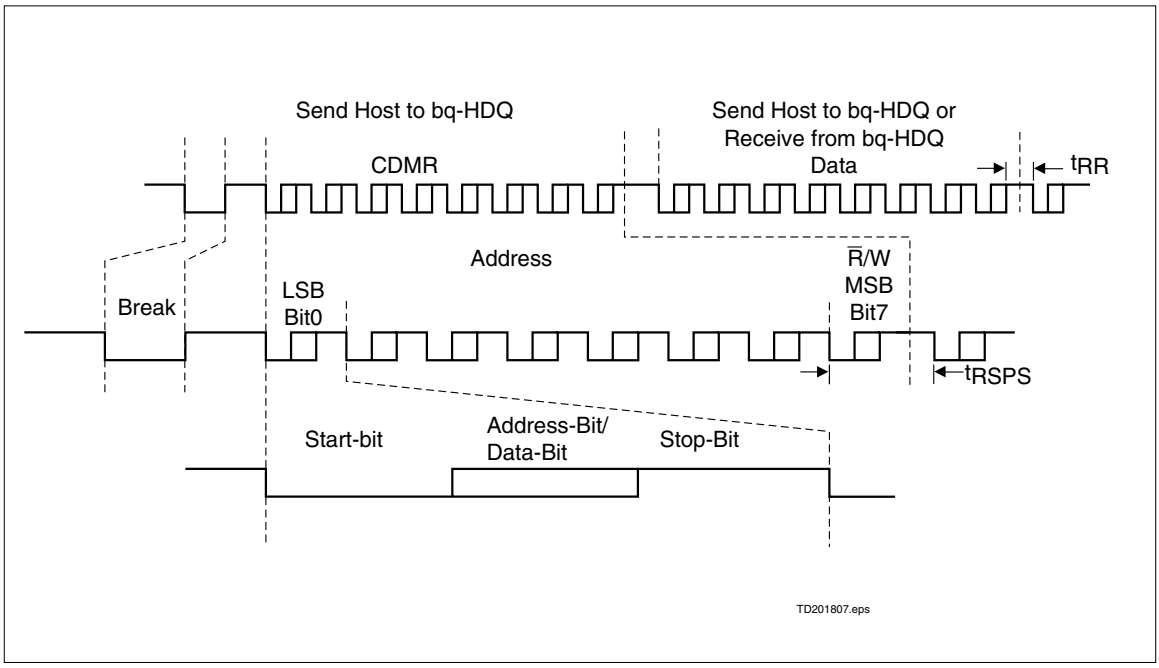


Figure 4. bq2052 Communication Example

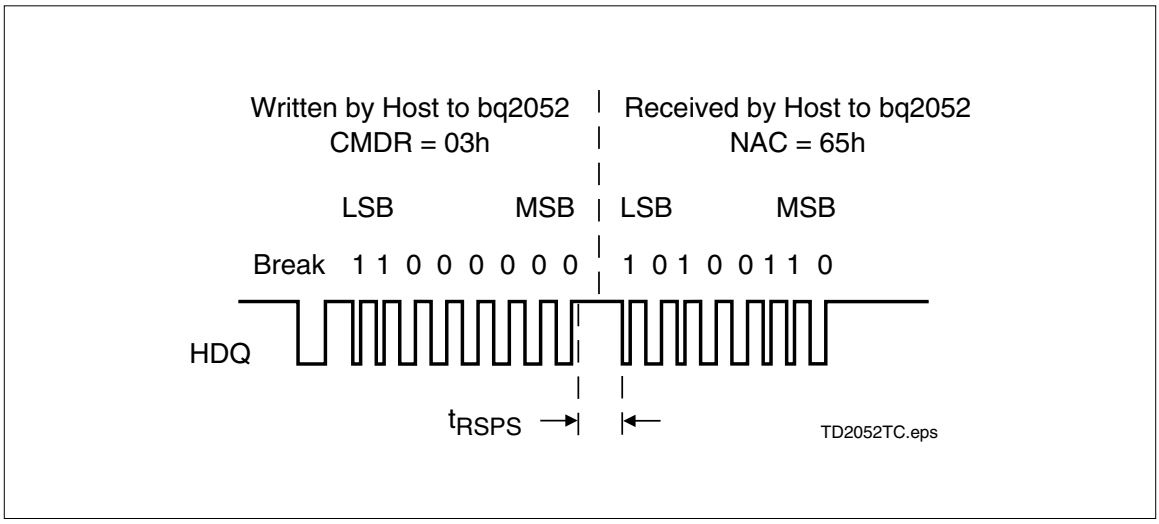


Figure 5. Typical Communication with the bq2052

Communicating With the bq2052

The bq2052 includes a simple single-pin (HDQ plus return) serial data interface. A host processor uses the interface to access various bq2052 registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain HDQ pin on the bq2052 should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2052. The command directs the bq2052 to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 5K bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2052 may be sampled using the pulse-width capture timers available on some microcontrollers.

If a communication error occurs, e.g., $t_{CYCB} > 250\mu s$, the bq2052 should be sent a BREAK to reinitiate the serial interface. A BREAK is detected when the HDQ pin is driven to a logic-low state for a time, t_B or greater. The HDQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2052 is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2052 taking the HDQ pin to a logic-low state for a period, $t_{STRH;B}$. The next section is the actual data transmission, where the data should be valid by a period, $t_{DSU;B}$, after the negative edge used to start communication. The data should be held for a period, $t_{DH;DV}$, to allow the host or bq2052 to sample the data bit.

The final section is used to stop the transmission by returning the HDQ pin to a logic-high state by at least a period, $t_{SSU;B}$, after the negative edge used to start communication. The final logic-high state should be until a period $t_{CYCH;B}$, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2052 is always performed with the least-significant bit being transmitted first. Figure 5 shows an example of a communication sequence to read the bq2052 NAC register.

bq2052 Command Code and Registers

The bq2052 status registers are listed in Table 6 and described below.

Command Code

The bq2052 latches the command code when eight valid command bits have been received by the bq2052. The command code contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command code is used to select whether the received command is for a read or a write function.

The W/$\overline{R}$ values are:

Command Code Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2052 outputs the requested register contents specified by the address portion of command code.

1 The following eight bits should be written to the register specified by the address portion of command code.

The lower seven-bit field of the command code contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

Command Code Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Command Word (CMDWD)

The CMDWD register (address = 00h) is used by the external host to control the CP pin and to reset the bq2052.

CMDWD	Action
0x55	CP high impedence, CPIN bit in FLGS1 set
0x66	CP driven low, CPIN bit in FLGS1 cleared
0x78	bq2052 reset

Primary Status Flags Register (FLGS1)

The FLGS1 register (address = 01h) contains the primary bq2052 flags.

The ***initialized*** flag (INIT) is asserted to a 1 or 0 whenever the bq2052 is initialized either by the application of Vcc or by a serial port command. INIT = 1 signifies that the device has been reset with FNAC set to PFC. INIT = 0 signifies that the battery has been reset with FNAC = 0.

The INIT location is:

FLGS1 Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INIT	-	-	-	-	-	-	-

where INIT is:

0 The bq2052 initialized with FNAC = 0.

1 The bq2052 initialized with FNAC = PFC.

The CPIN but reflects the state of the CP output. If set, the CP output is high impedance. If cleared, the CP output is asserted low. The CP output is an open drain output and requires an external pull-up register.

The CPIN location is

FLGS1 Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
-	-	-	CPIN	-	-	-	-

Where CPIN is:

0 CP is low

1 CP is high impedance

The bq2052 sets the ***first end-of-discharge warning*** flag (EDV1) when the battery voltage VSB is less than the EDV1 threshold VTS. The flag warns the user that the battery is almost empty. The bq2052 modulates the first segment pin, SEG1, at a 4Hz rate if the 4 or 5 segment display mode is enabled and EDV1 is asserted.

The EDV1 threshold has a default value of 0.76V but can be adjusted by writing the VTS register .

The EDV1 location is

FLGS1 Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
-	-	-	-	-	-	EDV1	-

Where EDV1 is:

0 $V_{SB} \geq V_{TS}$

1 $V_{SB} < V_{TS}$

The bq2052 sets the ***final end-of-discharge warning*** flag (EDVF) when VSB is less than the EDVF threshold. The EDVF threshold is set 100mV below the EDV1 threshold. The EDVF flag is used to warn the system or user that battery power is at a failure condition. The bq2052 turns all segment drivers off upon EDVF detection.

The EDVF location is:

FLGS1 Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
-	-	-	-	-	-	-	EDVF

Where EDVF is:

0 $V_{SB} \geq (V_{TS} - 100mV)$

1 $V_{SB} < (V_{TS} - 100mV)$

Temperature Register (TEMP)

The 8-bit TEMP register (address=02h) contains the battery temperature in degrees C. The bq2052 contains an internal temperature sensor. The temperature is used to set discharge efficiency factors. The temperature register contents are store in 2's complement form and represent the temperature ± 5°C.

Nominal Available Capacity Register (NAC)

The NAC register contains the uncompensated remaining capacity of the battery. The bq2052 determines NAC as

$$NAC = FNAC - DCR$$

Battery Identification Register (BATID)

The 8-bit BATID register (address=04h) is a general purpose memory register that can be used to uniquely identify a battery pack. The bq2052 maintains the BATID contents as long as VRBI is greater than 2V. The contents of this register have no effect on the operation of the bq2052.

Current Scale Registers (VSRL/VSRH)

The VSRH high-byte register and the VSRL low-byte register are used to calculate the average signal across the SR and VSS pins. This register pair is updated every 5.625 seconds. VSRH and VSRL form a 16-bit value representing the average current over this time. The battery pack current can be calculated by:

$$|I(mA)| = \frac{(VSRH * 256 + VSRL)}{(R_S)}$$

where

R_S = sense resistor value in Ω.

VSRH = high-byte value of current scale

VSRL = low-byte value of current scale

Program Pin Pull-Down Register (PPD)

The PPD register (address = 07h) contains the pull-down programming pin information for the bq2052. The program pins, $PROG_{1–6}$, have a corresponding PPD register location, $PPD_{1–6}$. A given location is set if the bq2052 detects a pull-down resistor on its corresponding segment driver. For example, if $PROG_1$ and $PROG_4$ have pull-down resistors, the contents of PPD are xx001001.

Program Pin Pull-Up Register (PPU)

The PPU register (address = 08h) contains the pull-up programming pin information for the bq2052. The segment drivers, $PROG_{1–6}$, have a corresponding PPU register location, $PPU_{1–6}$. A given location is set if a pull-up resistor has been detected on its corresponding segment driver. For example, if $PROG_3$ and $PROG_5$ have pull-up resistors, the contents of PPU are xx010100.

Battery Voltage (VSB)

The battery voltage register (address = 0bh) stored the voltage detected on the SB pin. The bq2052 updates the VSB register approximately once per second with the present value of the battery voltage.

$$V_{SB} = 1.2V * \left(\frac{VSB}{256}\right)$$

Voltage Threshold Register (VTS)

The end-of-discharge threshold voltages (EDV1 and EDVF) can be set using the VTS register. The VTS register sets the EDV1 trip point. EDVF is set 100mV below EDV1. The default value in the VTS register is A2h, representing EDV1 = 0.76V and EDVF = 0.66V.

$$EDV1 = 1.2V * \left(\frac{VTS}{256}\right).$$

Relative CAC Register (RCAC)

The RCAC register (address = 0dh) provides the relative battery state-of-charge by dividing CAC by FNAC. RCAC varies from 0 to 7dh representing relative state-of-charge from 0 to 125%.

Compensated Available Capacity (CAC)

The CAC registers (address = 0eh–0fh) contain the available capacity compensated for discharge rate and temperature. The CAC value is also used in calculating the LED display pattern relative to PFC.

Program Full Count (PFC)

The PFC register (address = 10h) contains the user selected programmed full count (PFC) setting.

Full Nominal Available Capacity (FNAC)

The FNAC (address = 11h) contains the full capacity reference of the battery.

Maximum Discharge Rate (MAXRATE)

The MAXRATE register (address = 12h) stores the highest discharge rate detected by the bq2052. The bq2052 uses the MAXRATE value to calculate the efficiency compensation factors.

Discharge Rate (RATE)

The RATE register (address = 13h) provides the current discharge rate of the battery.

Discharge Count Registers (DCRH/DCRL)

The DCRH high-byte register and the DCRL low-byte register are the main gas gauging registers for the bq2052. The DCR registers are incremented during discharge.

Writing to the DCR registers affects the available charge counts and, therefore, affects the bq2052 gas gauge operation.

Display

The bq2052 can directly display remaining capacity information using low-power LEDs. The bq2052 uses the CAC value in relation to FNAC as the basis for the display activity. The bq2052 displays the battery's remaining capacity in either of three modes selected with program pin $PROG_5$. The display is activated using the $\overline{DISP}$ input. When $\overline{DISP}$ is connected to V_{CC}, the SEG outputs are OFF. When pulled low, the segment outputs turn ON for a period of 4 ± 0.5s, depending on the selected mode.

The segment outputs are modulated as two banks, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period. In incremental and bar graph modes, SEG1 blinks at a 4Hz rate whenever VSB is below VEDV1 (EDV1 flag bit set in FLGS1), indicating a low-battery condition. When VSB is below VEDVF (EDVF flag bit set in FLGS1) the display outputs are disabled in all modes.

In incremental mode ($PROG_5$ = L), the battery charge state is displayed on pins SEG1–SEG4. The charge state condition indicated by each segment is shown in Table 7. Only the segment pin representing the present remaining capacity is ON (low); all other segments are OFF (high impedance). When $\overline{DISP}$ is pulled low, the display is active for 10s.

Table 7. Incremental Display Mode
$PROG_5$ = L

SEG Pin ON	Remaining Capacity
SEG4	90 -100%
SEG3	50 - < 90%
SEG2	20 - < 50%
SEG1	< 20%
SEG1—BLINK	$V_{SB} < V_{EDV1}$

In binary mode (PROG5 = H), the battery charge state is displayed using only pins SEG1 and SEG2, with the remaining capacity indication defined as in Table 8. When $\overline{DISP}$ is pulled low, the display is active for 4s.

Table 8. Binary Display Mode
$PROG_5$ = H

SEG 1	SEG 2	Remaining Capacity
ON	ON	70 -100%
ON	OFF	40 - < 70%
OFF	ON	10 - < 40%
OFF	OFF	< 10% or $V_{SB} < V_{EDVF}$

In bar graph mode ($PROG_5$ = Z), the battery charge state is displayed using pins SEG1 through SEG 5 according to Table 9. When $\overline{DISP}$ is pulled low, the display is active for 4s.

Microregulator

A micro-power source for the bq2052 can be inexpensively built using a FET and an external resistor as shown in Figure 1.

RBI Input

The RBI input pin should be used with a storage capacitor or external supply to provide backup potential to the internal bq2052 registers when V_{CC} drops below 3.0V. V_{CC} is output on RBI when V_{CC} is above 3.0V. If using an external supply (such as the bottom series cell) as the backup source, an external diode is required for isolation.

Initialization

The bq2052 can be initialized by removing V_{CC} and grounding the RBI pin for 5s or by a command over the serial port. The serial port reset command requires writing 78h to register CMDWD (address = 00h).

On initialization with PROG6 = H, the bq2052 sets the registers as

FNAC = PFC
CACH = PFC
CACL = 0x00
RCAC = 0x64
FLGS1 = 0x90

Table 9. Bar Graph Display Mode
$PROG_5$ = Z

SEG1	SEG2	SEG3	SEG4	SEG5	Remaining Capacity
ON	ON	ON	ON	ON	80 - 100%
ON	ON	ON	ON	OFF	60 - < 80%
ON	ON	ON	OFF	OFF	40 - < 60%
ON	ON	OFF	OFF	OFF	20 - < 40%
ON	OFF	OFF	OFF	OFF	< 20%
BLINK	OFF	OFF	OFF	OFF	VSB < VEDV1

On initialization with PROG6=L, the bq2052 sets the registers as

FNAC = 0x00
CACH = 0x00
CACL = 0x00
RCAC = 0x00
FLGS1 = 0x10

Layout Considerations

The bq2052 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
REF	Relative to V_{SS}	-0.3	+8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	Vcc+0.7	V	Recommended 100KΩ series resistor should be used to protect SR in case of a shorted battery.
T_{OPR}	Operating temperature	-20	+70	°C	Commercial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDV1}	First empty warning	0.73	0.76	0.79	V	SB, default
V_{EDVF}	Final empty warning	-	V_{EDV1} - 0.10	-	V	SB, default
V_{SRO}	SR sense range	-300	-	+500	mV	SR, $V_{SR} + V_{OS}$
V_{SRD}	Valid discharge	-	-	-250	µV	$V_{SR} + V_{OS}$ (see note)

Note: V_{OS} is affected by PC board layout. Proper layout guidelines should be followed for optimal performance. See "Layout Considerations."

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{OS}	Offset referred to V_{SR}	-	±50	±150	µV	$\overline{DISP} = V_{CC}$
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V, HDQ = 0
		-	120	180	µA	V_{CC} = 4.25V, HDQ = 0
		-	170	250	µA	V_{CC} = 6.5V, HDQ = 0
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	$V_{DISP} = V_{SS}$
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP} = V_{CC}$
I_{RBI}	RBI data retention current	-	-	100	nA	$V_{RBI} > V_{CC} < 3V$
R_{HDQ}	Internal pulldown	500	-	-	KΩ	
R_{SR}	SR input impedance	10	-	-	MΩ	$V_{SR} < V_{CC}$
V_{IHPFC}	PROG logic input high	V_{CC} - 0.2	-	-	V	$PROG_{1-6}$
V_{ILPFC}	PROG logic input low	-	-	V_{SS} + 0.2	V	$PROG_{1-6}$
V_{IZPFC}	PROG logic input Z	float	-	float	V	$PROG_{1-6}$
V_{OLSL}	SEG output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA $SEG_{1–5}$, CP
V_{OLSH}	SEG output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA $SEG_{1–5}$, CP
V_{OHML}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHLCOM} = -5.25mA
V_{OHMH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} > 3.5V, I_{OHLCOM} = -33.0mA
I_{OLS}	SEG sink current	11.0	-	-	mA	At V_{OLSH} = 0.4V, V_{CC} = 6.5V
I_{OL}	Open-drain sink current	5.0	-	-	mA	At $V_{OL} = V_{SS}$ + 0.3V, HDQ
V_{OL}	Open-drain output low	-	-	0.3	V	I_{OL} ≤ 5mA, HDQ
V_{IHDQ}	HDQ input high	2.5	-	-	V	HDQ
V_{ILDQ}	HDQ input low	-	-	0.8	V	HDQ
R_{PROG}	Soft pull-up or pull-down resistor value (for programming)	-	-	200	KΩ	$PROG_1$–$PROG_6$
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	$PROG_{1–6}$

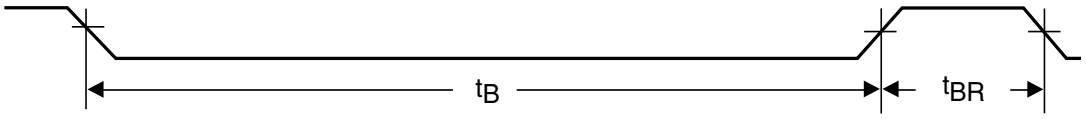
Note: All voltages relative to V_{SS}.

Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2052 (write)	190	-	-	µs	See note
t_{CYCB}	Cycle time, bq2052 to host (read)	190	205	250	µs	
t_{STRH}	Start hold, host to bq2052 (write)	5	-	-	ns	
t_{STRB}	Start hold, bq2052 to host (read)	32	-	-	µs	
t_{DSU}	Data setup	-	-	50	µs	
t_{DSUB}	Data setup	-	-	50	µs	
t_{DH}	Data hold	90	-	-	µs	
t_{DV}	Data valid	-	-	80	µs	
t_{SSU}	Stop setup	-	-	145	µs	
t_{SSUB}	Stop setup	-	-	145	µs	
t_{RSPS}	Response time, bq2052 to host	190	-	320	µs	
t_B	Break	190	-	-	µs	
t_{BR}	Break recovery	40	-	-	µs	

Note: The open-drain HDQ pin should be pulled to at least V_{CC} by the host system for proper HDQ operation. HDQ may be left floating if the serial interface is not used.

Break Timing



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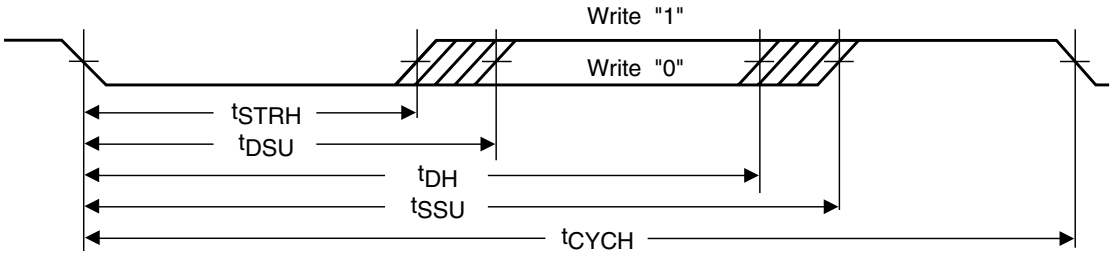
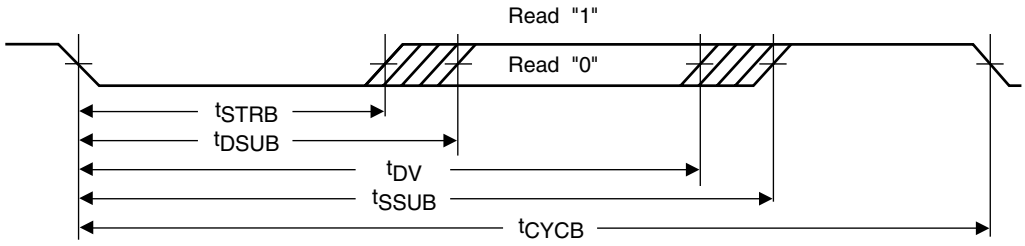
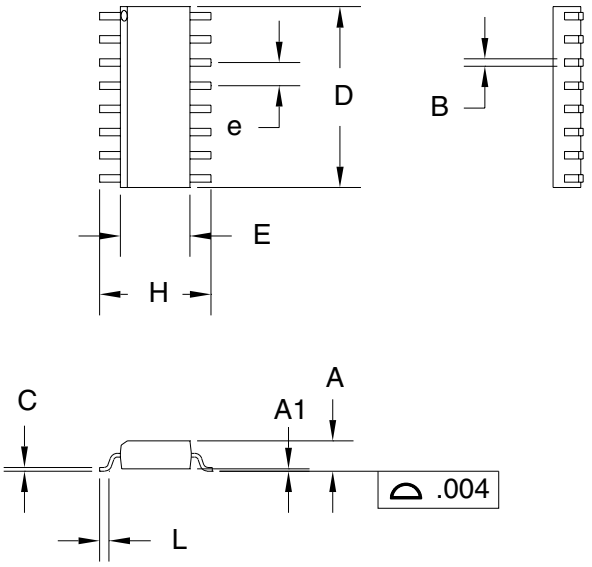
Host to bq2052



bq2052 to Host



16-Pin SOIC Narrow (SN)



16-Pin SN (SOIC Narrow)

Dimension	Minimum	Maximum
A	0.060	0.070
A1	0.004	0.010
B	0.013	0.020
C	0.007	0.010
D	0.385	0.400
E	0.150	0.160
e	0.045	0.055
H	0.225	0.245
L	0.015	0.035

All dimensions are in inches.

Ordering Information

bq2052

Temperature Range:
blank = Commercial (-20 to +70°C)

Package Option:
SN = 16-pin narrow SOIC

Device:
bq2052 Gas Gauge IC

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