



Process C1004

CMOS 1.0μm

5 Volt Digital

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	V_{TN}	0.55	0.75	0.95	V	100x1.0μm
Body Factor	γ_N		0.60		$V^{1/2}$	100x1.0μm
Conduction Factor	β_N	74	87	100	$\mu A/V^2$	100x100μm
Effective Channel Length	L_{effN}	0.60	0.75	0.90	μm	100x1.0μm
Width Encroachment	ΔW_N		0.8		μm	Per side
Punch Through Voltage	$BVDSS_N$	7			V	
Poly Field Threshold	$VTF_{P(N)}$	10			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	V_{TP}	-0.85	-1.0	-1.15	V	100x1.0μm
Body Factor	γ_P		0.4		$V^{1/2}$	100x1.0μm
Conduction Factor	β_P	24	28	32	$\mu A/V^2$	100x100μm
Effective Channel Length	L_{effP}	0.83	0.98	1.13	μm	100x1.0μm
Width Encroachment	ΔW_P		0.85		μm	Per side
Punch Through Voltage	$BVDSS_P$	-7			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	-10			V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N-well(f)}$	0.8	1.0	1.22	$K\Omega/\square$	n-well
N+ Sheet Resistance	ρ_{N+}	20	35	50	Ω/\square	
N+ Junction Depth	x_{jN+}		0.45		μm	
P+ Sheet Resistance	ρ_{P+}	60	80	100	Ω/\square	
P+ Junction Depth	x_{jP+}		0.5		μm	
Gate Oxide Thickness	T_{GOX}		20		nm	
Field Oxide Thickness	T_{FIELD}		700		nm	
Poly Sheet Resistance	ρ_{POLY}	15	22	30	Ω/\square	
Metal-1 Sheet Resistance	ρ_{M1}		50		$m\Omega/\square$	
Metal-2 Sheet Resistance	ρ_{M2}		30		$m\Omega/\square$	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

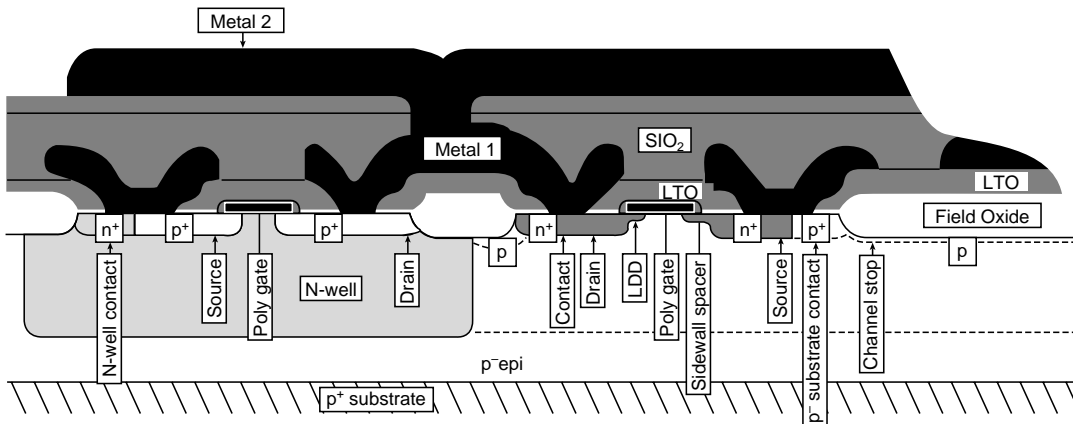
Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{ox}	1.52	1.64	1.82	fF/μm ²	
Metal-1 to Poly1	C_{M1P}		0.046		fF/μm ²	
Metal-1 to Silicon	C_{MIS}		0.028		fF/μm ²	
Metal-2 to Metal-1	C_{MM}		0.038		fF/μm ²	



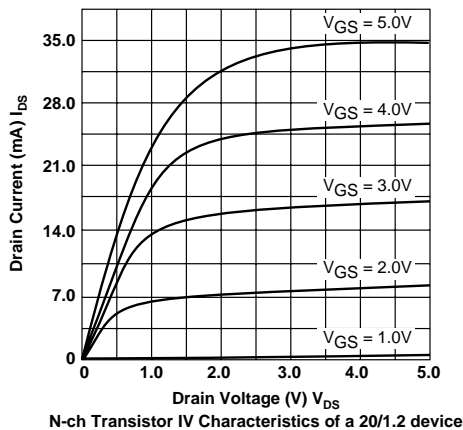
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Physical Characteristics

Starting Material	P <100>	N+/P+ Width/Space	2.0 / 1.2 μ m
Starting Mat. Resistivity	7-8.5 Ω -cm	N+ To P+ Space	7.0 μ m
Typ. Operating Voltage	5V	Contact To Poly Space	0.8 μ m
Well Type	N-well	Contact Overlap Of Diffusion	0.7 μ m
Metal Layers	2	Contact Overlap Of Poly	0.7 μ m
Poly Layers	1	Metal-1 Overlap Of Contact	0.7 μ m
Contact Size	1.2x1.2 μ m	Metal-1 Overlap Of Via	0.7 μ m
Via Size	1.2x1.2 μ m	Metal-2 Overlap Of Via	0.7 μ m
Metal-1 Width/Space	1.4 / 1.2 μ m	Minimum Pad Opening	65x65 μ m
Metal-2 Width/Space	2.0 / 1.4 μ m	Minimum Pad-to-Pad Spacing	5.0 μ m
Gate Poly Width/Space	1.0 / 1.4 μ m	Minimum Pad Pitch	80.0 μ m



ID vs VD, W/L = 20/1.2



ID vs VD, W/L = 20/1.2

