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intersil

# CA3304, CA3304A

August 1997

## 4-Bit, 25 MSPS, Flash A/D Converters

### Features

- CMOS/SOS Low Power with Video Speed (Typ) . . 25mW
- Parallel Conversion Technique
- Single Power Supply Voltage . . . . . 3V to 7.5V
- 25MHz Sampling Rate (40ns Conversion Time) at 5V Supply
- 4-Bit Latched Three-State Output with Overflow and Data Change Outputs
- $^1/_8$ LSB Maximum Nonlinearity (A Version)
- Inherent Resistance to Latch-Up Due to SOS Process
- Bipolar Input Range with Optional Second Supply
- Wide Input Bandwidth (Typ) . . . . . 25MHz

### Applications

- High Speed A/D Conversion
- Ultrasound Signature Analysis
- Transient Signal Analysis
- High Energy Physics Research
- General-Purpose Hybrid ADCs
- Optical Character Recognition
- Radar Pulse Analysis
- Motion Signature Analysis
- Robot Vision
- RSSI Circuits

### Description

The Intersil CA3304 is a CMOS parallel (FLASH) analog-to-digital converter designed for applications demanding both low-power consumption and high speed digitization. Digitizing at 25MHz, for example, requires only about 35mW.

The CA3304 operates over a wide, full-scale signal input voltage range of 0.5V up to the supply voltage. Power consumption is as low as 10mW, depending upon the clock frequency selected.

The intrinsic high conversion rate makes the CA3304 types ideally suited for digitizing high speed signals. The overflow bit makes possible the connection of two or more CA3304s in series to increase the resolution of the conversion system. A series connection of two CA3304s may be used to produce a 5-bit, 25MHz converter. Operation of two CA3304s in parallel doubles the conversion speed (i.e., increases the sampling rate from 25MHz to 50MHz). A data change pin indicates when the present output differs from the previous, thus allowing compaction of data storage.

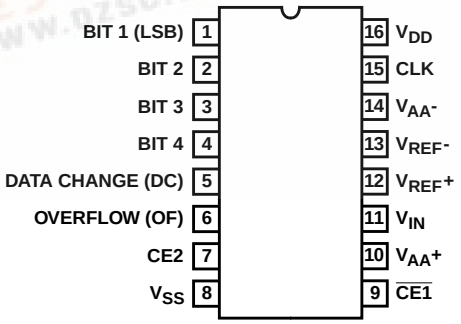
Sixteen paralleled auto-balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel-bit outputs in the CA3304. Fifteen comparators are required to quantize all input voltage levels in this 4-bit converter, and the additional comparator is required for the overflow bit.

### Ordering Information

| PART NUMBER | LINEARITY (INL, DNL) | SAMPLING RATE | TEMP. RANGE ($^o$C) | PACKAGE | PKG. NO. |
|---|---|---|---|---|---|
| CA3304E | ±0.25 LSB | 25MHz (40ns) | -40 to 85 | 16 Ld PDIP | E16.3 |
| CA3304AE | ±0.125 LSB | 25MHz (40ns) | -40 to 85 | 16 Ld PDIP | E16.3 |
| CA3304M | ±0.25 LSB | 25MHz (40ns) | -40 to 85 | 16 Ld SOIC (W) | M16.3 |
| CA3304AM | ±0.125 LSB | 25MHZ (40ns) | -40 to 85 | 16 Ld SOIC (W) | M16.3 |
| CA3304D | ±0.25 LSB | 25MHz (40ns) | -55 to 125 | 16 Ld SBDIP | D16.3 |
| CA3304AD | ±0.125 LSB | 25MHz (40ns) | -55 to 125 | 16 Ld SBDIP | D16.3 |

### Pinout

CA3304 (SBDIP, PDIP, SOIC)
TOP VIEW

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CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

## Absolute Maximum Ratings

DC Supply Voltage Range ($V_{DD}$ or $V_{AA}$+)
(Voltage Referenced to $V_{SS}$ or $V_{AA}$- Terminal, Whichever is More Negative) . . . . . -0.5V to +8V
Input Voltage Range
CE1, CE2 Inputs . . . . . $V_{SS}$ -0.5V to $V_{DD}$ +0.5V
Clock, $V_{REF}$+, $V_{REF}$-, $V_{IN}$ Inputs . . . . . $V_{AA}$- -0.5V to $V_{AA}$- +0.5V
DC Input Current, Any Input . . . . . ±20mA

## Operating Conditions

Recommended Supply Voltage Range ($V_{DD}$ or $V_{AA}$+) . . . . .3V to 7.5V
Recommended $V_{AA}$+ Voltage Range . . . . . $V_{DD}$ -1V to $V_{DD}$ +2.5V
Recommended $V_{AA}$- Voltage Range . . . . . $V_{SS}$ -2.5V to $V_{SS}$ +1V
Operating Temperature
CA3304D . . . . . -55°C to 125°C
CA3304E, CA3304M. . . . . -40°C to 85°C

## Thermal Information

| Thermal Resistance (Typical, Note 1) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| SBDIP Package | 80 | 22 |
| PDIP Package | 90 | N/A |
| SOIC Package | 100 | N/A |

Maximum Junction Temperature
Ceramic Package . . . . . 175°C
Plastic Package . . . . . 150°C
Maximum Storage Temperature Range ($T_{STG}$) . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications

$T_A$ = 25°C, $V_{REF}$+ = 2V, $V_{DD}$ = $V_{AA}$+ = 5V, $V_{AA}$- = $V_{REF}$- = $V_{SS}$ = GND, $f_{CLK}$ = 25MHz Unless Otherwise Specified

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **SYSTEM PERFORMANCE** | | | | | | | |
| Resolution | | | | 4 | - | - | Bits |
| Input Errors | Integral Linearity Error | CA3304A | | - | ±0.1 | ±0.125 | LSB |
| | | CA3304 | | - | ±0.125 | ±0.25 | LSB |
| | Differential Linearity Error | CA3304A | | - | ±0.1 | ±0.125 | LSB |
| | | CA3304 | | - | ±0.125 | ±0.25 | LSB |
| | Offset Error (Unadjusted) | CA3304A | | - | - | ±0.75 | LSB |
| | | CA3304 | | - | - | ±1.0 | LSB |
| | Gain Error (Unadjusted) | CA3304A | | - | - | ±0.75 | LSB |
| | | CA3304 | | - | - | ±1.0 | LSB |
| **DYNAMIC CHARACTERISTICS** (Input Signal Level 0.5dB Below Full Scale) | | | | | | | |
| Conversion Timing | Aperture Delay | | | - | 3 | - | ns |
| Signal to Noise Ratio, SNR = $\frac{\text{RMS Signal}}{\text{RMS Noise}}$ | | | $f_S$ = 25MHz, $f_{IN}$ = 100kHz | - | 23.7 | - | dB |
| | | | $f_S$ = 25MHz, $f_{IN}$ = 5MHz | - | 23.6 | - | dB |
| Signal to Noise Ratio, SINAD = $\frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$ | | | $f_S$ = 25MHz, $f_{IN}$ = 100kHz | - | 23.4 | - | dB |
| | | | $f_S$ = 25MHz, $f_{IN}$ = 5MHz | - | 22.8 | - | dB |
| Total Harmonic Distortion, THD | | | $f_S$ = 25MHz, $f_{IN}$ = 100kHz | - | -34.5 | - | dBc |
| | | | $f_S$ = 25MHz, $f_{IN}$ = 5MHz | - | -31.0 | - | dBc |
| Effective Number of Bits, ENOB | | | $f_S$ = 25MHz, $f_{IN}$ = 100kHz | - | 3.67 | - | Bits |
| | | | $f_S$ = 25MHz, $f_{IN}$ = 5MHz | - | 3.57 | - | Bits |
| **ANALOG INPUTS** | | | | | | | |
| Input Range | Full Scale Input Range | | (Notes 1, 4) | 0.5 | - | $V_{AA}$ | V |
| Input Loading | Input Capacitance | | | - | 10 | - | pF |
| | Input Current | | $V_{IN}$ = 2V (Note 2) | - | 150 | 200 | µA |

**Electrical Specifications** $T_A = 25^oC$, $V_{REF}+ = 2V$, $V_{DD} = V_{AA}+ = 5V$, $V_{AA}- = V_{REF}- = V_{SS} = GND$, $f_{CLK} = 25MHz$ Unless Otherwise Specified **(Continued)**

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Allowable Input Bandwidth | | | (Note 4) | - | 25 | $f_{CLK}/2$ | MHz |
| -3dB Input Bandwidth | | | | - | 40 | - | MHz |
| **REFERENCE INPUTS** | | | | | | | |
| Input Range | $V_{REF}+$ Range | | (Note 4) | $V_{AA}-+0.5$ | - | $V_{AA}+$ | V |
| | $V_{REF}-$ Range | | (Note 4) | $V_{AA}-$ | - | $V_{AA}+-0.5$ | V |
| Input Loading | Resistor Ladder Impedance | | $V_{IN}$ = 5V, CLK = Low | 640 | - | 960 | Ω |
| **DIGITAL INPUTS** | | | | | | | |
| Digital Input | Maximum $V_{IN}$, Low | CLOCK | (Notes 3, 4) | - | - | $0.3 \times V_{AA}$ | V |
| | | $\overline{CE1}$, CE2 | (Note 4) | - | - | $0.3 \times V_{DD}$ | V |
| | Minimum $V_{IN}$, High | CLOCK | (Notes 3, 4) | $0.7 \times V_{AA}$ | - | - | V |
| | | $\overline{CE1}$, CE2 | (Note 4) | $0.7 \times V_{DD}$ | - | - | V |
| | Input Leakage, Except CLK | | V = 0V, 5V | - | - | ±1 | µA |
| | Input Leakage, CLK | | (Note 3) | - | ±100 | ±150 | µA |
| **DIGITAL OUTPUTS** | | | | | | | |
| Digital Outputs | Output Low (Sink) Current | | $V_O$ = 0.4V | 6 | - | - | mA |
| | Output High (Source) Current | | $V_O$ = 4.6V | -3 | - | - | mA |
| | Three-State Leakage Current | | $V_O$ = 0V, 5V | - | ±0.2 | ±5 | µA |
| **TIMING CHARACTERISTICS** | | | | | | | |
| Conversion Timing | Maximum Conversion Speed | | CLK = Square Wave | 25 | 35 | - | MSPS |
| | Auto-Balance Time ($\phi$1) | | | 20 | - | - | ns |
| | Sample Time ($\phi$2) | | | 20 | - | 5000 | ns |
| Output Timing | Data Valid Delay | | (Note 4) | - | 30 | 40 | ns |
| | Data Hold Time | | (Note 4) | 15 | 25 | - | ns |
| | Output Enable Time | | | - | 15 | - | ns |
| | Output Disable Time | | | - | 10 | - | ns |
| **POWER SUPPLY CHARACTERISTICS** | | | | | | | |
| Device Current, $I_{AA}$ | | | Continuous Clock | - | 5.5 | - | mA |
| | | | Continuous $\phi$2 | - | 0.4 | - | mA |
| | | | Continuous $\phi$1 | - | 2 | - | mA |
| Device Current, $I_{DD}$ | | | Continuous Clock | - | 1.5 | - | mA |
| | $V_{AA}+ = 5V$, $V_{SS} = \overline{CE1} = V_{AA}- = CLK = GND$ | | Continuous $\phi$2 | - | 5 | 10 | mA |
| | $V_{AA}+ = 7V$ | | Continuous $\phi$1 | - | 5 | 20 | mA |

NOTES:

1. Full scale input range, $V_{REF}+ - V_{REF}-$, may be in the range of 0.5V to $V_{AA}+ - V_{AA}-$ volts. Linearity errors increase at lower full scale ranges, however.
2. Input current is due to energy transferred to the input at the start of the sample period. The average value is dependent on input and $V_{DD}$ voltage.
3. The CLK input is a CMOS inverter with a 50kΩ feedback resistor. It operates from the $V_{AA}+$ and $V_{AA}-$ supplies. It may be AC-coupled with a $1V_{P-P}$ minimum source.
4. Parameter not tested, but guaranteed by design or characterization.

## Pin Descriptions

| PIN NUMBER | NAME | DESCRIPTION | |
|---|---|---|---|
| 1 | Bit 1 | Bit 1 (LSB). | Output Data Bits (High = True) |
| 2 | Bit 2 | Bit 2. | |
| 3 | Bit 3 | Bit 3. | |
| 4 | Bit 4 | Bit 4 (MSB). | |
| 5 | DC | Data Change. | |
| 6 | OF | Overflow. | |
| 7 | CE2 | Three-State Output Enable Input, active low. See the Chip Enable Truth Table. | |
| 8 | $V_{SS}$ | Digital Ground. | |
| 9 | $\overline{CE1}$ | Three-State Output Enable Input, active high. See the Chip Enable Truth Table. | |
| 10 | $V_{AA}+$ | Analog Power Supply, +5V. | |
| 11 | $V_{IN}$ | Analog Signal Input. | |
| 12 | $V_{REF}+$ | Reference Voltage Positive Input. | |
| 13 | $V_{REF}-$ | Reference Voltage Negative Input. | |
| 14 | $V_{AA}-$ | Analog Ground. | |
| 15 | CLK | Clock Input. | |
| 16 | $V_{DD}$ | Digital Power Supply, +5V. | |

**CHIP ENABLE TRUTH TABLE**

| $\overline{CE1}$ | CE2 | BIT 1 - BIT 4 | DC, OF |
|---|---|---|---|
| 0 | 1 | Valid | Valid |
| 1 | 1 | Three-State | Valid |
| X | 0 | Three-State | Three-State |

X = Don't Care

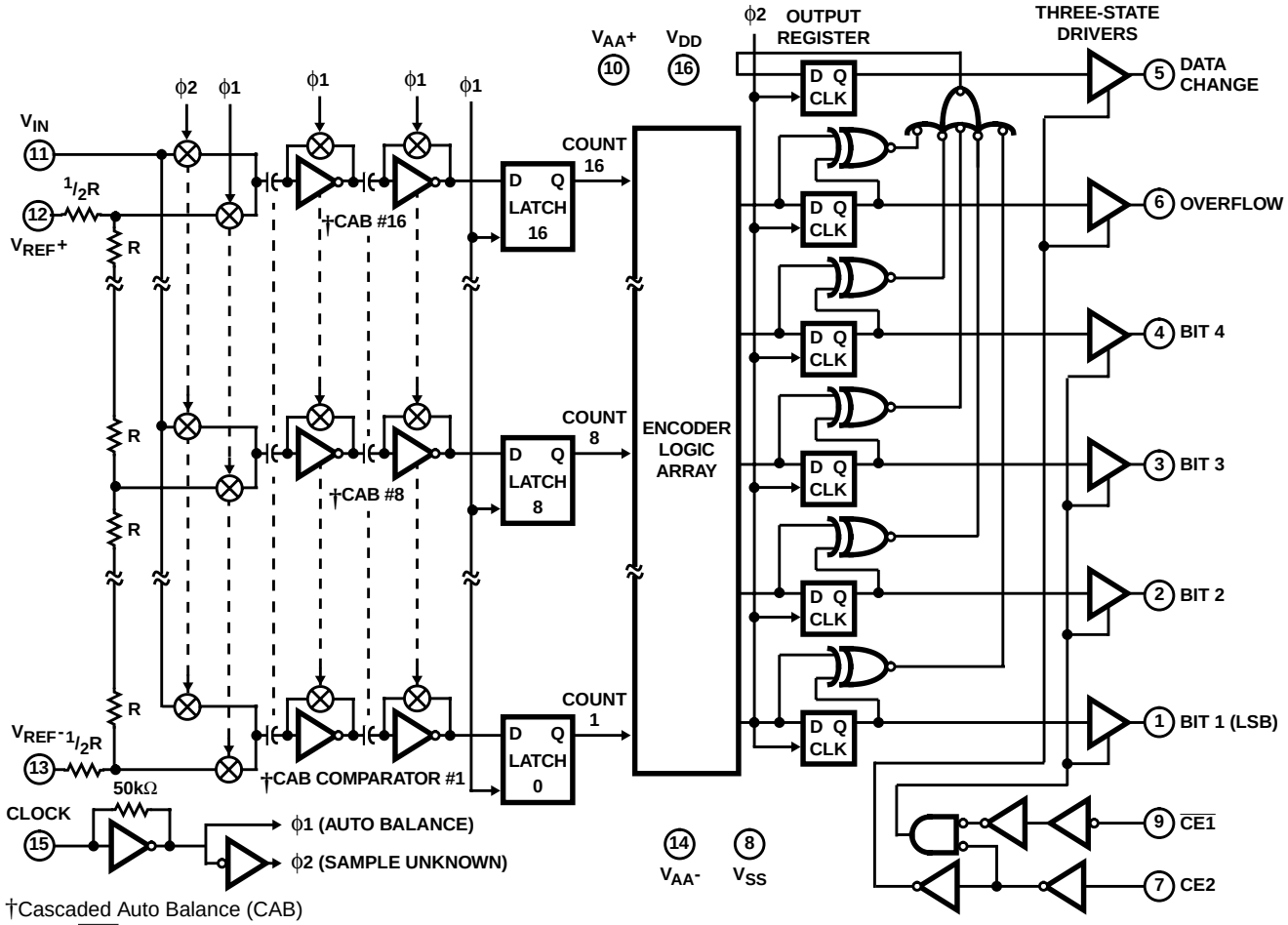
**TABLE 1. OUTPUT CODE TABLE**

| CODE DESCRIPTION | INPUT VOLTAGE (V) | | | | | OUTPUT CODE | | | | | DECIMAL COUNT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $V_{REF}+$ = 1V<br>$V_{REF}-$ = -1V | 1.6V<br>0V | 2V<br>0V | 3.2V<br>0V | 4.8V<br>0V | OF | B4 | B3 | B2 | B1 | |
| Zero | -1.000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 LSB | -0.875 | 0.1 | 0.125 | 0.2 | 0.3 | 0 | 0 | 0 | 0 | 1 | 1 |
| 2 LSB | -0.750 | 0.2 | 0.250 | 0.4 | 0.6 | 0 | 0 | 0 | 1 | 0 | 2 |
| • | • | • | • | • | • | • | • | • | • | • | • |
| • | • | • | • | • | • | • | • | • | • | • | • |
| • | • | • | • | • | • | • | • | • | • | • | • |
| • | • | • | • | • | • | • | • | • | • | • | • |
| $^1/_2$ Full Scale -1 LSB | -0.125 | 0.7 | 0.875 | 1.4 | 2.1 | 0 | 0 | 1 | 1 | 1 | 7 |
| $^1/_2$ Full Scale | 0 | 0.8 | 1.000 | 1.6 | 2.4 | 0 | 1 | 0 | 0 | 0 | 8 |
| $^1/_2$ Full Scale +1 LSB | 0.125 | 0.9 | 1.125 | 1.8 | 2.7 | 0 | 1 | 0 | 0 | 1 | 9 |
| • | • | • | • | • | • | • | • | • | • | • | • |
| • | • | • | • | • | • | • | • | • | • | • | • |
| • | • | • | • | • | • | • | • | • | • | • | • |
| • | • | • | • | • | • | • | • | • | • | • | • |
| Full Scale -1 LSB | 0.750 | 1.4 | 1.750 | 2.8 | 4.2 | 0 | 1 | 1 | 1 | 0 | 14 |
| Full Scale | 0.875 | 1.5 | 1.875 | 3.0 | 4.5 | 0 | 1 | 1 | 1 | 1 | 15 |
| Overflow | 1.000 | 1.6 | 2.000 | 3.2 | 4.8 | 1 | 1 | 1 | 1 | 1 | 31 |
| Step Size | 0.125 | 0.1 | 0.125 | 0.2 | 0.3 | | | | | | |

NOTE:

1. The voltages listed are the ideal centers of each output code shown as a function of its associated reference voltage See Ideal Transfer Curve Figure 6. The output code should exist for an input equal to the ideal center voltage $\pm^1/_2$ of the step size.

## Functional Diagram




†Cascaded Auto Balance (CAB)

NOTE: $\overline{CE1}$ and CE2 inputs and data outputs have standard CMOS protection networks to $V_{DD}$ and $V_{SS}$. Analog inputs and clock have standard CMOS protection networks to $V_{AA}+$ and $V_{AA}-$.

## Timing Diagrams

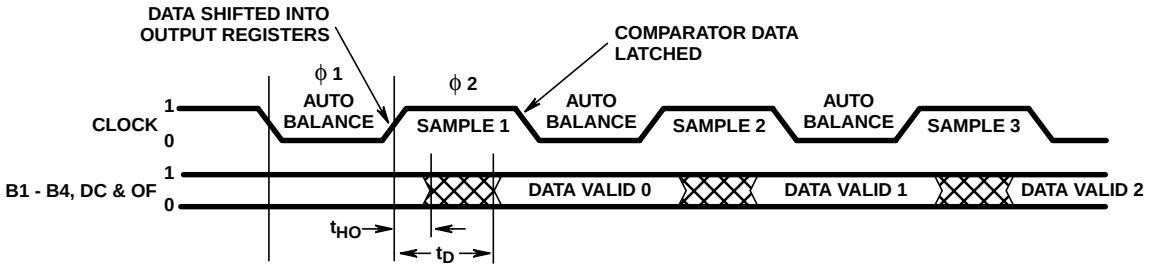



FIGURE 1. TIMING DIAGRAM

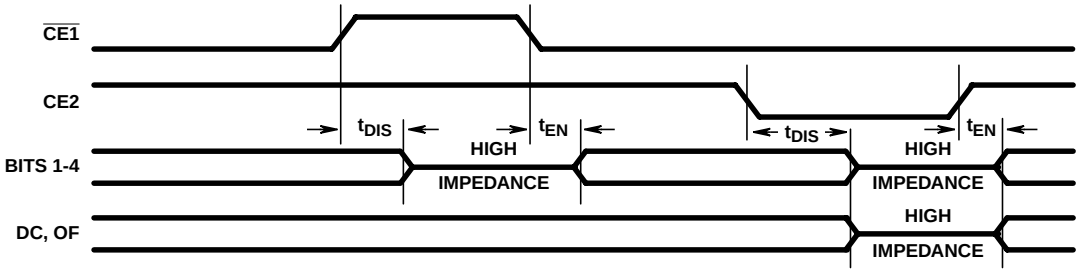



FIGURE 2. OUTPUT ENABLE/DISABLE TIMING

## Timing Diagrams (Continued)

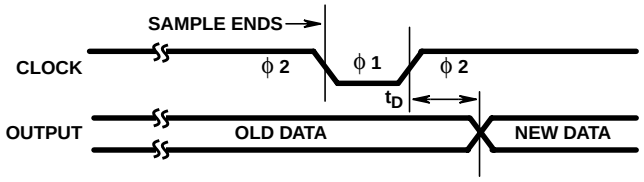



**FIGURE 3A.**
With ϕ2 as standby state (fastest method, but standby limited to 5μs maximum)

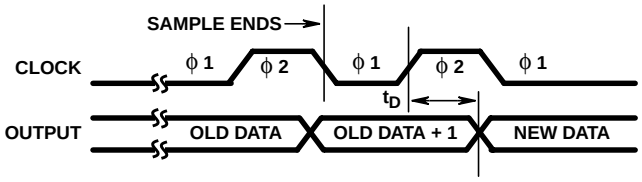



**FIGURE 3B.**
With ϕ1 as standby state (indefinite standby, double pulse needed)

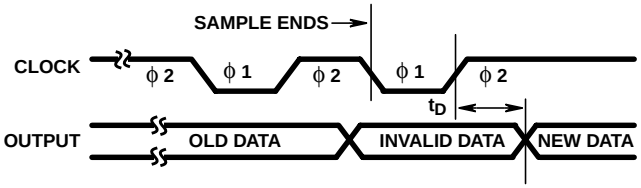



**FIGURE 3C.**
With ϕ2 as standby state (indefinite standby, lower power than 3B)

**FIGURE 3. PULSE-MODE TIMING DIAGRAMS**

## Typical Performance Curves

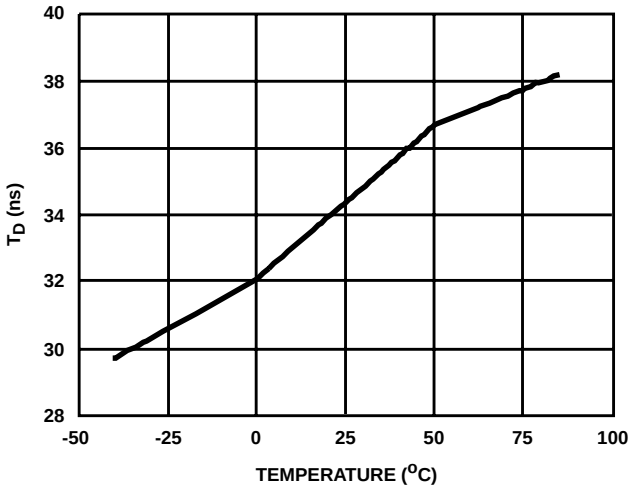



**FIGURE 4. DATA DELAY vs TEMPERATURE**

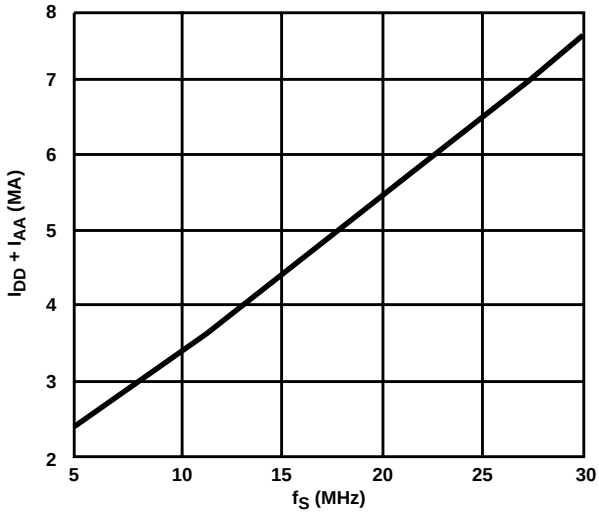



**FIGURE 5. DEVICE CURRENT vs SAMPLE FREQUENCY**

## Typical Performance Curves (Continued)

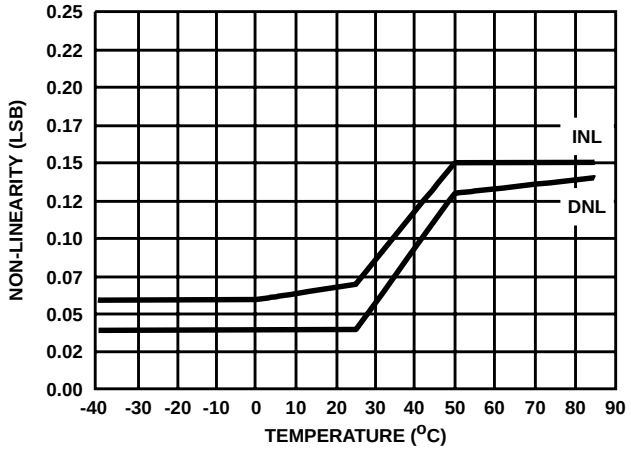



FIGURE 6. NON-LINEARITY vs TEMPERATURE

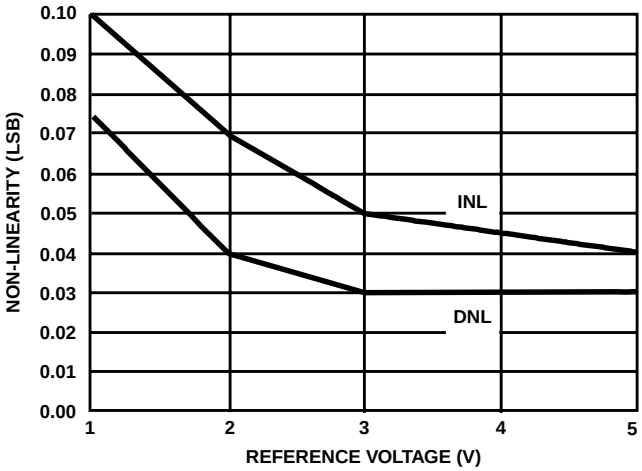



FIGURE 7. NON-LINEARITY vs REFERENCE VOLTAGE

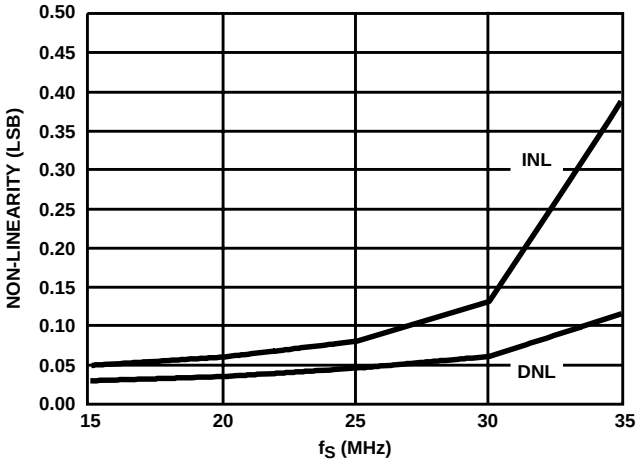



FIGURE 8. NON-LINEARITY vs SAMPLE FREQUENCY

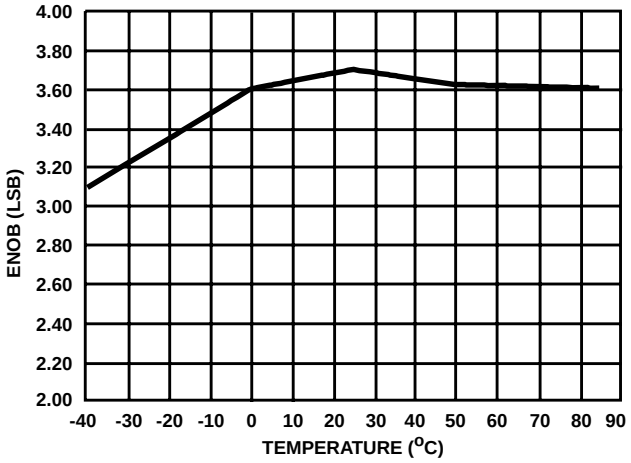



FIGURE 9. EFFECTIVE BITS vs TEMPERATURE

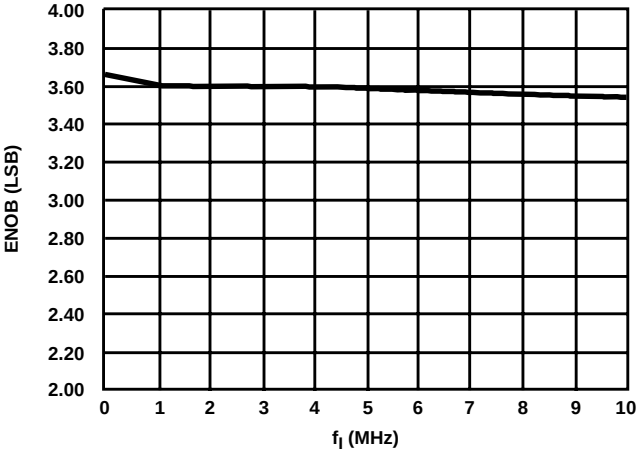



FIGURE 10. EFFECTIVE BITS vs INPUT FREQUENCY

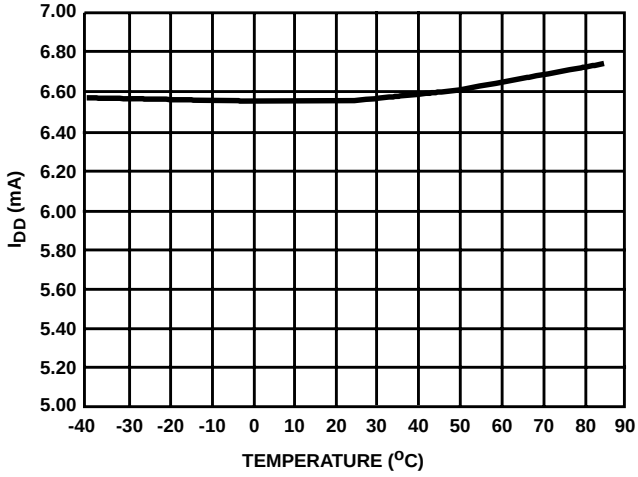



FIGURE 11. DEVICE CURRENT vs TEMPERATURE

## Typical Performance Curves (Continued)

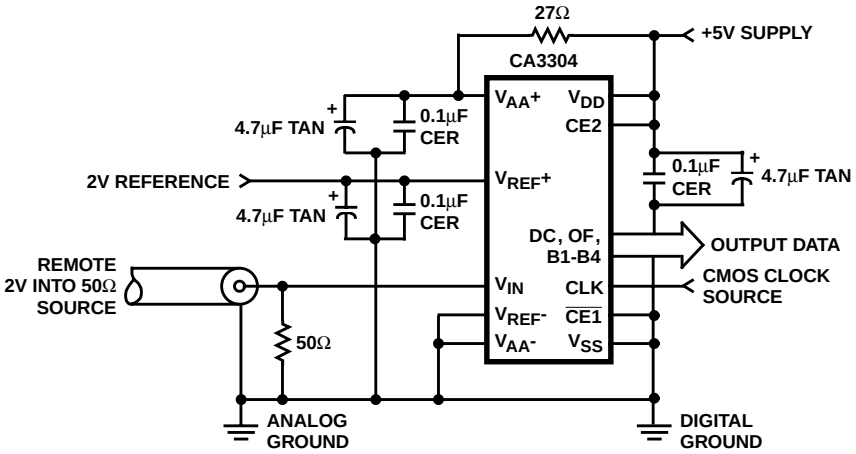



FIGURE 12A. TYPICAL CA3304 UNIPOLAR CIRCUIT CONFIGURATION

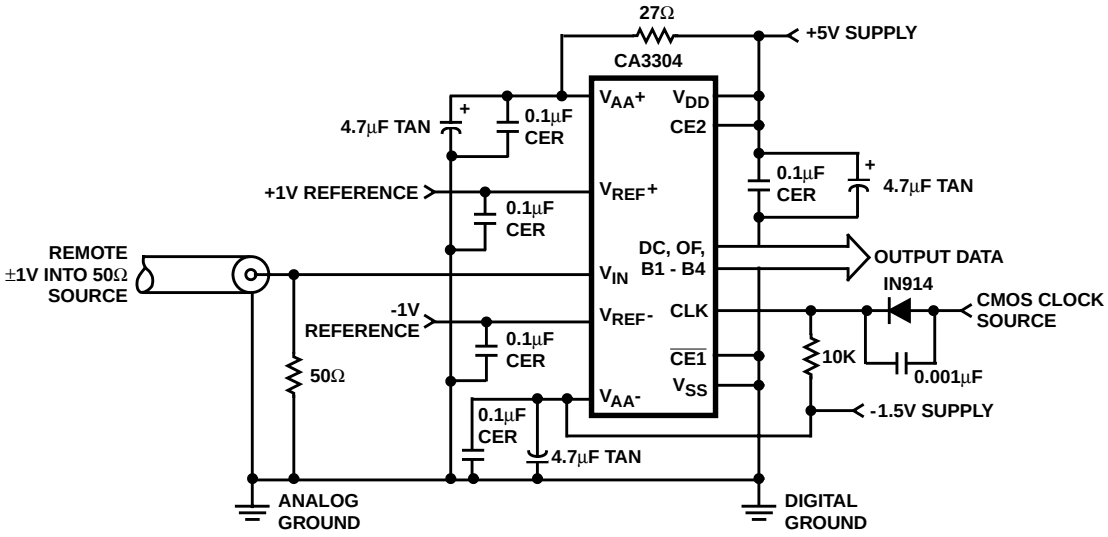



FIGURE 12B. TYPICAL CA3304 BIPOLAR CIRCUIT CONFIGURATION

FIGURE 12.

## Description

### Device Operation

A sequential parallel technique is used by the CA3304 converter to obtain its high speed operation. The sequence consists of the "Auto Balance" phase and the "Sample Unknown" phase (Refer to the circuit diagram). Each conversion takes one clock cycle (see Note). The "Auto Balance" ($\phi$1) occurs during the Low period of the clock cycle, and the "Sample Unknown" ($\phi$2) occurs during the High period of the clock cycle.

NOTE: This device requires only a single-phase clock. The terminology of $\phi$1 and $\phi$2 refers to the High and Low periods of the same clock.

During the "Auto Balance" phase, a transmission-gate switch is used to connect each of 16 commutating capacitors to their associated ladder reference tap. Those tap voltages will be as follows:

$$V_{TAP}(N) = [(V_{REF}/16) \times N] - [V_{REF}/(2 \times 16)]$$
$$= V_{REF}\,[(2N - 1)/32],$$

Where:

$V_{TAP}(N)$ = Reference ladder tap voltage at point N,
$V_{REF}$ = Voltage across $V_{REF}$- to $V_{REF}$+, and
N = Tap number (1 through 16).

The other side of the capacitor is connected to a single-stage inverting amplifier whose output is shorted to its input by a switch. This biases the amplifier at its intrinsic trip point, which is approximately $(V_{DD} - V_{SS})/2$. The capacitors now charge to their associated tap voltages, priming the circuit for the next phase.

In the "Sample Unknown" phase, all ladder tap switches are opened, the comparator amplifiers are no longer shorted, and $V_{IN}$ is switched to all 16 capacitors. Since the other end of the capacitor is now looking into an effectively open circuit, any voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators whose tap voltages were lower than $V_{IN}$ will drive the comparator outputs to a "low" state. All comparators whose tap voltages were higher than $V_{IN}$ will drive the comparator outputs to a "high" state. A second, capacitor-coupled, auto-zeroed amplifier further amplifies the outputs.

The status of all these comparator amplifiers are stored at the end of this phase ($\phi$2), by a secondary latching amplifier stage. Once latched, the status of the 16 comparators is decoded by a 16 to 5 bit decode array and the results are clocked into a storage register at the rising edge of the next $\phi$2.

If the input is greater than 31/32 x $V_{REF}$, the overflow output will go "high". (The bit outputs will remain high). If the output differs from that of the previous conversion, the data change output will go "high".

A three-state buffer is used at the output of the 7 storage registers which are controlled by two chip-enable signals. $\overline{CE1}$ will independently disable B1 through B4 when it is in a high state. CE2 will independently disable B1 through B4 and the OF and DC buffers when it is in the low state.

### Continuous Clock Operation

One complete conversion cycle can be traced through the CA3304 via the following steps. (Refer to timing diagram Figure 3). The rising edge of the clock input will start a "sample" phase. During this entire "High" state of the clock, the 16 comparators will track the input voltage and the 16 latches will track the comparator outputs. At the falling edge of the clock, all 16 comparator outputs are captured by the 16 latches. This ends the "sample" phase and starts the "auto balance" phase for the comparators. During this "Low" state of the clock the output of the latches propagates through the decode array and a 6-bit code appears at the D inputs of the output registers. On the next rising edge of the clock, this 6-bit code is shifted into the output registers and appears with time delay $t_D$ as valid data at the output of the three-state drivers. This also marks the start of a new "sample" phase, thereby repeating the conversion process for this next cycle.

### Pulse Mode Operation

For sampling high speed nonrecurrent or transient data, the converter may be operated in a pulse mode in one of three ways. The fastest method is to keep the converter in the Sample Unknown phase, $\phi$2, during the standby state. The device can now be pulsed through the Auto Balance phase with as little as 20ns. The analog value is captured on the leading edge of $\phi$1 and is transferred into the output registers on the trailing edge of $\phi$1. We are now back in the standby state, $\phi$2, and another conversion can be started within 20ns, but not later than 5$\mu$s due to the eventual droop of the commutating capacitors. Another advantage of this method is that it has the potential of having the lowest power drain. The larger the time ratio between $\phi$2 and $\phi$1, the lower the power consumption. (See Timing Diagram Figure 3A).

The second method uses the Auto Balance phase, $\phi$1, as the standby state. In this state the converter can stay indefinitely waiting to start a conversion. A conversion is performed by strobing the clock input with two $\phi$2 pulses. The first pulse starts a Sample Unknown phase and captures the analog value in the comparator latches on the trailing edge. A second $\phi$2 pulse is needed to transfer the date into the output registers. This occurs on the leading edge of the second pulse. The conversion now takes place in 40ns, but the repetition rate may be as slow as desired. The disadvantage to this method is the slightly higher device dissipation due to the low ratio of $\phi$2 to $\phi$1. (See Timing Diagram Figure 3B).

For applications requiring both indefinite standby and lowest power, standby can be in the $\phi$2 (Sample Unknown) state with two $\phi$1 pulses to generate valid data (see Figure 3C). The conversion process now takes 60ns. [Note that the above numbers do not include the $t_D$ (Output Delay) time.]

### Increased Accuracy

In most case the accuracy of the CA3304 should be sufficient without any adjustments. In applications where accuracy is of utmost importance, two adjustments can be made to obtain better accuracy; i.e., offset trim and gain trim.

**Offset Trim**

In general offset correction can be done in the preamp circuitry by introducing a DC shift to $V_{IN}$ or by the offset trim of the op amp. When this is not possible the $V_{REF}$- input can be adjusted to produce an offset trim.

The theoretical input voltage to produce the first transition is $^1/_2$ LSB. The equation is as follows:

$$V_{IN} \text{ (0 to 1 transition)} = {}^1/_2 \text{ LSB} = {}^1/_2(V_{REF}/16)$$
$$= V_{REF}/32.$$

Adjust offset by applying this input voltage and adjusting the $V_{REF}$- voltage or input amplifier offset until an output code alternating between 0 and 1 occurs.

**Gain Trim**

In general the gain trim can also be done in the preamp circuitry by introducing a gain adjustment for the op amp. When this is not possible, then a gain adjustment circuit should be made to adjust the reference voltage. To perform this trim, $V_{IN}$ should be set to the 15 to overflow transition. That voltage is $^1/_2$ LSB less than $V_{REF}$+ and is calculated as follows:

$$V_{IN} \text{ (15 to 16 transition)} = V_{REF} - V_{REF}/32$$
$$= V_{REF} (31/32).$$

To perform the gain trim, first do the offset trim and then apply the required $V_{IN}$ for the 15 to overflow transition. Now adjust $V_{REF}$+ until that transition occurs on the outputs.

**Layout, Input And Supply Considerations**

The CA3304 should be mounted on a ground-planed, printed-circuit board, with good high-frequency decoupling capacitors mounted as close as possible. If the supply is noisy, decouple $V_{AA}$+ with a resistor as shown in Figure 12A. The CA3304 outputs current spikes to its input at the start of the auto-balance and sample clock phases. A low impedance source, such as a locally-terminated 50Ω coax cable, should be used to drive the input terminal. A fast-settling buffer such as the HA-5033, HA-5242, or CA3450 should be used if the source is high impedance. The $V_{REF}$ terminals also have current spikes, and should be well bypassed.

Care should be taken to keep digital signals away from the analog input, and to keep digital ground currents away from the analog ground. If possible, the analog ground should be connected to digital ground only at the CA3304.

**Bipolar Operation**

The CA3304, with separate analog ($V_{AA}$+, $V_{AA}$-) and digital ($V_{DD}$, $V_{SS}$) supply pins, allows true bipolar or negative input operation. The $V_{AA}$- pin may be returned to a negative supply (observing maximum voltage ratings to $V_{AA}$+ or $V_{DD}$ and recommended rating to $V_{SS}$), thus allowing the $V_{REF}$- potential also to be negative. Figure 12B shows operation with an input range of -1V to +1V. Similarly, $V_{AA}$+ and $V_{REF}$+ could be maintained at a higher voltage than $V_{DD}$, for an input range above the digital supply.

**Digital Input And Output Levels**

The clock input is a CMOS inverter operating from and with logic input levels determined by the $V_{AA}$ supplies. If $V_{AA}$+ or $V_{AA}$- are outside the range of the digital supplies, it may be necessary to level shift the clock input to meet the required 30% to 70% of $V_{AA}$ input swing. Figure 12B shows an example for a negative $V_{AA}$-.

An alternate way of driving the clock is to capacitively couple the pin from a source of at least $1V_{P-P}$. An internal 50kΩ feedback resistor will keep the DC level at the intrinsic trip point. Extremely non-symmetrical clock waveforms should be avoided, however.

The remaining digital inputs and outputs are referenced to $V_{DD}$ and $V_{SS}$. If TTL or other lower voltage sources are to drive the CA3304, either pull-up resistors or CD74HCT series “QMOS” buffers are recommended.

**5-Bit Resolution**

To obtain 5-bit resolution, two CA3304s can be wired together. Necessary ingredients include an open-ended ladder network, an overflow indicator, three-state outputs, and chip-enable controls - all of which are available on the CA3304.

The first step for connecting a 5-bit circuit is to totem-pole the ladder networks, as illustrated in Figure 13. Since the absolute-resistance value of each ladder may vary, external trim of the mid-reference voltage may be required.

The overflow output of the lower device now becomes the fifth bit. When it goes high, all counts must come from the upper device. When it goes low, all counts must come from the lower device. This is done simply by connecting the lower overflow signal to the $\overline{CE1}$ control of the lower A/D converter and the CE2 control of the upper A/D converter. The three-state outputs of the two devices (bits 1 through 4) are now connected in parallel to complete the circuitry.

## *Definitions*

**Dynamic Performance Definitions**

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the CA3304. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from full scale for all these tests.

**Signal-to-Noise (SNR)**

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

**Signal-to-Noise + Distortion Ratio (SINAD)**

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

**Effective Number of Bits (ENOB)**

The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

$$ENOB = (SINAD - 1.76 + V_{CORR})/6.02,$$

where: $V_{CORR} = 0.5dB$.

**Total Harmonic Distortion (THD)**

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the measured input signal.

## *Operating and Handling Considerations*

**HANDLING**

All inputs and outputs of CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in lCAN-6525. “Guide to Better Handling and Operation of CMOS Integrated Circuits.”

**OPERATING**

**Operating Voltage**

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause the power supply voltages to exceed the absolute maximum rating.

**Input Signals**

To prevent damage to the input protection circuit, input signals should never be greater than $V_{DD}$ or $V_{AA}+$ nor less than $V_{SS}$ or $V_{AA}-$ (depending upon which supply the protection network is referenced. See Maximum Ratings.). Input currents must not exceed 20mA even when the power supply is off.

**Unused Inputs**

A connection must be provided at every input terminal. All unused input terminals must be connected to either $V_{DD}$ or $V_{SS}$, whichever is appropriate.

**Output Short Circuits**

Shorting of outputs to any supply potential may damage CMOS devices by exceeding the maximum device dissipation.

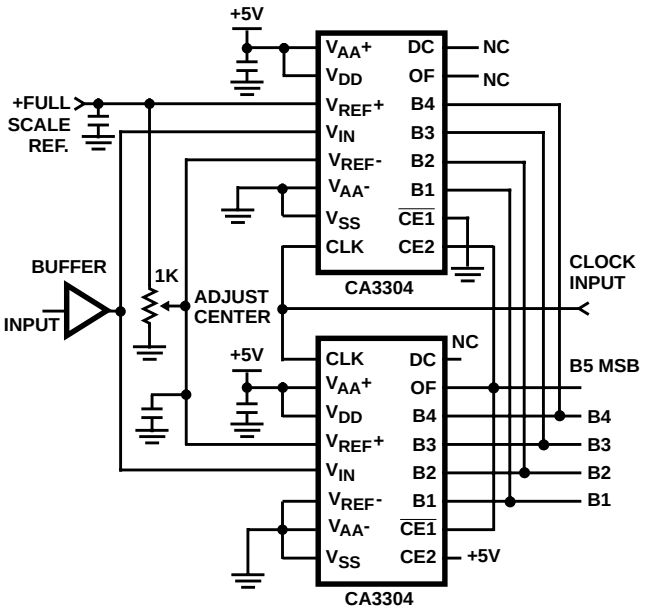



**FIGURE 13. TYPICAL CA3304 5-BIT CONFIGURATION**

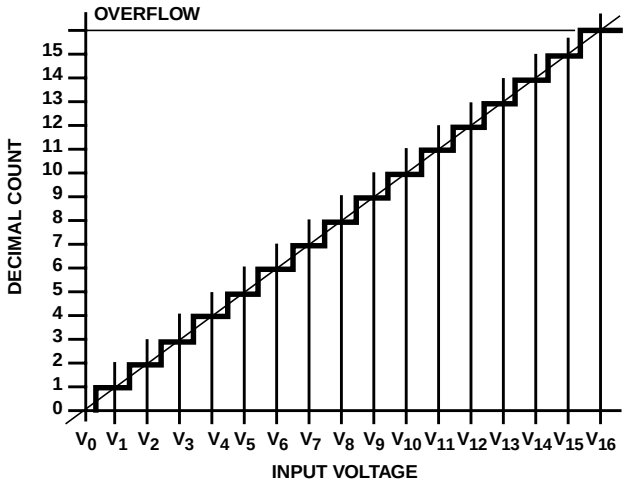



**FIGURE 14. IDEAL TRANSFER CURVE**

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