June 1999

National Semiconductor

CLC449
1.1GHz Ultra-Wideband Monolithic Op Amp

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General Description

The CLC449 is an ultra-high-speed monolithic op amp, with a typical -3dB bandwidth of 1.1GHz at a gain of +2. This wideband op amp supports rise and fall times less than 1ns, settling time of 6ns (to 0.2%) and slew rate of 2500V/µs. The CLC449 achieves 2nd harmonic distortion of -68dBc at 5MHz at a low supply current of only 12mA. These performance advantages have been achieved through improvements in National's proven current feedback topology combined with a high-speed complementary bipolar process.

The DC to 1.2GHz bandwidth of the CLC449 is suitable for many IF and RF applications as a versatile op amp building block for replacement of AC coupled discrete designs. Operational amplifier functions such as active filters, gain blocks, differentiation, addition, subtraction and other signal conditioning functions take full advantage of the CLC449's unity-gain stable closed-loop performance.

The CLC449 performance provides greater headroom for lower frequency applications such as component video, high-resolution workstation graphics, and LCD displays. The amplifier's 0.1dB gain flatness to beyond 200MHz, plus 0.8ns 2V rise and fall times are ideal for improved time domain performance. In addition, the 0.03%/0.02° differential gain/phase performance allows system flexibility for handling standard NTSC and PAL signals.

In applications using high-speed flash A/D and D/A converters, the CLC449 provides the necessary wide bandwidth (1.1GHz), settling (6ns to 0.2%) and low distortion into 50Ω loads to improve SFDR.

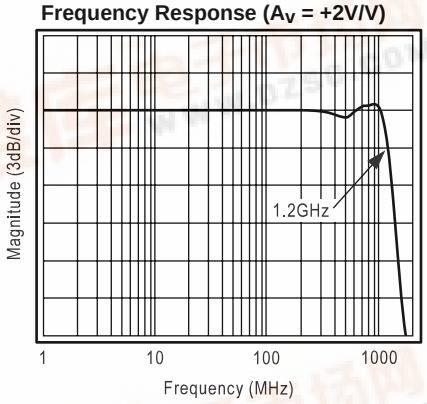
Features

- 1.1GHz small-signal bandwidth (A_V = +2)
- 2500V/µs slew rate
- 0.03%, 0.02° D_G, D_Φ
- 6ns settling time to 0.2%
- 3rd order intercept, 30dBm @ 70MHz
- Dual ±5V or single 10V supply
- High output current: 90mA
- 2.5dB noise figure

Applications

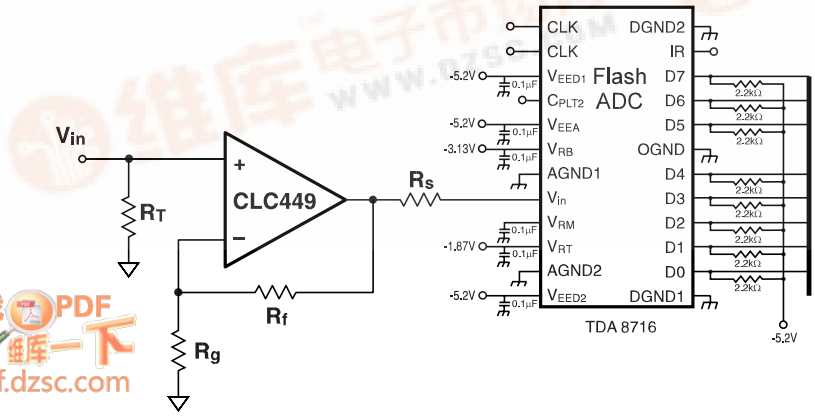
- High performance RGB video
- RF/IF amplifier
- Instrumentation
- Medical electronics
- Active filters
- High-speed A/D driver
- High-speed D/A buffer

Frequency Response (A_V = +2V/V)



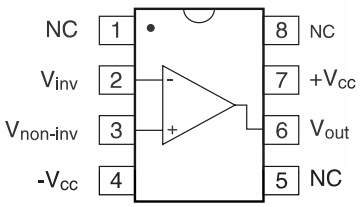
Typical Application

120MSPS High-Speed Flash ADC Driver



Pinout

DIP & SOIC



CLC449 Electrical Characteristics (A_v = +2, R_f = 250Ω, V_{cc} = ±5V, R_L = 100Ω; unless specified)

PARAMETERS	CONDITIONS	TYP	MIN/MAX RATINGS			UNITS	NOTES
	CLC449	+25°	+25°	0° to +70°	-40° to +85°		
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth							
small signal	<0.2V_{pp}	1100				MHz	
large signal	<2V_{pp}	500	380	380	360	MHz	
±0.1 dB bandwidth	<2V_{pp}	200				MHz	
gain flatness							
peaking	DC to 200MHz	0				dB	
rolloff	DC to 200MHz	0.1	0.5	0.5	0.5	dB	
linear phase deviation	<200MHz	0.8				deg	
differential gain	4.43MHz, R_L=150Ω	0.03	0.05	0.05	0.05	%	
differential phase	4.43MHz, R_L=150Ω	0.02	0.02	0.05	0.05	deg	
TIME DOMAIN RESPONSE							
rise and fall time	2V step	0.8	1.1	1.1	1.1	ns	
settling time to 0.2%	2V step	6				ns	
settling time to 0.1%	2V step	11				ns	
overshoot	2V step	10	18	18	18	%	
slew rate	4V step	2500	2000	2000	2000	V/µs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 5MHz	-63	59	59	59	dBc	
	2V_{pp}, 20MHz	-52	-48	-48	-48	dBc	
	2V_{pp}, 50MHz	-44	40	40	40	dBc	
3rd harmonic distortion	2V_{pp}, 5MHz	-84	77	75	75	dBc	
	2V_{pp}, 20MHz	-73	-66	-64	-64	dBc	
	2V_{pp}, 50MHz	-62	55	53	53	dBc	
3rd order intercept	70MHz	30				dBm	
1dB gain compression @ 50MHz		16				dBm	
equivalent input noise							
non-inverting voltage	1MHz	2.2	2.9			nV/√Hz	
inverting current	1MHz	15	20.0			pA/√Hz	
non-inverting current	1MHz	3	5.0			pA/√Hz	
STATIC DC PERFORMANCE							
input offset voltage		3	7	9	9	mV	A
average drift		25				µV/°C	
input bias current	non-inverting	6	30	45	60	µA	A
average drift		50				nA/°C	
input bias current	inverting	2	20	25	40	µA	A
average drift		25				nA/°C	
power supply rejection ratio	DC	48	43	41	41	dB	A
common-mode rejection ratio	DC	47	44	45	46	dB	
supply current	R_L= ∞	12	13.5	14	14	mA	A
MISCELLANEOUS PERFORMANCE							
input resistance	non-inverting	400	200	200	150	kΩ	
input capacitance	non-inverting	1.3				pF	
output resistance	closed loop	0.1	0.15	0.15	0.25	Ω	
output voltage range	R_L= ∞	3.3	3.1	3.1	3.1	V	
	R_L=100Ω	2.9	2.8	2.8	2.8	V	
input voltage range	common-mode	2.4	2.2	2.1	1.9	V	
output current		80	60	50	40	mA	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

V_{oc}	±6V
I_{out} is short circuit protected to ground	
common-mode input voltage	±V_{cc}
maximum junction temperature	+150°C
operating temperature range	
AJ	-40°C to +85°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C
ESD (human body model)	500V

Notes

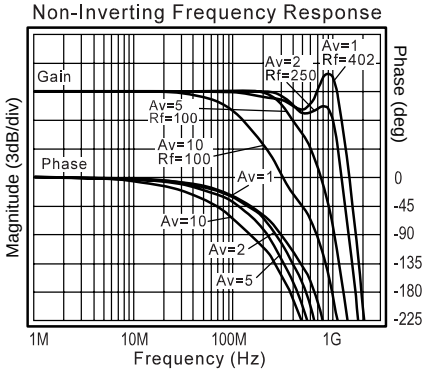
A) J-level: spec is 100% tested at +25°C.

Package Thermal Resistance

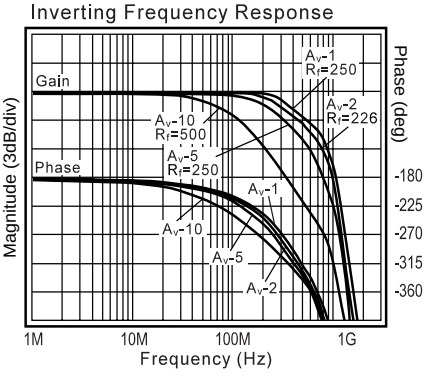
Package	θ_{JC}	θ_{JA}
Plastic (AJP)	90°C/W	105°C/W
Surface Mount (AJE)	110°C/W	130°C/W

CLC449 Typical Performance Characteristics (T_A = 25°C, V_{cc} = ± 5V, R_f = 250Ω, A_v = +2, R_L = 100Ω)

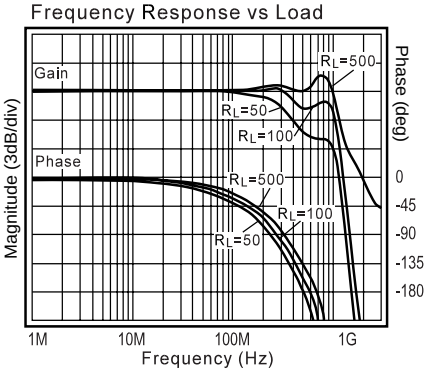
Non-Inverting Frequency Response



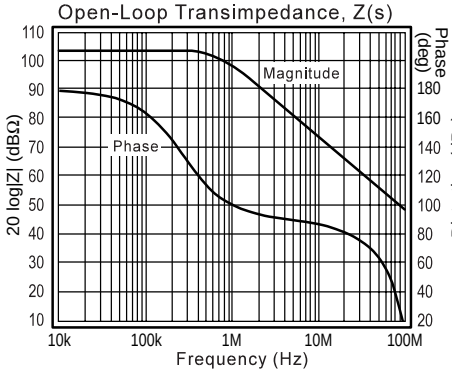
Inverting Frequency Response



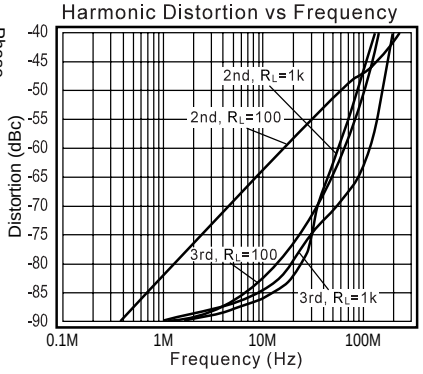
Frequency Response vs Load



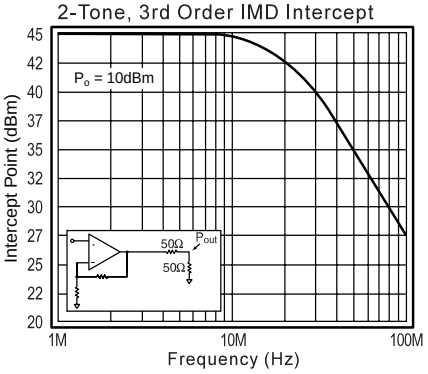
Open-Loop Transimpedance, Z(s)



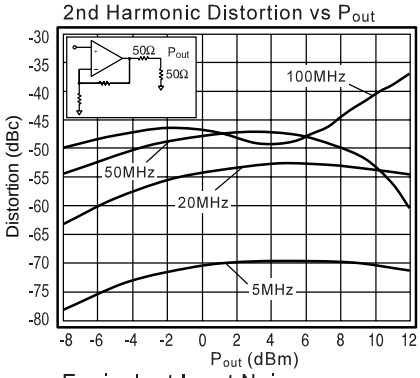
Harmonic Distortion vs Frequency



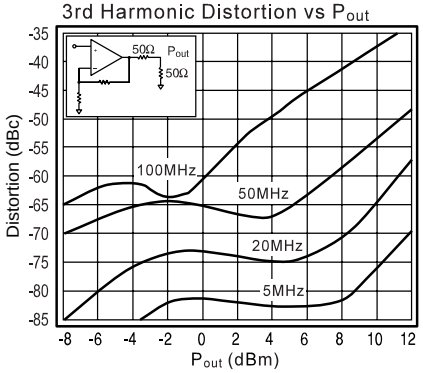
2-Tone, 3rd Order IMD Intercept



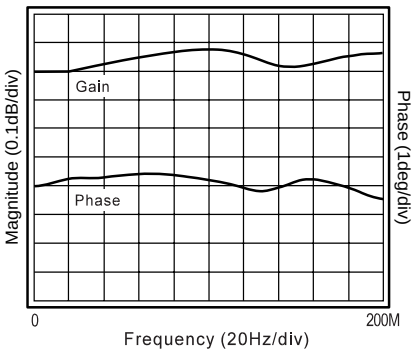
2nd Harmonic Distortion vs P_{out}



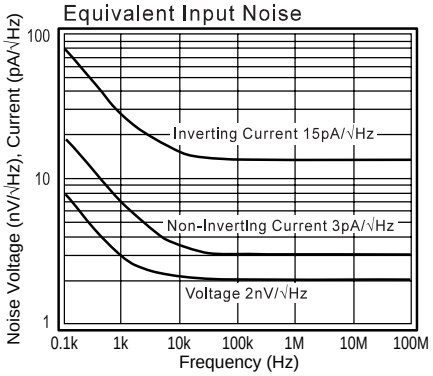
3rd Harmonic Distortion vs P_{out}



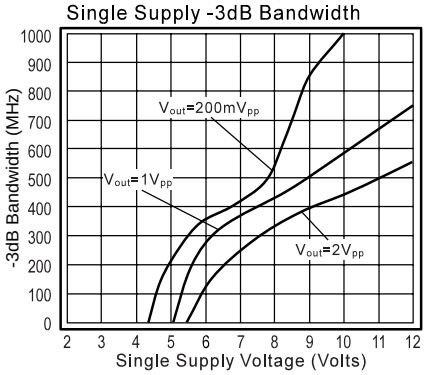
Gain Flatness and Linear Phase



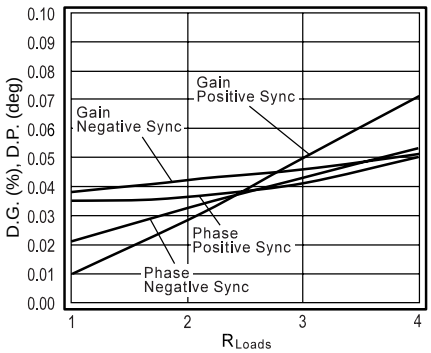
Equivalent Input Noise



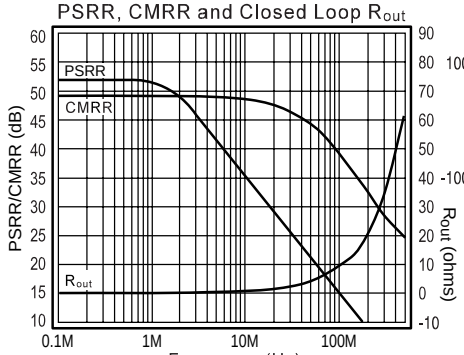
Single Supply -3dB Bandwidth



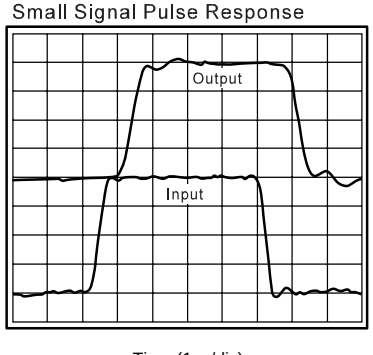
Differential Gain and Phase



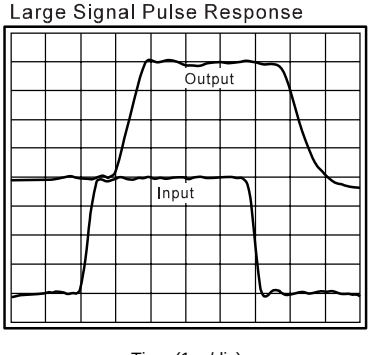
PSRR, CMRR and Closed Loop R_{out}



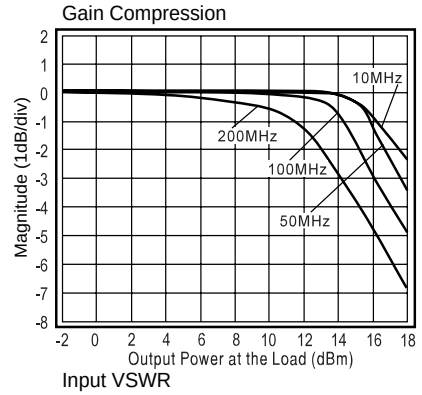
Small Signal Pulse Response

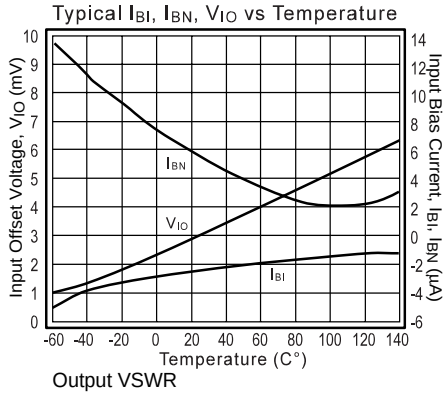


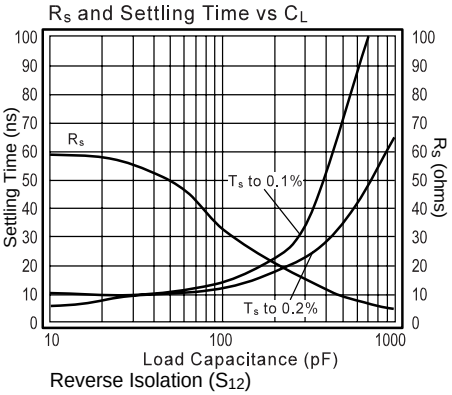
Large Signal Pulse Response

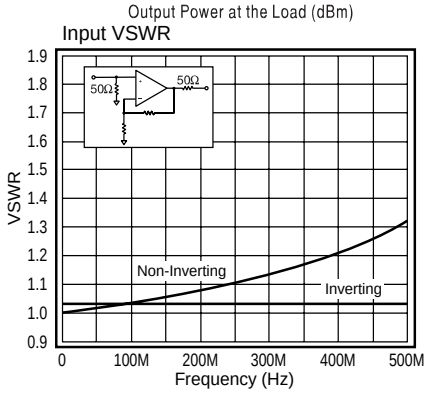


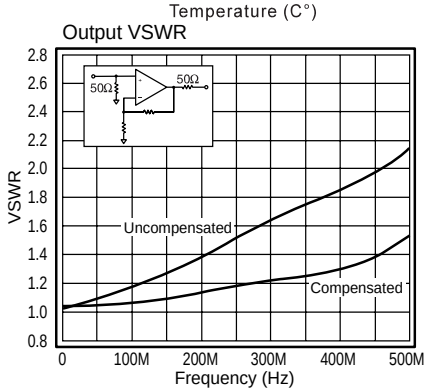
CLC449 Typical Performance Characteristics (T_A = 25°C, V_{cc} = ± 5V, R_f = 250Ω, A_v = +2, R_L = 100Ω)

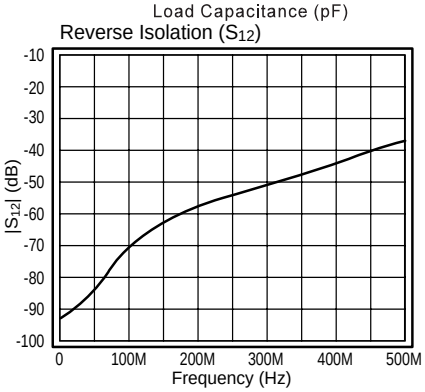












CLC449 OPERATION

CLC449 Extended Application Information

The following design and application topics will supply you with:

- A comprehensive set of design parameters and design parameter adjustment techniques.
- A set of formulas that support design parameter change prediction.
- A series of common applications that the CLC449 supports.
- A set of easy to use design guidelines for the CLC449.

Additional design applications are possible with the CLC449. If you have application questions, call 1-800-272-9959 in the U.S. to contact a technical staff member.

DC Gain (Non-Inverting)

The non-inverting DC voltage gain for the configuration shown in Figure 1 is:

$$A_V = 1 + \frac{R_f}{R_g}$$

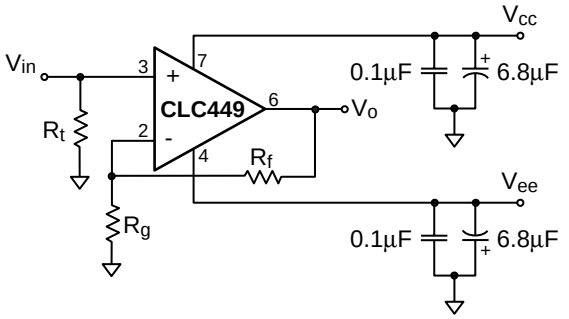


Figure 1: Non-Inverting Gain

The normalized gain plots in the ***Typical Performance Characteristics*** section show different feedback resistors, R_f, for different gains. These values of R_f are recommended for obtaining the highest bandwidth with minimal peaking. The resistor R_t in Figure 1 provides DC bias for the non-inverting input.

For $A_v \leq 5$, calculate the recommended R_f as follows: $R_f \cong 340 - A_v \cdot R_i$, where $R_i = 45\Omega$. For $A_v > 5$, the minimum recommended feedback resistor is $R_f = 100\Omega$.

Select R_g to set the DC gain: $R_g = \frac{R_f}{A_v - 1}$

Accuracy of DC gain is usually limited by the tolerance of the external resistors R_f and R_g.

DC Gain (Unity Gain Buffer)

Unity gain buffers are easily designed with a current-feedback amplifier as long as the recommended feedback resistor $R_f = 402\Omega$ is used and $R_g = \infty$, i.e. open. Parasitic capacitance at the inverting node may require a slight increase of the feedback resistor R_f to maintain a flat frequency response.

DC Gain (Inverting)

The inverting DC voltage gain for the configuration shown in Figure 2 is:

$$A_v = -\frac{R_f}{R_g}$$

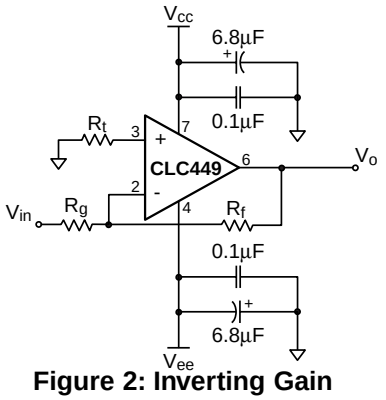


Figure 2: Inverting Gain

The normalized gain plots in the ***Typical Performance Characteristics*** section show different feedback resistors, R_f, for different gains. These values of R_f are recommended for obtaining the highest bandwidth with minimal peaking. The resistor R_t in Figure 2 provides DC bias for the non-inverting input.

For $|Av| \leq 4$, calculate the recommended R_f as follows: $Rf \cong 295 - |A_v| \cdot R_i$, where $R_i = 45\Omega$. For $|A_v| > 4$, the minimum recommended feedback resistor is $R_f = 100\ \Omega$.

Select R_g to set the DC gain:

$$R_g = \frac{R_f}{|A_v|}$$

At large gains, R_g becomes small and will load the previous stage. This situation is resolved by driving R_g with a low impedance buffer like the CLC111, or increasing R_f and R_g (see the ***Bandwidth (Small Signal)*** sub-section for the tradeoffs).

Accurate DC gain is usually limited by the tolerance of the external resistors R_f and R_g.

Bandwidth (Small Signal)

The CLC449 current-feedback amplifier bandwidth is a function of the feedback resistor (R_f), not of the DC voltage gain (A_v). The bandwidth is approximately proportional to $1/R_f$. As a rule, if R_f doubles, the bandwidth is cut in half. Other AC specifications will also be degraded. ***Decreasing R_f from the recommended value increases peaking and for very small values of R_f oscillation will occur.***

With an inverting amplifier design, peaking is sometimes observed. This is often the result of layout parasitics caused by inadequate ground planes or long traces. If this is observed, placing a 50 to 200Ω resistor between the non-inverting pin and ground will usually reduce the peaking.

Bandwidth (Minimum Slew Rate)

Slew rate influences the bandwidth for large signal sinusoids. To determine an approximate value of slew rate, necessary to support large sinusoids use the following equation:

$$SR \cong 5 \cdot f \cdot V_{peak}$$

V_{peak} is the peak output sinusoidal voltage, f is the frequency of the sinusoid.

The slew rate of the CLC449 in inverting gains is always higher than in non-inverting gains.

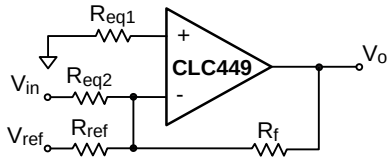
DC Design (Level Shifting)

Figure 3 shows a DC level shifting circuit for inverting gain configurations. V_{ref} produces a DC output level shift of

$$-V_{ref} \cdot \frac{R_f}{R_{ref}}$$

which is independent of the DC output produced by V_{in}.

Figure 3: Level Shifting Circuit



DC Design (Single Supply)

Figure 4 is a typical single-supply circuit. Resistors R_1 and R_2 form a voltage divider that sets the non-inverting input DC voltage. This circuit has a DC gain of 1. The coupling capacitor C_1 isolates the DC bias point from the previous stage. Both capacitors make a high pass response; the high frequency gain is determined by R_f and R_g.

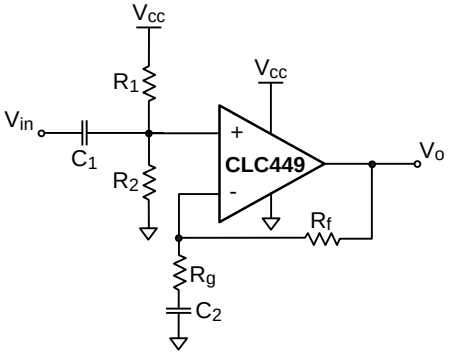


Figure 4: Single Supply Circuit

The complete gain equation for the circuit in Figure 4 is:

$$\frac{V_o}{V_{in}} = \frac{s\tau_1}{1+s\tau_1} \cdot \frac{1+s\tau_2 \cdot \left(1+\frac{R_f}{R_g}\right)}{1+s\tau_2}$$

where $s = j\omega$, $\tau_1 = (R_1 || R_2) \cdot C_1$, and $\tau_2 = R_g C_2$.

DC Design (DC Offsets)

The DC offset model shown in Figure 5 is used to calculate the output offset voltage. The equation for output offset voltage is:

$$V_o = -\left(V_{os} + I_{BN} \cdot R_{eq1}\right) \cdot \left(1+\frac{R_f}{R_{eq2}}\right) + \left(I_{BI} \cdot R_f\right)$$

The current offset terms, I_{BN} and I_{BI}, ***do not track each other***. The specifications are stated in terms of magnitude only. Therefore, the terms V_{os}, I_{BN}, and I_{BI} may have either positive or negative polarity. Matching the equivalent resistance seen at both input pins does not reduce the output offset voltage.

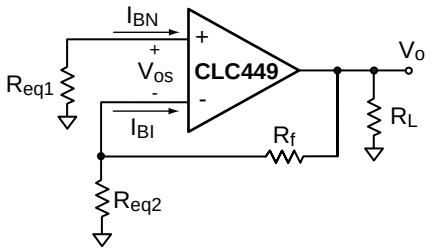


Figure 5: DC Offset Model

DC Design (Output Loading)
R_L, R_f, and R_g load the op amp output. The equivalent closed-loop load impedance seen by the output in Figure 5 is:

- $R_{L\_eq} = R_L \parallel (R_f + R_{eq2})$, non-inverting gain
- $R_{L\_eq} = R_L \parallel R_f$, inverting gain

R_{L_eq} needs to be kept large enough so that the minimum available output current can produce the required output voltage swing.

Capacitive Loads
Capacitive loads, such as found in A/D converters, require a series resistor (R_s) in the output to improve settling performance. The ***R_s and Settling Time vs. C_L*** plot in the ***Typical Performance Characteristics*** section provides the information for selecting this resistor.

Also, use a series resistor to reduce the effects of reactive loads on amplifier loop dynamics. For instance, driving coaxial cables without an output series resistor may cause peaking or oscillation.

Transmission Line Matching
One method for matching the characteristic impedance of a transmission line is to place the appropriate resistor at the input or output of the amplifier. Figure 6 shows the typical circuit configurations for matching transmission lines.

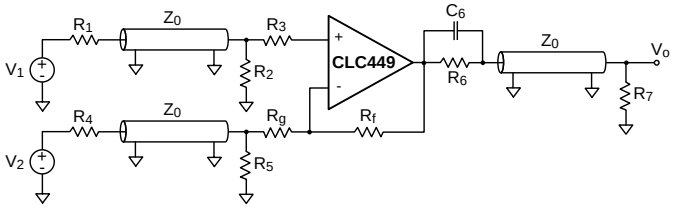


Figure 6: Transmission Line Matching

In non-inverting gain applications, R_g is connected directly to ground. The resistors R_1, R_2, R_6, and R_7 are equal to the characteristic impedance, Z_o, of the transmission line or cable.

In inverting gain applications, R_3 is connected directly to ground. The resistors R_4, R_6, and R_7 are equal to Z_o. The parallel combination of R_5 and R_g is also equal to Z_o.

The input and output matching resistors attenuate the signal by a factor of 2, therefore additional gain is needed. Matching the output transmission line over greater frequency ranges is accomplished by placing C_6 in parallel with R_6, reducing the output impedance to compensate for the internal increase of the op-amp's output impedance with frequency.

Thermal Design
To calculate the power dissipation for the CLC449, follow these steps:

- Calculate the no-load op amp power:
  $P_{amp} = I_{cc} \cdot (V_{cc} - V_{ee})$
- Calculate the output stage's RMS power:
  $P_o = (V_{cc} - V_{load}) \cdot I_{load}$
  where V_{load} and I_{load} are the RMS voltage and current across the external load.
- Calculate the total op amp RMS power:
  $P_t = P_{amp} + P_o$

To calculate the maximum allowable ambient temperature, solve the following equation: $T_{amb} = 175 - P_t \cdot \theta_{JA}$, where θ_{JA} is the thermal resistance from junction to ambient in °C/W and T_{amb} is in °C. Thermal resistance for the various packages are found in the ***Package Thermal Resistance*** section.

Dynamic Range (Input /Output Protection)
Input ESD diodes are present on all connected pins for protection from static voltage damage. For a signal that may exceed the supply voltages, we recommend using diode clamps at the amplifier's input to limit the signals to less than the supply voltages.

Dynamic Range (Input /Output Levels)
The ***Electrical Characteristics*** section contains the Common-Mode Input Range and Output Voltage Range; these voltage ranges scale with the supplies. Output Current is also specified in the ***Electrical Characteristics*** section.

Unity gain applications are limited by the Common-Mode Input Range. At greater non-inverting gains, the Output Voltage Range becomes the limiting factor. Inverting gain applications are limited by the Output Voltage Range.

For transimpedance or inverting gain applications, the current (I_{inv}) injected at the inverting input pin of the op amp needs to be:

$$|I_{inv}| \leq \frac{V_{max}}{R_f}$$

where V_{max} is the Output Voltage Range.

The voltage ranges discussed above are achieved as long as the equivalent output load is large enough so that the output current can produce the required output voltage swing. See the ***DC Design (Output Loading)*** sub-section for details.

Dynamic Range (Intermods)
For RF applications, the CLC449 specifies a third order intercept of 30dBm at 70MHz and P_o = 10dBm.

A ***2-Tone, 3rd Order IMD Intercept*** plot is found in the ***Typical Performance Characteristics*** section. The output power level is taken at the load. Third-order harmonic distortion is calculated with the formula:

$$HD3^{rd} = 2 \cdot (IP3_o - P_o)$$

where:

- $IP3_o$ = third-order output intercept, dBm at the load.
- P_o = output power level, dBm at the load.
- $HD3^{rd}$ = third-order distortion from the fundamental, -dBc.
- dBm is the power in mW, at the load, expressed in dB.

Realized third-order output distortion is highly dependent upon the external circuit. Some of the common external circuit choices that improve 3rd order distortion are:

- short and equal return paths from the load to the supplies.
- de-coupling capacitors of the correct value.
- higher load resistance.
- a lower ratio of the output swing to the power supply voltage.

Dynamic Range (Noise)

In RF applications, noise is frequently specified as Noise Figure (NF). Figure 7 plots NF for the CLC449 at a gain of 10, with a feedback resistor R_f of 100Ω, and with no input matching resistor. The minimum Noise Figure (2.5dB) for these conditions occurs when the source resistance equals 700Ω.

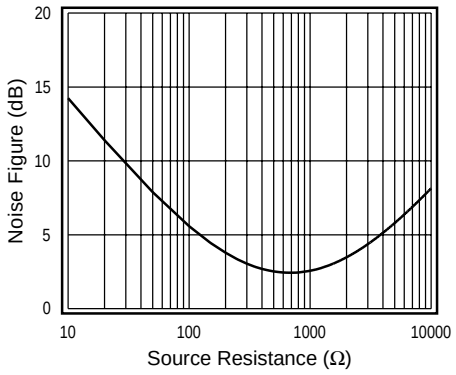


Figure 7. Noise Figure Plot

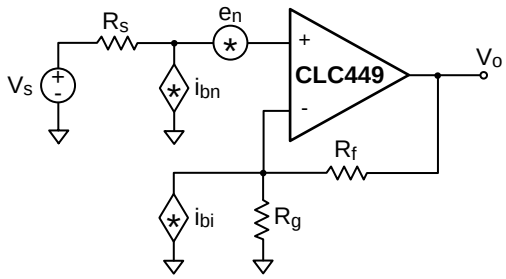


Figure 8: CLC449 Noise Model

The CLC449 noise model in Figure 8 is used to develop the equation below.

The equation for Noise Figure (NF) is:

$$NF = 10LOG\left(\frac{e_{ni^2} + \left(i_{bn}R_s\right)^2 + 4kTR_s + \left(i_{bi} \cdot R_f \,||\, R_g\right)^2 + 4kT \cdot R_f \,||\, R_g}{4kTR_s}\right)$$

where:

- R_s is the source resistance at the non-inverting input.
- There is no matching resistor from the input to ground.
- e_{ni}, i_{bn}, i_{bi} are the voltage and current noise density terms (see in the ***Distortion and Noise Response*** sub-section of the ***Electrical Characteristics*** section).
- $4kT = 16 \times 10^{-21}$J, T = 290°K.
- R_f is the feedback resistor and R_g is the gain setting resistor.

Printed Circuit Board Layout and Measurement

High Frequency op amp performance is strongly dependent on proper layout, proper resistive termination and adequate power supply decoupling. The most important layout points to follow are:

- Use a ground plane.
- Bypass power supply pins with monolithic capacitors of about 0.1µF value and place the capacitors less than 0.1" (3mm) from the pin.
- Bypass power supply pins with 6.8µF tantalum capacitors for large signal current swings or improved power supply noise rejection.
- Minimize trace and lead lengths for components between the inverting and output pins.
- Remove ground plane underneath the amplifier package and within 0.1" (3mm) of all input/output pads.
- If parts must be socketed, always use flush-mount socket pins instead of high profile sockets.

Evaluation boards are available for proto-typing and measurements. Additional layout information is available in the evaluation board literature.

CLC449 APPLICATIONS

Low Noise Composite Amp With Input Matching

The composite circuit shown in Figure 9 eliminates the need for a matching resistor to ground at the input. By connecting two amplifiers in series, the first non-inverting and the second inverting, an overall inverting gain is realized. The feedback resistor (R_f) connected from the output of the second amplifier to the non-inverting input of the first amplifier closes the loop, and generates a set input resistance (R_{in}) that can be matched to R_S. This resistor generates less noise than a matching resistor to ground at the input.

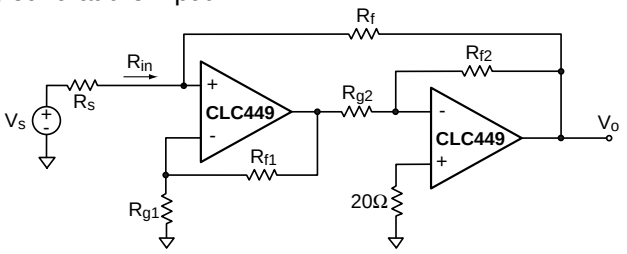


Figure 9: Composite Amplifier

Input resistance and DC voltage gain of the amplifier are:

$$R_{in} = \frac{R_f}{1+G}, \text{ where } G = \left(1+\frac{R_{f1}}{R_{g1}}\right)\cdot\left(\frac{R_{f2}}{R_{g2}}\right)$$

$$\frac{V_o}{V_s} = -G\cdot\left(\frac{R_{in}}{R_{in}+R_S}\right)$$

Match the source resistance by setting: $R_{in} = R_S$

Noise voltage produced by R_f, referred to the source V_S, is:

$$e^2_{R_f} = 4kTR_S\cdot\left(\frac{R_S}{R_{in}\cdot(1+G)}\right)$$

The noise of a simple input matching resistor connected to ground can be calculated by setting G to 0 in this equation. Thus, this circuit reduces the thermal noise produced by the matching resistor by a factor of (1+G).

Rectifier Circuit

Wide bandwidth rectifier circuits have many applications. Figure 10 shows a 200MHz wideband full-wave rectifier circuit using a CLC449 and CLC522 amplifier. Schottky or PIN diodes are used for D1 and D2. They produce an active half-wave rectifier whose signals are taken at the feedback diode connection. The CLC522 takes the difference of the two half-wave rectified signal, producing a full-wave rectifier. The CLC522 is used at a gain of 5 to achieve high differential bandwidth. For best high frequency performance, maintain low parasitic capacitance from the diodes D1 and D2 to ground, and from the input of the CLC522, to ground.

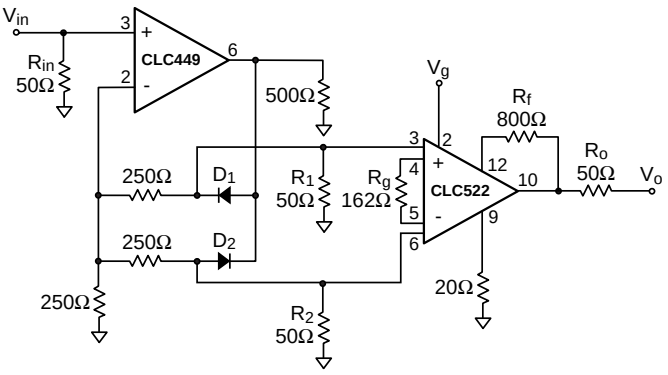


Figure 10: Full-Wave Rectifier

Flash A/D Application

The Typical Application circuit on the front page shows the CLC449 driving a flash A/D. Flash A/D's require fast settling, low distortion, low noise and wide bandwidth to achieve high Effective Number of Bits and Spurious Free Dynamic Range (SFDR).

This circuit connects a CLC449 to a TDA8716, 8-bit, 120MHz Flash Converter. The input capacitance for this converter is typically 13pF plus layout capacitance. From the ***R_S and Settling Time vs. C_L*** plot in the ***Typical Performance Characteristics*** section, select a series resistor (R_S) of 55Ω. Place R_S in series with the output of the CLC449 to achieve settling to 0.1% in approximately 11ns.

Keep the amplifier noise seen at the A/D input at least 3dB lower than the A/D's noise, to avoid degrading A/D noise performance.

Ordering Information

Model	Temperature Range	Description
CLC449AJP	-40°C to +85°C	8-pin PDIP
CLC449AJE	-40°C to +85°C	8-pin SOIC
CLC449AMC	-55°C to +125°C	dice, MIL-STD-883

Contact factory for other packages and DESC SMD number.

Reliability Information

Transistor count	26

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CLC449
1.1GHz Ultra-Wideband Monolithic Op Amp

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