SONY CXL1009P

CMOS-CCD Signal Processor for TBC

Description

CXL1009P is a CMOS-CCD signal processor developed for Time Base Corrector (TBC).

Features

- Low power consumption 160 mW (Typ.)
- Wide variable frequency range (15.2 to 27.2 MHz)
- Built-in peripheral circuits

Functions

- 680 bit CCD register x 2
- Clock drivers
- Autobias circuit (For Audio/Video)
- Sync tip clamp circuit
- T-type flip-flop circuit
- Timing generator circuit
- Output feedback circuit

Structure

CMOS-CCD

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}		11		V
• Supply voltage	V_{CL}		6		V
• Operating temperature	Topr	−10	to	+60	°C
• Storage temperature	Tstg	−55	to	+150	°C
• Allowable power dissipation	P_D		1		W

Recommended Operating Conditions

• Supply voltage	V_{DD}	9	V ±5%
• Supply voltage	V_{CL}	9	V ±5%

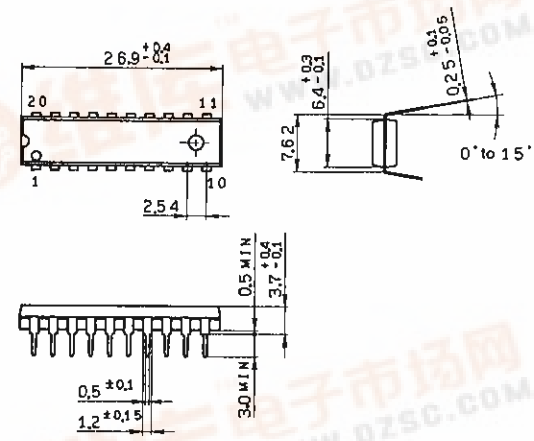
Recommended Input Signal Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Input amplitude	V_{INP-P}	--	1.0	1.28	Vp-p

Package Outline

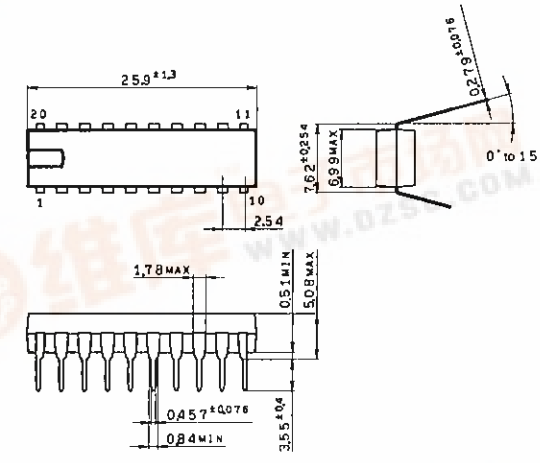
Unit: mm

20 pin DIP (Plastic)



DIP-20P-02

20 pin DIP (Plastic)



DIP-20P-121

Recommended Clock Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Clock frequency	f_{CK}	15.2	21.4	27.2	MHz	Pulse or Sinewave*
Clock amplitude	V_{CKP-P}	1.0	2.0	4.0	Vp-p	
Duty (during pulse)	Dy	40	50	60	%	

***Note)** During pulse the clock requires a pulse as shown in Fig. 1.

E88Z37-YA

Recommended Clock Waveform (Pulse)

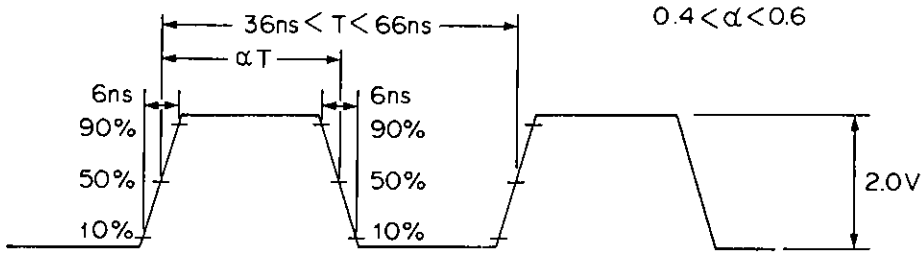
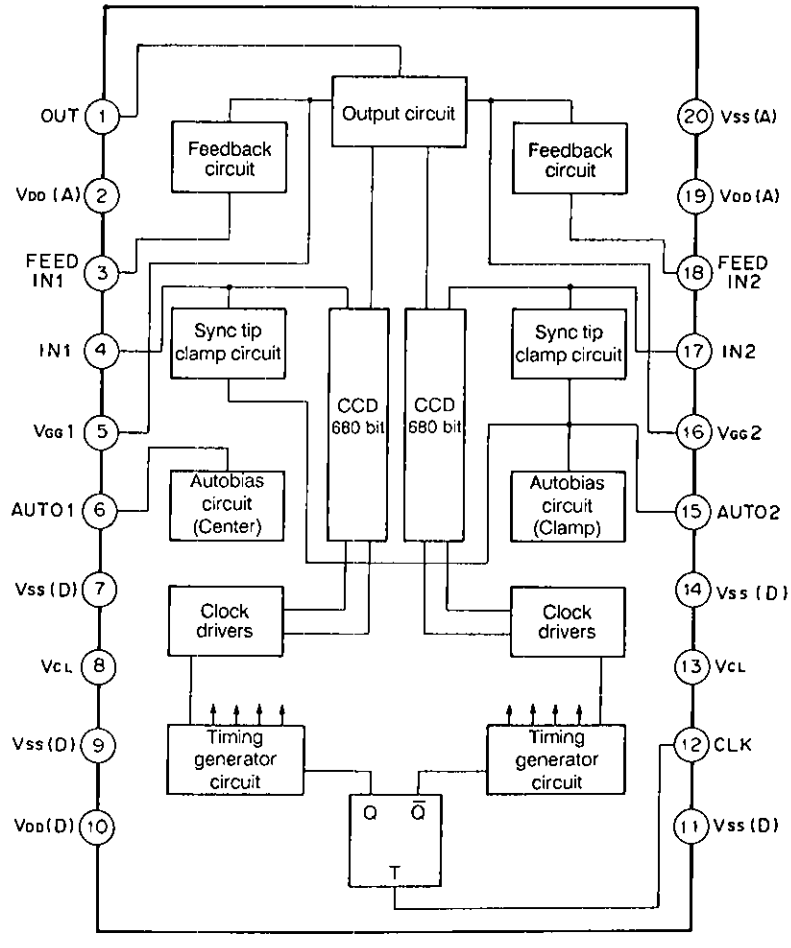


Fig. 1

Block Diagram and Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	OUT	O	Output
2	V_{DD} (A)		Power supply 1 (Analog)
3	FEED IN1	I	Feedback input 1
4	IN1	I	Input 1
5	V_{GG} 1	I	Gate1
6	AUTO1	O	Autobias 1
7	Vss (D)		GND (Digital)
8	V_{CL}		Power supply 2 (Digital)
9	Vss (D)		GND (Digital)
10	V_{DD} (D)		Power supply 1 (Digital)
11	Vss (D)		GND (Digital)
12	CLK	I	Clock input
13	V_{CL}		Power supply 2 (Digital)
14	Vss (D)		GND (Digital)
15	AUTO2	O	Autobias 2
16	V_{GG} 2	I	Gate 2
17	IN2	I	Input 2
18	FEED IN2	I	Feedback input 2
19	V_{DD} (A)		Power supply 1 (Analog)
20	Vss (A)		GND (Analog)

Electrical Characteristics 1

Ta = 25°C, V_{DD} = 9.0V, V_{CL} = 5.0V, See the Electrical Characteristics Test Circuit.

Item	Symbol	Test conditions	SW condition				Test point	Min.	Typ.	Max.	Unit
			SW1	SW2	SW3	SW4					
Pin voltage	$V_{AUTO1-DC}$	Pin 6 voltage	b	a	a	a	V6	4.0	5.5	7.0	V
	$V_{AUTO2-DC}$	Pin 15 voltage	b	a	a	a	V5	3.5	5.0	6.5	V
	V_{IN-DC}	Pins 4 and 17 voltage	b	b	a	a	V7	3.5	5.0	6.5	V
	V_{GG-DC}	Pins 5 and 16 voltage	a	a	a	a	V8	1.0	2.0	3.0	V
			b								
			c								

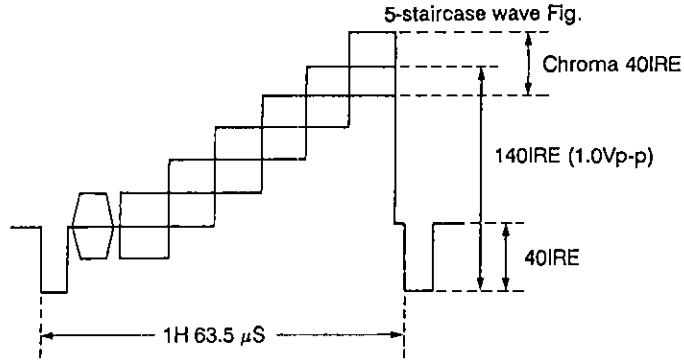
Electrical Characteristics 2

Ta = 25°C, V_{DD} = 9.0V, V_{CL} = 5.0V, See the Electrical Characteristics Test Circuit.
Test conditions: Set the voltage of pins E1 and E2 as follows:
E1 = V_{GG-DC}, E2 = $V_{AUTO2-DC}$ + 0.65V or $V_{AUTO1-DC}$

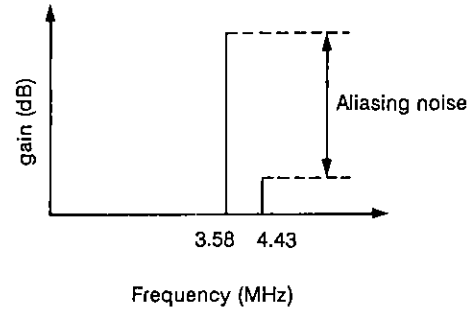
Item	Symbol	Test conditions	SW condition				Test point	Min.	Typ.	Max.	Unit
			SW1	SW2	SW3	SW4					
Supply current	I_{DD}	250 kHz, 1.0Vp-p sine wave input	b	a	a	a	A1	–	7	12	mA
	I_{CL}						A2	–	20	28	mA
Insertion gain	IG	250 kHz, 1.0Vp-p sine wave input $IG = 20\log\left[\frac{\text{Output voltage (Vp-p)}}{1\text{Vp-p}}\right]$	a to c	a	a	b	V2	–3	0	3	dB
Frequency response	f_G	Dissipation at 3.58 MHz vs. 250 kHz $f_G = 20\log(V_{3.58MHz}/V_{250kMz})$ $V_{3.58MHz}$: Output signal voltage during 3.58 MHz input V_{250kMz}: Output signal voltage during 250 kHz input	a to c	a	b	b	V2	–3	–1	0	dB
Differential gain	DG	5-staircase wave (See Fig.) input Y = 140IRE (= 1.0Vp-p) Measuring with vectorscope.*1	a to c	a	c	b	S	–	3	5	%
Differential phase	DP							–	3	5	Deg
Noise	S/N1	S: Input = 250 kHz, 1.0Vp-p sine wave	b	a	a	c	V3	50	55	–	dB
		N: Input = Alternating grounding point (rms)	b	a	d	c					
Aliasing noise	S/N2	Input = 3.58 MHz, 1.0Vp-p sine wave *2	d	a	b	d	SA	35	50	–	dB
Insertion gain difference	⊿IG	250 kHz, 1.0Vp-p sine wave *3	a to c	a	a	b	V2	–	1	2.4	%
DC output voltage difference	⊿V_{O-DC}	250 kHz, 1.0Vp-p sine wave *4	a to c	a	a	a	V1	–	–	0.3	V

Note)

*1. Differential gain and differential phase conditions.



*2. Aliasing noise
Measure with a spectrum analyzer the 4.43 MHz output signal voltage at 3.58 MHz input (clock frequency 16.02 MHz).



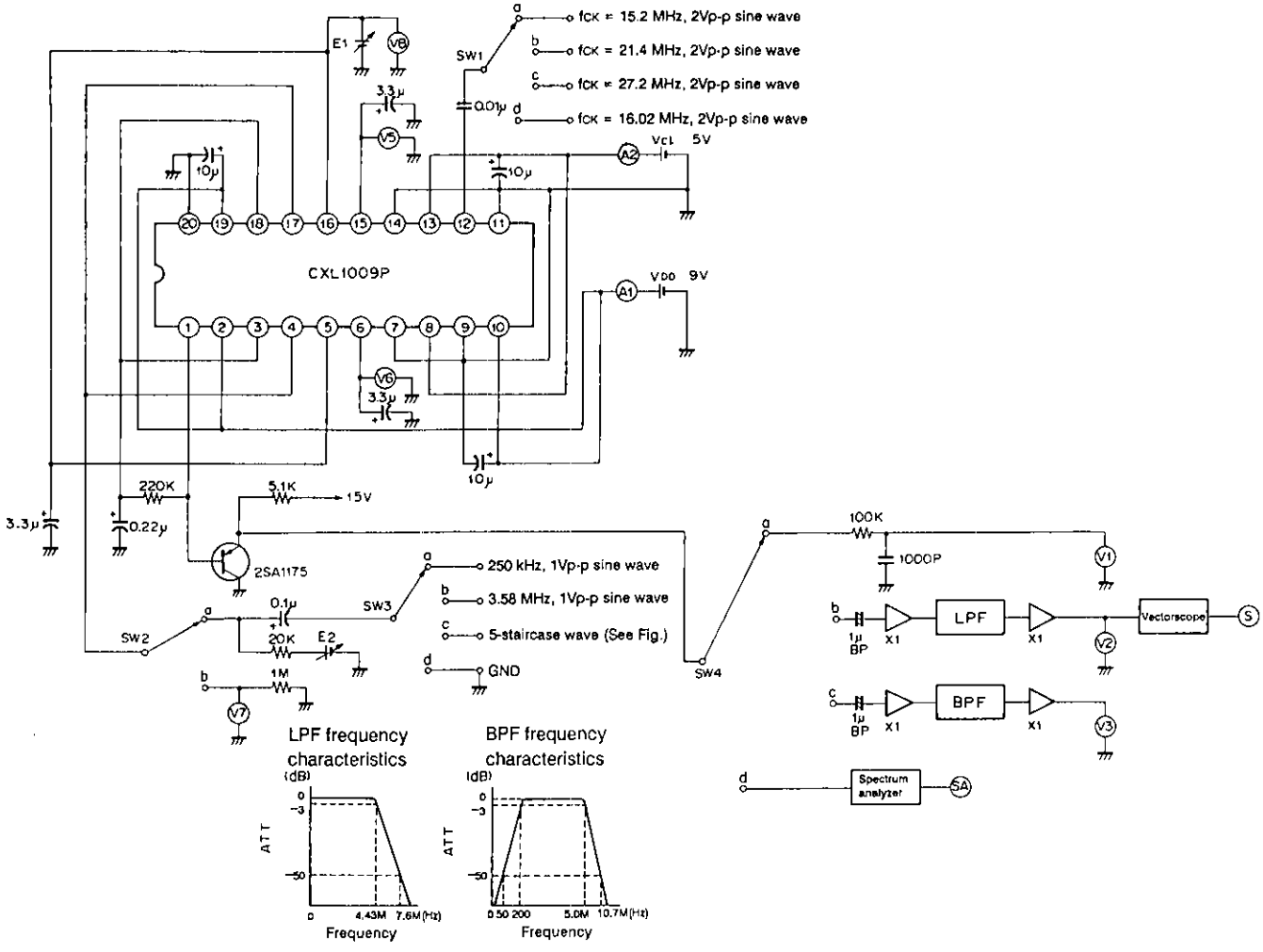
*3. Insertion gain difference
With the insertion gain of clock frequencies of 15.2 MHz, 21.4 MHz and 27.2 MHz, determine maximum value as IGmax [dB] and minimum value as IGmin [dB]. Insertion gain difference ⊿IG is defined as follows.

$$\Delta IG = \frac{10^{(IGmax/20)} - 10^{(IGmin/20)}}{10^{(IGmax/20)} + 10^{(IGmin/20)}} \times 200\ [\%]$$

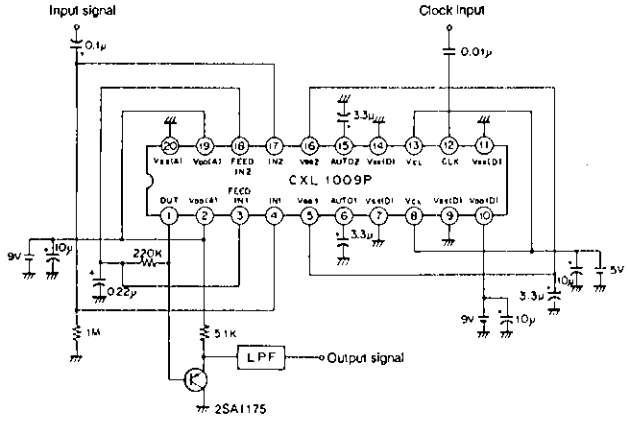
*4. DC output voltage difference
With the DC output voltage of clock frequencies of 15.2 MHz, 21.4MHz and 27.2 MHz, determine maximum value as $V_{O\text{-}DC}max$ and minimum value as $V_{O\text{-}DC}min$. DC output voltage difference $\Delta V_{O\text{-}DC}$ is defined as follows.

$$\Delta V_{O\text{-}DC} = V_{O\text{-}DC}\ max - V_{O\text{-}DC}\ min\ [V]$$

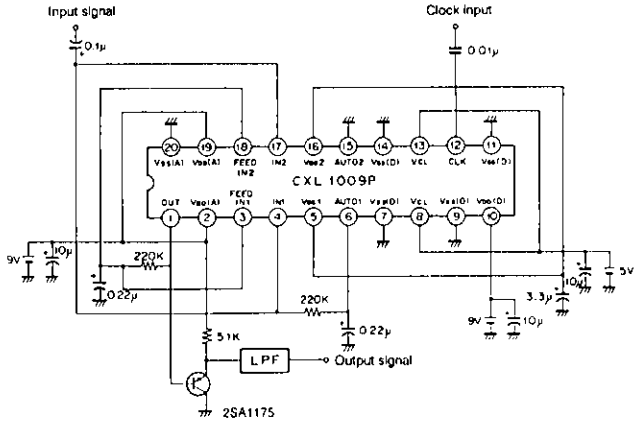
Electrical Characteristics Test Circuit



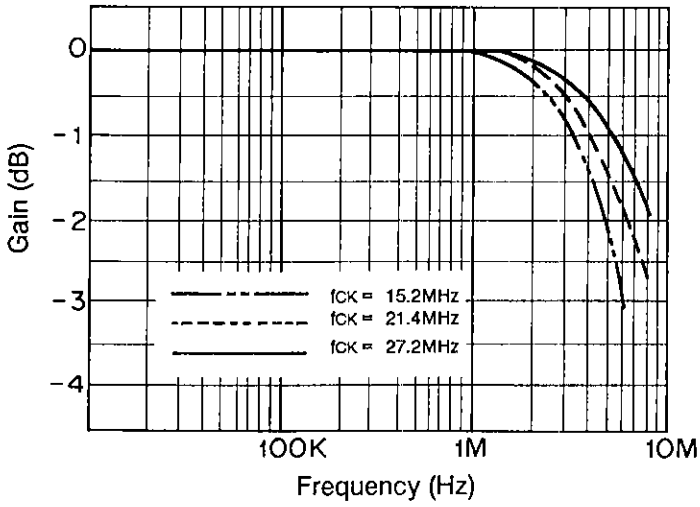
Application Circuit (Video)



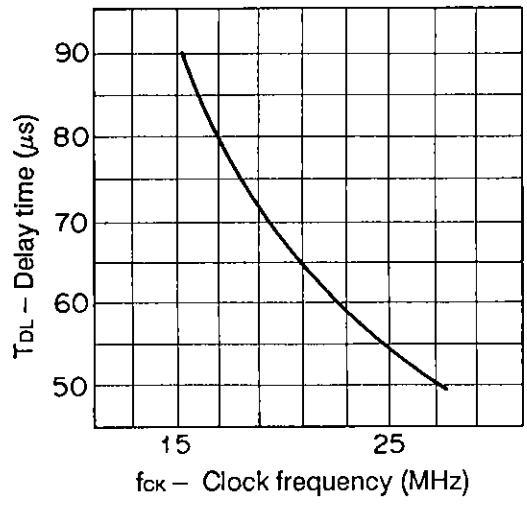
Application Circuit (Audio)



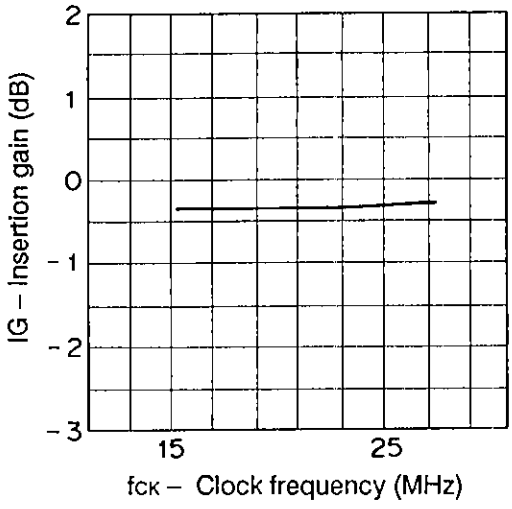
Frequency characteristics



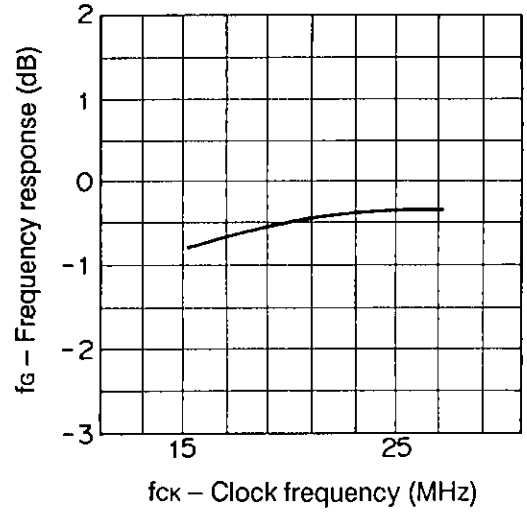
Delay time vs. Clock frequency



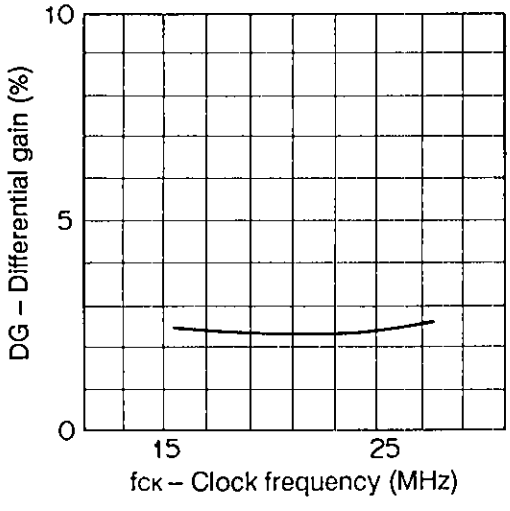
Insertion gain vs. Clock frequency



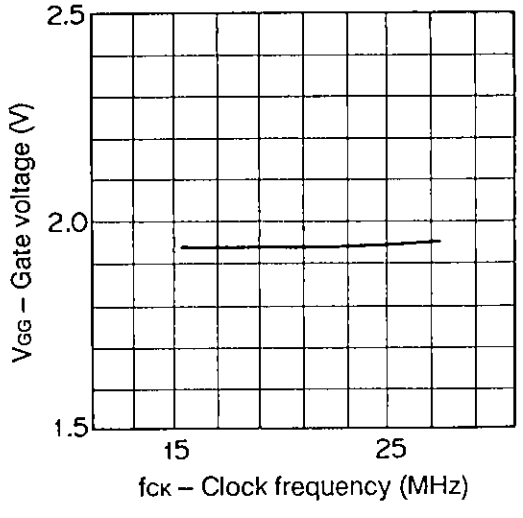
Frequency response vs. Clock frequency



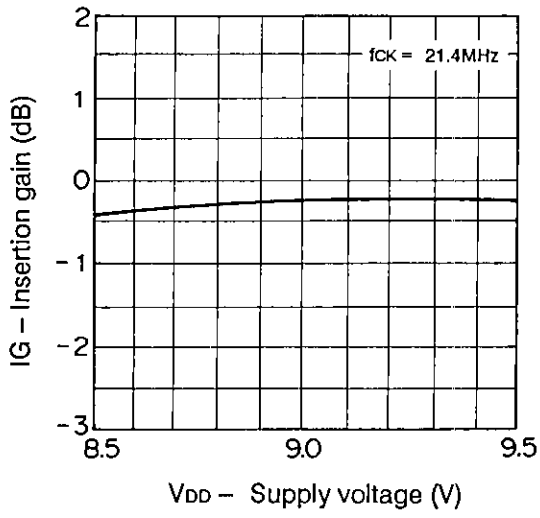
Differential gain vs. Clock frequency



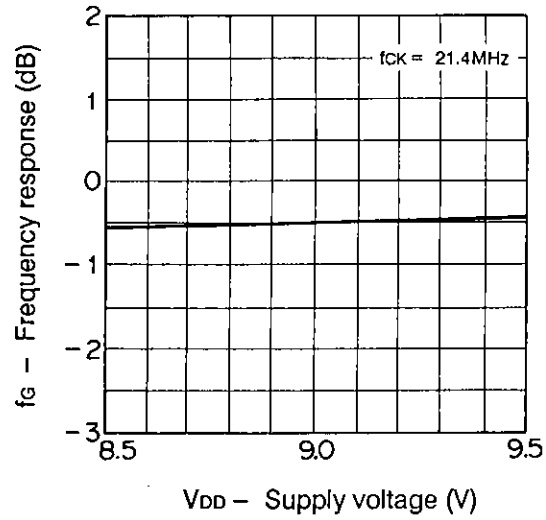
Gate voltage vs. Clock frequency



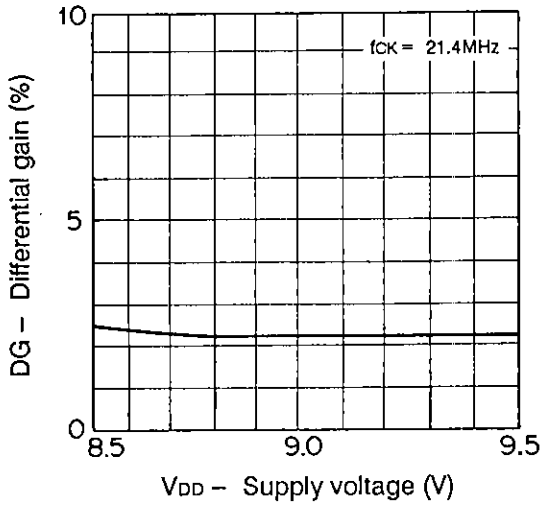
Insertion gain vs. Supply voltage



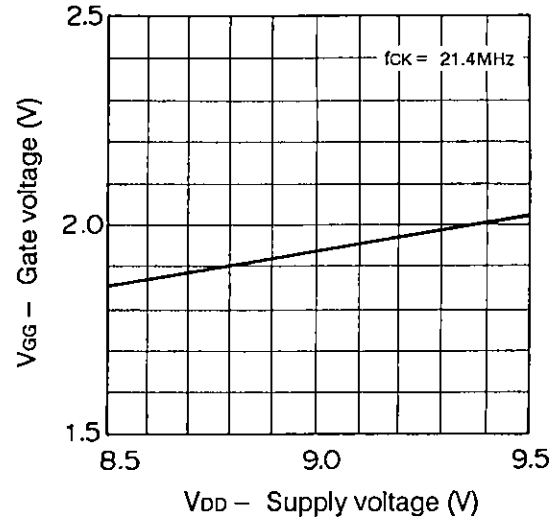
Frequency response vs. Supply voltage



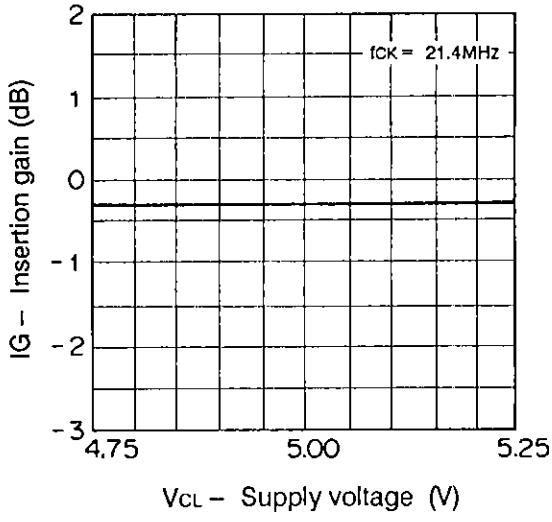
Differential gain vs. Supply voltage



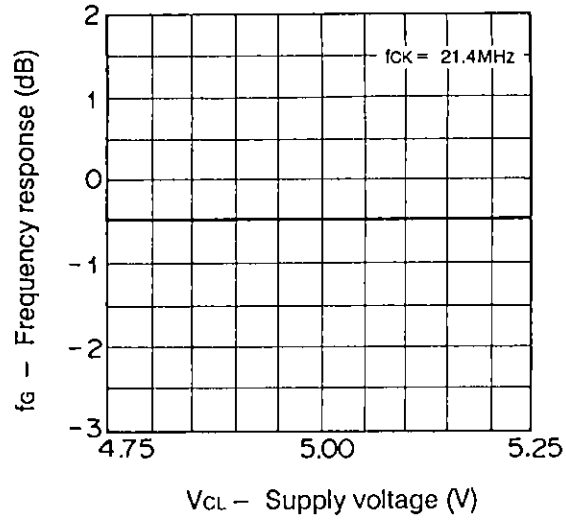
Gate voltage vs. Supply voltage



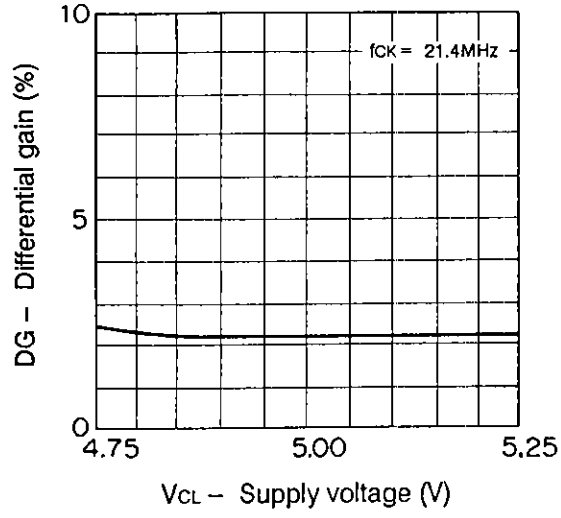
Insertion gain vs. Supply voltage



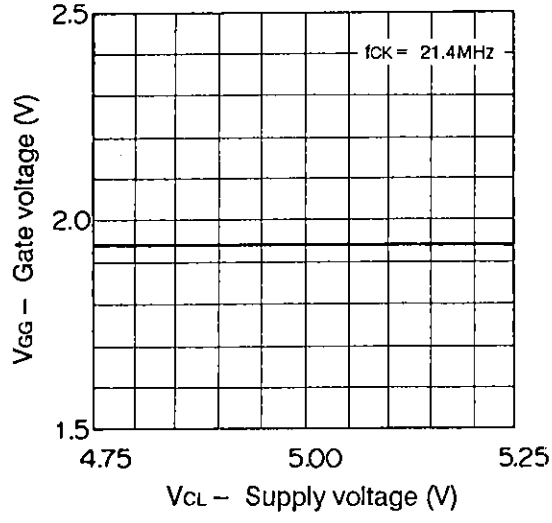
Frequency response vs. Supply voltage



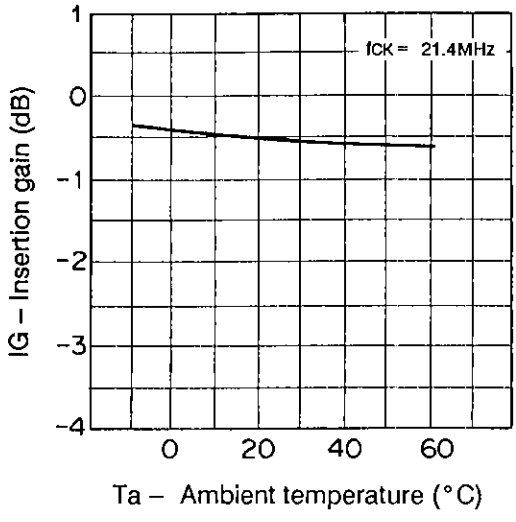
Differential gain vs. Supply voltage



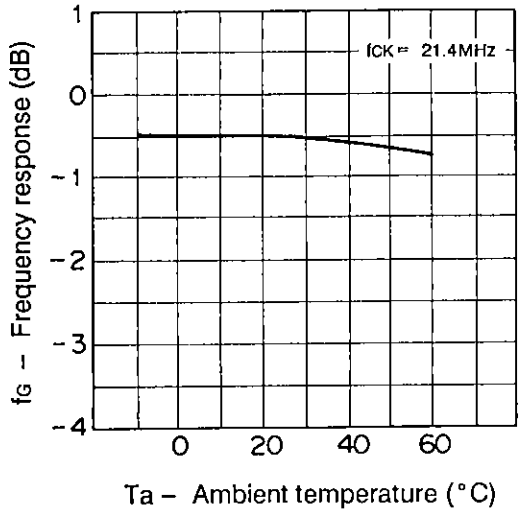
Gate voltage vs. Supply voltage



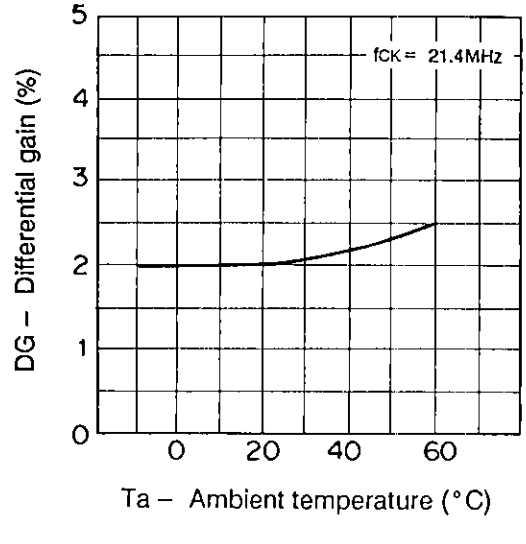
Insert gain vs. Ambient temperature



Frequency response vs. Ambient temperature



Differential gain vs. Ambient temperature



Gate voltage vs. Ambient temperature