

Applications

- 5GHz WLAN, IEEE 802.11a and HIPERLAN
- VSAT at 3.6 to 4.2 GHz
- Satellite Communications at 4.5 to 4.8 GHz
- 5 Gbps Clock Generator

Features

- Low Phase Noise, -141dBc/Hz at 1kHz offset
- Single Supply Voltage, 2.7 - 4.0 V
- Low Power Consumption, 42mW
- Power Down Mode, 0.2µA
- Compatible with common PLL synthesizer ICs
- 8-Pin Plastic SOIC Package

Product Description

The D602 is a SiGe divide-by-2 low noise static prescaler capable of operation up to 6.0 GHz. The D602 operates over a wide range of input frequencies and levels, and provides differential outputs for low noise operation with the common PLL style frequency synthesizer ICs.

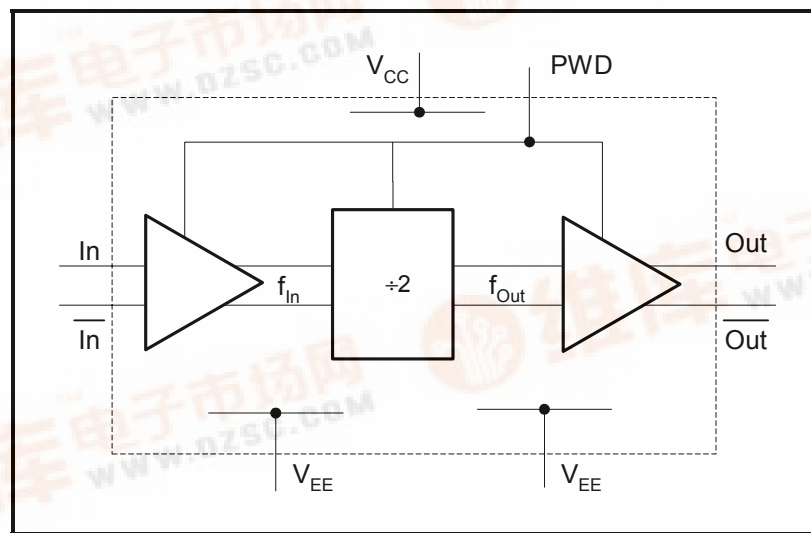
The static nature of the prescaler prevents spurious generation.

The D602 prescaler can operate from either a single positive or single negative supply with power down mode for low standby power consumption.

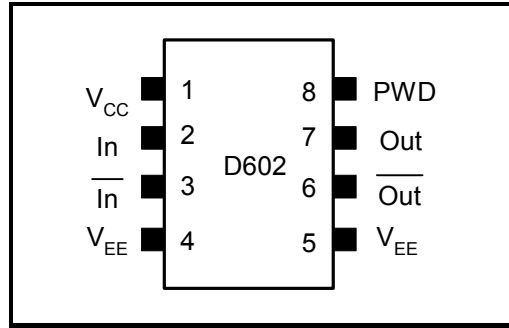
Ordering Information

Type	Package	Remark
D602	8-Pin SOIC	Plastic Package

Functional Block Diagram



Pin Out Diagram



Pin Out Description

Pin No.	Name	Description
1	V _{CC}	Power Supply Voltage Input
2	In	Prescaler Input (internally-biased)
3	In-bar	Prescaler Complementary Input (internally-biased)
4	V _{EE}	Ground for Input (pins 4 and 5 must be connected to the same potential)
5	V _{EE}	Ground for Output (pins 4 and 5 must be connected to the same potential)
6	Out-bar	Complementary Output (open-collector)
7	Out	Output (open-collector)
8	PWD	Power Down high impedance CMOS input. When PWD is high, the part is powered down.

Absolute Maximum Ratings

Operation in excess of any one of above Absolute Maximum Ratings may result in permanent damage. This device is a high performance RF integrated and is ESD sensitive. The RF inputs on this device are Class 0 ESD rated; therefore suitable precaution should be taken during handling, assembly and testing.

Symbol	Parameter	Min.	Max.	Unit
	Supply Voltage	-0.3	+4.3	V
	Voltage on any pin with respect to V _{EE}	-0.3	V _{CC} + 0.3	V
	Differential input voltage	-2.0	+2.0	V
	Storage Temperature	-65	+150	°C

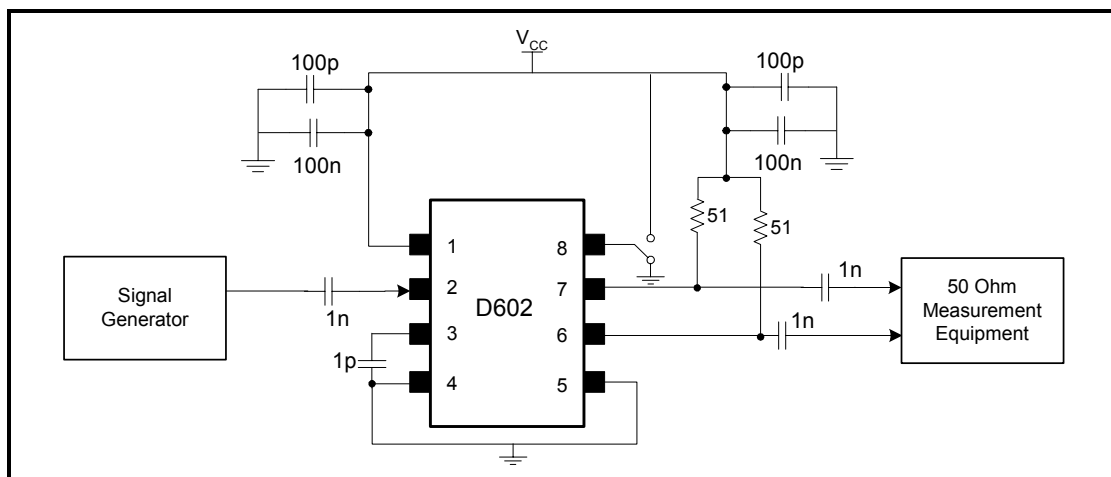
Electrical Characteristics

Conditions: $V_{CC} = 3.0V$, $-40^{\circ}C < T_A < 85^{\circ}C$ unless otherwise specified

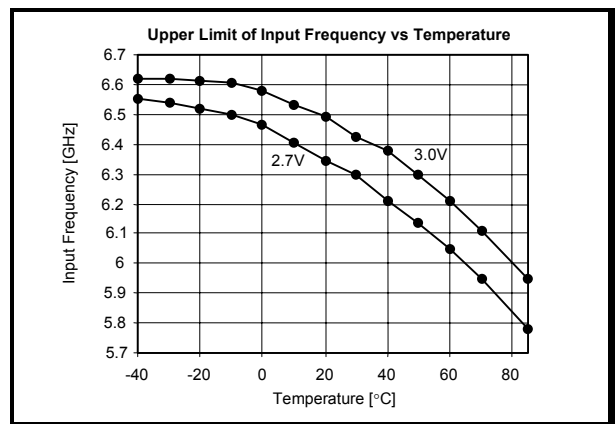
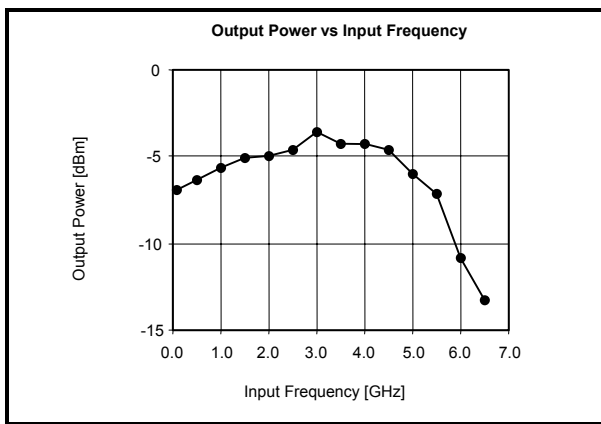
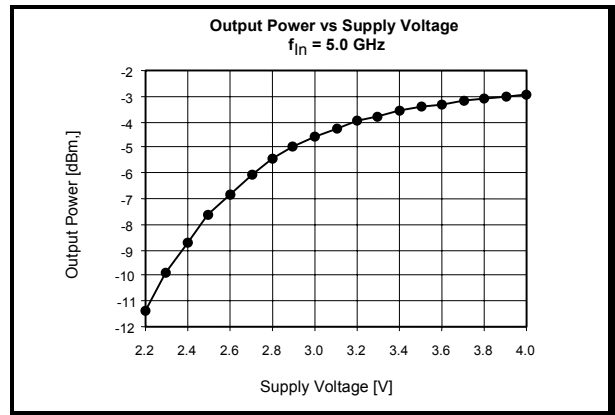
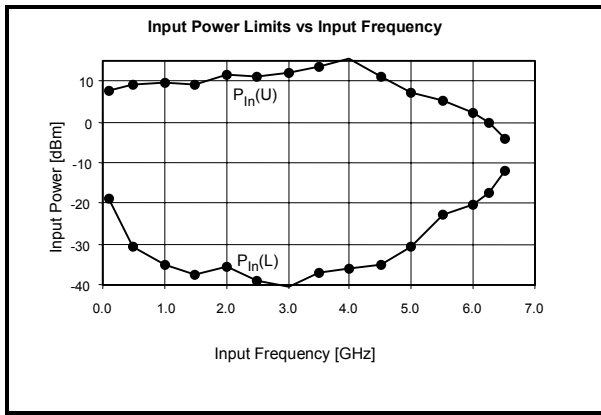
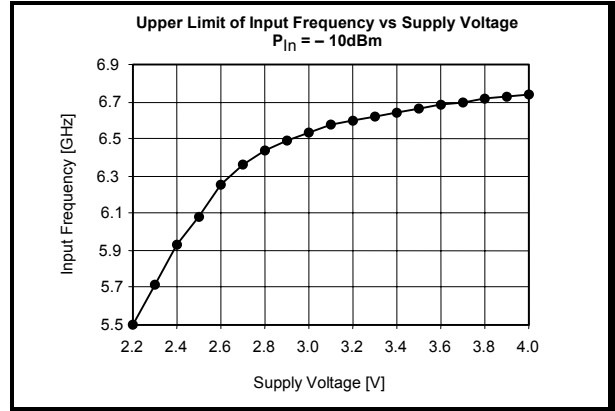
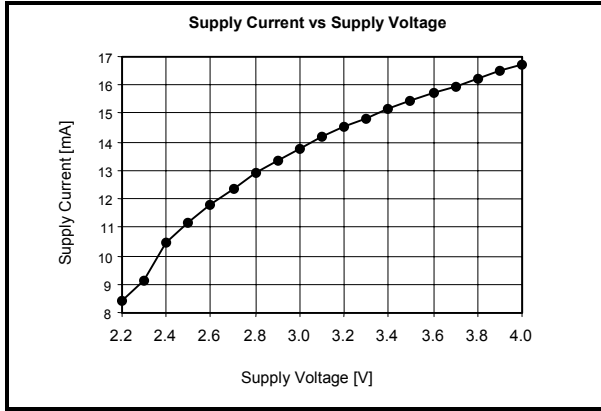
Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		2.7	3.0	4.0	V
T_A	Operating Temperature	1	-40	25	85	$^{\circ}C$
I_{CC}	Supply Current			14	18	mA
$I_{CC-PWDN}$	Power-Down Supply Current ($V_{PWD} = \text{High}$)			0.2	1.0	μA
$f_{In(U)}$	Upper Limit of Input Frequency	2	5.8	6.4		GHz
$f_{In(L)}$	Lower Limit of Input Frequency	2		0.6	1.0	GHz
f_{Osc}	Self Oscillation Output Frequency	3		1.0		GHz
$P_{In(U)}$	Upper Limit of Input Power		0	3		dBm
$P_{In(L)}$	Lower Limit of Input Power			-20	-10	dBm
P_{Out}	Output Power	4	-15.0		0	dBm
V_{IH}	High-Level PWD Input Voltage		$V_{CC} - 0.2$			V
V_{IL}	Low-Level PWD Input Voltage				0.2	V
I_{IH}	High-Level PWD Input Current		-100.0		100.0	nA
I_{IL}	Low-Level PWD Input Current		-100.0		100.0	nA
PN	Residual Phase Noise at 1kHz offset from a 2.5GHz (f_{Out}) carrier			-141		dBc/Hz

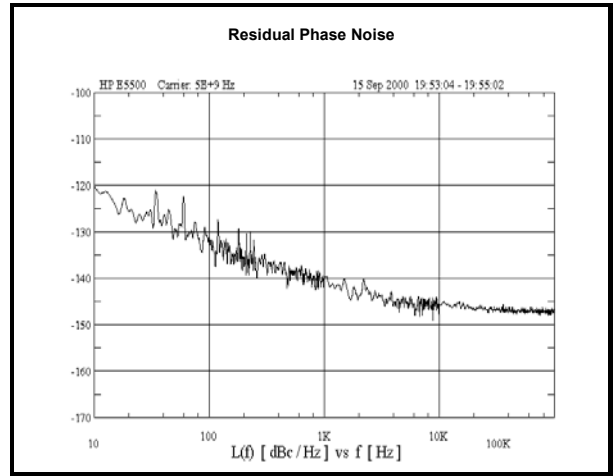
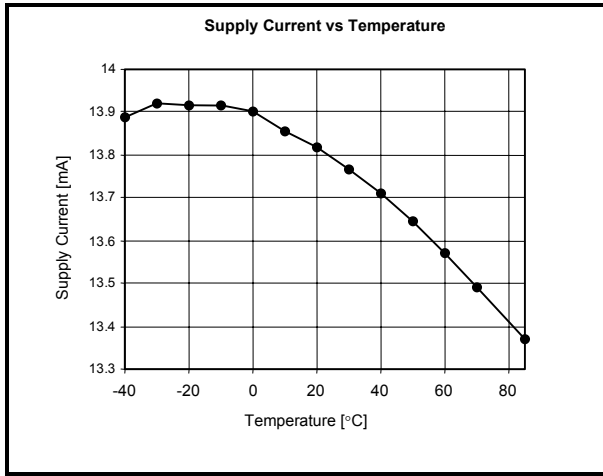
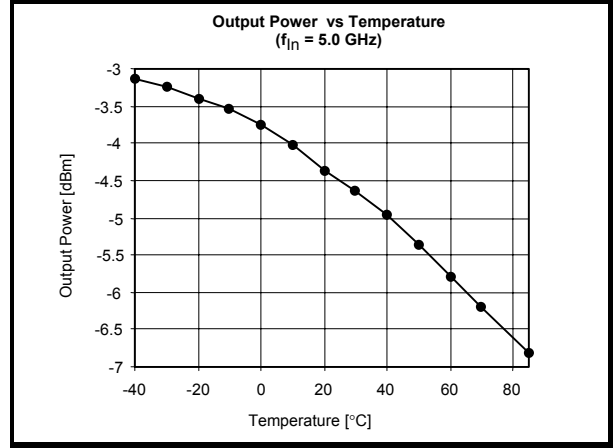
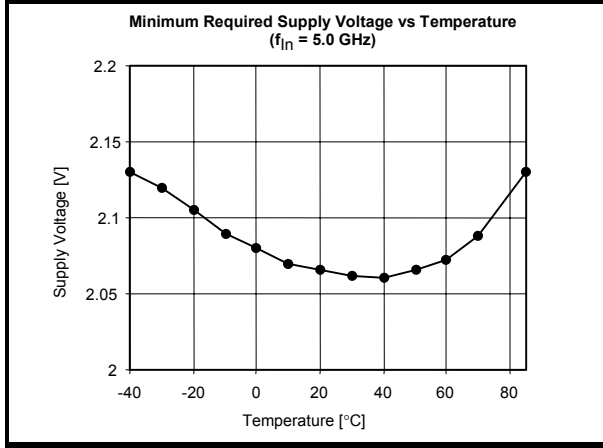
- Notes:**
- (1) Sample Tested
 - (2) For a sine-wave input
 - (3) Since the input signal is AC coupled, in the absence of an RF input, the prescaler may self oscillate and provide an output at this frequency. Self oscillation can be eliminated by powering down the prescaler, or applying a differential DC input voltage (a 47k Ω resistor placed between pin 3 and V_{CC}).
 - (4) This power is delivered to a 50 Ω load. It excludes the power dissipated in the external pull-up resistors.

Test Circuit

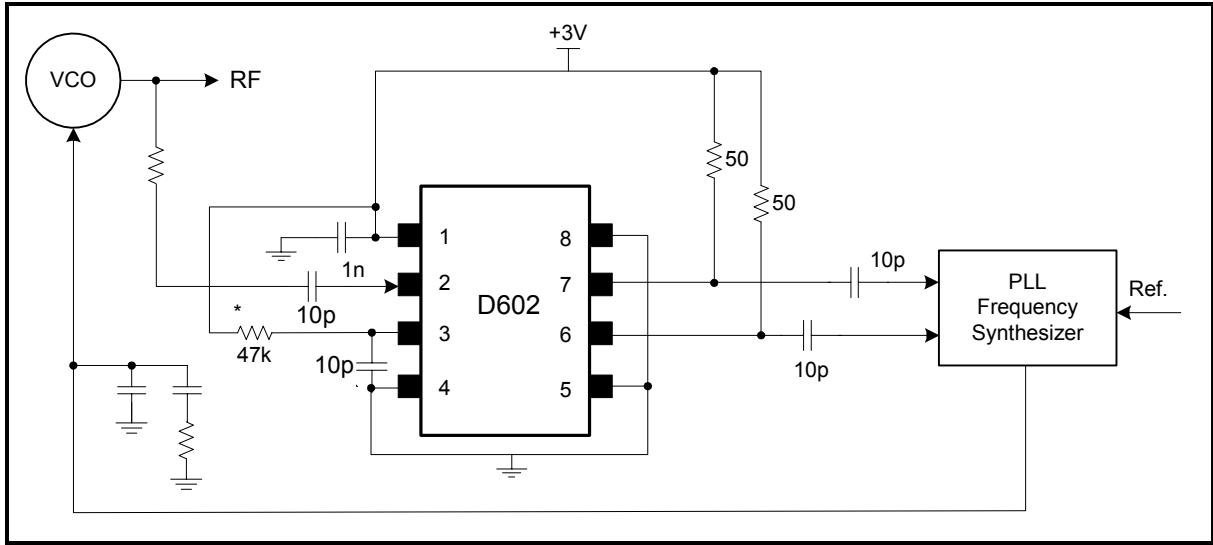


Typical Performance Characteristics





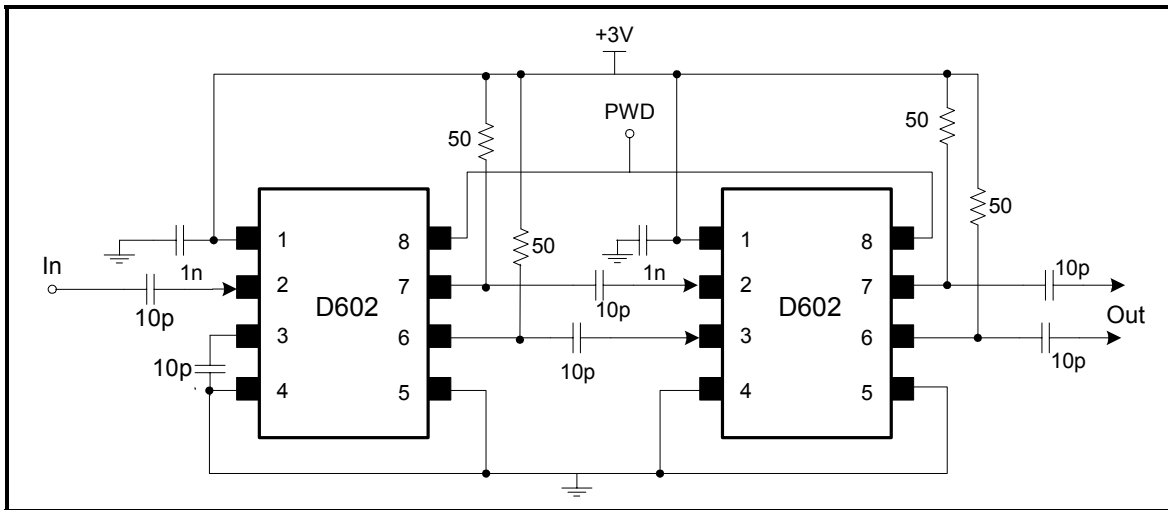
Typical Application Information



* The 47kΩ resistor provides a DC offset that disables self oscillation in the absence of an RF input.

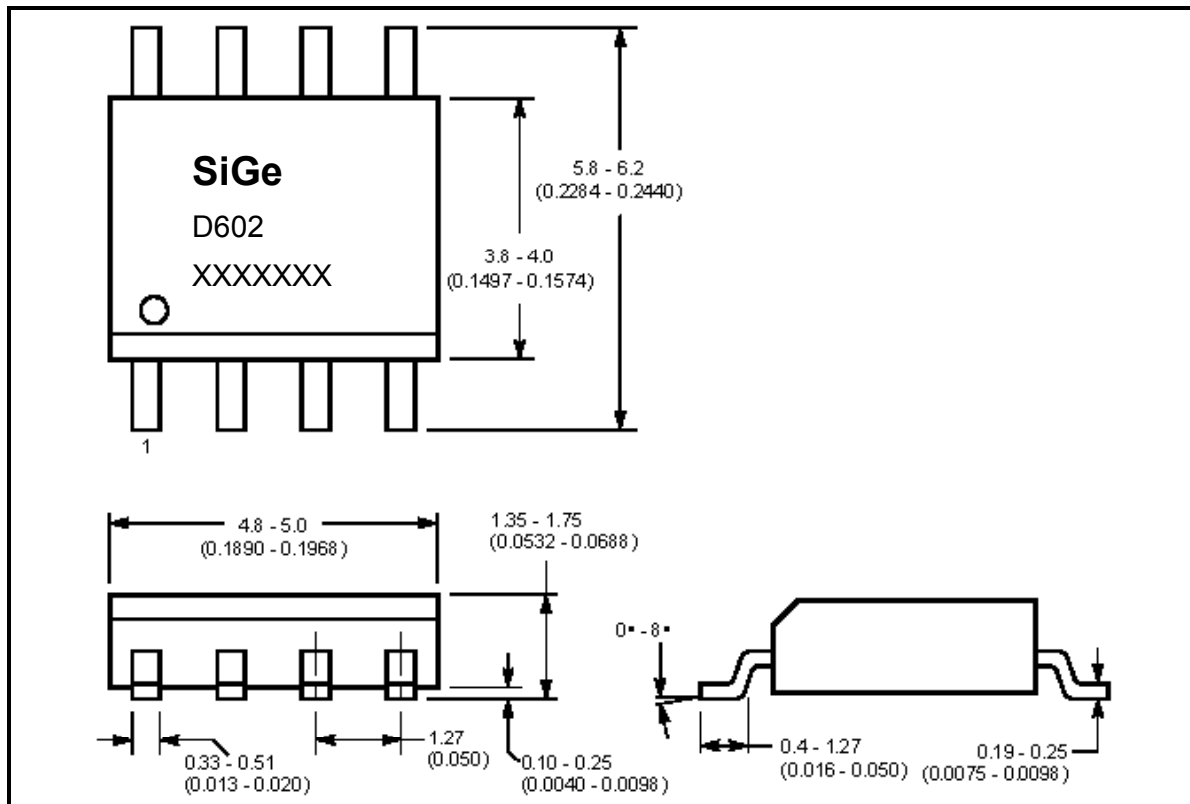
Cascading D602 Prescalers

D602 prescalers can be cascaded to achieve division ratios other than 2. For example two D602 prescalers can be used as shown in the following diagram to perform frequency division by 4.



Package Information

Package dimensions in millimeters (inches)
8-Lead Plastic SOIC



Packing Details

Note : Refer to JEDEC MS-012 for additional information

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Product Preview

The datasheet contains information from the product concept specification. SiGe Semiconductor Inc. reserves the right to change information at any time without notification.

Preliminary Information

The datasheet contains information from the design target specification. SiGe Semiconductor Inc. reserves the right to change information at any time without notification.

Final

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