

CMOS Quad SPST Analog Switch

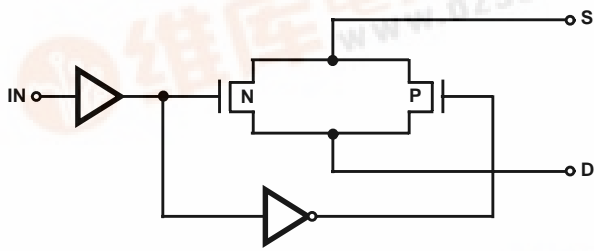
The DG201 solid state analog switch is designed using an improved, high voltage CMOS monolithic technology. It provides ease-of-use and performance advantages not previously available from solid state switches. Destructive latch-up of solid state analog gates have been eliminated by Intersil's CMOS technology.

The DG201 is completely specification and pinout compatible with the industry standard devices.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG201CJ	0 to 70	16 Ld PDIP	E16.3

Functional Diagram



DG201 SWITCH CELL

TRUTH TABLE

LOGIC	DG201
0	ON
1	OFF

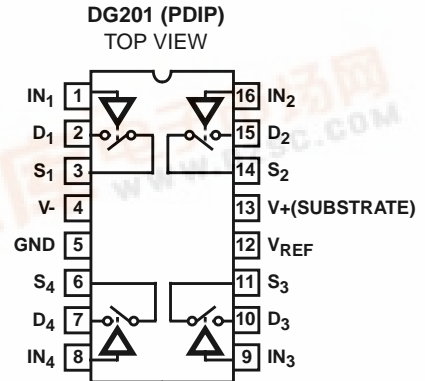
Features

- Switches Greater than 28V_{P-P} Signals with ±15V Supplies
- Break-Before-Make Switching
 - t_{OFF} 250ns
 - t_{ON} 700ns
- TTL, DTL, CMOS, PMOS Compatible
- Non-Latching with Supply Turn-Off
- Complete Monolithic Construction
- Industry Standard (DG201)

Applications

- Data Acquisition
- Sample and Hold Circuits
- Operational Amplifier Gain Switching Networks

Pinout

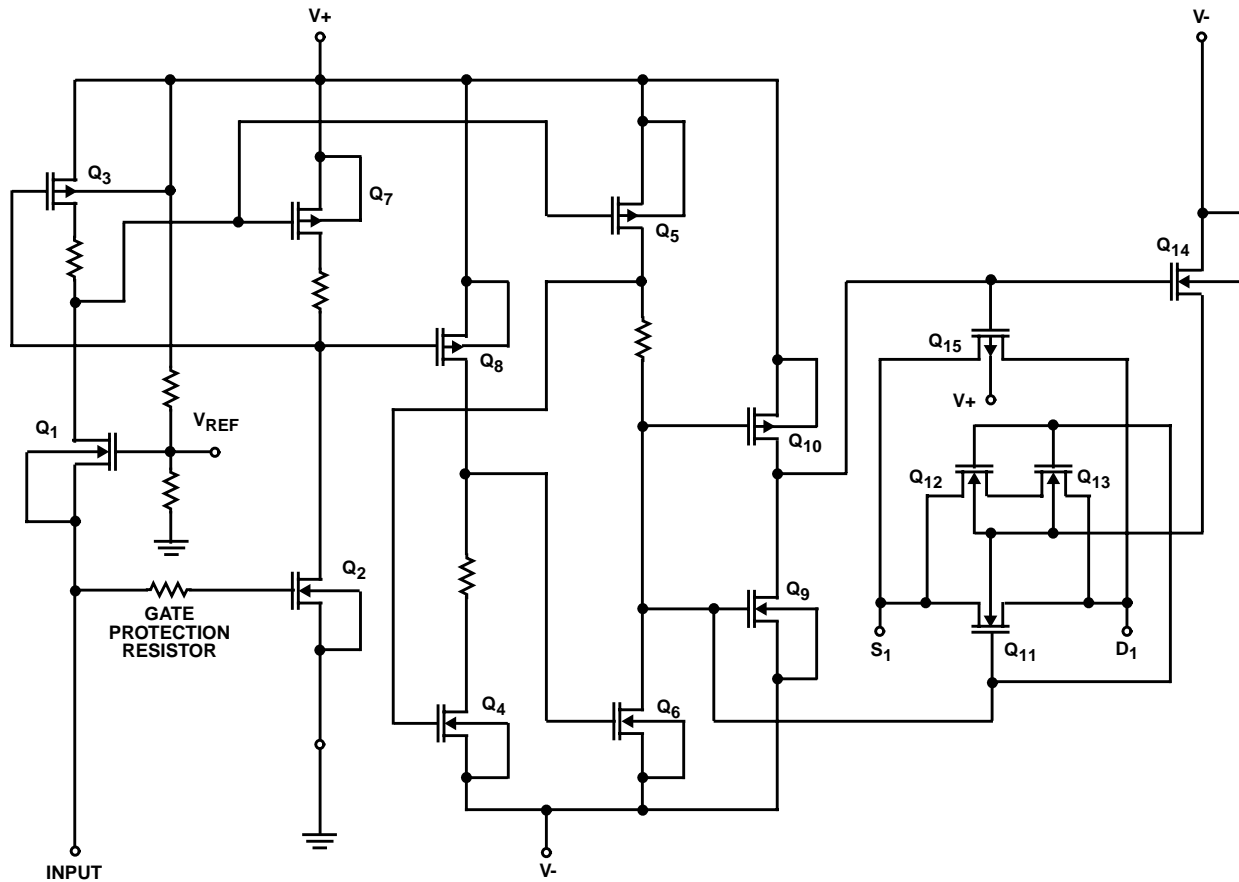


SWITCHES SHOWN FOR LOGIC "1" INPUT



DG201

Functional Diagram (1/4 DG201)



Pin Descriptions

PIN	SYMBOL	DESCRIPTION
1	IN ₁	Logic Control for Switch 1
2	D ₁	Drain (Output) Terminal for Switch 1
3	S ₁	Source (Input) Terminal for Switch 1
4	V-	Negative Power Supply Terminal
5	GND	Ground Terminal (Logic Common)
6	S ₄	Source (Input) Terminal for Switch 4
7	D ₄	Drain (Output) Terminal for Switch 4
8	IN ₄	Logic Control for Switch 4
9	IN ₃	Logic Control for Switch 3
10	D ₃	Drain (Output) Terminal for Switch 3
11	S ₃	Source (Input) Terminal for Switch 3
12	V _{REF}	Logic Reference Voltage
13	V+	Positive Power Supply Terminal (Substrate)
14	S ₂	Source (Input) Terminal for Switch 2
15	D ₂	Drain (Output) Terminal for Switch 2
16	IN ₂	Logic Control for Switch 2

DG201

Absolute Maximum Ratings

V+ to V-	36V
V+ to V _D	30V
V _D to V-	30V
V _D to V _S	28V
V _{REF} to V-	33V
V _{REF} to V _{IN}	30V
V _{REF} to GND	20V
V _{IN} to GND	20V
Current (Any Terminal)	30mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	90	N/A
Maximum Junction Temperature		
Plastic Package	150°C	
Maximum Storage Temperature Range	-65°C to 150°C	
Maximum Lead Temperature (Soldering 10s)	300°C	

Operating Conditions

Temperature Range	0°C to 70°C
“C” Suffix	0°C to 70°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^\circ\text{C}$, V+ = +15V, V- = -15V

PARAMETER	TEST CONDITIONS	“C” SUFFIX			UNITS
		0°C	(NOTE 2) 25°C	70°C	
DYNAMIC CHARACTERISTICS					
Turn-ON Time (Note 3), t_{ON}	$R_L = 1\text{k}\Omega$, $V_{ANALOG} = -10\text{V to } +10\text{V}$ (Figure 1)	-	1.0	-	μs
Turn-OFF Time (Note 3), t_{OFF}	$R_L = 1\text{k}\Omega$, $V_{ANALOG} = -10\text{V to } +10\text{V}$ (Figure 1)	-	0.5	-	μs
Charge Injection, Q	Figure 2	-	20 (Typ)	-	mV
Off Isolation Rejection Ratio, OIRR	$f = 1\text{MHz}$, $R_L = 100\Omega$, $C_L \leq 5\text{pF}$, (Figure 3)	-	50 (Typ)	-	dB
Crosstalk (Channel-to-Channel), CCRR	One Channel Off	-	-50 (Typ)	-	dB
DIGITAL INPUT CHARACTERISTICS					
Input Logic Current, $I_{IN(ON)}$	$V_{IN} = 0.8\text{V}$ (Note 3)	± 1	± 1	± 10	μA
Input Logic Current, $I_{N(OFF)}$	$V_{IN} = 2.4\text{V}$ (Note 3)	± 1	± 1	± 10	μA
ANALOG SWITCH CHARACTERISTICS					
Analog Signal Range, V_{ANALOG}		-	± 15 (Typ)	-	V
Drain-Source ON Resistance, $r_{DS(ON)}$	$I_S = 10\text{mA}$, $V_{ANALOG} = \pm 10\text{V}$	100	100	125	Ω
Channel-to-Channel $r_{DS(ON)}$ Match, $r_{DS(ON)}$		-	30 (Typ)	-	Ω
Drain OFF Leakage Current, $I_{D(OFF)}$	$V_{ANALOG} = -14\text{V to } +14\text{V}$	-	± 5	100	nA
Source OFF Leakage Current, $I_{S(OFF)}$	$V_{ANALOG} = -14\text{V to } +14\text{V}$	-	± 5	100	nA
Channel ON Leakage Current, $I_{D(ON)} + I_{S(ON)}$	$V_D = V_S = -14\text{V to } +14\text{V}$	-	± 5	200	nA
POWER SUPPLY CHARACTERISTICS					
Supply Current, I+ Positive	$V_{IN} = 0\text{V}$ or $V_{IN} = 5\text{V}$	2000	1000	2000	μA
Supply Current, I- Negative		2000	1000	2000	μA

NOTES:

- Typical values are for design aid only, not guaranteed and not subject to production testing.
- All channels are turned off by high “1” logic inputs and all channels are turned on by low “0” inputs; however 0.8V to 2.4V describes the minimum range for switching properly. Peak input current required for transition is typically -120 μA .

Test Circuits

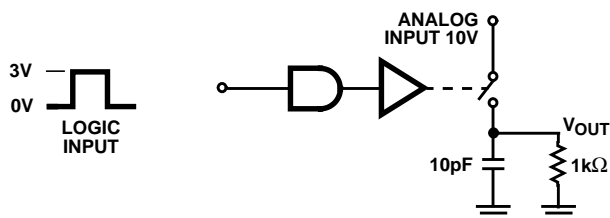


FIGURE 1. t_{ON} AND t_{OFF} TEST CIRCUIT

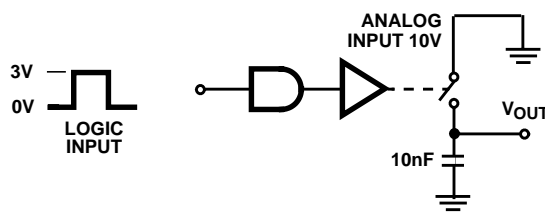


FIGURE 2. CHARGE INJECTION TEST CIRCUIT

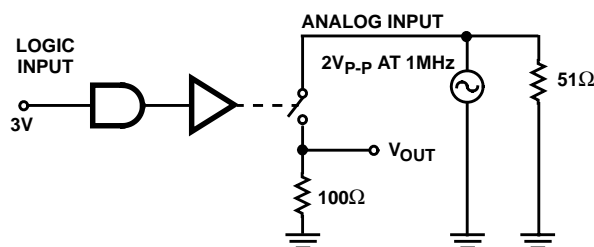


FIGURE 3. OFF ISOLATION TEST CIRCUIT

Typical Applications

Using the V_{REF} Terminal

The DG201 has an internal voltage divider setting the TTL threshold on the input control lines for $V+$ equal to +15V. The schematic shown in Figure 4 with nominal resistor values, gives approximately 2.4V on the V_{REF} pin. As the TTL input signal goes from +0.8V to +2.4V, Q_1 and Q_2 switch states to turn the switch ON and OFF. If the power supply voltage is less than +15V, then a resistor (R_{EXT}) must be added between $V+$ and the V_{REF} pin, to restore +2.4V at V_{REF} . The table shows the value of this resistor for various supply voltages, to maintain TTL compatibility. If CMOS logic levels with a +5V supply are being used, the threshold shifts are less critical, but a separate column of suitable values is given in the table. For logic swings of -5V to +5V, no resistor is needed.

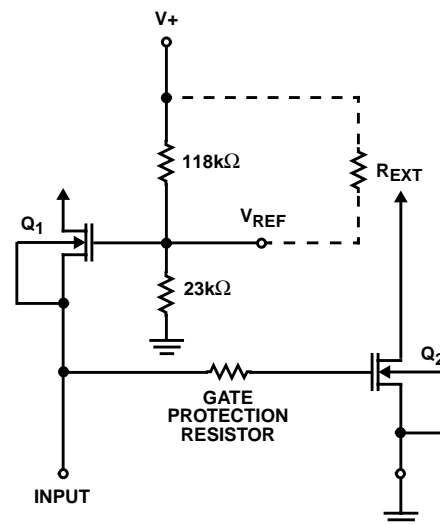


FIGURE 4.

In general, the “low” logic level should be <0.8V to prevent Q_1 and Q_2 from both being ON together (this will cause incorrect switch function).

TABLE 1.

$V+$ SUPPLY (V)	R_{EXT} FOR TTL LEVELS (k Ω)	R_{EXT} FOR CMOS LEVELS (k Ω)
+15	-	-
+12	420	-
+10	190	-
+9	136	136
+8	98	98
+7	70	70

Typical Performance Curves

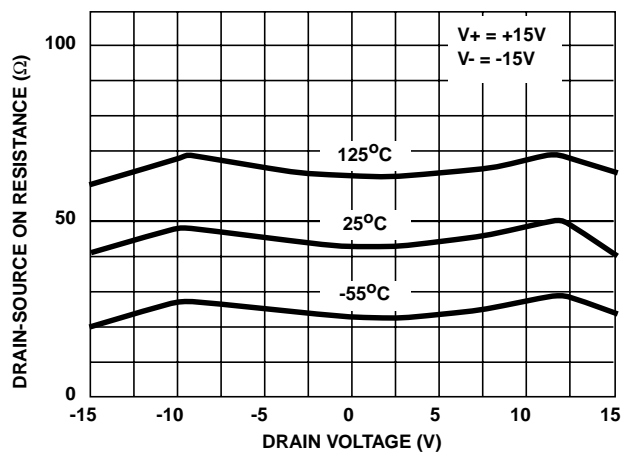


FIGURE 5. $r_{DS(ON)}$ vs V_D AND TEMPERATURE

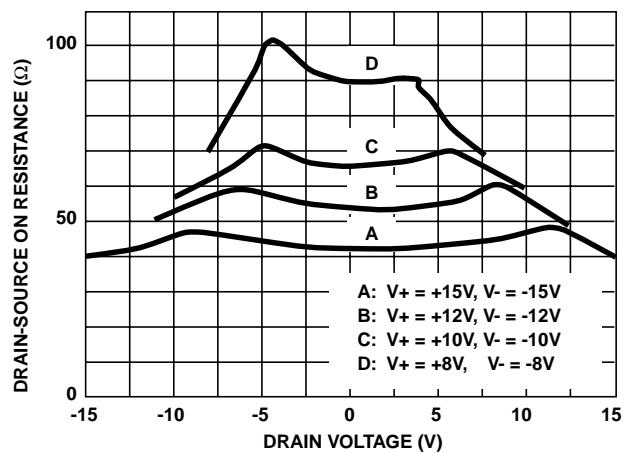


FIGURE 6. $r_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE

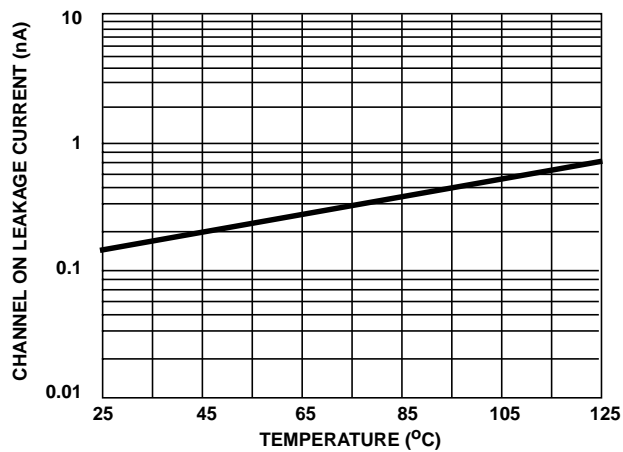


FIGURE 7. $I_{D(ON)}$ vs TEMPERATURE

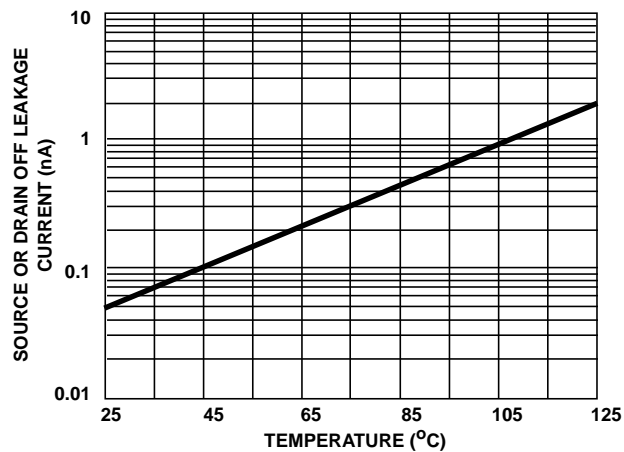


FIGURE 8. $I_{S(OFF)}$ OR $I_{D(OFF)}$ vs TEMPERATURE

DG201

Die Characteristics

DIE DIMENSIONS:

94 mils x 101 mils x 14 mils

METALLIZATION:

Type: Al
Thickness: 10kÅ

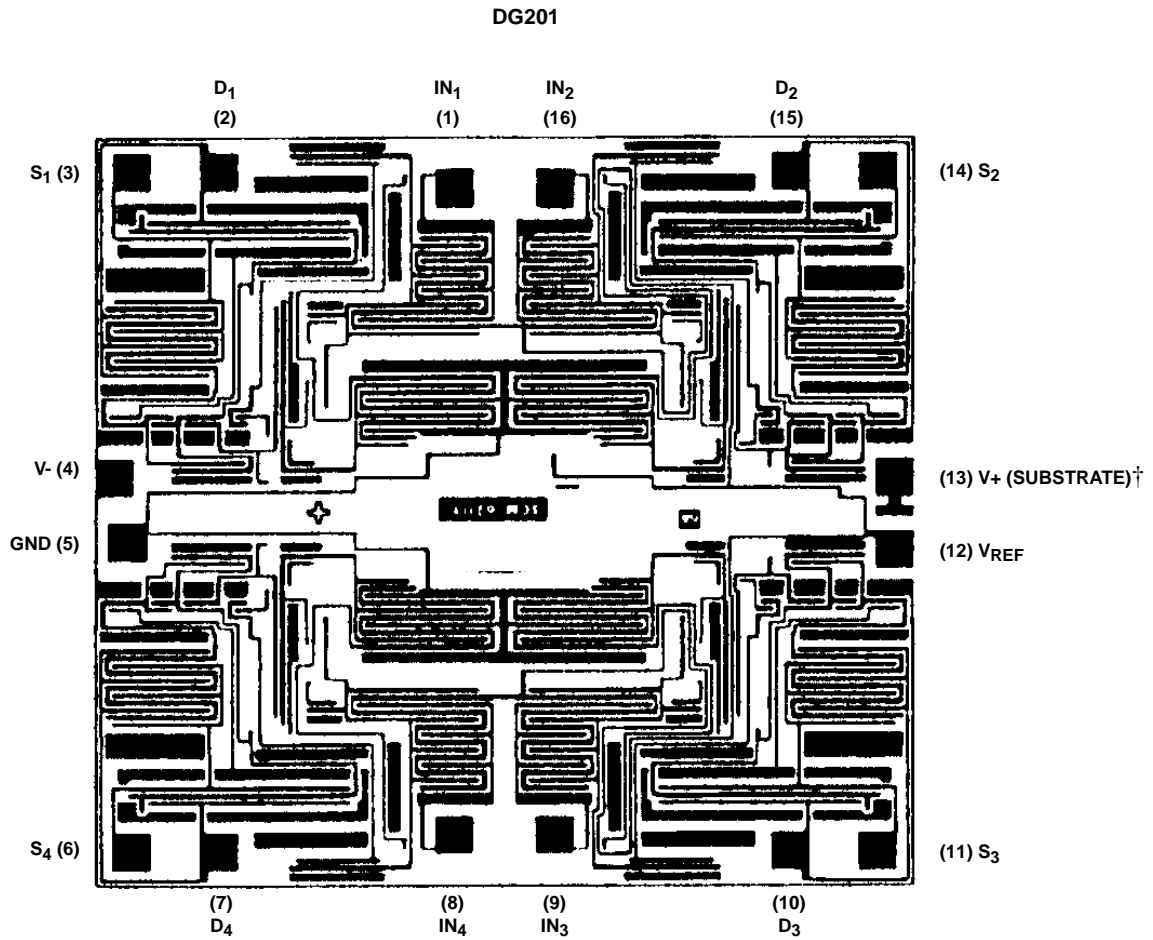
PASSIVATION:

Type: SiO₂/Si₃N₄
SiO₂ Thickness: 7kÅ
Si₃N₄ Thickness: 8kÅ

WORST CASE CURRENT DENSITY:

$1 \times 10^5 \text{ A/cm}^2$

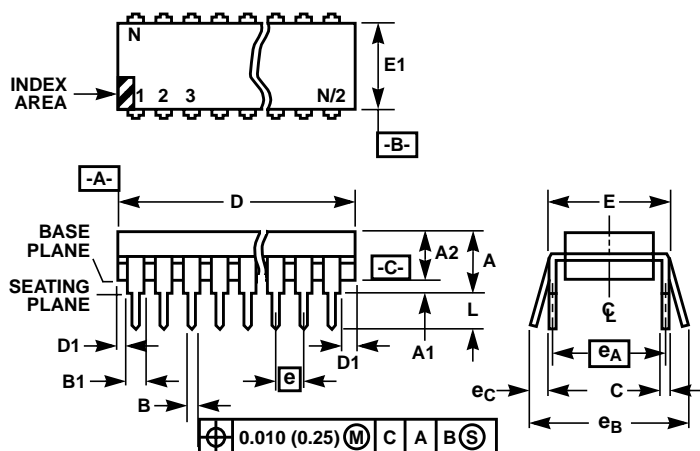
Metallization Mask Layout



† BACKSIDE OF CHIP IS V+

DG201

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum $-C-$.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D) 16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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