PRELIMINARY

Differential Hall Sensor **TLE4925/TLE4925C**

Features

- Advanced performance by dynamic self calibration principle
- High sensitivity
- Single chip solution
- Symmetrical thresholds
- High resistance to Piezo effects
- South and north pole pre-induction possible
- low cut-off frequency
- Digital output signal
- Two-wire and three-wire configuration possible
- Wide operating temperature range
- Fast start-up time
- Large operating air-gaps
- Reverse voltage protection at Vs- PIN
- Short- circuit and over temperature protection of output
- No external filter capacitor required (TLE4925C)
- Digital output signal (voltage interface)
- Module style package with two 4.7nF integrated capacitors (TLE4925C)

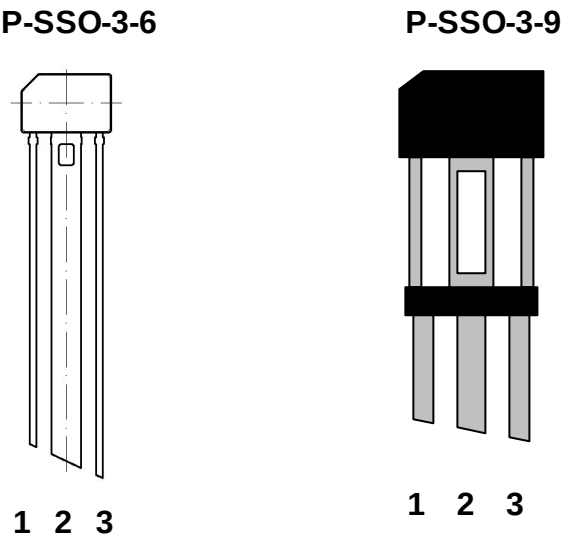


Figure 1: Pin configuration in P-SSO-3-6 and P-SSO-3-9

Pin No.	Symbol	Function
1	V_S	Supply Voltage
2	GND	Ground
3	Q	Open Drain Output

General Information

The TLE4925/TLE4925C is an active Hall sensor suited to detects the motion and position of ferromagnetic and permanent magnet structures. An additional self-calibration module has been implemented to achieve optimum accuracy during normal running operation. It comes in a three-pin package for the supply voltage and an open drain output.

Functional Description

The differential Hall sensor IC detects the motion and position of ferromagnetic and permanent magnet structures by measuring the differential flux density of the magnetic field. To detect ferromagnetic objects the magnetic field must be provided by a back biasing permanent magnet (south or north pole of the magnet attached to the rear unmarked side of the IC package).

Offset cancellation is achieved by advanced digital signal processing. Immediately after power-on motion is detected (start-up mode). After a few transitions the sensor has finished self-calibration and switches to a high-accuracy mode (running mode). In running mode switching occurs at signal zero-crossing of the arithmetic mean of max and min value of magnetic differential signal. ΔB is defined as difference between hall plate 1 and hall plate 2.

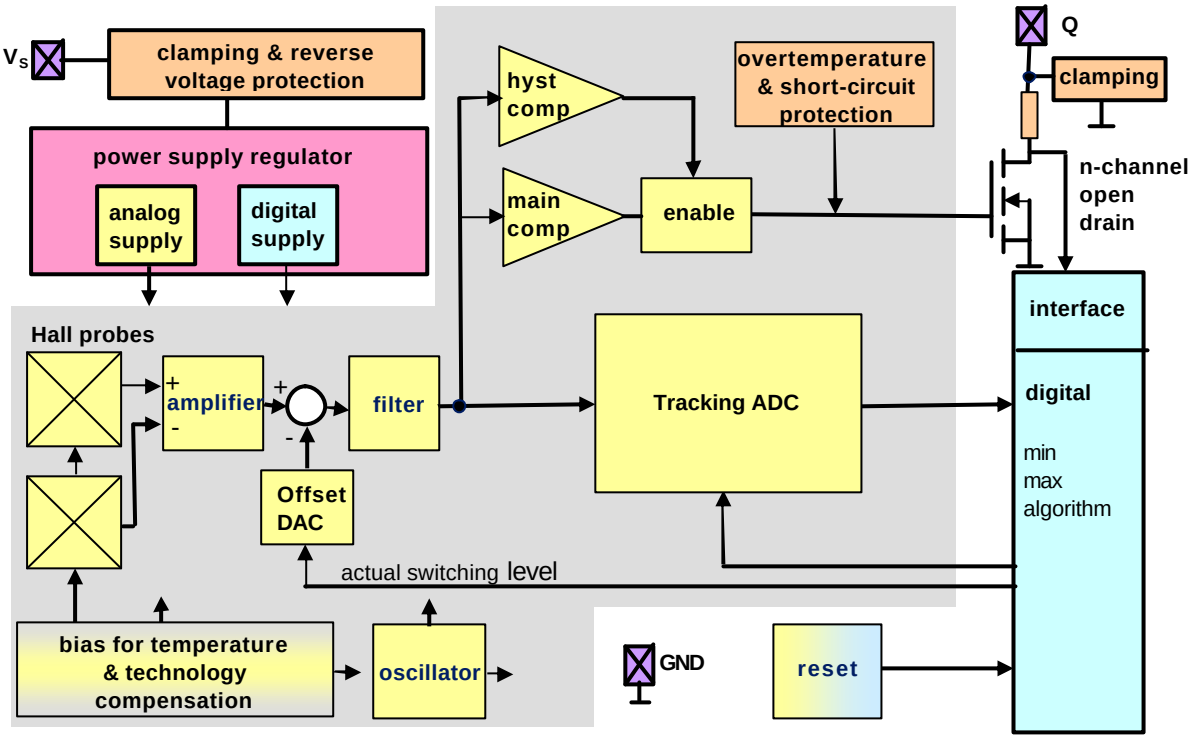


Figure 2: Block Diagram of TLE4925/TLE4925C

Circuit Description

The TLE4925/TLE4925C is comprised of a supply voltage regulator, a pair of hall probes, spaced at 2.5mm, differential amplifier, noise-shaping filter, comparator, advanced digital signal processor (DSP), A/D and D/A converter and an open drain output.

Startup mode:
The differential signal is digitized in the A/D converter and fed into the dsp part of the circuit. There a rising or falling transition is detected and the output stage is triggered accordingly. As the signal is not offset compensated at this time, the output does not neccessarily switch at zero-crossing of the magnetic signal. Signal peaks are also detected in the digital circuit and their arithmetic mean value can be calculated. The offset of this mean value is determined and fed into the offset cancellation DAC. This procedure can be repeated with increasing accuracy. After few increments the IC is switched into the high accuracy running mode.

Running mode:
In running mode the output is triggered by the comparator. An offset cancellation feedback loop is formed by the A/D converter, dsp and offset cancellation D/A converter. In running mode switching always occurs at zero-crossing. It is only affected by the (small) remaining offset of the comparator and by the remaining propagation delay time of the signal path, mainly determined by the noise-shaping filter. Nevertheless signals below a defined threshold are not detected to avoid unwanted parasitic switching.

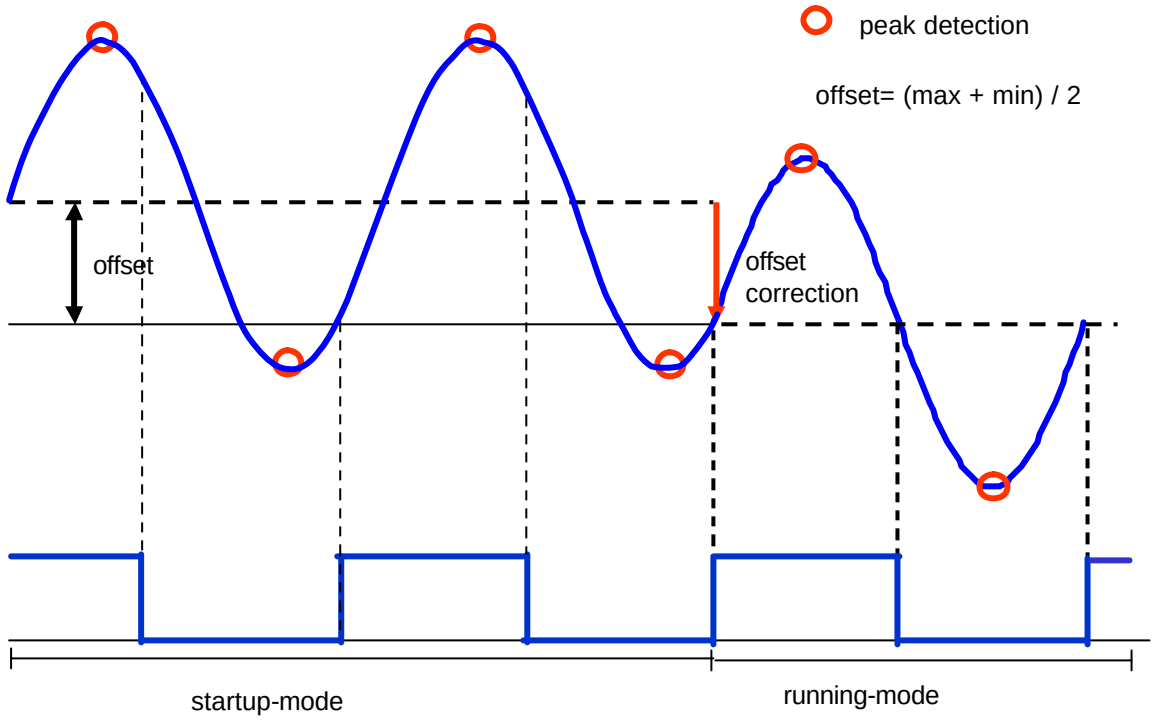


Figure 3: Startup of the device

At transition from startup-mode to running mode switching timing is moving from low-accuracy to high accuracy zero-crossing.

1.1 Absolute Maximum Ratings

No.	Parameter	Symbol	min	Typ	max	Unit	Remarks
1.1.1	Supply voltage	V_S	-18		18	V	-
			-24		24	V	1h with $R_{Series} \geq 200\Omega$[1]
			-26		26	V	5min with $R_{Series} \geq 200\Omega$[1]
			-28		28	V	1min with $R_{Series} \geq 200\Omega$[1]
1.1.2	Supply current	I_S	-10		25	mA	-
1.1.3	Output OFF voltage	V_Q	-0.3		18	V	-
			-0.3		24	V	1h with $R_{Load} \geq 500\Omega$
			-0.3		26	V	5min with $R_{Load} \geq 500\Omega$
			-1.0		-	V	1h (protected by internal series resistor)
1.1.4	Output ON voltage	V_Q	-		16	V	Current internal limited by short circuit protection (72h @ $T_A < 40°C$).
			-		18	V	Current internal limited by short circuit protection (1h @ $T_A < 40°C$).
			-		24	V	Current internal limited by short circuit protection (1min @ $T_A < 40°C$).
1.1.5	Continuous output current	I_Q	-50		50	mA	-
1.1.6	Junction temperature	T_j	-40			°C	-
					155	°C	2000h (not additive)
					165	°C	1000h (not additive)
					175	°C	168 h (not additive)
					195	°C	3 x1 h (additive to the other life times).
1.1.7	Storage temperature	T_S	-40		150	°C	-
1.1.8	Thermal resistance junction-air for P-SSO-3-6 P-SSO-3-9	$R_{th\ JA}$			190	K/W	Lower values are possible with overmoulded devices.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1] Accumulated life time.

1.2 Electro Magnetic Compatibility - *(values depend on R_{Series}!)*

Ref. ISO 7637-1; see test circuit of figure 4 and 5;

ΔB_{PP} = 10mT (ideal sinusoidal signal); V_S=13.5V ± 0.5V, f_B= 1000Hz; T= 25°C; $R_{Series} \geq 200\Omega$;

No.	Parameter	Symbol	Level/typ	Status
1.2.1	Testpulse 1	V_{EMC}	IV / -100V	C[2]
	Testpulse 2		IV / 100V	C[2]
	Testpulse 3a		IV / -150V	A
	Testpulse 3b		IV / 100V	A
	Testpulse 4		IV / -7V	A
	Testpulse 5		IV / 86.5V	C

Note: Test criteria for status A: No missing pulse no additional pulse on the IC output signal plus duty cycle and jitter are in the specification limits.
Test criteria for status B: No missing pulse no additional pulse on the IC output signal. (Output signal "OFF" means switching to the voltage of the pull-up resistor).
Test criteria for status C: One or more parameter can be out of specification during the exposure but returns automatically to normal operation after exposure is removed.
Test criteria for status E: IC destroyed.

Ref. ISO 7637-3; TP 1 and TP 2 ref. DIN 40839-3; see test circuit of figure 4 and 5;

ΔB_{PP} = 10mT (ideal sinusoidal signal); V_S=13.5V ± 0.5V, f_B= 1000Hz; T= 25°C; $R_{Series} \geq 200\Omega$;

No.	Parameter	Symbol	Level/typ	Status
1.2.2	Testpulse 1	V_{EMC}	IV / -30V	A
	Testpulse 2		IV / 30V	A
	Testpulse 3a		IV / -60V	A
	Testpulse 3b		IV / 40V	A

Ref. ISO 11452-3; see test circuit of figure 4 and 5; measured in TEM-cell;
ΔB_{PP} = 4mT (ideal sinusoidal signal); V_S=13.5V ± 0,5V, f_B= 200Hz; T= 25°C; $R_{Series} \geq 200\Omega$;

No.	Parameter	Symbol	Level/max	Remarks
1.2.3	EMC field strength	$E_{TEM-Cell}$	IV / 200V/m	AM=80%, f=1kHz;

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Test condition for the trigger window: $f_{B-field}$=200Hz, B_{pp}=4mT, vertical limits are ±200mV and horizontal limits are ±200µs.

[2] According to 7637-1 the supply switched „OFF" for t=200ms. For battery „ON" is valid status „A".

1.3 ESD Protection

No.	Parameter	Symbol		max	Unit	Remarks
1.3.1	ESD – protection P-SSO-3-9 P-SSO-3-6	V_{ESD}		± 8 ± 6	kV kV	According to standard EIA/JESD22-A114-B Human Body Model (HBM).

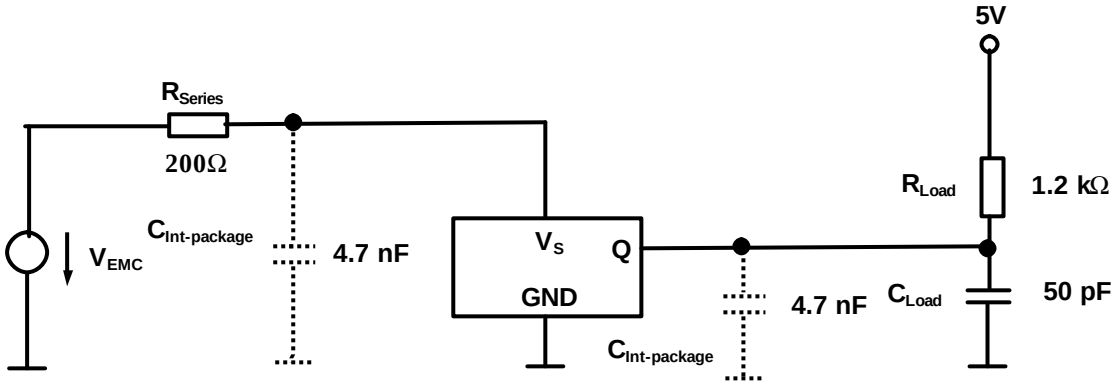


Figure 4: Test Circuit for EMC tests (TLE4925C) – P-SSO-3-9 Package

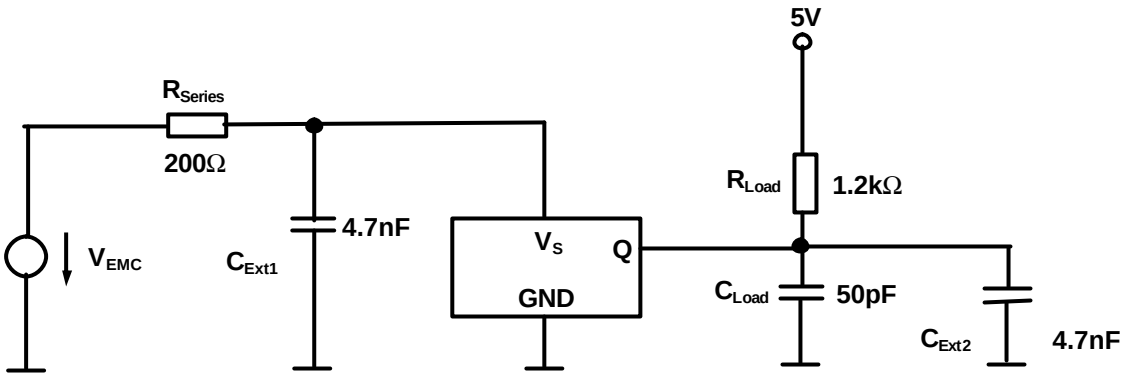


Figure 5: Test Circuit for EMC tests (TLE4925) – P-SSO-3-6 Package

2.1 Operating Range

No.	Parameter	Symbol	min	typ	max	Unit	Remarks
2.1.1	Supply voltage	V_S	3.3		18	V	Continuous
					24	V	1h with $R_{Series} \geq 200\Omega$
					26	V	5min with $R_{Series} \geq 200\Omega$. Extended limits for parameters in characteristics.
			3			V	During test pulse 4.
2.1.2	Supply voltage ripple	V_{SAC}			6	V_{pp}	V_S=13V; 0 < f < 50kHz
2.1.3	Continuous output OFF voltage	V_Q	-0.3		18	V	Continuous
			-18		24	V	1h with $R_{Load} \geq 500\Omega$
2.1.4	Continuous output ON current	I_Q	0		20	mA	V_{Qmax}=0.6V
2.1.5	Power on time	t_{on}			1	ms	Time to achieve specified accuracy. After power on the output of the IC is always in high-state. After internal resets output is locked[3].
2.1.6	Operating junction temperature	T_j	-40			°C	-
					155	°C	2000 h (not additive)
					165	°C	1000 h (not additive)
					175	°C	168 h (not additive) reduced signal quality permittable (e.g. jitter)

Note: Unless otherwise noted, all temperatures refer to junction temperature.
For the supply voltage lower than 28V ($R_{Series} \geq 200\Omega$) and junction temperature lower than 195°C the magnetic and AC/DC characteristics can exceed the specification limits.

[3] Output of the IC is locked in present state (high-state or low-state) after an internal reset is launched. This reset happens typically every 780ms when there is no significant signal change. See also 2.2.14. A voltage reset causes a release of the output and output is in high state after power on again.

2.2 AC/DC Characteristics

Over operating range, unless otherwise specified. Typical values correspond to V_S=12V and T_A=25°C

No.	Parameter	Symbol	min	typ	max	Unit	Remarks
2.2.1	Supply current	I_S	3	6.8	9	mA	-
2.2.2	Supply current @ 3.3V	I_{SVmin}	3	6.7	8	mA	V_S=3.3V
2.2.3	Supply current @ 24V	I_{Smax}	3	7	9.5	mA	V_S=24V $R_{Series} \geq 200\Omega$
2.2.4	Output saturation voltage	V_{Qsat}		0.25	0.6	V	I_Q= 20mA
2.2.5	Output leakage current	I_{Qleak}		0.1	10	µA	V_Q= 18V
2.2.6	Current limit for short-Circuit protection	I_{Qshort}	30	60	80	mA	-
2.2.7	Junction temperature limit for output protection	T_{prot}	195	210	230	°C	-
2.2.8	Output rise time	t_r[4]					
	TLE4925C (P-SSO-3-9)		4	12	20	µs	V_{Load}= 4.5 to 24V R_{Load}= 1.2kΩ; C_{Load}= 4.7nF included in package.
	TLE4925 (P-SSO-3-6)		4	12	20	µs	V_{Load}= 4.5 to 24V R_{Load}= 1.2kΩ; C_{Load}= 4.7nF external capacitor.
2.2.9	Output fall time	t_f[5]					
	TLE4925C (P-SSO-3-9)		0.5	0.9	1.3	µs	V_{Load}= 5V
			0.65	1.15	1.65	µs	V_{Load}= 12V R_{Load}= 1.2kΩ; C_{Load}= 4.7nF included in package.
	TLE4925 (P-SSO-3-6)		0.5	0.9	1.3	µs	V_{Load}= 5V
			0.65	1.15	1.65	µs	V_{Load}= 12V R_{Load}= 1.2kΩ; C_{Load}= 4.7nF external capacitor.

[4] value of capacitor: 4.7nF±10%; (excluded drift due to temperature); ceramic: X7R; maximum voltage: 100V.

2.2.10	delay time	t_d	7	12.5	18 20[6]	µs µs	Only valid for Tj=25°C. Valid for Tj=-40°C till Tj=175°C. Higher magnetic slopes and overshoots reduce t_d, because the signal is filtered internal.
2.2.11	Temperature drift of delay time of output to magnetic edge	Δt_d	-6	3[7]	6	µs	Time over specified temperature range; not additional to t_d
2.2.12	Frequency range	f	0.001		8	kHz	Operation below 1Hz[8]
2.2.13	Oscillator frequency	f_{OSC}	1.08	1.34	1.68	MHz	-
2.2.14	Offset recalibration time after last output change	t_{reset}	625	780	970	ms	Output locked to state before recalibration
2.2.15	Clamping voltage V_S-Pin	V_{Sclamp}	24	27.5		V	I_S = 20mA < 5min.
2.2.16	Clamping voltage Q- Pin	V_{Qclamp}	24	27.5		V	I_Q = 20mA < 5min.
2.2.17	Analog reset voltage	V_{sReset}		2.35	2.9	V	-

Note: The listed AC/DC and magnetic characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not other specified, typical characteristics apply at T_j = 25 °C and V_S = 12 V.

2.3 Magnetic Characteristics in Running Mode

No.	Parameter	Symbol	min	typ	max	Unit	Remarks
2.3.1	Bias preinduction	B_0	-500		500	mT	-
2.3.2	Differential bias induction	ΔB_0	-30		30	mT	-
2.3.3	Minimum signal amplitude	$\lvert\Delta B_{min}\rvert$	0.55		1.5	mT	[9]
2.3.4	Maximum signal amplitude	$\lvert\Delta B_{max}\rvert$			100	mT	Additional to B_0 [10]
2.3.5	Resistivity against mechanical stress (piezo)	$\lvert\Delta B_{min}\rvert$	-0.2		0.2	mT	F= 2N

[5] see footnote 6.
[6] only valid for the falling edge.
[7] related to Tj= 175°C.
[8] output will switch if magnetic signal is changing more that 2x $\lvert\Delta B_{min}\rvert$ within offset recalibration time even below 1Hz once per magnetic edge
[9] includes also former B_m of TLE4941-2.
[10] exceeding this limit might result in decreased duty cycle performance. With higher values the internal measured signal will be clipped. This will decrease the phase accuracy.

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_j=25°C and the given supply voltage.

3.1 Self-calibration Characteristics

No.	Parameter	Symbol	min	typ	max	Unit	Remarks
3.1.1	No. of transitions for signal output at startup (startup mode)	n_{Start}			2	-	-
3.1.2	No. of transitions for entering running mode	n_{Calib}			7	-	Low accuracy of switching timing permitted
3.1.3	Duty cycle in running mode[11]	Dty	45[7]	50[7]	55[7]	%	ΔB_{PP} = 10mT ideal sinusoidal input signal (T_j=25°C)
			40[7]	50[7]	60[7]	%	ΔB_{PP} = 10mT ideal sinusoidal input signal (-40°C ≤ T_j < 175°C)
3.1.4	Signal jitter in running mode; 1 sigma value[7]	σ1		≤ ±0.11[12]		%	ΔB_{PP} = 10mT ideal sinusoidal input signal; T_j<150°C
		σ2		≤ ±0.16[8]		%	ΔB_{PP} = 10mT ideal sinusoidal input signal; 150°C ≤ T_j < 175°C
3.1.5	Signal Jitter in running mode at power supply of Vs=13V and ripple ±3V; 1 sigma value*	σ3		≤ ±0.11		%	ΔB_{PP} = 10mT ideal sinusoidal input signal; T_j<150°C

[11] this corresponds to a ΔB_0 = 0mT (magnetic offset).
[12] typical half value of TLE4941-2 performance (depends largely on $|\Delta B_{min}|$ and also on f).

3.1.6	Effective noise value of the magnetic switching points	B_{neff}		25		µT	T_j = 25°C; The magnetic noise is normal distributed, nearly independent to frequency and without sampling noise or digital noise effects. The effective value corresponds to 1σ probability of normal distribution. Consequently a 3σ value corresponds to 0.3% probability of appearance.
					70	µT	Typical value corresponds to 1σ. Max value corresponds to 1σ values in the full temperature range and include technological spreads.
3.1.7	Phase error in startup mode				≤ ±55	°	ΔB_{PP} = 10mT ideal sinusoidal input signal;[13]
3.1.8	Frequency distribution of signal jitter		Jitter shall be distributed like white noise				-

[13] smaller phase errors are possible at higher signal amplitudes, because sinus signal changes to a more rectangle signal.

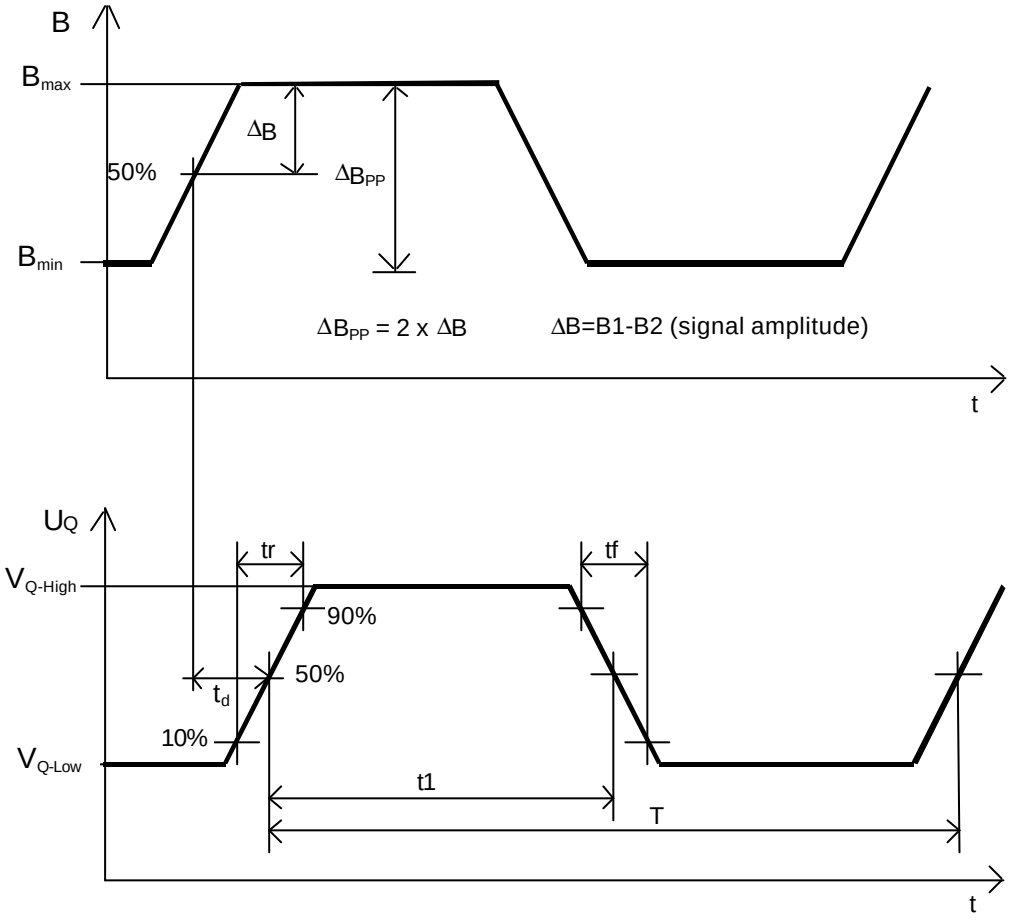
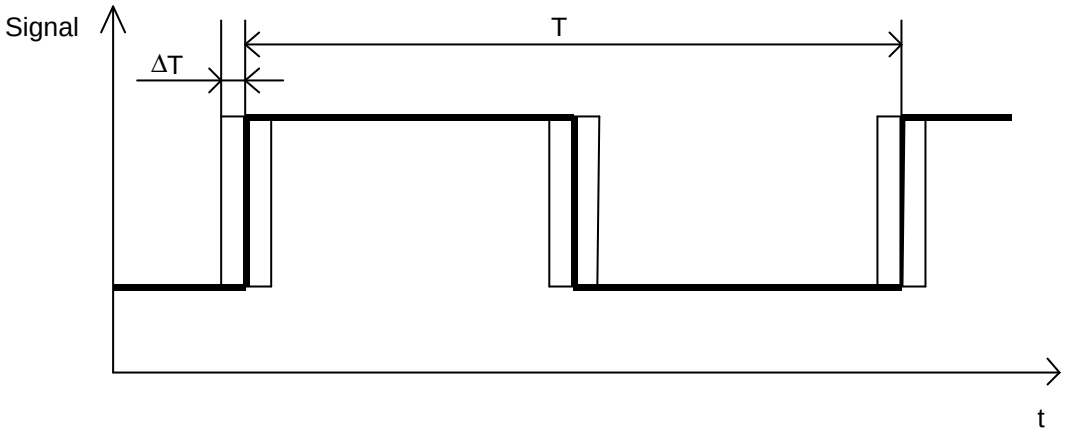


Figure 6 Switching direction



$$\sigma 1..\sigma 3 = \frac{1}{T} \cdot \sqrt{\frac{1}{(n-1)} \cdot \sum (\Delta T)^2}$$

measurement condition: n ≥ 1000

Figure 7 Definition of signal jitter

Application Configurations

Two possible applications are shown in **Figure 8** and **Figure 9** (Toothed and Magnet Wheel).

The difference between two-wire and three-wire application is shown in **Figure 12** for the TLE4925C and in **Figure 13** for the TLE4925.

Gear Tooth Sensing

In the case of ferromagnetic toothed wheel application the IC has to be biased by the south or north pole of a permanent magnet (e.g. $SmCO_5$ (Vacuumschmelze VX145)) with the dimensions 8 mm × 5 mm × 3 mm) which should cover both Hall probes.

The maximum air gap depends on

- the magnetic field strength (magnet used; pre-induction) and
- the toothed wheel that is used (dimensions, material, etc.; resulting differential field).

a centered distance of Hall probes
b Hall probes to IC surface
L IC surface to tooth wheel

a = 2.5 mm

b = 0.3 mm

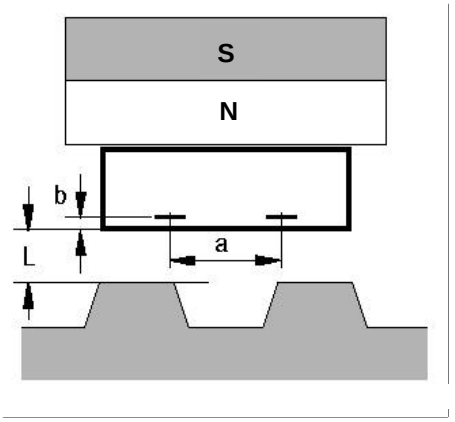
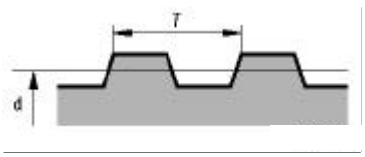


Figure 8 Sensor Spacing



Conversion DIN – ASA

m = 25.4 mm/p

T = 25.4 mm CP

DIN		ASA		
d	diameter (mm)	p	diameter pitch	$p = z/d$ (inch)
z	number of teeth	PD	pitch diameter	PD = z/p (inch)
m	module $m = d/z$ (mm)	CP	circular pitch	CP = 1 inch × π/p
T	pitch $T = \pi \times m$ (mm)			

Figure 9 Toothed Wheel Dimensions

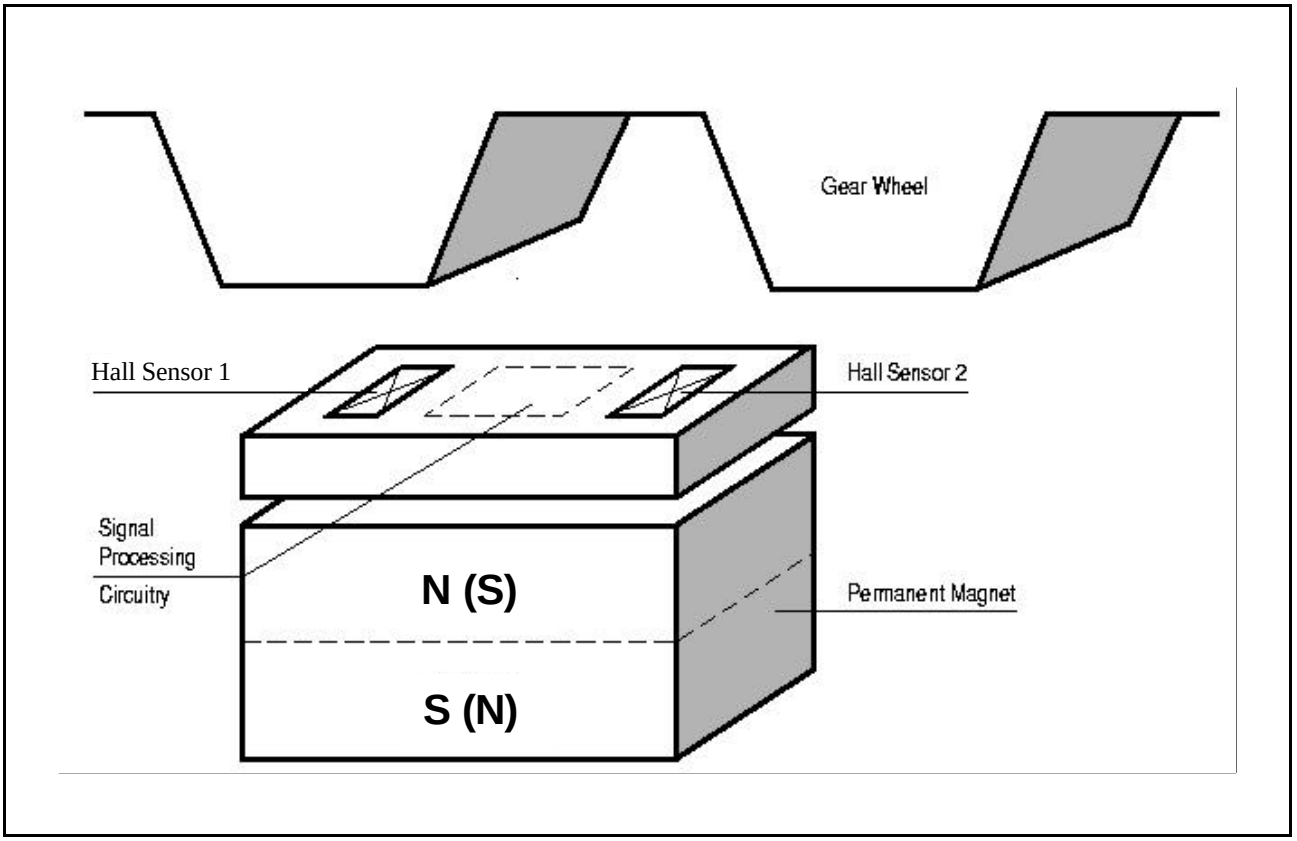


Figure 10 TLE4925/TLE 4925C, with Ferromagnetic Toothed Wheel

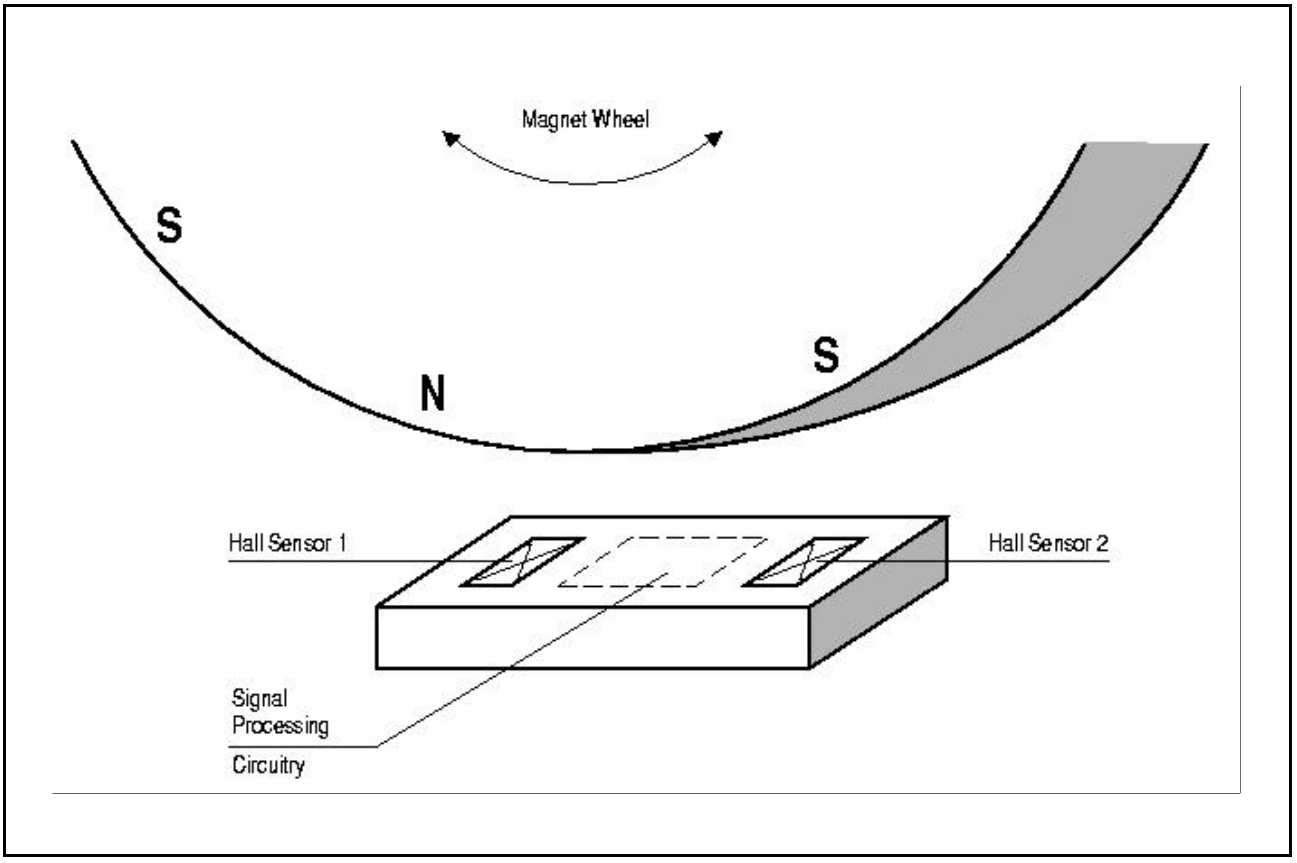
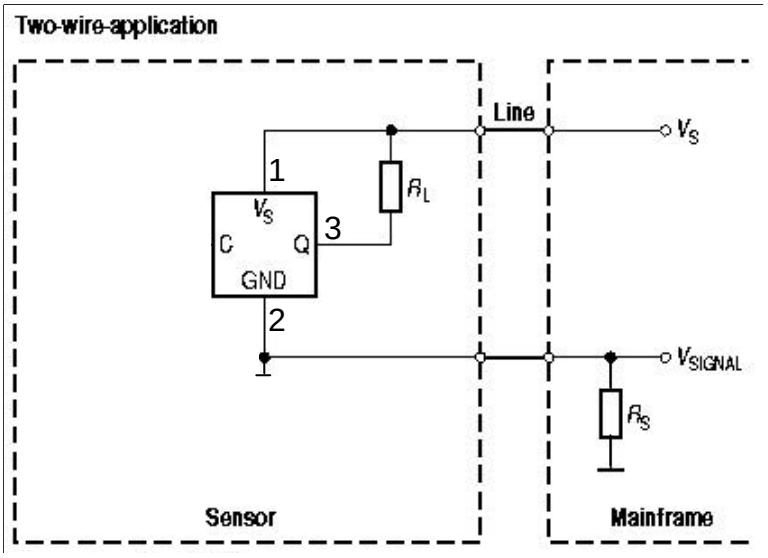
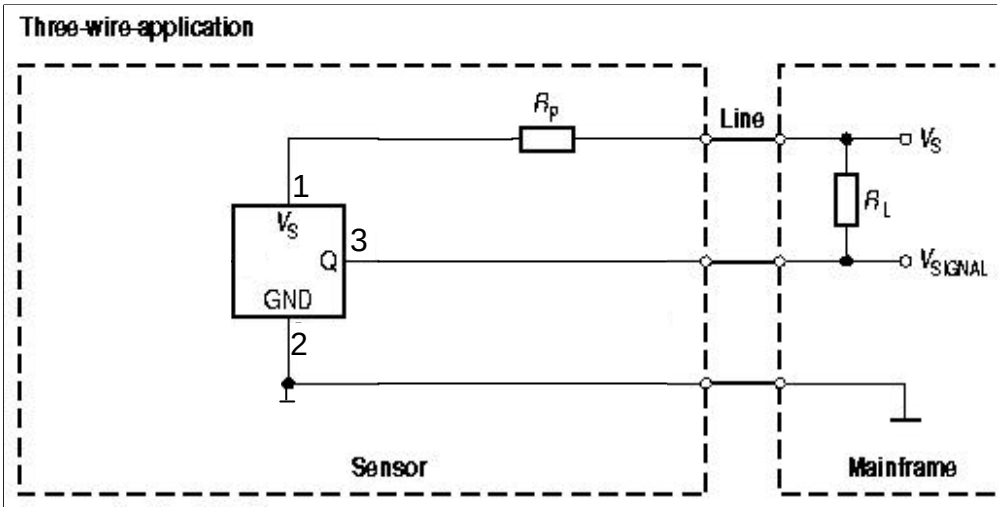


Figure 11 TLE4925/TLE 4925C, with Magnet Wheel

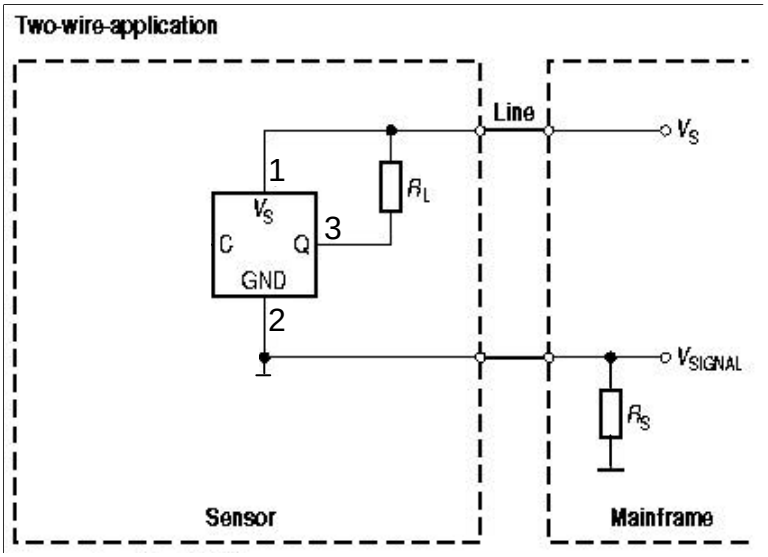


for example: R_L=1,2kΩ
R_S=120Ω

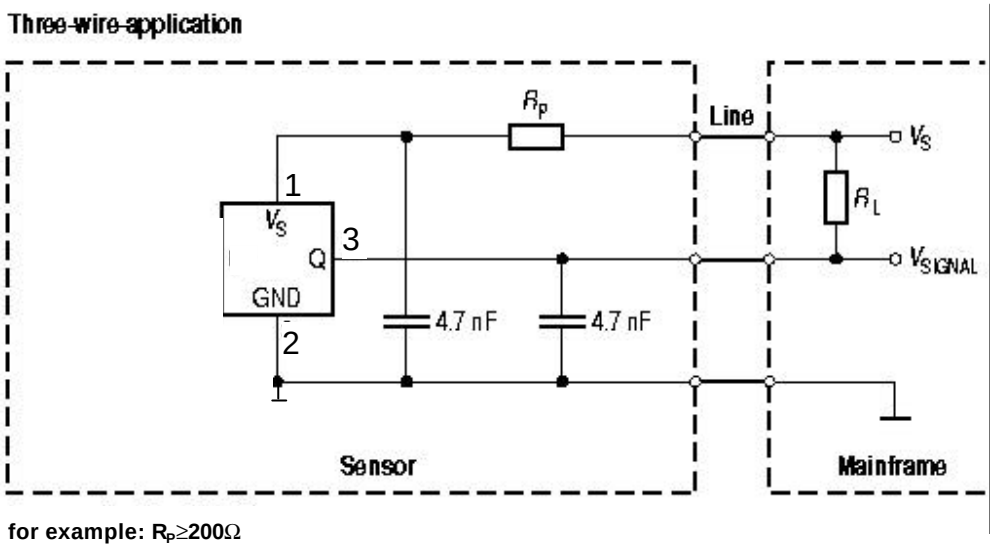


for example: R_P≥200Ω
R_L=1,2kΩ

Figure 12 Application Circuits TLE4925C

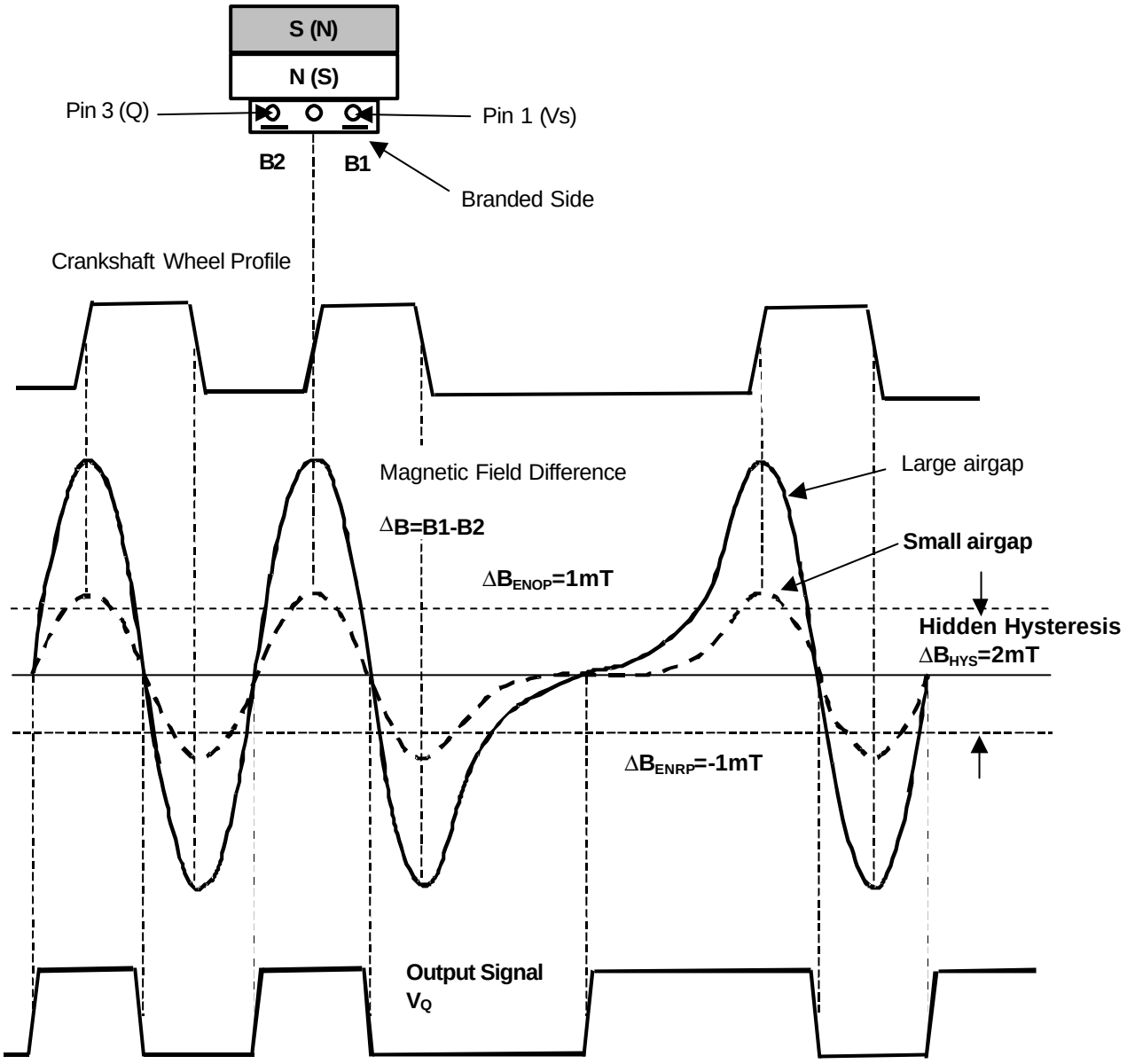


for example: R_L=1,2kΩ
R_S=120Ω



for example: R_P≥200Ω
R_L=1,2kΩ

Figure 13 Application Circuits TLE4925



Enabling point for releasing output: B1-B2>ΔB_{ENRP} switches the output OFF (V_Q=HIGH)
Enabling point for operate point: B1-B2<ΔB_{ENOP} switches the output ON (V_Q=LOW)
$\Delta B_{HYS}=|\Delta B_{ENOP}-\Delta B_{ENRP}|$
Outside of a permanent magnet the magnetic induction (=flux density) points from north to the south pole. It is common to define positive flux if the south pole of a magnet is on the branded side of the IC. This is equivalent to the north pole of the magnet on the rear side of the IC.

Figure 14 System Operation with hidden hysteresis

P-SSO-3-9
(**P**lastic **S**ingle **S**mall **O**utline)

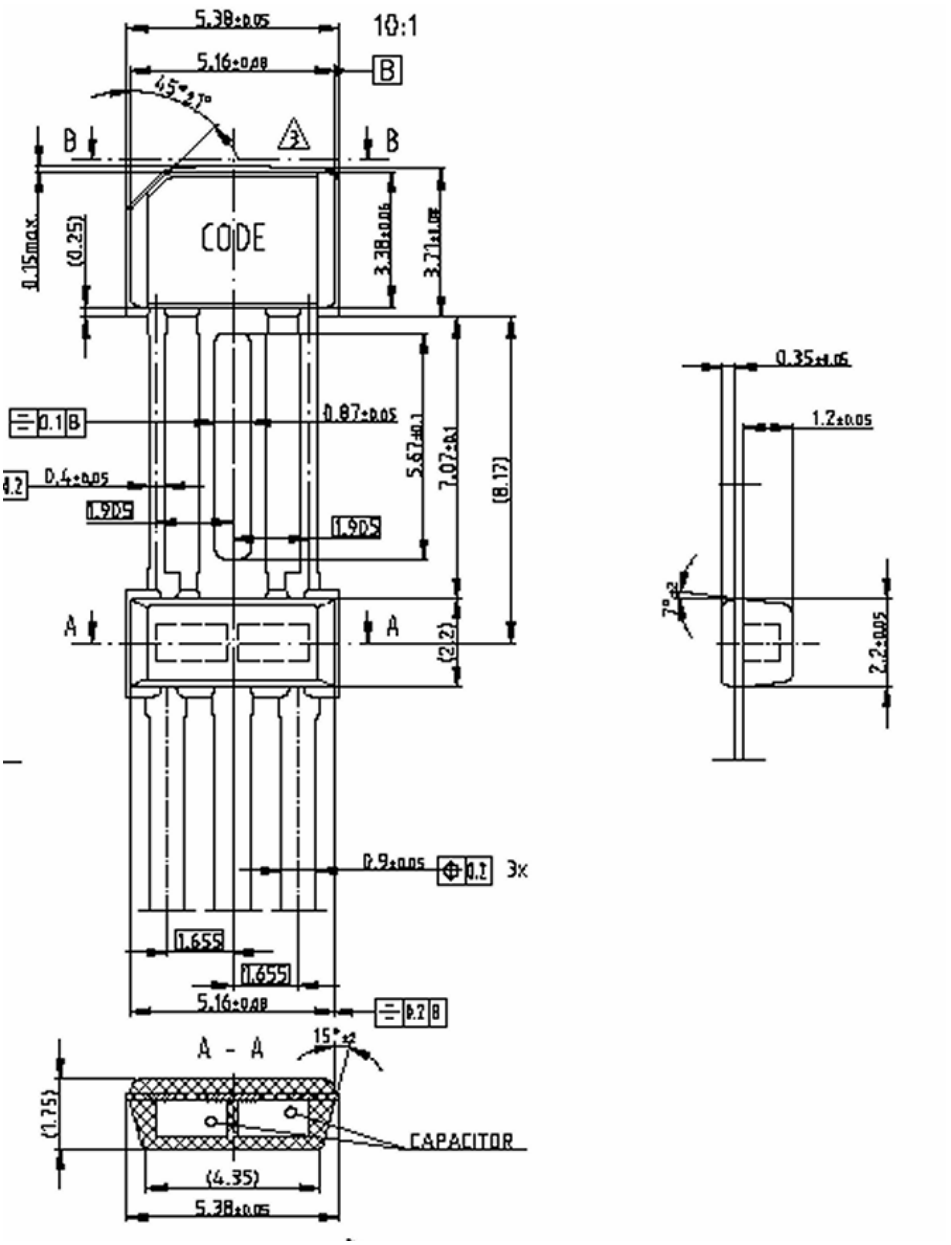


Figure 15 Package Dimensions (P-SSO-3-9)

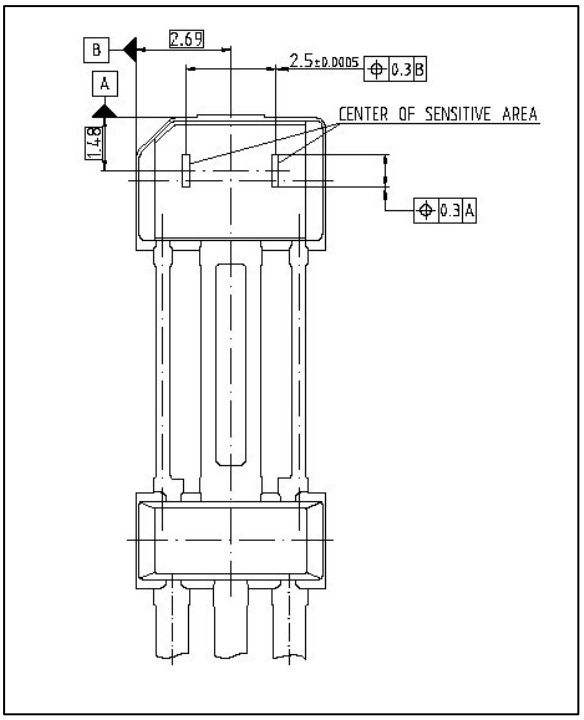


Figure 16 Hall probe spacing in the P-SSO-3-9 package

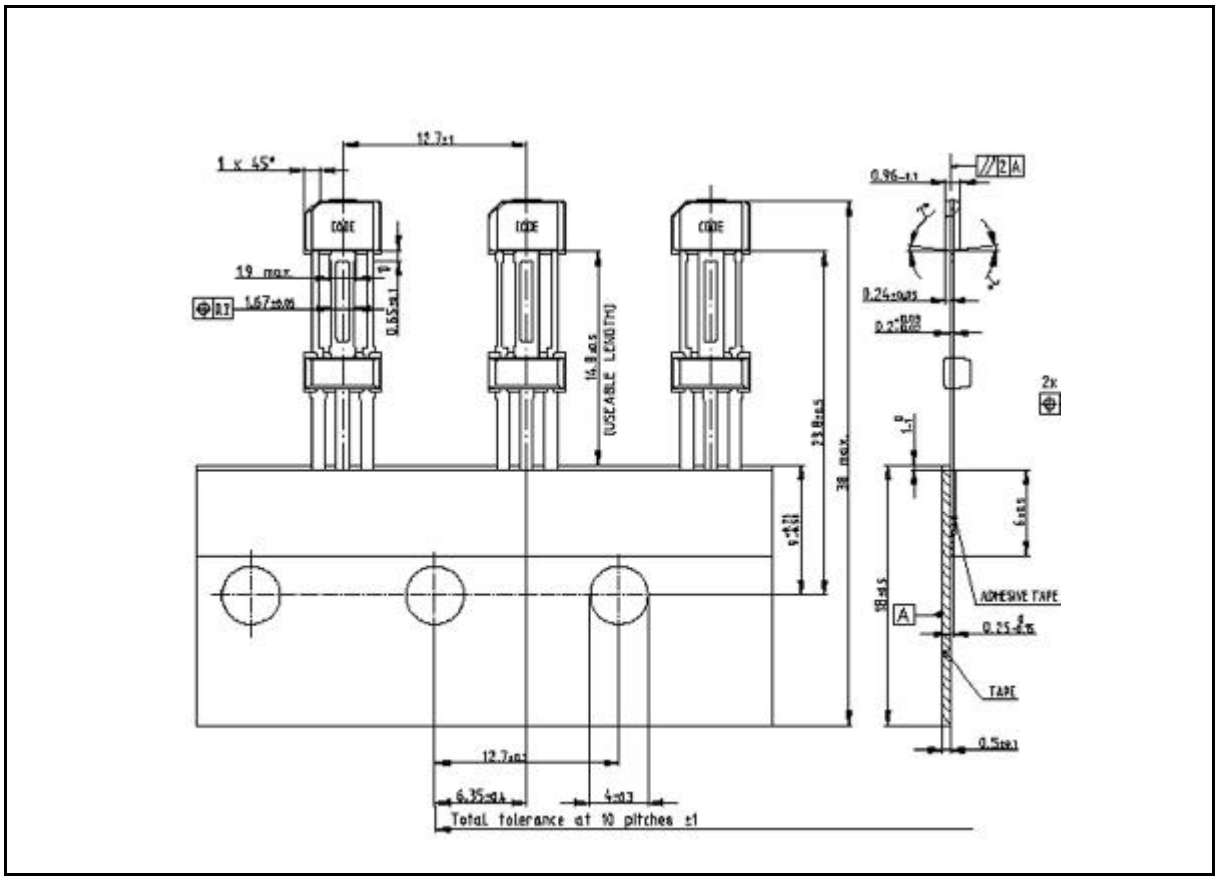


Figure 17 Tape Loading Orientation in the P-SSO-3-9 package

Package Outlines

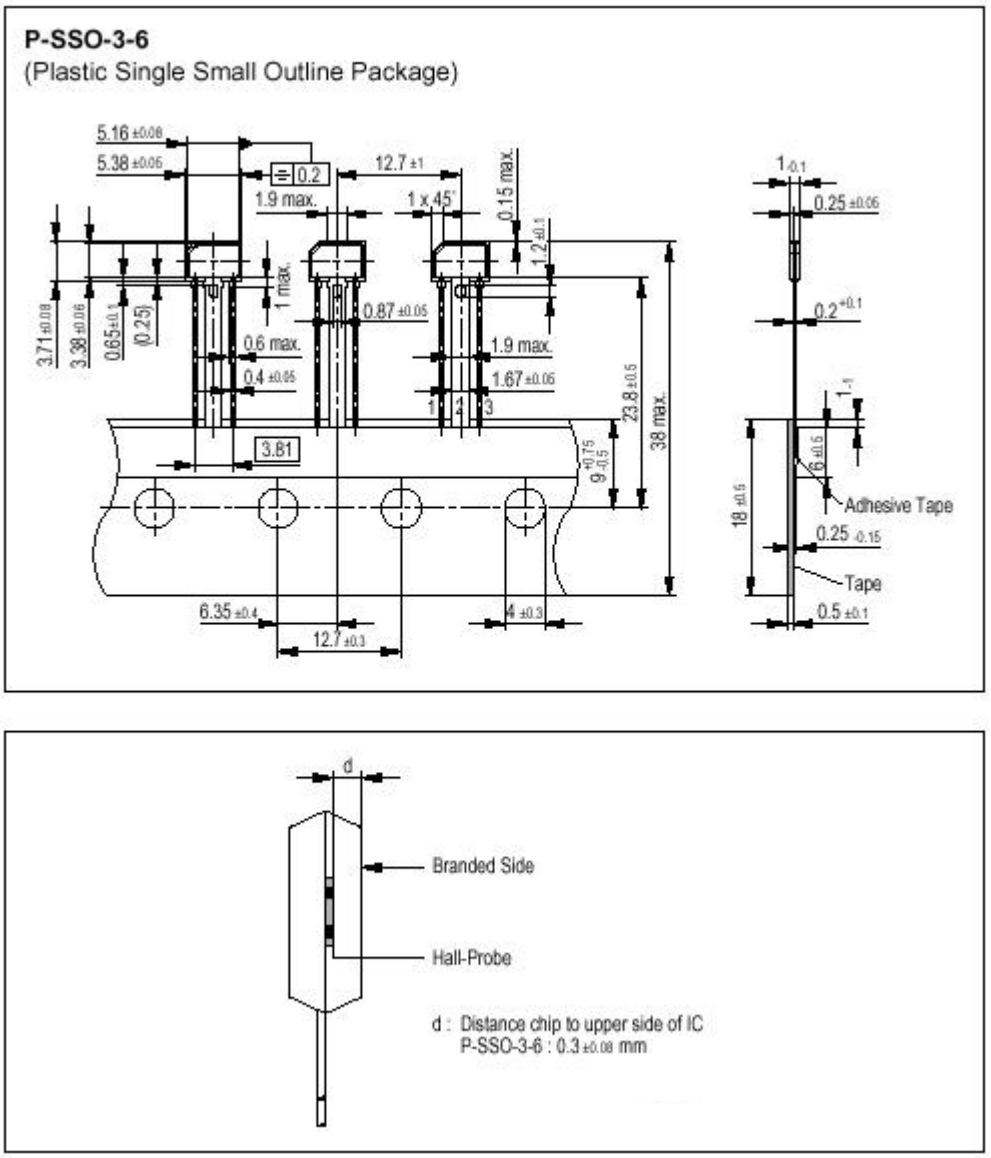


Figure 18 Tape Loading Orientation in the P-SSO-3-6 package

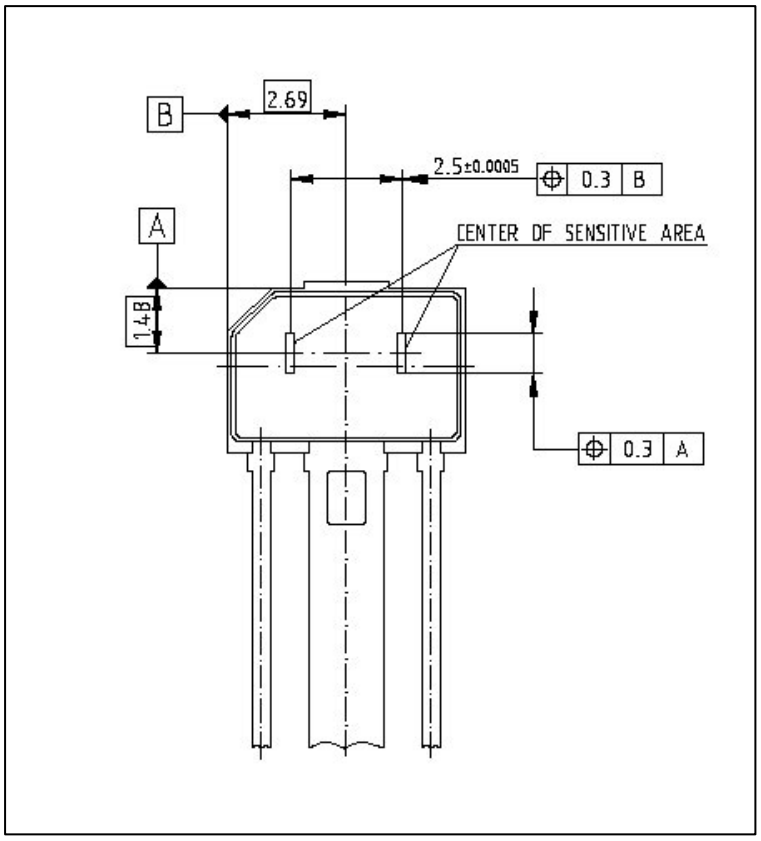


Figure 19 Hall probe spacing in the P-SSO-3-6 package

Appendix:

Calculation of mechanical errors:

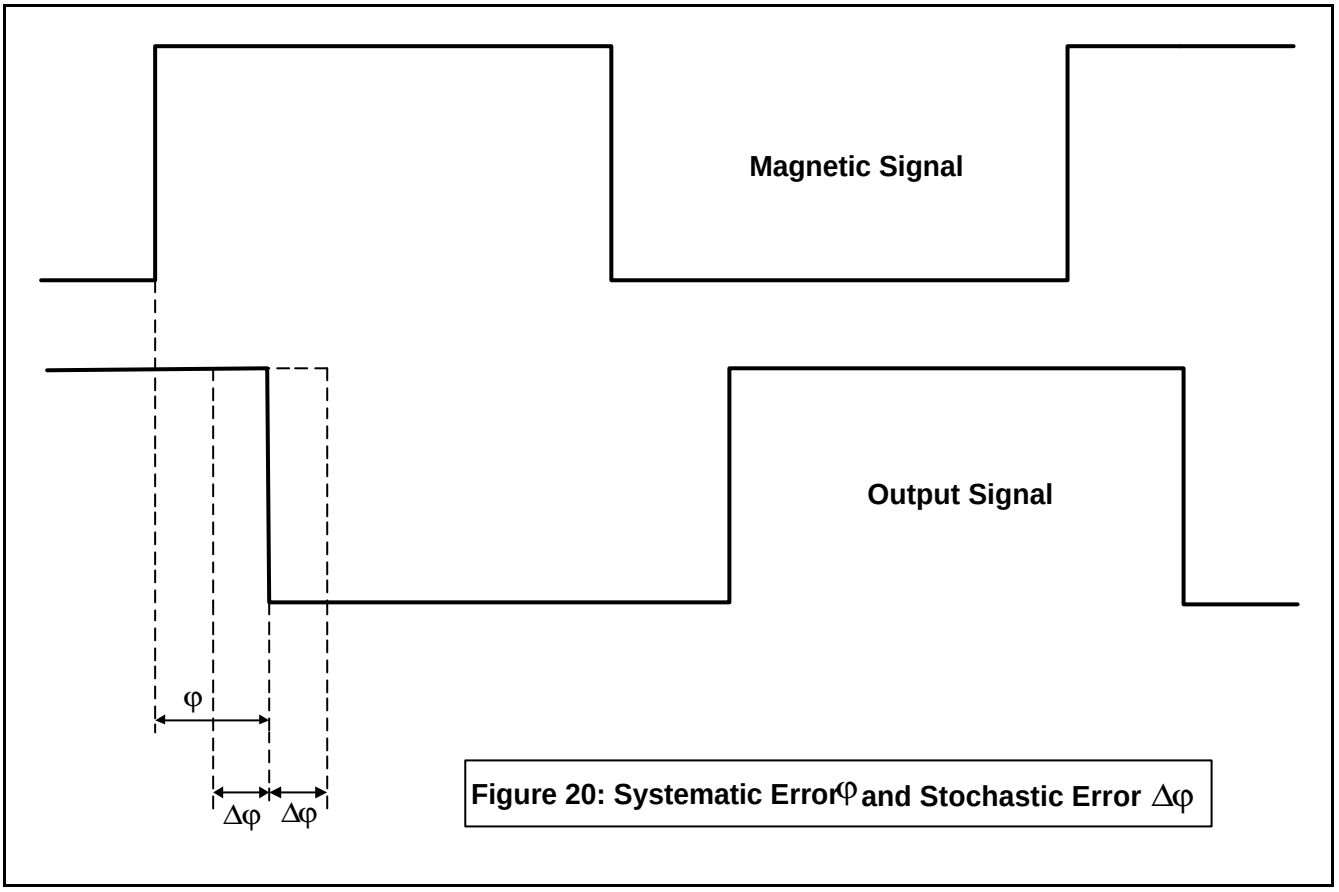


Figure 20: Systematic Error φ and Stochastic Error Δφ

Systematic Phase Error φ

The systematic error comes in because of the delay-time between the threshold point and the time when the output is switching. It can be calculated as follows:

$$\varphi = \frac{360° \bullet n}{60} \bullet t_d$$

φ ... systematic phase error in °
n ... speed of the camshaft-wheel in min^{-1}
t_d ... delay time (see specification) in *sec*

Stochastic Phase Error $\Delta\varphi$

The stochastic phase error includes the error due to the variation of the delay time with temperature and the error caused by the resolution of the threshold. It can be calculated in the following way:

$$\Delta\varphi_d = \frac{360^\circ \bullet n}{60} \bullet \Delta t_d$$

$\Delta\varphi_d$ ... stochastic phase error due to the variation of the delay time over temperature in °
n … speed of the camshaft wheel in *min*$^{-1}$
Δt_d … variation of delay time over temperature in *sec*

Jitter (Repeatability)

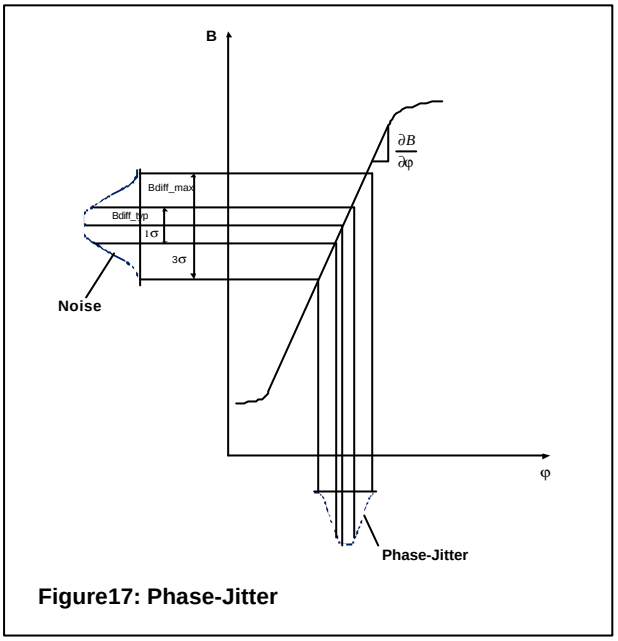


Figure17: Phase-Jitter

The phase jitter is normally caused by the analogue system noise. If there is an update of the offset-DAC due to the algorithm, what could happen after each tooth, then an additional step in the phase occurs (see description of the algorithm). This is not included in the following calculations. The noise is transformed through the slope of the magnetic edge into a phase error. The phase jitter is determined by the two formulas:

$$\varphi_{Jitter\_typ} = \frac{\partial\varphi}{\partial B} \bullet \left(B_{neff\_typ}\right)$$

$$\varphi_{Jitter\_\max} = \frac{\partial\varphi}{\partial B} \bullet \left(B_{neff\_\max}\right)$$

φ_{Jitter_typ}	…	typical phase jitter at Tj=25°C in ° (1Sigma)
φ_{Jitter_max}	…	maximum phase jitter at Tj=175°C in ° (3Sigma)
$\frac{\partial\varphi}{\partial B}$	…	inverse of the magnetic slope of the edge in °/*T*
B_{neff_typ}	…	typical value of B_{diff} in *T* (1σ-value at Tj=25°C)
B_{neff_max}	…	maximum value of B_{diff} in *T* (3σ-value at Tj=175°C)

Example:

Assumption:

$n = 4500\ min^{-1}$

$t_d = 14\ \mu s$

$\Delta t_d = \pm 3\ \mu s$

$\frac{\partial B}{\partial \varphi} = 3\ mT/°$

$B_{neff\_typ} = \pm 40\ \mu T$ (1σ-value at Tj=25°C)

$B_{neff\_max} = \pm 210\ \mu T$ (3σ-value at Tj=175°C)

Calculation:

φ	= 0.378°	…	systematic phase error
$\Delta\varphi_d$	= ±0.081°	…	stochastic phase error due to delay time variation
φ_{Jitter_typ}	= ±0.013°	…	typical phase jitter (1σ-value at Tj=25°C)
φ_{Jitter_max}	= ±0.07°	…	maximum phase jitter (3σ-value at Tj=175°C)