

DATA SHEET

TEA152x family **STARplug™**

Product specification
File under Integrated Circuits, IC11

2000 Sep 08

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TEA152x family

FEATURES

- Designed for general purpose supplies up to 50 W
- Integrated power switch:
 - TEA1520: 48 Ω ; 650 V
 - TEA1521: 24 Ω ; 650 V
 - TEA1522: 12 Ω ; 650 V
 - TEA1523: 6.5 Ω ; 650 V
 - TEA1524: 3.4 Ω ; 650 V.
- Operates from universal AC mains supplies (80 to 276 V)
- Adjustable frequency for flexible design
- RC oscillator for load insensitive regulation loop constant
- Valley switching for minimum switch-on loss (not implemented in TEA152xAJM versions)
- Frequency reduction at low power output makes low standby power possible (<100 mW)
- Adjustable overcurrent protection
- Under voltage protection
- Temperature protection
- Short circuit winding protection
- Simple application with both primary and secondary (opto) feedback
- Available in 8-pin DIP, 14-pin SO and 9-pin DBS packages.

GENERAL DESCRIPTION

The TEA152x family is a Switched Mode Power Supply (SMPS) controller IC that operates directly from the rectified universal mains. It is implemented in the high voltage EZ-HV SOI process, combined with a low voltage BICMOS process. The device includes a high voltage power switch and a circuit for start-up directly from the rectified mains voltage.

A dedicated circuit for valley switching is built in (not implemented in TEA152xAJM versions), which makes a very efficient slim-line electronic powerplug concept possible.

In its most basic version of application, the TEA152x family acts as a voltage source. Here, no additional secondary electronics are required. A combined voltage and current source can be realized with minimum costs for external components. Implementation of the TEA152x family renders an efficient and low cost power supply system.

Table 1 Available type numbers

R _{DS(on)}	DIP8	SO14	DBS9P
48 Ω	TEA1520P	TEA1520T	–
24 Ω	TEA1521P	TEA1521T	–
12 Ω	TEA1522P	TEA1522T	TEA1522AJM
6.5 Ω	TEA1523P	TEA1523T	TEA1523AJM
3.4 Ω	TEA1524P	–	TEA1524AJM

APPLICATIONS

Typical application areas for the STARplug™ are:

- Chargers
- Adapters
- STB (Set Top Box)
- DVD
- CD(R)
- TV/monitor standby supplies
- PC peripherals
- Microcontroller supplies in home applications and small portable equipment, etc.

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{\text{drain(max)}}$	maximum voltage at the DRAIN pin	$T_j > 0\text{ °C}$	–	–	650	V
$R_{\text{DS(on)}}$	drain-source on-state resistance of TEA1520	$T_j = 25\text{ °C}; I_{\text{source}} = -0.06\text{ A}$	–	48	55.2	Ω
		$T_j = 100\text{ °C}; I_{\text{source}} = -0.06\text{ A}$	–	68	78.2	Ω
	drain-source on-state resistance of TEA1521	$T_j = 25\text{ °C}; I_{\text{source}} = -0.125\text{ A}$	–	24	27.6	Ω
		$T_j = 100\text{ °C}; I_{\text{source}} = -0.125\text{ A}$	–	34	39.1	Ω
	drain-source on-state resistance of TEA1522	$T_j = 25\text{ °C}; I_{\text{source}} = -0.25\text{ A}$	–	12	13.8	Ω
		$T_j = 100\text{ °C}; I_{\text{source}} = -0.25\text{ A}$	–	17	19.6	Ω
	drain-source on-state resistance of TEA1523	$T_j = 25\text{ °C}; I_{\text{source}} = -0.5\text{ A}$	–	6.5	7.5	Ω
		$T_j = 100\text{ °C}; I_{\text{source}} = -0.5\text{ A}$	–	9.0	10.0	Ω
drain-source on-state resistance of TEA1524	$T_j = 25\text{ °C}; I_{\text{source}} = -1.0\text{ A}$	–	3.4	3.9	Ω	
	$T_j = 100\text{ °C}; I_{\text{source}} = -1.0\text{ A}$	–	4.8	5.5	Ω	
$V_{\text{CC(max)}}$	maximum supply voltage		–	–	40	V
f_{osc}	frequency range of oscillator		10	100	200	kHz
I_{drain}	supply current drawn from DRAIN pin	no auxiliary supply	–	1.5	–	mA
T_{amb}	ambient temperature		–20	–	+85	°C

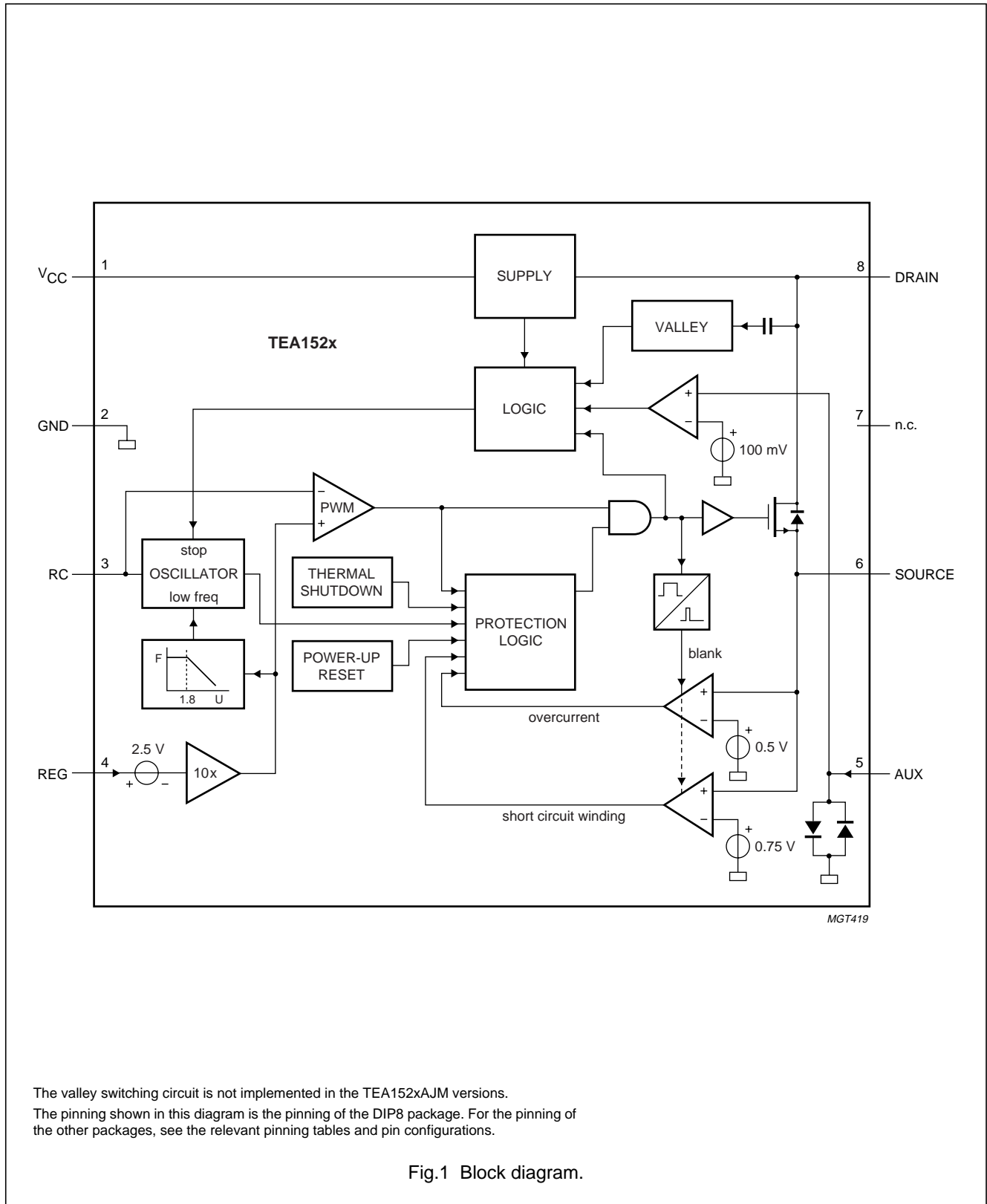
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA152xP	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
TEA152xT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TEA152xAJM	DBS9P	plastic DIL-bent-SIL power package; 9 leads (lead length 12/11 mm); exposed die pad	SOT523-1

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BLOCK DIAGRAM



The valley switching circuit is not implemented in the TEA152xAJM versions.
 The pinning shown in this diagram is the pinning of the DIP8 package. For the pinning of the other packages, see the relevant pinning tables and pin configurations.

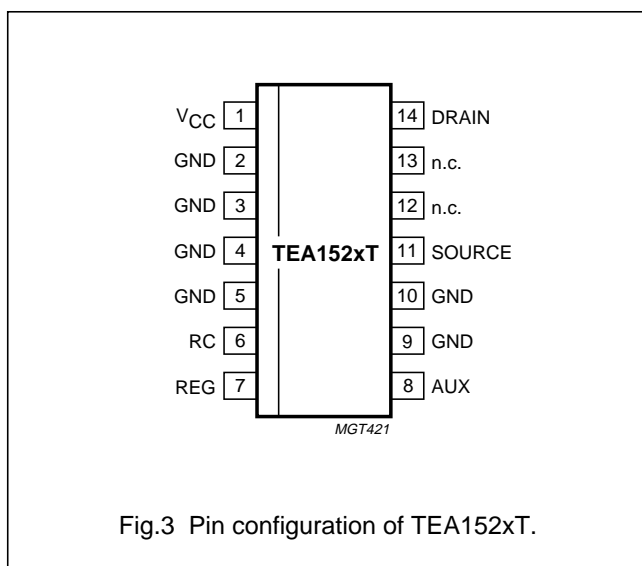
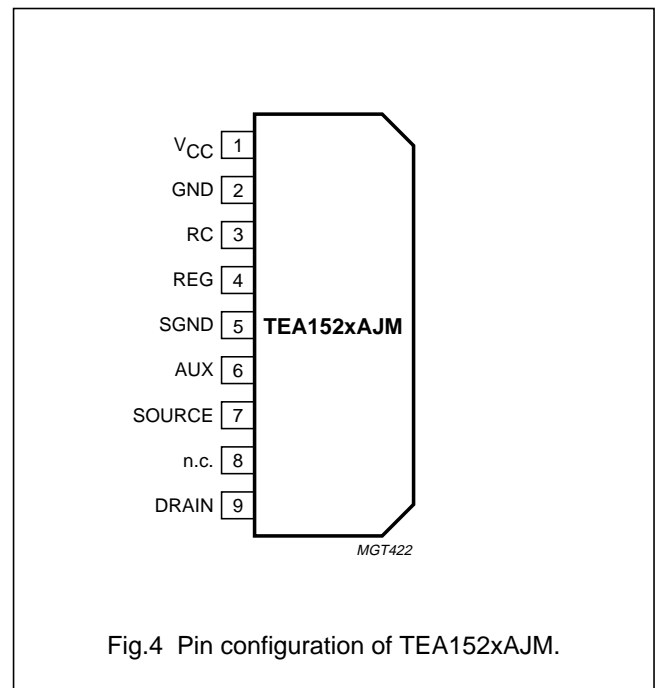
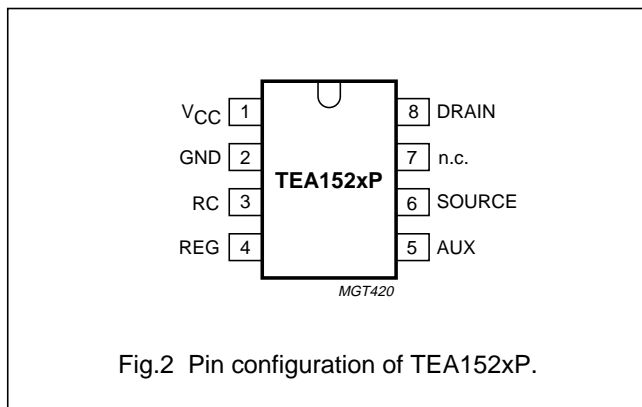
Fig.1 Block diagram.

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PINNING

SYMBOL	PIN			DESCRIPTION
	TEA152xP	TEA152xT	TEA152xAJM	
V _{CC}	1	1	1	supply voltage
GND	2	2, 3, 4, 5, 9 and 10	2	ground
RC	3	6	3	frequency setting
REG	4	7	4	regulation input
SGND	–	–	5	signal ground; connected to exposed die pad; must be connected to pin 2
AUX	5	8	6	input for voltage from auxiliary winding for timing (demagnetization)
SOURCE	6	11	7	source of internal MOS switch
n.c.	7	12 and 13	8	not connected
DRAIN	8	14	9	drain of internal MOS switch; input for start-up current and valley sensing



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FUNCTIONAL DESCRIPTION

The TEA152x family is the heart of a compact flyback converter, with the IC placed at the primary side. The auxiliary winding of the transformer can be used for indirect feedback to control the isolated output. This additional winding also powers the IC. A more accurate control of the output voltage and/or current can be implemented with an additional secondary sensing circuit and optocoupler feedback.

The TEA152x family uses voltage mode control. The frequency is determined by the maximum transformer demagnetizing time and the time of the oscillator. In the first case, the converter operates in the Self Oscillating Power Supply (SOPS) mode. In the latter case, it operates at a constant frequency, which can be adjusted with external components R_{RC} and C_{RC} . This mode is called Pulse Width Modulation (PWM). Furthermore, a primary stroke is started only in a valley of the secondary ringing. This valley switching principle minimizes capacitive switch-on losses.

Start-up and under voltage lock-out

Initially, the IC is self supplying from the rectified mains voltage. The IC starts switching as soon as the voltage on pin V_{CC} passes the $V_{CC(start)}$ level. The supply is taken over by the auxiliary winding of the transformer as soon as V_{CC} is high enough and the supply from the line is stopped for high efficiency operation.

When for some reason the auxiliary supply is not sufficient, the high voltage supply also supplies the IC. As soon as the voltage on pin V_{CC} drops below the $V_{CC(stop)}$ level, the IC stops switching and restarts from the rectified mains voltage.

Oscillator

The frequency of the oscillator is set by the external resistor and capacitor on pin RC. The external capacitor is charged rapidly to the $V_{RC(max)}$ level and, starting from a new primary stroke, it discharges to the $V_{RC(min)}$ level. Because the discharge is exponential, the relative sensitivity of the duty factor to the regulation voltage at low duty factor is almost equal to the sensitivity at high duty factors. This results in a more constant gain over the duty factor range compared to PWM systems with a linear sawtooth oscillator. Stable operation at low duty factors is easily realized. For high efficiency, the frequency is reduced as soon as the duty factor drops below a certain value. This is accomplished by increasing the oscillator charge time.

Duty factor control

The duty factor is controlled by the internal regulation voltage and the oscillator signal on pin RC. The internal regulation voltage is equal to the external regulation voltage (minus 2.5 V) multiplied by the gain of the error amplifier (typical 20 dB (10 ×)).

Valley switching (not implemented in TEA152xAJM versions)

A new cycle is started when the primary switch is switched on (see Fig.5). After a certain time (determined by the oscillator voltage RC and the internal regulation level), the switch is turned off and the secondary stroke starts. The internal regulation level is determined by the voltage on pin REG. After the secondary stroke, the drain voltage shows an oscillation with a frequency of approximately

$$\frac{1}{(2 \times \pi \times \sqrt{L_p \times C_p})}$$

where L_p is the primary self inductance and C_p is the parasitic capacitance on the drain node.

As soon as the oscillator voltage is high again and the secondary stroke has ended, the circuit waits for a low drain voltage before starting a new primary stroke. Figure 5 shows the drain voltage together with the valley signal, the signal indicating the secondary stroke and the RC voltage.

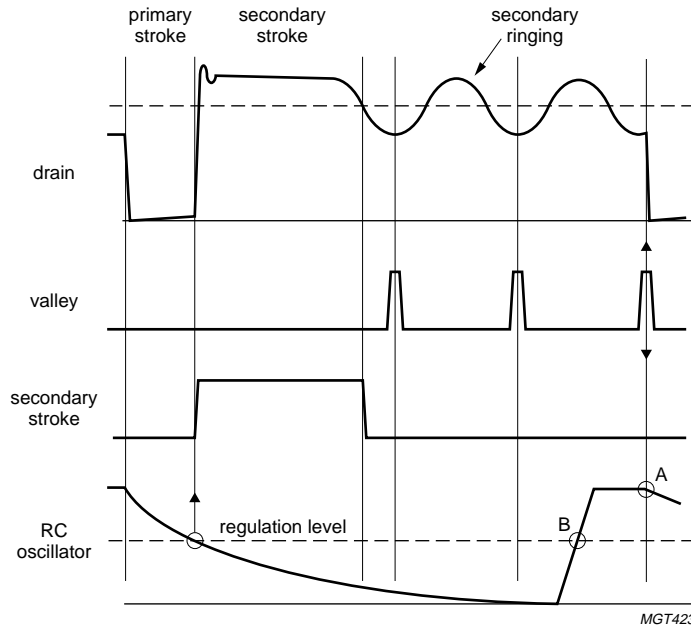
The primary stroke starts some time before the actual valley at low ringing frequencies, and some time after the actual valley at high ringing frequencies. Figure 6 shows a typical curve for a reflected output voltage $N \times V_o$ of 80 V. This voltage is the output voltage V_o (see Fig.7) transferred to the primary side of the transformer with the factor N (determined by the turns ratio of the transformer). Figure 6 shows that the system switches exactly at minimum drain voltage for ringing frequencies of 480 kHz, thus reducing the switch-on losses to a minimum. At 200 kHz, the next primary stroke is started at 33° before the valley. The switch-on losses are still reduced significantly.

Demagnetization

The system operates in discontinuous conduction mode all the time. As long as the secondary stroke has not ended, the oscillator will not start a new primary stroke. During the first t_{suppr} seconds, demagnetization recognition is suppressed. This suppression may be necessary in applications where the transformer has a large leakage inductance and at low output voltages.

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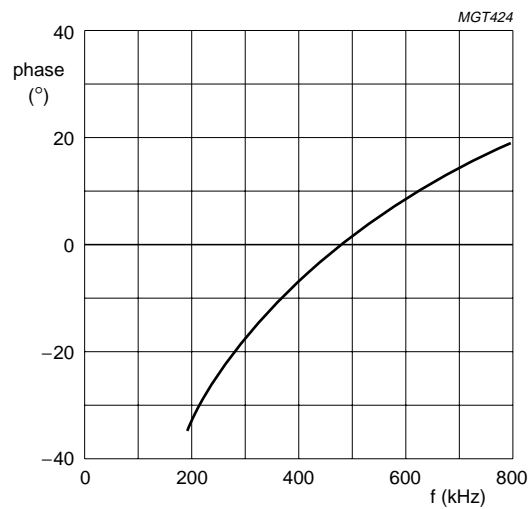
TEA152x family



MGT423

- A: Start of new cycle with valley switching.
- B: Start of new cycle in a classical PWM system.

Fig.5 Signals for valley switching.



MGT424

Fig.6 Typical phase of drain ringing at switch-on (at $N \times V_o = 80$ V).

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Minimum and maximum duty factor

The minimum duty factor of the switched mode power supply is 0%. The maximum duty factor is set to 75% (typical value at 100 kHz oscillation frequency).

Overcurrent protection

The cycle-by-cycle peak drain current limit circuit uses the external source resistor to measure the current. The circuit is activated after the leading edge blanking time t_{leb} . The protection circuit limits the source voltage to $V_{SRC(max)}$, and thus limits the primary peak current.

Short circuit winding protection

The short circuit winding protection circuit is also activated after the leading edge blanking time. If the source voltage exceeds the short circuit winding protection voltage V_{swp} , the IC stops switching. Only a Power-on reset will restart normal operation. The short circuit winding protection also protects in case of a secondary diode short circuit.

Overtemperature protection

An accurate temperature protection is provided in the device. When the junction temperature exceeds the thermal shutdown temperature, the IC stops switching. During thermal protection, the IC current is lowered to the start-up current. The IC continues normal operation as soon as the overtemperature situation has disappeared.

Overvoltage protection

Overvoltage protection can be achieved in the application by pulling pin REG above its normal operation level. The current primary stroke is terminated immediately, and no new primary stroke is started until the voltage on pin REG drops to its normal operation level. Pin REG has an internal clamp. The current feed into this pin must be limited.

Output characteristics of complete powerplug

OUTPUT POWER

A wide range of output power levels can be handled by choosing the $R_{DS(on)}$ and package of the TEA152x family. Power levels up to 50 W can be realised.

ACCURACY

The accuracy of the complete converter, functioning as a voltage source with primary sensing, is approximately 8% (mainly dependent on the transformer coupling). The accuracy with secondary sensing is defined by the accuracy of the external components. For safety requirements in case of optocoupler feedback loss, the primary sensing remains active when an overvoltage circuit is connected.

EFFICIENCY

An efficiency of 75% at maximum output power can be achieved for a complete converter designed for universal mains.

RIPPLE

A minimum ripple is obtained in a system designed for a maximum duty factor of 50% under normal operating conditions, and a minimized dead time. The magnitude of the ripple in the output voltage is determined by the frequency and duty factor of the converter, the output current level and the value and ESR of the output capacitor.

Input characteristics of complete powerplug

INPUT VOLTAGE

The input voltage range comprises the universal AC mains (80 to 276 V).

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are measured with respect to ground; positive currents flow into the device; pins V_{CC} and RC are not allowed to be current driven, pins REG and AUX are not allowed to be voltage driven.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Voltages					
V_{CC}	low supply voltage	continuous	-0.4	+40	V
V_{RC}	oscillator input voltage		-0.4	+3	V
V_{source}	source of the DMOS power transistor voltage		-0.4	+5	V
V_{drain}	drain of the DMOS power transistor voltage		-0.4	+650	V
Currents					
I_{REG}	regulation input current		-	6	mA
I_{AUX}	auxiliary winding input current		-10	+5	mA
I_{source}	source current of				
	TEA1520		-0.25	+0.25	A
	TEA1521		-0.5	+0.5	A
	TEA1522		-1	+1	A
	TEA1523		-2	+2	A
I_{drain}	drain current of				
	TEA1520		-0.25	+0.25	A
	TEA1521		-0.5	+0.5	A
	TEA1522		-1	+1	A
	TEA1523		-2	+2	A
I_{drain}	TEA1524		-3	+3	A
General					
P_{tot}	total power dissipation				
	TEA152xP	$T_{amb} < 45\text{ °C}$	-	1.0	W
	TEA152xT	$T_{amb} < 50\text{ °C}$	-	1.0	W
	TEA152xAJM	$T_{amb} < 45\text{ °C without heatsink}$	-	1.5	W
T_{stg}	storage temperature		-55	+150	°C
T_{amb}	ambient temperature		-20	+85	°C
T_j	junction temperature		-20	+145	°C
V_{esd}	electrostatic discharge voltage	human body model; note 1	-	2500	V
		machine model; note 2	-	200	V

Notes

- Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 k Ω series resistor. All pins are 2500 V maximum, except pin DRAIN, which is 1000 V maximum.
- Machine model: equivalent to discharging a 200 pF capacitor through a 0.75 μ H coil and a 10 Ω series resistor.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	note 1		
	TEA152xP	in free air	100	K/W
	TEA152xT	in free air	91	K/W
	TEA152xAJM	in free air	65	K/W

Note

1. Thermal resistance $R_{th(j-a)}$ can be lower when the GND pins are connected to sufficient copper area on the printed-circuit board. See the TEA152x application notes for details.

QUALITY SPECIFICATION

In accordance with "SNW-FQ-611 part E".

CHARACTERISTICS

$T_{amb} = 25\text{ °C}$; no overtemperature; all voltages are measured with respect to ground; currents are positive when flowing into the IC; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$I_{CC(operate)}$	supply current	normal operation	–	1.3	1.9	mA
$I_{CC(startup)}$	start-up supply current	start-up	–	180	400	μA
I_{drain}	supply current drawn from DRAIN pin	no auxiliary supply; $V_{drain} > 60\text{ V}$	–	1.5	2	mA
		with auxiliary supply; $V_{drain} > 60\text{ V}$	–	30	125	μA
$I_{CC(ch)}$	V_{CC} pin charging current	$V_{drain} > 60\text{ V}$	–6	–4	–3	mA
$V_{CC(start)}$	V_{CC} start voltage		9	9.5	10	V
$V_{CC(stop)}$	V_{CC} stop voltage (under voltage lock-out)		7.0	7.5	8.0	V
Pulse width modulator						
δ_{min}	minimum duty factor		–	0	–	%
δ_{max}	maximum duty factor	$f = 100\text{ kHz}$	–	75	–	%
SOPS						
V_{demag}	demagnetization recognition voltage level		50	100	150	mV
t_{suppr}	suppression of transformer ringing at start of secondary stroke		1.0	1.5	2.0	μs
RC oscillator						
$V_{RC(min)}$	minimum voltage of RC oscillator setting		60	75	90	mV
$V_{RC(max)}$	maximum voltage of RC oscillator setting		2.4	2.5	2.6	V
$t_{RC(ch)}$	RC charging time		–	1	–	μs
f_{osc}	frequency range of oscillator		10	100	200	kHz

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Duty factor regulator (pin REG)						
V_{REG}	input voltage		2.4	2.5	2.6	V
$G_{V(\text{erroramp})}$	voltage gain of error amplifier		–	20	–	dB
$V_{REG(\text{clamp})}$	clamping voltage at pin REG	$I_{REG} = 6 \text{ mA}$	–	–	7.5	V
Valley switching (not implemented in TEA152xAJM versions)						
dV/dt_{valley}	dV/dt for valley recognition		–102	–	102	V/ μs
f_{valley}	ringing frequency for valley switching	$N \times V_o = 100 \text{ V}$	200	550	800	kHz
$t_{d(\text{valley-swon})}$	delay from valley recognition to switch-on		–	150	–	ns
Current and short circuit winding protection						
$V_{\text{source(max)}}$	maximum source voltage	$dV/dt = 0.1 \text{ V}/\mu\text{s}$	0.47	0.50	0.53	V
$t_{d(\text{propagation})}$	delay from detecting $V_{\text{SRC(max)}}$ to switch-off	$dV/dt = 0.5 \text{ V}/\mu\text{s}$	–	160	185	ns
V_{swp}	short circuit winding protection voltage	$dV/dt = 0.5 \text{ V}/\mu\text{s}$	0.7	0.75	0.8	V
t_{leb}	blanking time for current and short circuit winding protection		250	350	450	ns
Output stage (FET)						
$I_{L(\text{drain})}$	drain leakage current	$V_{\text{drain}} = 650 \text{ V}$	–	–	125	μA
$V_{(\text{BR})\text{drain}}$	drain breakdown voltage	$T_j > 0 \text{ }^\circ\text{C}$	650	–	–	V
$R_{\text{DS(on)}}$	drain-source on-state resistance of TEA1520	$T_j = 25 \text{ }^\circ\text{C}; I_{\text{source}} = -0.06 \text{ A}$	–	48	55.2	Ω
		$T_j = 100 \text{ }^\circ\text{C}; I_{\text{source}} = -0.06 \text{ A}$	–	68	78.2	Ω
	drain-source on-state resistance of TEA1521	$T_j = 25 \text{ }^\circ\text{C}; I_{\text{source}} = -0.125 \text{ A}$	–	24	27.6	Ω
		$T_j = 100 \text{ }^\circ\text{C}; I_{\text{source}} = -0.125 \text{ A}$	–	34	39.1	Ω
	drain-source on-state resistance of TEA1522	$T_j = 25 \text{ }^\circ\text{C}; I_{\text{source}} = -0.25 \text{ A}$	–	12	13.8	Ω
		$T_j = 100 \text{ }^\circ\text{C}; I_{\text{source}} = -0.25 \text{ A}$	–	17	19.6	Ω
	drain-source on-state resistance of TEA1523	$T_j = 25 \text{ }^\circ\text{C}; I_{\text{source}} = -0.5 \text{ A}$	–	6.5	7.5	Ω
		$T_j = 100 \text{ }^\circ\text{C}; I_{\text{source}} = -0.5 \text{ A}$	–	9.0	10.0	Ω
drain-source on-state resistance of TEA1524	$T_j = 25 \text{ }^\circ\text{C}; I_{\text{source}} = -1.0 \text{ A}$	–	3.4	3.9	Ω	
	$T_j = 100 \text{ }^\circ\text{C}; I_{\text{source}} = -1.0 \text{ A}$	–	4.8	5.5	Ω	
$t_{\text{drain(f)}}$	drain fall time	$V_i = 300 \text{ V};$ no external capacitor at drain	–	75	–	ns
Temperature protection						
$T_{\text{prot(max)}}$	maximum temperature threshold		150	160	170	$^\circ\text{C}$
$T_{\text{prot(hys)}}$	hysteresis temperature		–	2	–	$^\circ\text{C}$

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APPLICATION INFORMATION

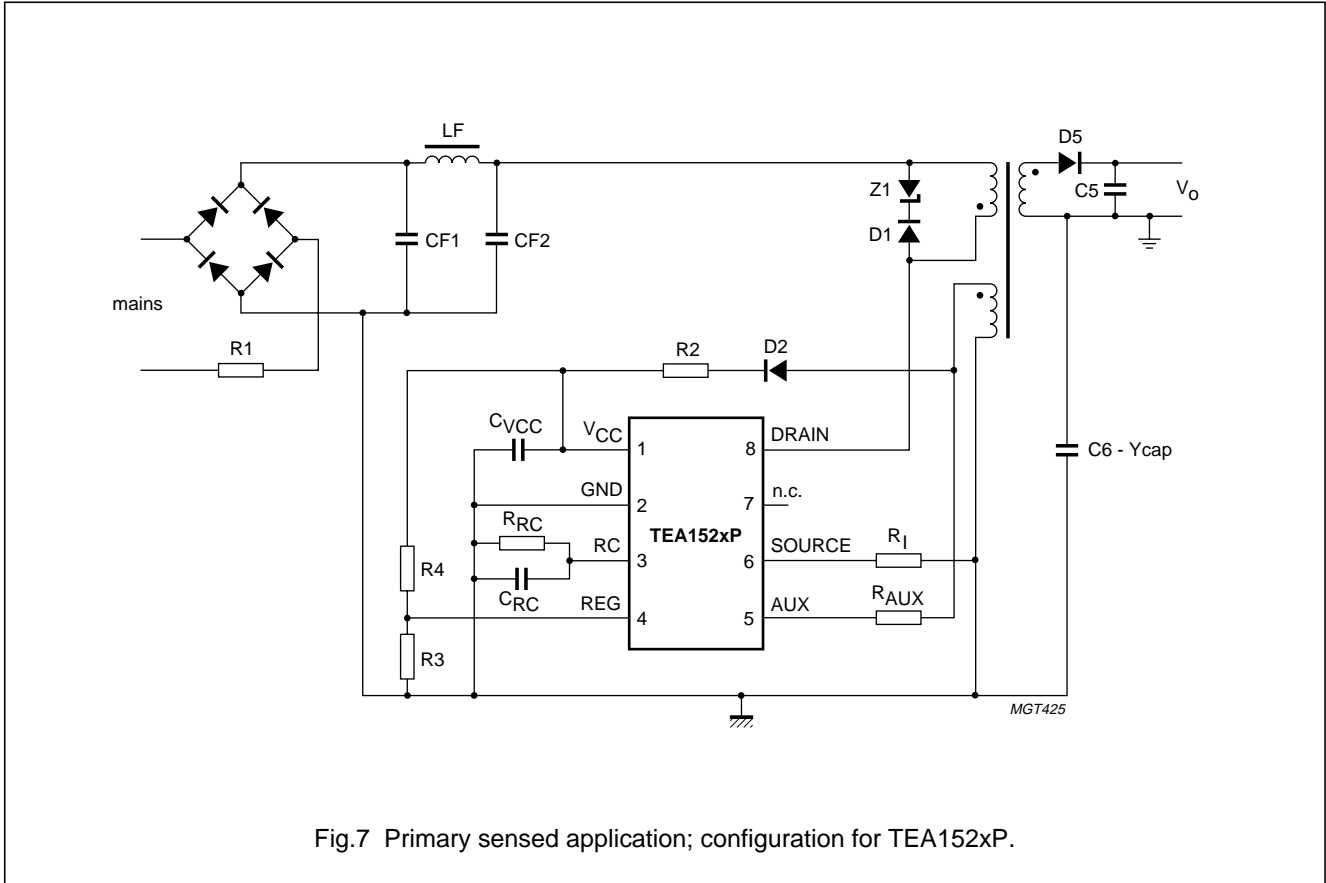


Fig.7 Primary sensed application; configuration for TEA152xP.

Further application information can be found in the TEA152x application notes.

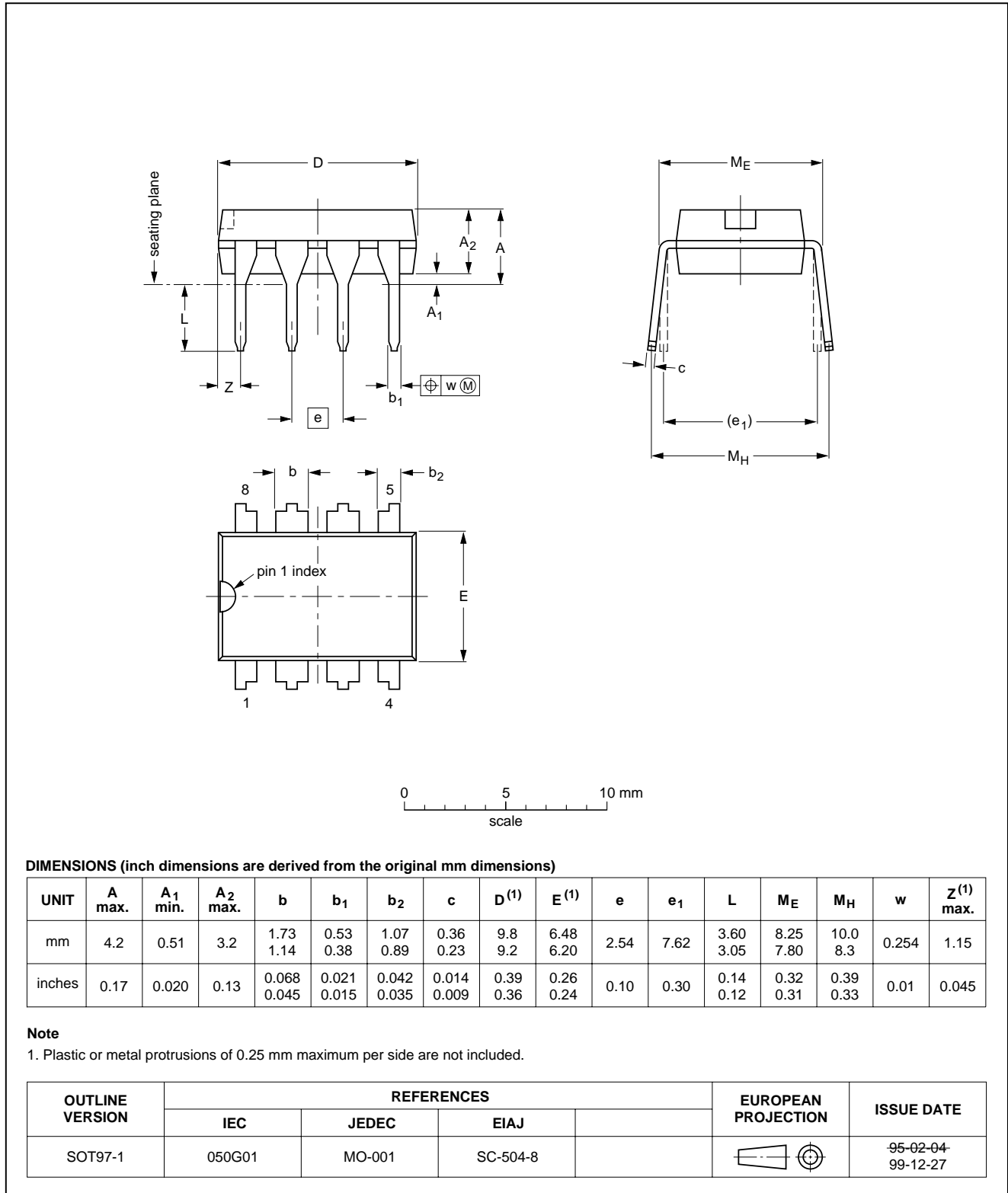
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PACKAGE OUTLINES

DIP8: plastic dual in-line package; 8 leads (300 mil)

SOT97-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

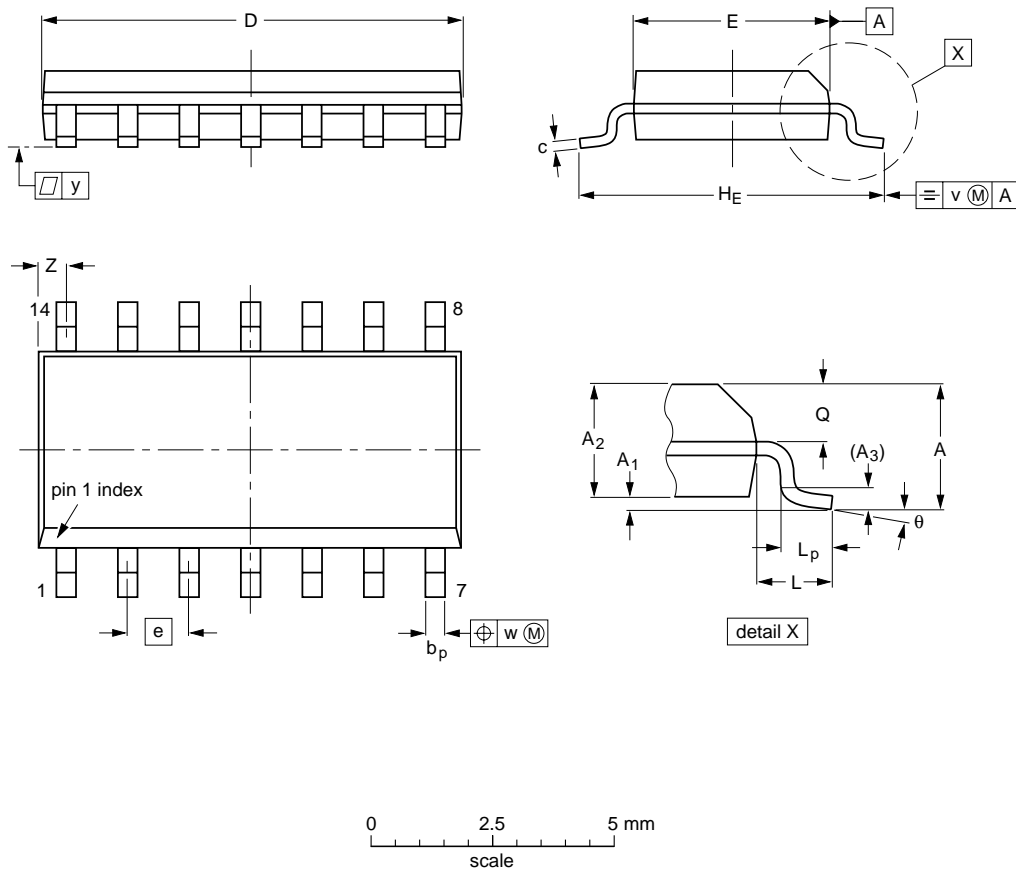
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT97-1	050G01	MO-001	SC-504-8		95-02-04 99-12-27

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

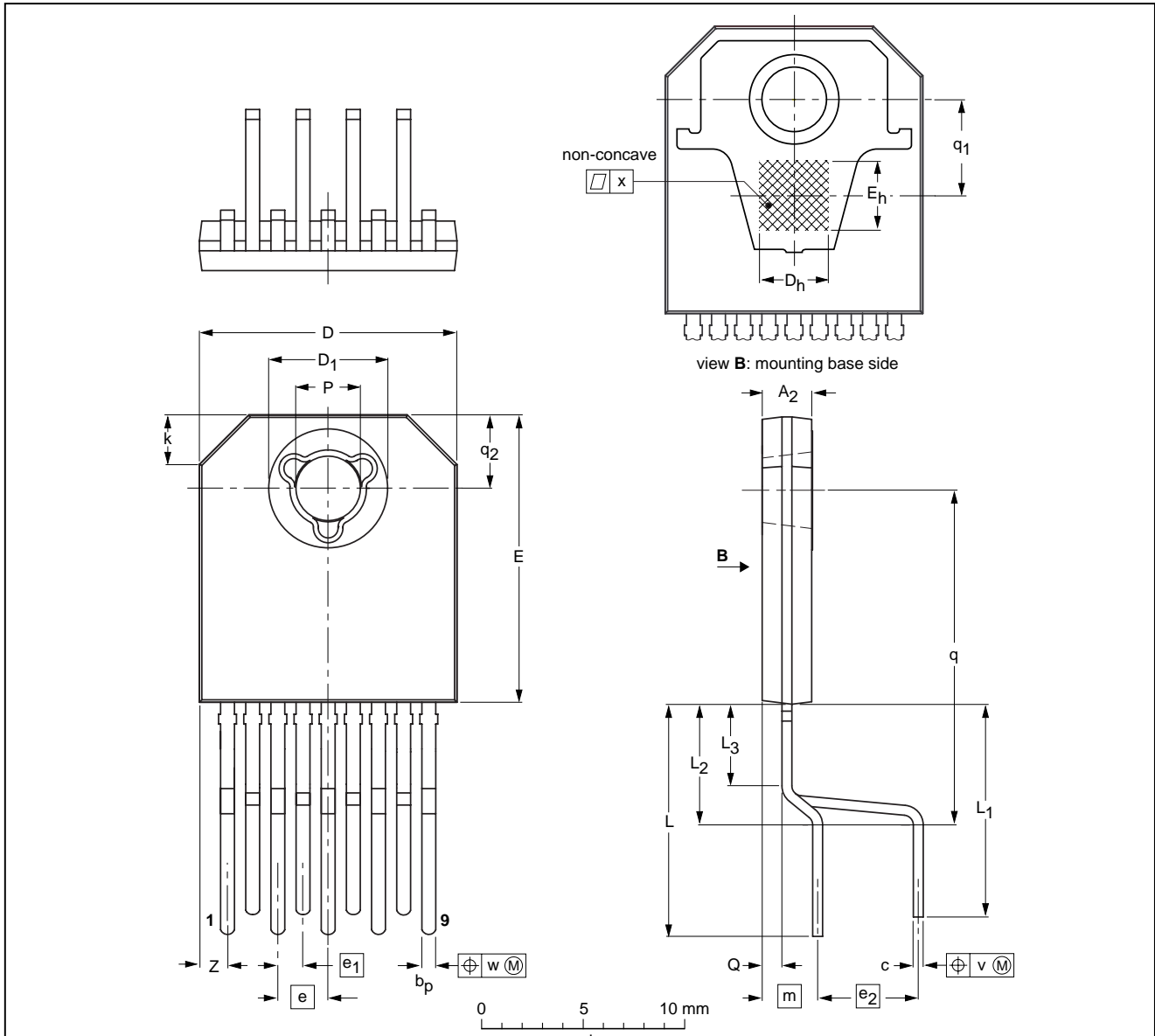
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	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				97-05-22 99-12-27

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DBS9P: plastic DIL-bent-SIL power package; 9 leads (lead length 12/11 mm); exposed die pad

SOT523-1



DIMENSIONS (mm are the original dimensions)

UNIT	A ₂ ⁽²⁾	b _p	c	D ⁽¹⁾	D ₁ ⁽²⁾	D _h	E ⁽¹⁾	E _h	e	e ₁	e ₂	k	L	L ₁	L ₂	L ₃	m	P	Q	q	q ₁	q ₂	v	w	x	z ⁽¹⁾
mm	2.7 2.3	0.80 0.65	0.58 0.48	13.2 12.8	6.2 5.8	3.5 3.5	14.7 14.3	3.5	2.54	1.27	5.08	3.0 2.0	12.4 11.0	11.4 10.0	6.7 5.5	4.5 3.7	2.8	3.4 3.1	1.15 0.85	17.5 16.3	4.85	3.8 3.6	0.8	0.3	0.02	1.65 1.10

- Notes
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.
 2. Plastic surface within circle area D₁ may protrude 0.04 mm maximum.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT523-1						98-11-12-00-07-03

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SOLDERING

Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our “*Data Handbook IC26; Integrated Circuit Packages*” (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Through-hole mount packages

SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages

REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW ⁽¹⁾	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable ⁽²⁾	–	suitable
Surface mount	BGA, LFBGA, SQFP, TFBGA	not suitable	suitable	–
	HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable ⁽³⁾	suitable	–
	PLCC ⁽⁴⁾ , SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended ⁽⁴⁾⁽⁵⁾	suitable	–
	SSOP, TSSOP, VSO	not recommended ⁽⁶⁾	suitable	–

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
2. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
3. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS ⁽¹⁾
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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