19-3166; Rev 0; 1/04

MAXIM

3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers

MAX1447/MAX1496/MAX1498

General Description

The MAX1447/MAX1496/MAX1498 low-power, 3.5- and 4.5-digit, analog-to-digital converters (ADCs) with integrated light-emitting diode (LED) drivers operate from a single 2.7V to 5.25V power supply. They include an internal reference, a high-accuracy on-chip oscillator, and a multiplexed LED display driver. An internal charge pump generates the negative supply needed to power the integrated input buffers for single-supply operation. The ADC is configurable for either a ±2V or ±200mV input range and it outputs its conversion results to an LED. The MAX1496 is a 3.5-digit (±1999 count) device and the MAX1447/MAX1498 are 4.5-digit (±19,999 count) devices.

The MAX1447/MAX1496/MAX1498 do not require external precision integrating capacitors, autozero capacitors, crystal oscillators, charge pumps, or other circuitry required with dual-slope ADCs (commonly used in panel meter circuits).

These devices also feature on-chip buffers for the differential signal and reference input, allowing direct interface with high-impedance signal sources. In addition, they use continuous internal offset-calibration and offer >100dB rejection of 50Hz and 60Hz line noise. Other features include data hold and peak detection and overrange/underrange detection. The MAX1447 features on-demand enhanced offset calibration for improved offset performance.

The MAX1447/MAX1498 are available in a 32-pin, 7mm × 7mm TQFP package and the MAX1496 is available in 28-pin SSOP and 28-pin PDIP packages. All devices in this family operate over the -40°C to +85°C extended temperature range.

Applications

Digital Panel Meters

Hand-Held Meters

Digital Voltmeters

Digital Multimeters

Pin Configurations appear at end of data sheet.

Features

- **High Resolution**
  - **MAX1447/MAX1498: 4.5 Digits (±19,999 Count)**
  - **MAX1496: 3.5 Digits (±1999 Count)**
- **Sigma-Delta ADC Architecture**
  - **No Integrating Capacitors Required**
  - **No Autozeroing Capacitors Required**
  - **>100dB of Simultaneous 50Hz and 60Hz Rejection**
- **Selectable Input Range of ±200mV or ±2V**
- **Selectable Voltage Reference: Internal 2.048V or External**
- **Internal High-Accuracy Oscillator Needs No External Components**
- **Automatic Offset Calibration**
- **On-Demand Enhanced Offset Calibration (MAX1447)**
- **Operate from a Single 2.7V to 5.25V Supply**
- **Low Power (Exclude LED-Driver Current)**
  - **Maximum 744µA Operating Current (MAX1496)**
  - **Maximum 960µA Operating Current (MAX1447/MAX1498)**
  - **Maximum 325µA Shutdown Current**
- **Multiplexed Common-Cathode LED Drivers**
  - **Resistor-Programmable Segment Current**
- **Small 32-Pin, 7mm x 7mm TQFP Package (4.5 Digits), 28-Pin SSOP Package (3.5 Digits)**
- **Also Available in a PDIP Package (3.5 Digits)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	RESOLUTION (DIGITS)
MAX1447ECJ	-40°C to +85°C	32 TQFP	4.5
MAX1496EAI*	-40°C to +85°C	28 SSOP	3.5
MAX1496EPI	-40°C to +85°C	28 PDIP	3.5
MAX1498ECJ	-40°C to +85°C	32 TQFP	4.5

**Future product—contact factory for availability.*

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at

3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to GND (MAX1447/MAX1498) ....-0.3V to +6V
DV_{DD} to GND (MAX1447/MAX1498) ....-0.3V to +6V
AIN+, AIN- to GND
(MAX1447/MAX1498) ....VNEG to (AV_{DD} to +0.3V)
REF+, REF- to GND
(MAX1447/MAX1498) .... VNEG to (AV_{DD} to +0.3V)
INTREF, RANGE, DPSET1, DPSET2, HOLD, PEAK,
DPON to GND (MAX1447/MAX1498) ..-0.3V to (DV_{DD} + 0.3V)
VNEG to GND (MAX1447/MAX1498).......-2.6V to (AV_{DD} + 0.3V)
LED_EN to GND (MAX1447/MAX1498) ...-0.3V to (DV_{DD} + 0.3V)
ISET to GND (MAX1447/MAX1498) ....-0.3V to (AV_{DD} + 0.3V)
V_{DD} to GND (MAX1496)...-0.3V to +6V
AIN+, AIN- to GND (MAX1496).............VNEG to (V_{DD} to +0.3V)
REF+, REF- to GND (MAX1496) .... VNEG to (V_{DD} to +0.3V)
INTREF, RANGE, DPSET1, DPSET2, HOLD, PEAK,
DPON to GND (MAX1496) ....-0.3V to (V_{DD} + 0.3V)
VNEG to GND (MAX1496)..........................-2.6V to (V_{DD} + 0.3V)
ISET to GND (MAX1496) ....-0.3V to (V_{DD} + 0.3V)
VLED to GLED ....-0.3V to +6V
GLED to GND ....-0.3V to +0.3V
SEG_ to GLED...-0.3V to (VLED + 0.3V)
DIG_ to GLED ....-0.3V to (VLED + 0.3V)
DIG_ Sink Current 300mA
DIG_ Source Current..50mA
SEG_ Sink Current 50mA
SEG_ Source Current..50mA
Maximum Current Input into Any Other Pin 50mA
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFP (derate 20.7mW/°C above +70°C).....1652.9mW
28-Pin SSOP (derate 9.5mW/°C above +70°C) 762mW
28-Pin PDIP (derate 14.3mW/°C above +70°C)......1142.9mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature...+150°C
Storage Temperature Range ....-60°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = DV_{DD} = V_{DD} = +2.7V to +5.25V, GND = 0, V_{LED} = +2.7V to +5.25V, GLED = 0, V_{REF+} - V_{REF-} = 2.048V (external reference), C_{REF+} = C_{REF-} = 0.1µF, C_{VNEG} = 0.1µF. Internal clock mode, unless otherwise noted. All specifications are at T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Noise-Free Resolution		MAX1447/MAX1498	-19,999		+19,999	Counts
		MAX1496	-1999		+1999	
Integral Nonlinearity (Note 1)	INL	2.000V range		±1		Counts
		200mV range		±1		
Range Change Ratio		(V_{AIN+} - V_{AIN-} = 0.100V) on 200mV range (V_{AIN+} - V_{AIN-} = 0.100V) on 2.0V range		10:1		Ratio
Rollover Error		V_{AIN+} - V_{AIN-} = full scale V_{AIN-} - V_{AIN+} = full scale		±1		Counts
Output Noise				10		$µV_{P-P}$
Offset Error (Zero Input Reading)	Offset	V_{IN} = 0 (Note 2)	-0		0	Readings
Gain Error		(Note 3)	-0.5		+0.5	% FSR
Offset Drift (Zero Reading Drift)		V_{IN} = 0 (Note 4)		0.1		µV/°C
Gain Drift				±1		ppm/°C
INPUT CONVERSION RATE						
Conversion Rate				5		Hz

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = V_{DD} = +2.7V to +5.25V, GND = 0, V_{LED} = +2.7V to +5.25V, GLED = 0, V_{REF+} - V_{REF-} = 2.048V (external reference), C_{REF+} = C_{REF-} = 0.1µF, C_{VNEG} = 0.1µF. Internal clock mode, unless otherwise noted. All specifications are at T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUTS (AIN+, AIN-) (bypass to GND with 0.1µF or greater capacitors)						
AIN Input Voltage Range (Note 5)		RANGE = GND	-2.0		+2.0	V
		RANGE = DV_{DD} (MAX1447/MAX1498) or V_{DD} (MAX1496)	-0.2		+0.2	
AIN Absolute Input Voltage Range to GND			-2.2		+2.2	V
Normal-Mode 50Hz and 60Hz Rejection (Simultaneously)		50Hz and 60Hz ±2%		100		dB
Common-Mode 50Hz and 60Hz Rejection (Simultaneously)	CMR	For 50Hz and 60Hz ±2%, R_{SOURCE} < 10kΩ		150		dB
Common-Mode Rejection	CMR	At DC		100		dB
Input Leakage Current				10		nA
Input Capacitance				10		pF
Average Dynamic Input Current		(Note 6)	-20		+20	nA
INTERNAL REFERENCE (REF- = GND, INTREF = DV_{DD} (MAX1447/MAX1498) or V_{DD} (MAX1496) (bypass REF+ to GND with a 4.7µF capacitor)						
REF Output Voltage	V_{REF}		2.007	2.048	2.089	V
REF Output Short-Circuit Current				1		mA
REF Output Temperature Coefficient	TC_{VREF}			40		ppm/°C
Load Regulation		I_{SOURCE} = 0 to 300µA, I_{SINK} = 0 to 30µA		6		mV/µA
Line Regulation				50		µV/V
Noise Voltage		0.1Hz to 10Hz		25		$µV_{P-P}$
		10Hz to 10kHz		400		
EXTERNAL REFERENCE (INTREF = GND) (bypass REF+ and REF- to GND with 0.1µF or greater capacitors)						
REF Input Voltage		Differential, V_{REF+} - V_{REF-}		2.048		V
Absolute REF+, REF- Input Voltage to GND			-2.2		+2.2	V
Normal-Mode 50Hz and 60Hz Rejection (Simultaneously)		50Hz and 60Hz ±2%		100		dB
Common-Mode 50Hz and 60Hz Rejection (Simultaneously)	CMR	For 50Hz and 60Hz ±2%, R_{SOURCE} < 10kΩ		150		dB
Common-Mode Rejection	CMR	At DC		100		dB
Input Leakage Current				10		nA
Input Capacitance				10		pF
Average Dynamic Input Current		(Note 6)	-20		+20	nA

ELECTRICAL CHARACTERISTICS (continued)

($AV_{DD} = DV_{DD} = V_{DD}$ = +2.7V to +5.25V, GND = 0, V_{LED} = +2.7V to +5.25V, GLED = 0, $V_{REF+} - V_{REF-}$ = 2.048V (external reference), $C_{REF+} = C_{REF-}$ = 0.1µF, C_{VNEG} = 0.1µF. Internal clock mode, unless otherwise noted. All specifications are at $T_A = T_{MIN}$ to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGE PUMP						
Output Voltage	VNEG	C_{VNEG} = 0.1µF to GND	-2.60	-2.42	-2.30	V
DIGITAL INPUTS (INTREF, RANGE, PEAK, HOLD, DPSET1, DPSET2, DPON)						
Input Current	I_{IN}	V_{IN} = 0 or $DV_{DD} = V_{DD}$	-10		+10	µA
Input Low Voltage	V_{INL}	MAX1447/MAX1498			0.3 x DV_{DD}	V
		MAX1496			0.3 x V_{DD}	
Input High Voltage	V_{INH}	MAX1447/MAX1498	0.7 x DV_{DD}			V
		MAX1496	0.7 x V_{DD}			
Input Hysteresis	V_{HYS}			200		mV
POWER SUPPLY (Note 7)						
V_{DD} Voltage	V_{DD}	MAX1496	2.70		5.25	V
AV_{DD} Voltage	AV_{DD}	MAX1447/MAX1498	2.70		5.25	V
DV_{DD} Voltage	DV_{DD}	MAX1447/MAX1498	2.70		5.25	V
Power-Supply Rejection V_{DD}	PSRR	(Note 8)		80		dB
Power-Supply Rejection AV_{DD}	$PSRR_A$	(Note 8)		80		dB
Power-Supply Rejection DV_{DD}	$PSRR_D$	(Note 8)		100		dB
MAX1496 V_{DD} Current (Note 9)	I_{VDD}	V_{DD} = 5.25V		664	744	µA
		V_{DD} = 3.3V		618	663	
		Standby mode		268	325	
MAX1447/MAX1498 AV_{DD} Current (Note 9)	I_{AVDD}	AV_{DD} = 5.25V			640	µA
		AV_{DD} = 3.3V			600	
		Standby mode			305	
MAX1447/MAX1498 DV_{DD} Current (Note 9)	I_{DVDD}	DV_{DD} = 5.25V			320	µA
		DV_{DD} = 3.3V			180	
		Standby mode			20	
LED Drivers Bias Current		From AV_{DD} or V_{DD}		120		µA

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = V_{DD} = +2.7V to +5.25V, GND = 0, V_{LED} = +2.7V to +5.25V, GLED = 0, V_{REF+} - V_{REF-} = 2.048V (external reference), C_{REF+} = C_{REF-} = 0.1µF, C_{VNEG} = 0.1µF. Internal clock mode, unless otherwise noted. All specifications are at T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LED DRIVERS (Table 5)						
LED Supply Voltage	V_{LED}		2.70		5.25	V
LED Shutdown Supply Current	I_{SHDN}	LED driver shutdown mode			10	µA
LED Supply Current	I_{LED}	Seven segments and decimal point on, R_{ISET} = 25kΩ		176	180	mA
Display Scan Rate	f_{OSC}	MAX1447/MAX1498		512		Hz
		MAX1496		640		
Segment Current Slew Rate	$\Delta I_{SEG}/\Delta t$			25		mA/µs
DIG_ Voltage Low	V_{DIG}	$I_{DIG\_}$ = 176mA		0.178	0.300	V
Segment Drive Source Current Matching	ΔI_{SEG}			3	±10	%
Segment Drive Source Current	I_{SEG}	V_{LED} - V_{SEG} = 0.6V, R_{ISET} = 25kΩ	16.0	21.5	25.5	mA
Interdigit Blanking Time				4		µs

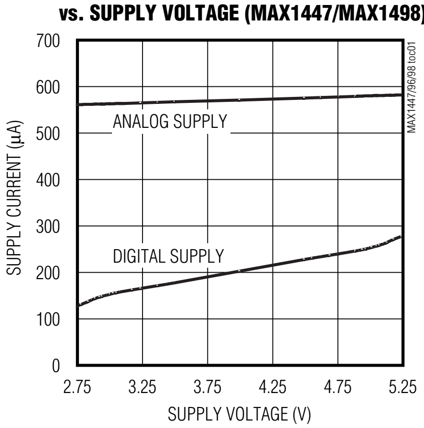
Note 1: Integral nonlinearity is the deviation of the analog value at any code from its theoretical value after nulling the gain error and offset error.
Note 2: Offset calibrated.
Note 3: Offset nulled.
Note 4: Drift error is eliminated by recalibration at the new temperature.
Note 5: The input voltage range for the analog inputs is given with respect to the voltage on the negative input of the differential pair.
Note 6: V_{AIN+} or V_{AIN-} = -2.2V to +2.2V. V_{REF+} or V_{REF-} = -2.2V to +2.2V. All input structures are identical. Production tested on AIN+ and REF+ only.
Note 7: Power-supply currents are measured with all digital inputs at either GND or DV_{DD}.
Note 8: Measured at DC by changing the power-supply voltage from 2.7V to 5.25V and measuring the effect on the conversion error with external reference. PSRR at 50Hz and 60Hz exceeds 120dB with filter notches at 50Hz and 60Hz (Figure 2).
Note 9: LED drivers are disabled.

3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers

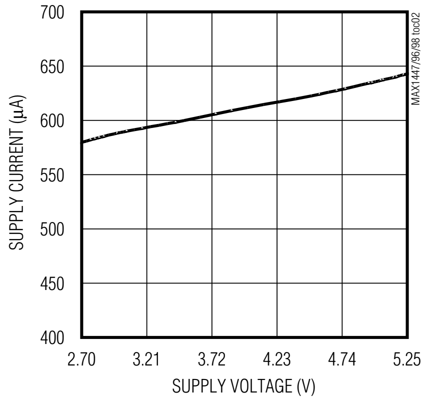
Typical Operating Characteristics

(AV_{DD} = DV_{DD} = V_{DD} = V_{LED} = +2.7V to +5.25V, GND = 0, GLED = 0, external reference mode, REF+ = 2.048V, REF- = GND, RANGE = 1, internal clock mode, T_A = +25°C, unless otherwise noted.)

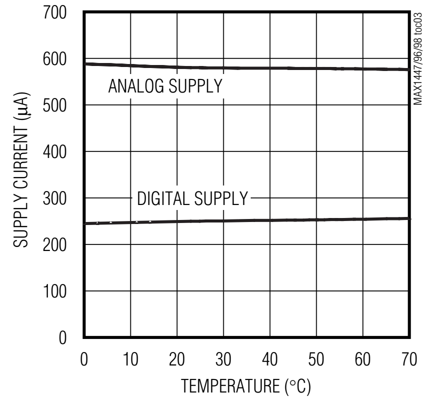
SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX1447/MAX1498)



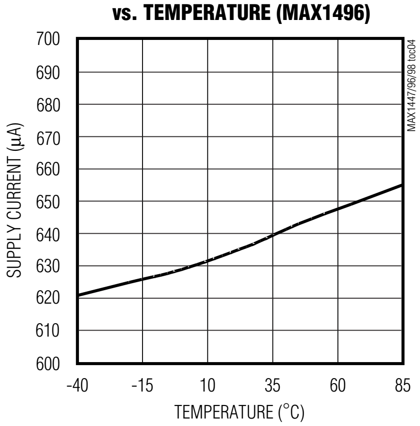
SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX1496)



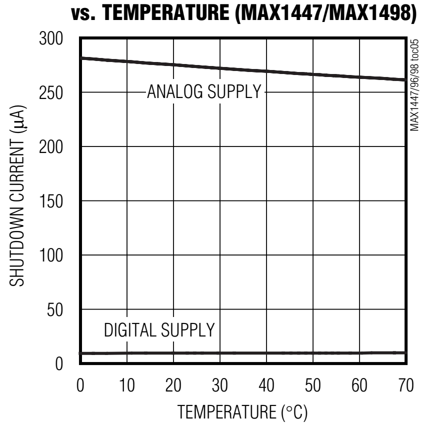
SUPPLY CURRENT vs. TEMPERATURE (MAX1447/MAX1498)



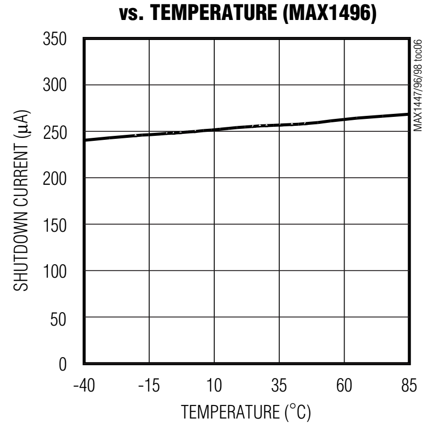
SUPPLY CURRENT vs. TEMPERATURE (MAX1496)



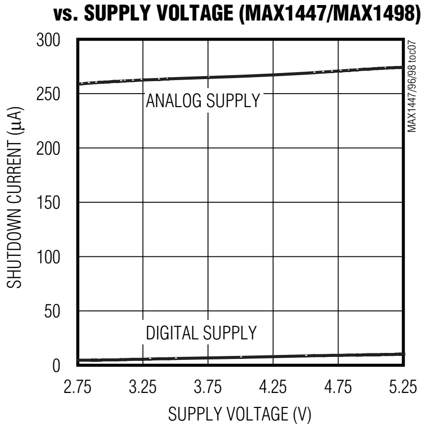
SHUTDOWN CURRENT vs. TEMPERATURE (MAX1447/MAX1498)



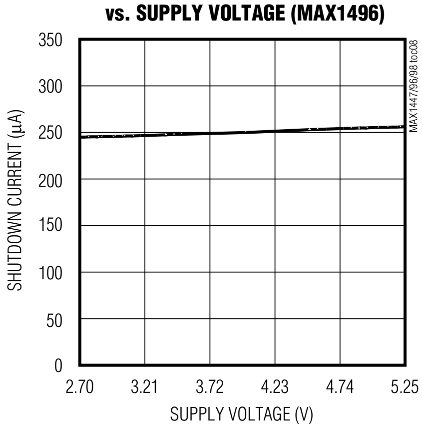
SHUTDOWN CURRENT vs. TEMPERATURE (MAX1496)



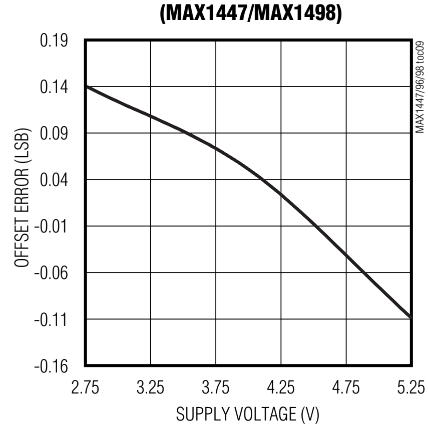
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE (MAX1447/MAX1498)



SHUTDOWN CURRENT vs. SUPPLY VOLTAGE (MAX1496)



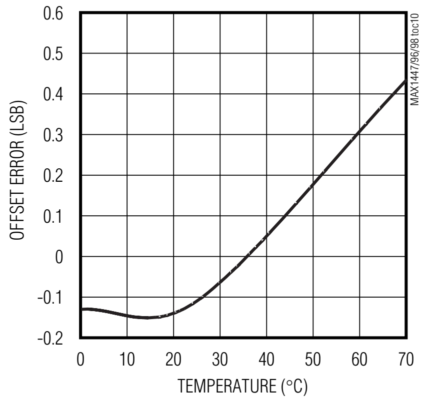
OFFSET ERROR vs. SUPPLY VOLTAGE (MAX1447/MAX1498)



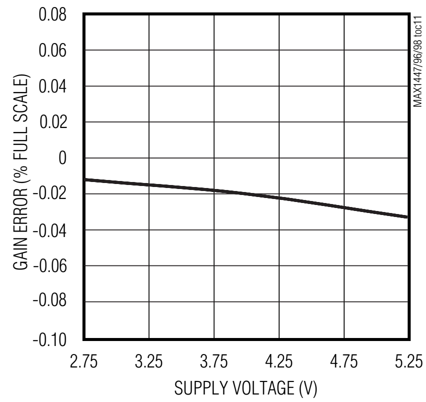
Typical Operating Characteristics (continued)

($AV_{DD} = DV_{DD} = V_{DD} = V_{LED}$ = +2.7V to +5.25V, GND = 0, GLED = 0, external reference mode, REF+ = 2.048V, REF- = GND, RANGE = 1, internal clock mode, T_A = +25°C, unless otherwise noted.)

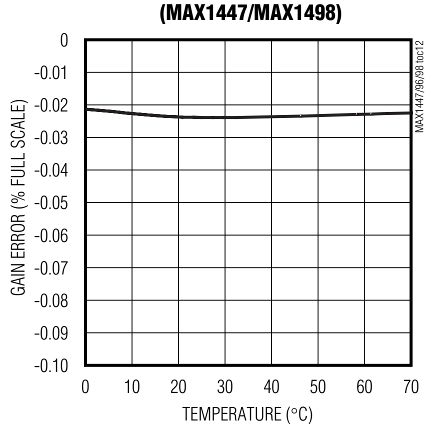
OFFSET ERROR vs. TEMPERATURE (MAX1447/MAX1498)



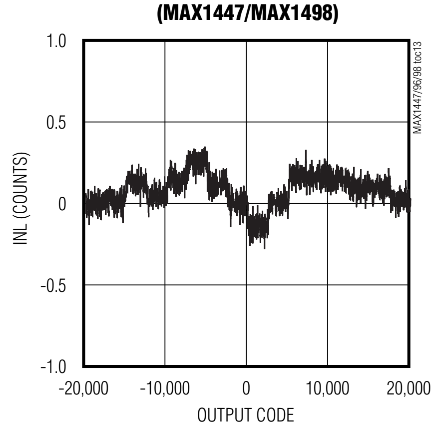
GAIN ERROR vs. SUPPLY VOLTAGE (MAX1447/MAX1498)



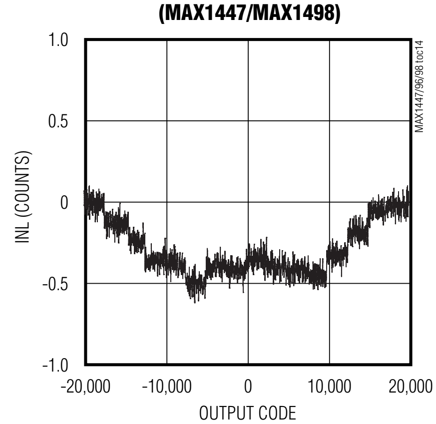
GAIN ERROR vs. TEMPERATURE (MAX1447/MAX1498)



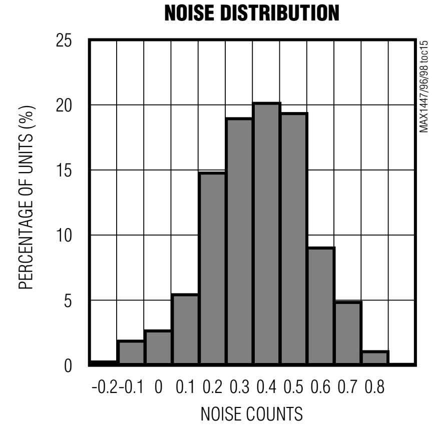
(±200mV INPUT RANGE) INL vs. OUTPUT CODE (MAX1447/MAX1498)



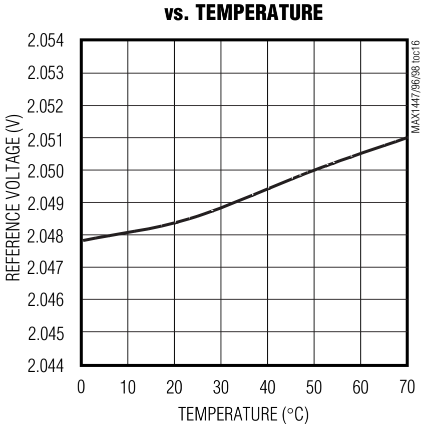
(±2V INPUT RANGE) INL vs. OUTPUT CODE (MAX1447/MAX1498)



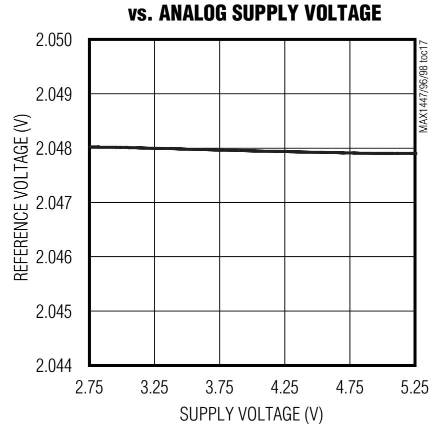
NOISE DISTRIBUTION



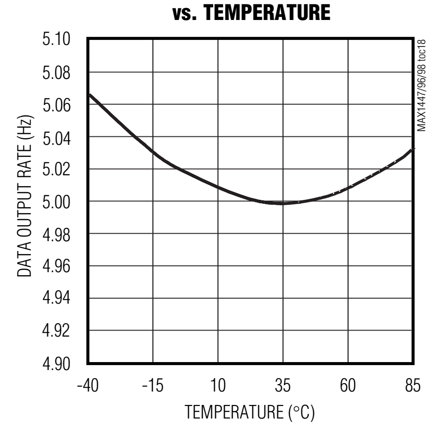
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



INTERNAL REFERENCE VOLTAGE vs. ANALOG SUPPLY VOLTAGE



DATA OUTPUT RATE vs. TEMPERATURE

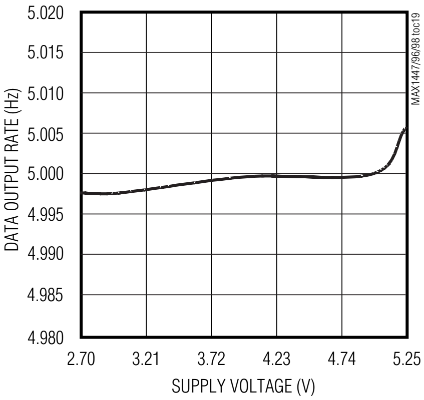


3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers

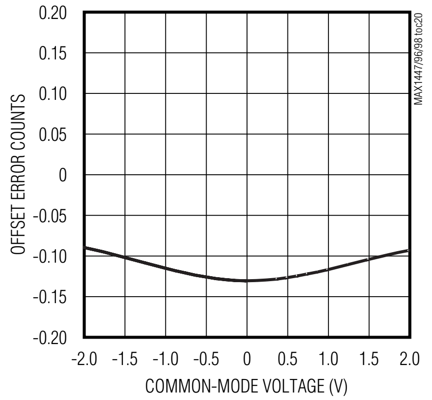
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = V_{DD} = V_{LED} = +2.7V to +5.25V, GND = 0, GLED = 0, external reference mode, REF+ = 2.048V, REF- = GND, RANGE = 1, internal clock mode, T_A = +25°C, unless otherwise noted.)

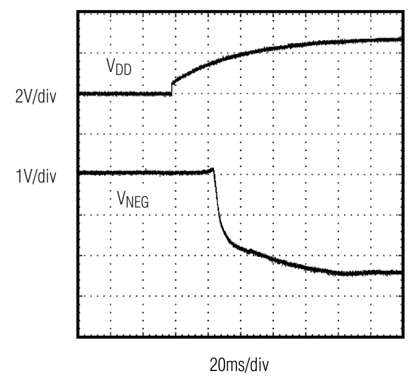
DATA OUTPUT RATE vs. SUPPLY VOLTAGE



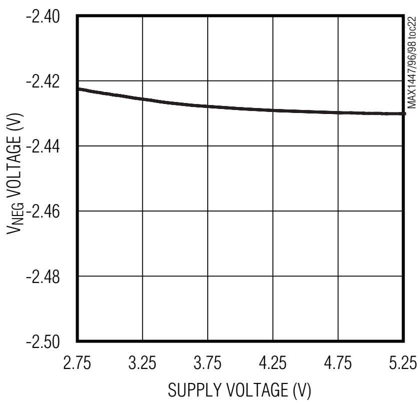
OFFSET ERROR vs. COMMON-MODE VOLTAGE



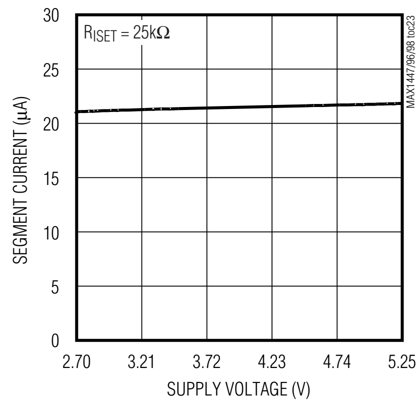
V_{NEG} STARTUP SCOPE SHOT



CHARGE-PUMP OUTPUT VOLTAGE vs. ANALOG SUPPLY VOLTAGE



SEGMENT CURRENT vs. SUPPLY VOLTAGE



Pin Description

PIN		NAME	FUNCTION
MAX1496	MAX1447/ MAX1498		
1	31	VNEG	-2.5V Charge-Pump Voltage Output. Connect a 0.1µF capacitor to GND.
2	32	REF-	Negative Reference Voltage Input. For internal-reference operation, connect REF- to GND. For external-reference operation, bypass REF- to GND with a 0.1µF capacitor and set V_{REF-} from -2.2V to +2.2V, provided $V_{REF+} > V_{REF-}$.
3	1	REF+	Positive Reference Voltage Input. For internal-reference operation, connect a 4.7µF capacitor from REF+ to GND. For external-reference operation, bypass REF+ to GND with a 0.1µF capacitor and set V_{REF+} from -2.2V to +2.2V, provided $V_{REF+} > V_{REF-}$.
4	2	AIN+	Positive Analog Input. Positive side of fully differential analog input. Bypass AIN+ to GND with a 0.1µF or greater capacitor.
5	3	AIN-	Negative Analog Input. Negative side of fully differential analog input. Bypass AIN- to GND with a 0.1µF or greater capacitor.
6	4	ISET	Segment Current Controller. Connect to ground through a resistor to set the segment current. See Table 5 for current selection.
7	5	GND	Ground
8	—	V_{DD}	Analog and Digital Circuit Supply Voltage. Connect V_{DD} to a +2.7V to +5.25V power supply. Bypass V_{DD} to GND with a 0.1µF capacitor and a 4.7µF capacitor.
9	8	INTREF	Internal-Reference Logic Input. Connect to GND to select external-reference mode. Connect to DV_{DD} for the MAX1447/MAX1498 and V_{DD} for the MAX1496 to select the internal-reference mode.
10	9	RANGE	Range Logic Input. RANGE controls the fully differential analog input range. Connect to GND for the ±2V input range. Connect to DV_{DD} (MAX1447/MAX1498) or V_{DD} (MAX1496) for the ±200mV input range.
11	10	DPSET1	Decimal-Point Logic-Input 1. Controls the decimal point of the LED. See the *Decimal-Point Control* section.
12	11	DPSET2	Decimal-Point Logic-Input 2. Controls the decimal point of the LED. See the *Decimal-Point Control* section.
13	12	PEAK	Peak Logic Input. Connect to DV_{DD} (MAX1447/MAX1498) or V_{DD} (MAX1496) to display the highest ADC value on the LED. Connect to GND to disable the peak function.
14	13	HOLD	Hold Logic Input. Connect to DV_{DD} (MAX1447/MAX1498) or V_{DD} (MAX1496) to hold the current ADC value on the LED. Connect to GND to update the LED at a rate of 2.5Hz and disable the hold function. For the MAX1447, only placing the device into hold mode initiates an offset mismatch calibration. Assert HOLD high for a minimum of 2s to ensure the completion of offset mismatch calibration.
15	14	DIG0	Digit 0 Driver
16	15	DIG1	Digit 1 Driver
17	16	GLED	Ground for LED Display Digit Driver
18	17	DIG2	Digit 2 Driver

Pin Description (continued)

PIN		NAME	FUNCTION
MAX1496	MAX1447/ MAX1498		
19	18	DIG3	Digit 3 Driver
20	20	SEGA	Segment A Driver
21	21	SEGB	Segment B Driver
22	22	SEGC	Segment C Driver
23	23	SEGD	Segment D Driver
24	24	SEGE	Segment E Driver
25	25	VLED	LED Display Segment Driver Supply. Connect to a +2.7V to +5.25V supply. Bypass with a 0.1µF capacitor to GLED.
26	26	SEGF	Segment F Driver
27	27	SEGG	Segment G Driver
28	28	SEGDP	Segment DP Driver
—	6	AV_{DD}	Analog Positive Supply Voltage. Connect AV_{DD} to a +2.7V to +5.25V power supply. Bypass AV_{DD} to GND with a 0.1µF capacitor.
—	7	DV_{DD}	Digital Positive Supply Voltage. Connect DV_{DD} to a +2.7V to +5.25V power supply. Bypass DV_{DD} to GND with a 0.1µF capacitor.
—	19	DIG4	Digit 4 Driver
—	29	LED_EN	Active-High LED Enable. The MAX1447/MAX1498 display driver turns off when the LED_EN is driven to logic low. The MAX1447/MAX1498 LED display driver turns on when LED_EN is driven to logic high.
—	30	DPON	Decimal-Point Enable Input. Controls the decimal point of the LED. See the *Decimal-Point Control* section. Connect to DV_{DD} (MAX1447/MAX1498) or V_{DD} (MAX1496) to enable the decimal point.

Detailed Description

The MAX1447/MAX1496/MAX1498 low-power, highly integrated ADCs with LED drivers convert a ±2V differential input voltage (one count is equal to 100µV for the MAX1447/MAX1498 and 1mV for the MAX1496) with a sigma-delta ADC and output the result to an LED. An additional ±200mV input range (one count is equal to 10µV for the MAX1447/MAX1498 and 100µV for the MAX1496) is available to measure small signals with increased resolution.

The devices operate from a single 2.7V to 5.25V power supply and offer 3.5-digit (MAX1496) or 4.5-digit (MAX1447/MAX1498) conversion results. An internal 2.048V reference, internal charge pump, and a high-accuracy on-chip oscillator eliminate external components.

The devices also feature on-chip buffers for the differential input signal and external-reference inputs, allowing direct interface with high-impedance signal sources. In addition, they use continuous internal offset-calibration and offer >100dB of 50Hz and 60Hz line-noise rejection. Other features include data hold and peak detection and overrange/underrange detection.

Analog Input Protection

Internal protection diodes limit the analog input range from VNEG to (AV_{DD} + 0.3V) for the MAX1447/ MAX1498, and from VNEG to (V_{DD} + 0.3V) for the MAX1496. If the analog input exceeds this range, limit the input current to 10mA.

Internal Analog Input/Reference Buffers

The MAX1447/MAX1496/MAX1498 analog input/reference buffers allow the use of high-impedance signal sources. The input buffers' common-mode input range allows the analog inputs and the reference to range from -2.2V to +2.2V.

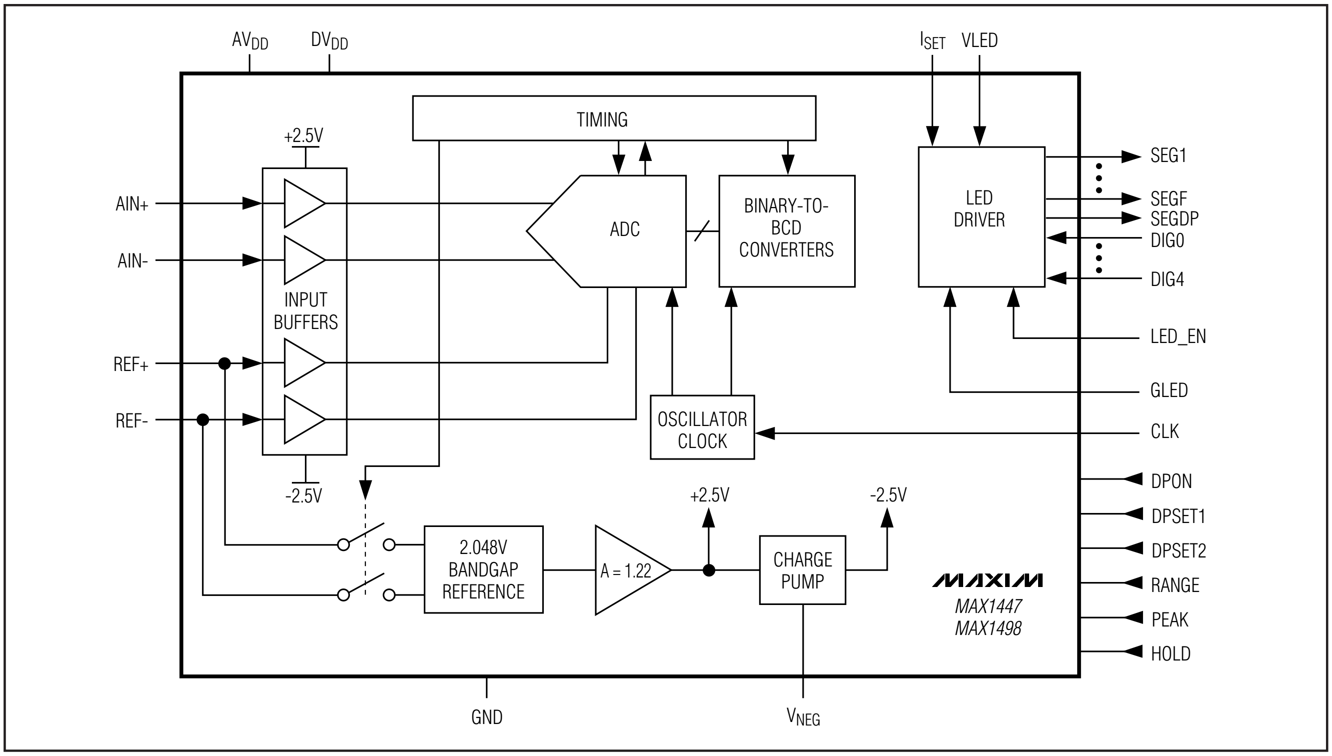


Figure 1. MAX1447/MAX1498 Functional Diagram

Modulator

The MAX1447/MAX1496/MAX1498 perform analog-to-digital conversions using a single-bit, 3rd-order, sigma-delta modulator. The sigma-delta modulator converts the input signal into a digital pulse train whose average duty cycle represents the digitized signal information. The modulator quantizes the input signal at a much higher sample rate than the bandwidth of the input.

The MAX1447/MAX1496/MAX1498 modulator provides 3rd-order frequency shaping of the quantization noise resulting from the single-bit quantizer. The modulator is fully differential for maximum signal-to-noise ratio and minimum susceptibility to power-supply noise. A single-bit data stream is then presented to the digital filter to remove the frequency-shaped quantization noise.

Digital Filtering

The MAX1447/MAX1496/MAX1498 contain an on-chip digital lowpass filter that processes the data stream from the modulator using a SINC^4 response:

$$\left(\frac{\sin(x)}{x}\right)^4$$

The SINC^4 filter has a settling time of four output data periods (4 x 200ms).

The MAX1447/MAX1496/MAX1498 have 25% over-range capability built into the modulator and digital filter. The digital filter is optimized for the f_{CLK} equal to 4.9152MHz. The frequency response of the SINC^4 filter is calculated as follows:

$$H(z) = \left[\frac{1}{N}\frac{(1 - Z^{-N})}{(1 - Z^{-1})}\right]^4$$

$$H(f) = \frac{1}{N}\left[\frac{\sin\left(N\pi\frac{f}{f_m}\right)}{\sin\left(\frac{\pi f}{f_m}\right)}\right]^4$$

where N is the oversampling ratio, and f_m = N x output data rate = 5Hz.

3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers

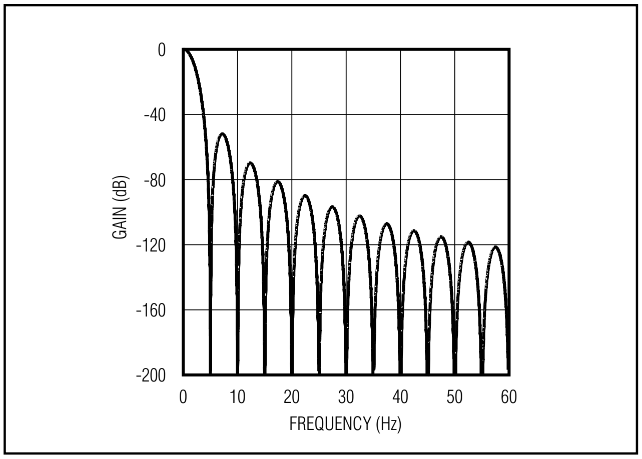


Figure 2. Frequency Response of the SINC4 Filter (Notch at 50Hz and 60Hz)

Filter Characteristics

Figure 2 shows the filter frequency response. The SINC4 characteristic -3dB cutoff frequency is 0.228 times the first notch frequency (5Hz). The oversampling ratio (OSR) for the MAX1496 is 128 and the OSR for the MAX1447/MAX1498 is 1024.

The output data rate for the digital filter corresponds to the positioning of the first notch of the filter's frequency response. The notches of the SINC4 filter are repeated at multiples of the first notch frequency. The SINC4 filter provides an attenuation of better than 100dB at these notches. For example, 50Hz is equal to 10 times the first notch frequency and 60Hz is equal to 12 times the first notch frequency.

For large step changes at the input, allow a settling time of 800ms before valid data is read.

Internal Clock

The MAX1447/MAX1496/MAX1498 contain an internal oscillator. Using the internal oscillator saves board space by removing the need for an external clock source. The oscillator is optimized to give 50Hz and 60Hz power-supply and common-mode rejection.

Charge Pump

The MAX1447/MAX1496/MAX1498 contain an internal charge pump to provide the negative supply voltage for the internal analog input/reference buffers. The bipolar input range of the analog input/reference buffers allows this device to accept negative inputs with high source impedances. Connect a 0.1µF capacitor from VNEG to GND.

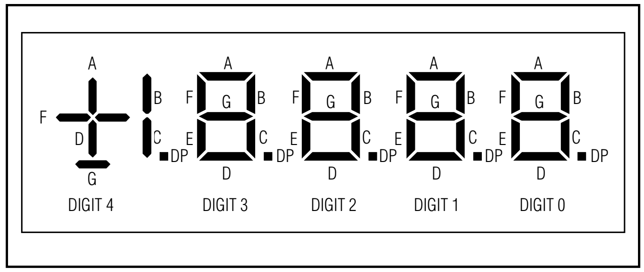


Figure 3. Segment Connection for the MAX1447/MAX1498 (4.5 Digits)

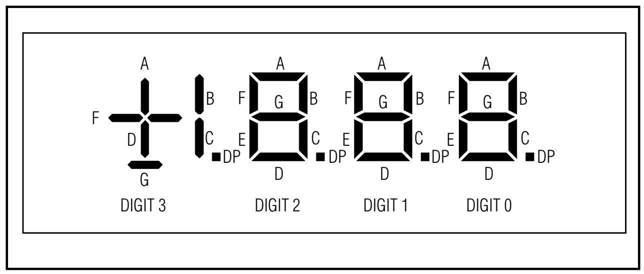


Figure 4. Segment Connection for the MAX1496 (3.5 Digits)

Table 1. LED Priority Table

HOLD	PEAK	DISPLAY VALUES FORM
1	X	Hold value
0	1	Peak value
0	0	Latest ADC result

X = *Don't care.*

LED Driver

The MAX1447/MAX1498 have a 4.5-digit common-cathode display driver, and the MAX1496 has a 3.5-digit common-cathode display driver. Figures 3 and 4 show the connection schemes for a standard seven-segment LED display. The LED update rate is 2.5Hz. The MAX1447/MAX1496/MAX1498 automatically display the results of the ADC, if desired (Table 1).

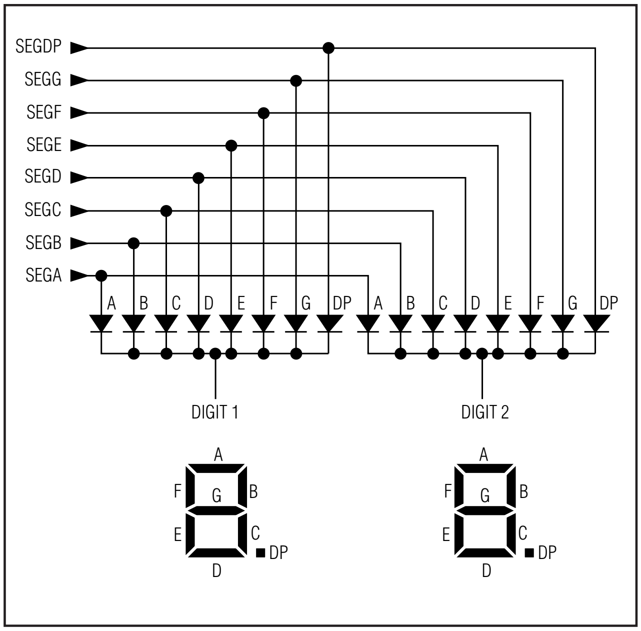


Figure 5. Two-Digit Common-Cathode Configuration

Figure 5 shows a typical common-cathode configuration for two digits. In common-cathode configuration, the cathodes of all LEDs in a digit are connected together. Each segment driver of the MAX1447/MAX1496/MAX1498 connects to its corresponding LED's anodes. For example, segment driver SEGA connects to all LED segments designated as A. Similar configurations are used for other segment drivers.

The MAX1447/MAX1496/MAX1498 use a multiplexing scheme to drive one digit at a time. The scan rate is fast enough to make the digits appear to be lit. Figures 6 and 7 show data-timing diagrams for the MAX1447/MAX1496/MAX1498, where T is the display scan period (typically around 1/512Hz or 1.9531ms for the MAX1447/MAX1498, and 1/640Hz or 1.5625ms for the MAX1496). T_{ON} in Figures 6 and 7 denotes the amount of time each digit is on and is calculated as follows:

$$T_{ON} = \frac{T}{5} = \frac{1.95312\text{ms}}{5} = 390.60\mu\text{s} \quad \text{(MAX1447/MAX1498)}$$

$$T_{ON} = \frac{T}{4} = \frac{1.5625\text{ms}}{4} = 390.60\mu\text{s} \quad \text{(MAX1496)}$$

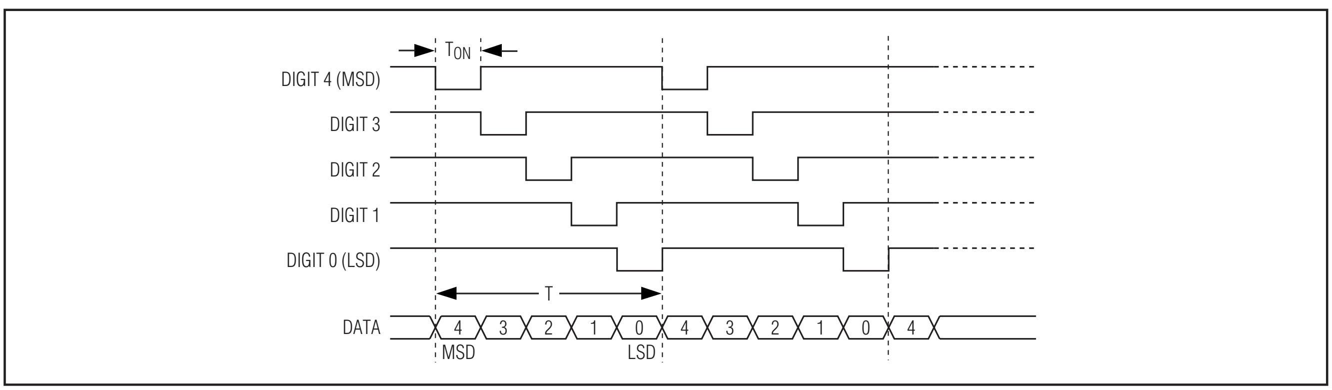


Figure 6. LED Voltage Waveform—MAX1447/MAX1498

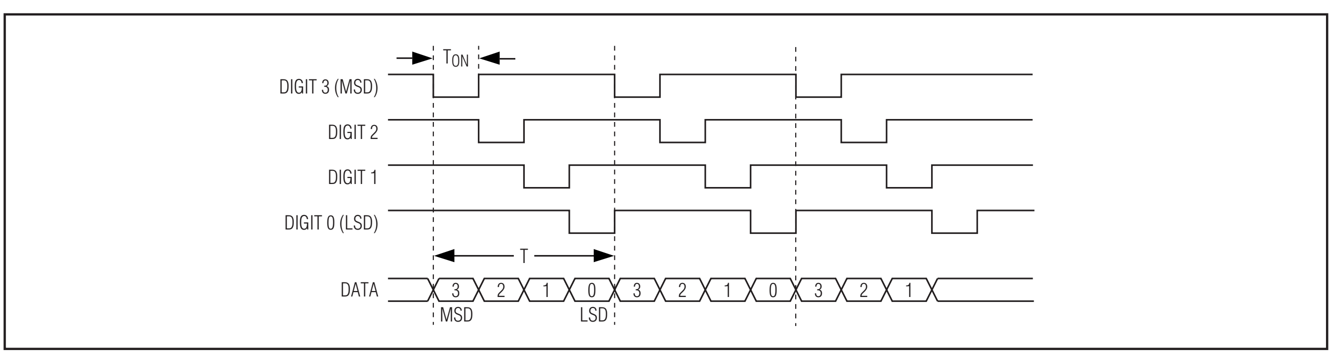


Figure 7. LED Voltage Waveform—MAX1496

3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers

Decimal-Point Control

The MAX1447/MAX1496/MAX1498 allow for full decimal-point control and feature leading-zero suppression. Use the DPON, DPSET1, and DPSET2 bits in the control register to set the value of the decimal point (Tables 2 and 3). The MAX1447/MAX1496/MAX1498 overrange and underrange display is shown in Table 4.

Leading-Zero Suppression

The MAX1447/MAX1496/MAX1498 include a leading-zero suppression circuitry to turn off unnecessary zeros. For example, when DPSET1 and DPSET2 = [0,0], 0.0 is displayed instead of 000.0. This feature saves a substantial amount of power from being wasted.

Interdigit Blanking

The MAX1447/MAX1496/MAX1498 also include an interdigit blanking circuitry. Without this feature, it is possible to see a faint digit next to a digit that is completely on. The interdigit blanking circuitry prevents bleeding over into the next digit for a short period of time. The typical interdigit blanking time is 4μs.

Reference

The MAX1447/MAX1496/MAX1498 reference sets the full-scale range of the ADC transfer function. With a nominal 2.048V reference, the ADC full-scale range is ±2V with RANGE = GND. With RANGE = DV_{DD} (MAX1447/MAX1498) or V_{DD} (MAX1496), the full-scale range is ±200mV. A decreased reference voltage decreases full-scale range (see the *Transfer Functions* section).

The MAX1447/MAX1496/MAX1498 accept either an external reference or an internal reference (INTREF). The INTREF logic selects the reference mode.

For internal-reference operation, set INTREF to DV_{DD} (MAX1447/MAX1498) or V_{DD} (MAX1496), connect REF- to GND, and bypass REF+ to GND with a 4.7μF capacitor. The internal reference provides a nominal 2.048V source between REF+ and GND. The internal-reference temperature coefficient is typically 40ppm/°C.

Table 2. Decimal-Point Control Table—MAX1447/MAX1498

DPON	DPSET1	DPSET2	DISPLAY OUTPUT	ZERO INPUT READING
0	0	0	18888	0
0	0	1	18888	0
0	1	0	18888	0
0	1	1	18888	0
1	0	0	1888.8	0.0
1	0	1	188.88	0.00
1	1	0	18.888	0.000
1	1	1	1.8888	0.0000

Table 3. Decimal-Point Control Table—MAX1496

DPSET1	DPSET2	DISPLAY OUTPUT	ZERO INPUT READING
0	0	188.8	0.0
0	1	18.88	0.00
1	0	1888	0
1	1	1.888	0.000

X = *Don't care.*

Table 4. LED During Overrange and Underrange Conditions

CONDITION	MAX1496	MAX1447/MAX1498
Overrange	1---	1----
Underrange	-1---	-1----

For external-reference operation, set INTREF to GND. REF+ and REF- are fully differential. For a valid external-reference input, V_{REF+} must be greater than V_{REF-}. Bypass REF+ and REF- with a 0.1µF or greater capacitor to GND in external-reference mode.

Figure 8 shows the MAX1447/MAX1496/MAX1498 operating with an external differential reference. In this figure, REF- is connected to the top of the strain gauge and REF+ is connected to the midpoint of the resistor-divider of the supply.

Figure 9 shows the MAX1447/MAX1496/MAX1498 operating with an external single-ended reference. In this figure, REF- is connected to GND and REF+ is driven with an external 2.048V reference. Bypass REF+ to GND with a 0.47µF capacitor.

Applications Information

Power-On Reset

At power-up, the digital filter and modulator circuits reset.

The MAX1447/MAX1498 allows 6s for the reference to stabilize before performing enhanced offset calibration. During these 6s, the MAX1447/MAX1498 display 1.2V to 1.5V when a stable reference is detected. If a valid reference is not found, the MAX1447/MAX1498 time out after 6s and begin enhanced offset calibration. Enhanced offset calibration typically lasts 2s. The MAX1447/MAX1498 begin converting after enhanced offset calibration.

Offset Calibration

The MAX1447/MAX1496/MAX1498 offer on-chip offset calibration. The device offset calibrates during every conversion cycle.

Enhanced Offset Calibration (MAX1447 Only)

Enhanced offset calibration is a more accurate calibration method that is needed in the case of the ±200mV range and 4.5-digit resolution. In addition to enhanced offset calibration at power-up, the MAX1447 performs enhanced calibration on demand by connecting HOLD to AV_{DD} for > 2s.

Peak

The MAX1447/MAX1496/MAX1498 feature peak-detection circuitry. When activated (PEAK connected to AV_{DD} for the MAX1498/MAX1447 or to V_{DD} for the MAX1496), the devices display only the highest voltage measured to the LED.

First, the current ADC result is displayed. The new ADC conversion result is compared to the current result. If the new value is larger than the previous peak value, the new value is displayed. If the new value is less than the previous peak value, the display remains unchanged.

Connect PEAK to GND to clear the peak value and disable the peak function.

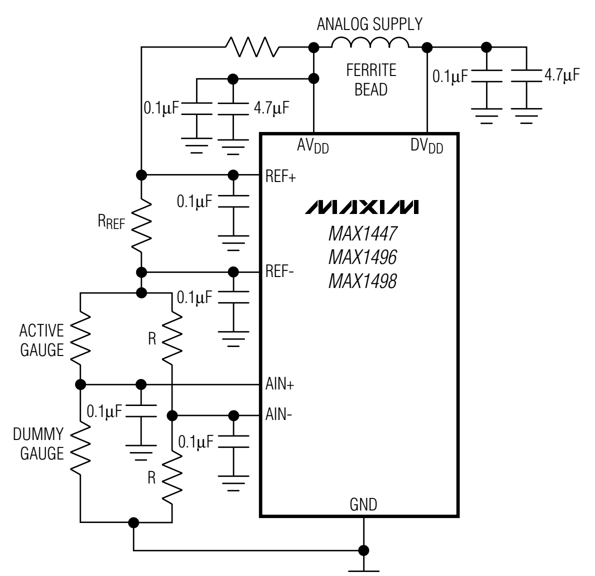


Figure 8. Strain-Gauge Application with the MAX1447/MAX1496/MAX1498

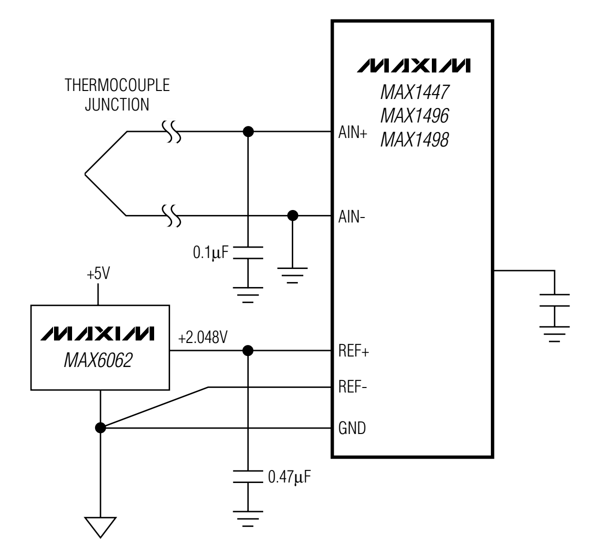


Figure 9. Thermocouple Application with the MAX1447/MAX1496/MAX1498

3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers

Hold

The MAX1447/MAX1496/MAX1498 feature data-hold circuitry. When activated (HOLD is set to AV_{DD} for the MAX1447/MAX1498 or to V_{DD} for the MAX1496), the device holds the current reading on the LED.

Strain-Gauge Measurement

Connect the differential inputs of the MAX1447/MAX1496/MAX1498 to the bridge network of the strain gauge. In Figure 8, the analog supply voltage powers the bridge network and the MAX1447/MAX1496/MAX1498, along with the reference voltage. The MAX1447/MAX1496/MAX1498 handle an analog input voltage range of ±200mV and ±2V full scale. The analog/reference inputs of the parts allow the analog input range to have an absolute value of anywhere between -2.2V and +2.2V.

Thermocouple Measurement

Figure 9 shows a connection from a thermocouple to the MAX1447/MAX1496/MAX1498. In this application, the MAX1447/MAX1496/MAX1498 take advantage of the on-chip input buffers that allow large source impedances on the front end. The decoupling capacitors reduce noise pickup from the thermocouple leads. To place the differential voltage from the thermocouple at a suitable common-mode voltage, the AIN- input of the MAX1447/MAX1496/MAX1498 is biased to GND. Use an external temperature sensor, such as the DS75, and a microcontroller to perform cold-junction temperature compensation.

Transfer Functions

Figures 10–13 show the transfer functions of the MAX1447/MAX1496/MAX1498.

The transfer function for the MAX1447/MAX1498 with AIN+ - AIN- ≥ 0, RANGE = GND is:

$$COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 20{,}000\right)$$

The transfer function for the MAX1447/MAX1498 with AIN+ - AIN- < 0, RANGE = GND is:

$$COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 20{,}000\right) + 1$$

The transfer function for the MAX1447/MAX1498 with AIN+ - AIN- ≥ 0, RANGE = DV_{DD} is:

$$COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 20{,}000\right) \times 10$$

The transfer function for the MAX1447/MAX1498 with AIN+ - AIN- < 0, RANGE = DV_{DD} is:

$$COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 20{,}000\right) \times 10 + 1$$

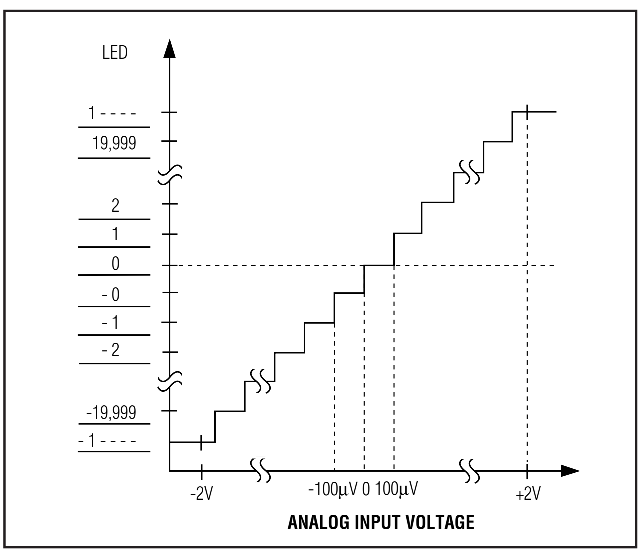


Figure 10. MAX1447/MAX1498 Transfer Function, ±2V Range

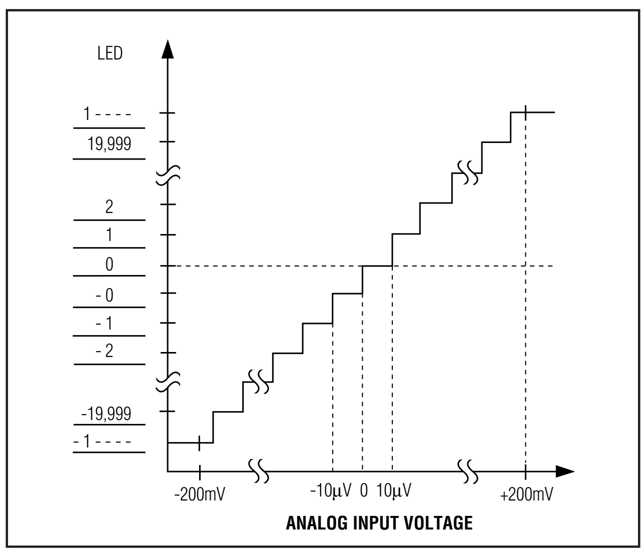


Figure 11. MAX1447/MAX1498 Transfer Function, ±200mV Range

The transfer function for the MAX1496 with AIN+ - AIN- ≥ 0, RANGE = GND is:

$$COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 2000\right)$$

The transfer function for the MAX1496 with AIN+ - AIN- < 0, RANGE = GND is:

$$COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 2000\right) + 1$$

The transfer function for the MAX1496 with AIN+ - AIN- ≥ 0, RANGE = V_{DD} is:

$$COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 2000\right) \times 10$$

The transfer function for the MAX1496 with AIN+ - AIN- < 0, RANGE = V_{DD} is:

$$COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 2000\right) \times 10 + 1$$

Supplies, Layout, and Bypassing

Power up AV_{DD} and DV_{DD} (MAX1447/MAX1498) and V_{DD} (MAX1496) before applying an analog input and external-reference voltage to the device. If this is not possible, limit the current into these inputs to 50mA. When the analog and digital supplies come from the same source, isolate the digital supply from the analog supply with a low-value resistor (10Ω) or ferrite bead. For best performance, ground the MAX1447/MAX1496/MAX1498 to the analog ground plane of the circuit board.

Avoid running digital lines under the device as this can couple noise onto the IC. Run the analog ground plane under the MAX1447/MAX1496/MAX1498 to minimize coupling of digital noise. Make the power-supply lines to the MAX1447/MAX1496/MAX1498 as wide as possible to provide low-impedance paths and reduce the effects of glitches on the power-supply line.

Shield fast-switching signals, such as clocks, with digital ground to avoid radiating noise to other sections of the board. Avoid running clock signals near the analog inputs. Avoid crossover of digital and analog signals. Running traces that are on opposite sides of the board at right angles to each other reduces feedthrough effects.

Good decoupling is important when using high-resolution ADCs. Decouple the supplies with 0.1µF ceramic capacitors to GND. Place these components as close to the device as possible to achieve the best decoupling.

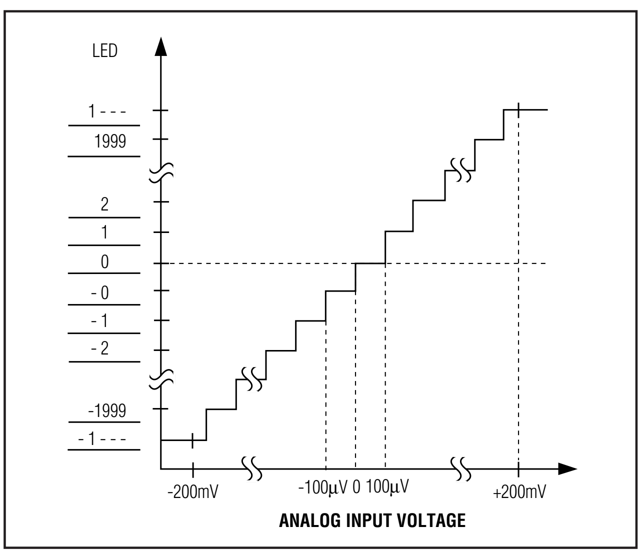


Figure 12. MAX1496 Transfer Function, ±200mV Range

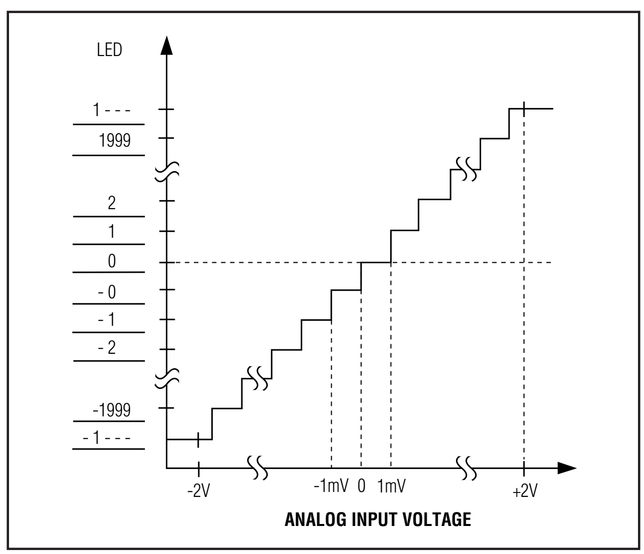


Figure 13. MAX1496 Transfer Function, ±2V Range

Selecting Segment Current

A resistor from ISET to ground sets the current for each LED segment. See Table 5 for more detail. Use the following formula to set the segment current:

$$I_{SEG} = \left(\frac{1.20V}{R_{ISET}}\right) \times 450$$

R_{ISET} values below 25kΩ increase the I_{SEG}. However, the internal current-limit circuit limits the I_{SEG} to less than 30mA. At higher I_{SEG} values, proper operation of the device is not guaranteed. In addition, the power dissipated may exceed the package power-dissipation limit.

Choosing Supply Voltage to Minimize Power Dissipation

The MAX1447/MAX1496/MAX1498 drive a peak current of 25.5mA into LEDs with a 2.2V forward voltage drop when operated from a supply voltage of at least 3.0V. Therefore, the minimum voltage drop across the internal LED drivers is (3.0V - 2.2V) = 0.8V. The MAX1447/MAX1496/MAX1498 sink (8 x 25.5mA = 204mA) when the outputs are operating and the LED segment drivers are at full current. For a 3.3V supply, the MAX1447/MAX1496/MAX1498 dissipate (3.3V - 2.2V) x 204 = 224.4mW. If a higher supply voltage is used, the driver absorbs a higher voltage, and the driver's power dissipation increases accordingly. However, if the LEDs used have a higher forward voltage drop than 2.2V, the supply voltage must be raised accordingly to ensure that the driver always has at least 0.8V headroom.

For a VLED supply voltage of 2.7V, the maximum LED forward voltage is 1.9V to ensure 0.8V driver headroom. The voltage drop across the drivers with a nominal +5V supply (5.0V - 2.2V = 2.8V) is almost three times the drop across the drivers with a nominal 3.3V supply (3.3V - 2.2V = 1.1V). Therefore, the driver's power dissipation increases three times. The power dissipation in the part causes the junction temperature to rise accordingly. In the high ambient temperature case, the total junction temperature may be very high (>+125°C). At higher junction temperatures, the ADC performance degrades. To ensure the dissipation limit for the MAX1447/MAX1496/MAX1498 is not exceeded and the ADC performance is not degraded, a diode can be inserted between the power supply and VLED.

Table 5. Segment-Current Selection

R_{ISET} (kΩ)	I_{SEG} (mA)
25	21.6
50	10.8
100	5.4
500	1.1
>2500	LED driver disabled

Computing Power Dissipation

The following can be used to compute power dissipation:

$$PD = (VLED \times I_{VLED}) + (VLED - V_{DIODE}) (DUTY \times I_{SEG} \times N) + V_{SUPPLY} \times I_{SUPPLY}$$

VLED = LED driver supply voltage

I_{VLED} = VLED bias current

V_{DIODE} = LED forward voltage

DUTY = segment ON time during each digit ON time

I_{SEG} = segment current set by R_{ISET}

N = number of segments driven (worst case is eight)

V_{SUPPLY} = supply voltage of the part

I_{SUPPLY} = supply current from V_{DD} for the MAX1496 or AV_{DD} + DV_{DD} for the MAX1447/MAX1498.

Dissipation Example

For I_{SEG} = 25.5mA, N = 8, DUTY = 127 / 128, V_{DIODE} = 1.5V at 25.5mA, VLED = V_{SUPPLY} = 5.25V:

$$PD = (5.25 \times 2mA) + (5.25V - 1.5) [(127 / 128) \times 25.5mA \times 8)] + 5.25 \times 1.080mA$$

$$PD = 0.7751W$$

28-Pin SSOP-Package Example

For the 28-pin SSOP package (T_{JA} = 1 / 0.009496 = +105.3°C/W), the maximum allowed ambient temperature T_A is given by:

$$T_J (max) = T_A + (PD \times T_{JA}) =$$

$$+125°C = T_A + (0.7751W \times +105.3°C/W)$$

$$T_A = +43°C$$

Thus, the device cannot operate safely at a maximum package temperature of +85°C. The power dissipates in the part need to be lowered.

$(PD \times T_{JA})$ max = (+125°C) - (+85°C) = +40°C

PD (max) = +40°C /+105.3°C/W = 380mW

$(VLED - V_{DIODE})$ = [380mW - (5.25V x 2mA) - 5.25V x 1.080mA] / [(127 / 128) x 25.5mA x 8]

$VLED - V_{DIODE}$ = 1.854V

$VLED - V_{DIODE}$ should have the following condition to ensure it operates safely:

$0.8V < VLED - V_{DIODE} < 1.854V$

28-Pin PDIP-Package Example

$PD \times T_{JA}$ (max) = (+125°C) - (+85°C) = +40°C

PD (max) = +40°C / +70°C/W = 571mW

$VLED - V_{DIODE}$ = [571mW - (5.25V x 2mA) - 5.25V x 1.080mA] / [(127 / 128) x 25.5mA x 8]

$VLED - V_{DIODE}$ = 2.80V

For a 28-pin PDIP package, $VLED - V_{DIODE}$ should have the following condition to ensure it operates safely:

$0.8V < VLED - V_{DIODE} < 2.80V$

32-Pin TQFP Package

The MAX1447/MAX1498 TQFP package can operate safely for all supply voltages provided $V_{DIODE} > 1.5V$.

Definitions

INL

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line is either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. INL for the MAX1447/MAX1496/MAX1498 is measured using the end-point method.

DNL

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of ±1 LSB. A DNL error specification of less than ±1 LSB guarantees no missing codes and a monotonic transfer function.

Rollover Error

Rollover error is defined as the absolute-value difference between a near positive full-scale reading and near negative full-scale reading. Rollover error is tested by applying a full-scale positive voltage, swapping AIN+ and AIN-, and adding the results.

Zero Input Reading

Ideally, with AIN+ connected to AIN-, the MAX1447/MAX1496/MAX1498 LED displays zero. Zero input reading is the measured deviation from the ideal zero and the actual measured point.

Gain Error

Gain error is the amount of deviation between the measured full-scale transition point and the ideal full-scale transition point.

Common-Mode Rejection

Common-mode rejection (CMR) is the ability of a device to reject a signal that is common to both input terminals. The common-mode signal can be either an AC or a DC signal or a combination of the two. CMR is often expressed in decibels.

Normal-Mode 50Hz and 60Hz Rejection (Simultaneously)

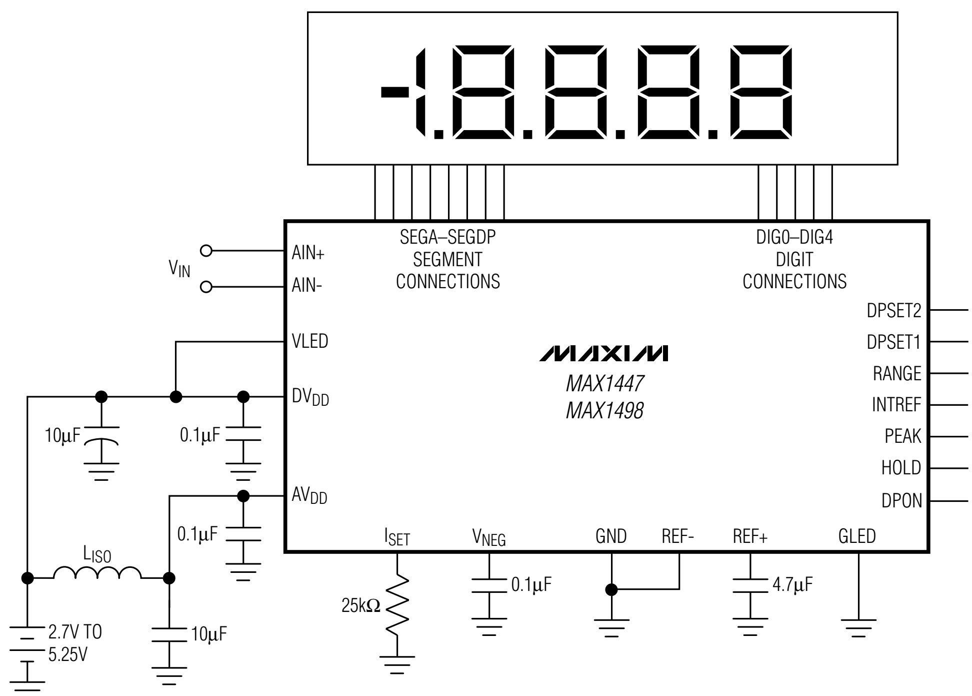
Normal-mode rejection is a measure of how much output changes when 50Hz and 60Hz signals are injected into only one of the differential inputs. The MAX1447/MAX1496/MAX1498 sigma-delta converter uses its internal digital filter to provide normal-mode rejection to both 50Hz and 60Hz power-line frequencies simultaneously.

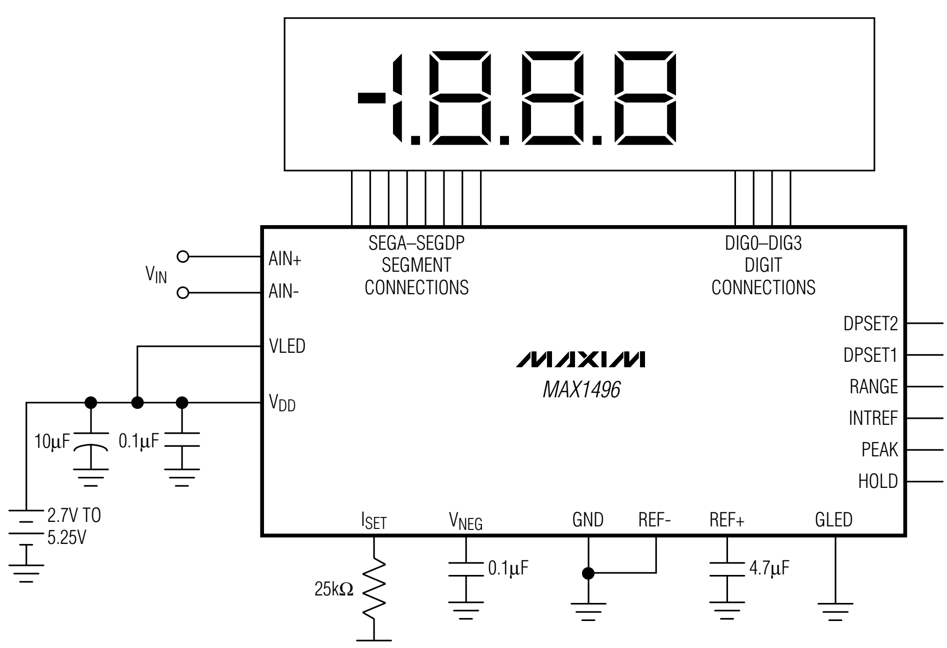
Power-Supply Rejection Ratio

Power-supply rejection ratio (PSRR) is the ratio of the input supply change (in volts) to the change in the converter output (in volts). It is typically measured in decibels.

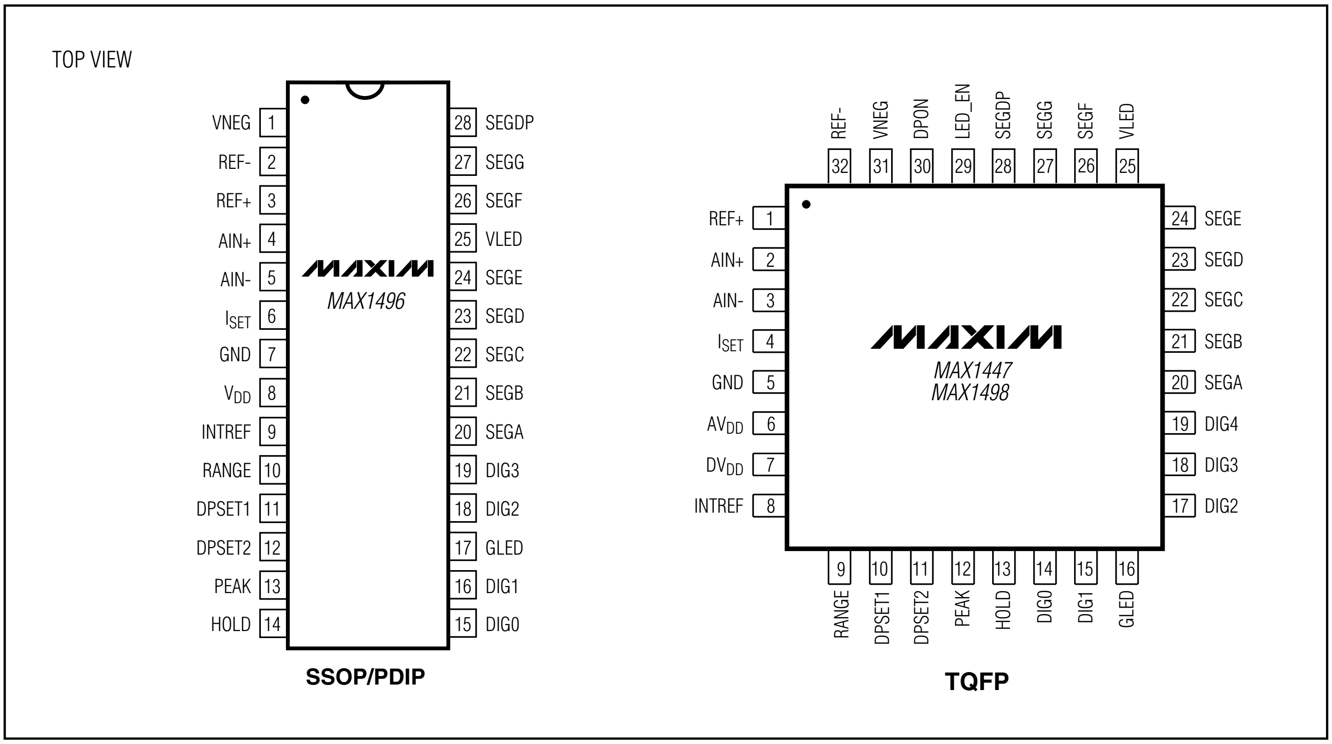
3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers

Typical Operating Circuits





Pin Configurations



Chip Information

TRANSISTOR COUNT: 80,000

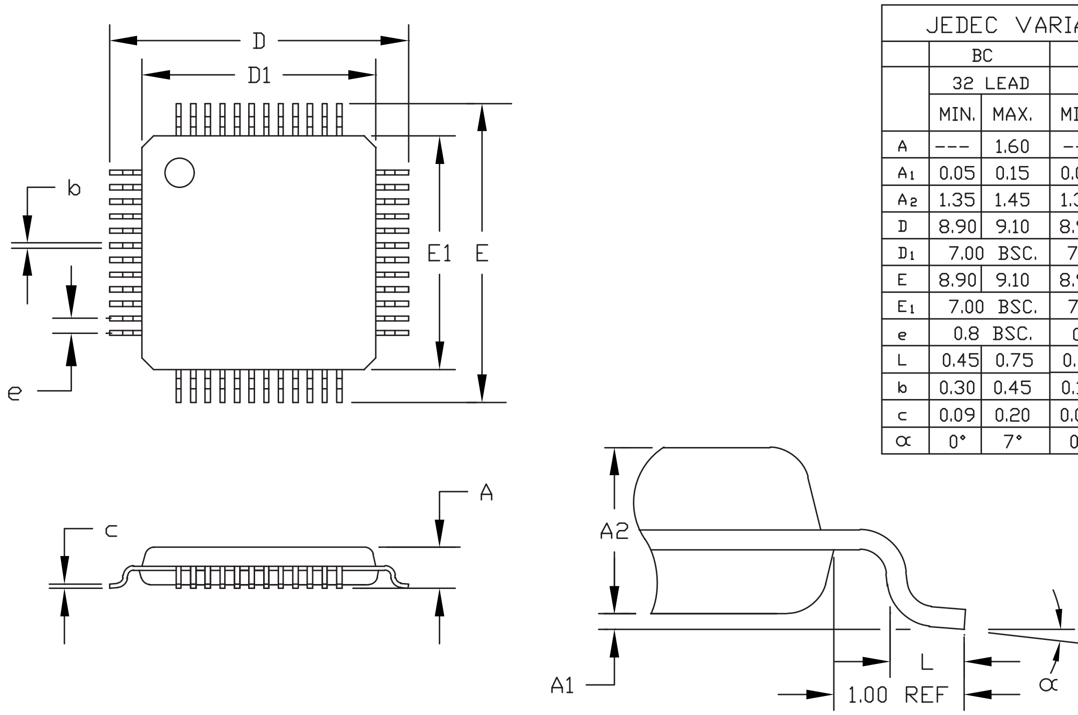
PROCESS: BiCMOS

3.5- and 4.5-Digit, Single-Chip ADCs with LED Drivers

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

32L/48L,TQFP.EPS



JEDEC VARIATION				
	BC		BE	
	32 LEAD		48 LEAD	
	MIN.	MAX.	MIN.	MAX.
A	---	1.60	---	1.60
A_1	0.05	0.15	0.05	0.15
A_2	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10
D_1	7.00 BSC.		7.00 BSC.	
E	8.90	9.10	8.90	9.10
E_1	7.00 BSC.		7.00 BSC.	
e	0.8 BSC.		0.5 BSC.	
L	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27
c	0.09	0.20	0.09	0.20
α	0°	7°	0°	7°

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS BC AND BE.
4. LEADS SHALL BE COPLANAR WITHIN .004 INCH.

MAXIM

PROPRIETARY INFORMATION

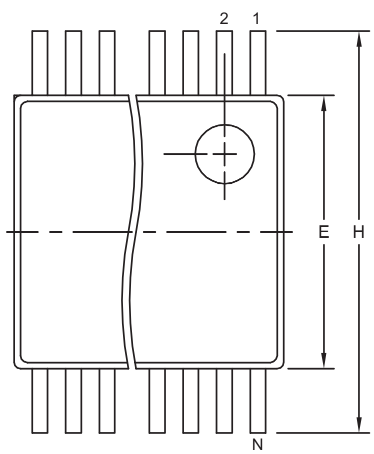
TITLE: PACKAGE OUTLINE, 32/48L, 7x7x1.4 MM TQFP

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0054	D	1/1

Package Information (continued)

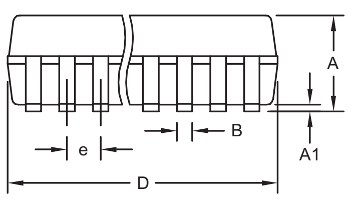
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

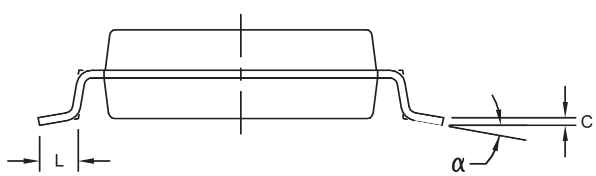
SSOP.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.212	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0∞	8∞	0∞	8∞

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	N
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L



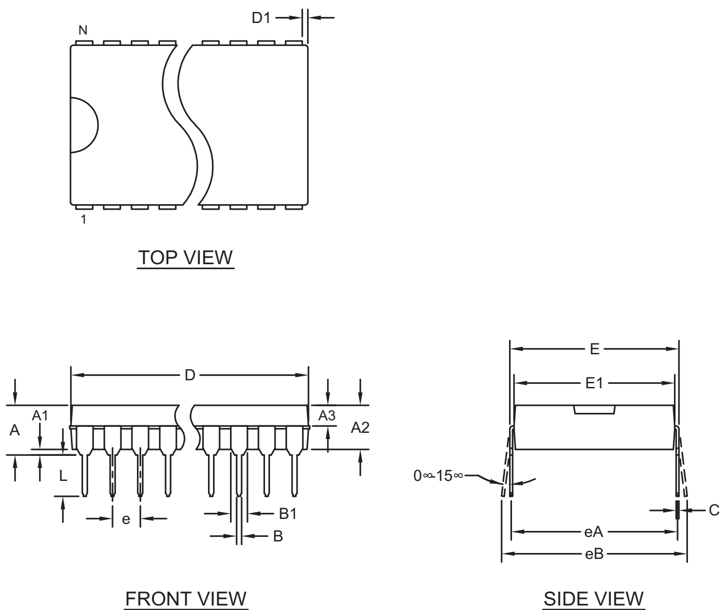


NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO150.
5. LEADS TO BE COPLANAR WITHIN 0.10 MM.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, SSOP, 5.3 MM
APPROVAL | DOCUMENT CONTROL NO. 21-0056 | REV. C | 1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.200	-	5.08
A1	0.015	-	0.39	-
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.020	0.41	0.51
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.21	0.30
D1	0.005	0.009	0.13	0.22
E	0.600	0.625	15.24	15.87
E1	0.525	0.575	13.34	14.61
e	0.100 BSC		2.54 BSC	
eA	0.600 BSC		15.24 BSC	
eB	-	0.700	-	17.78
L	0.120	0.150	3.05	3.81

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS011
D	1.230	1.270	31.24	32.26	24	AA
D	1.430	1.470	36.32	37.34	28	AB
D	2.025	2.075	51.44	52.71	40	AC

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006”).
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MS011.
5. N = NUMBER OF PINS.

PDIPW.EPS

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, .600" PDIP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0044	B	1/1