FAIRCHILD SEMICONDUCTOR®

LVTTL/LVCMOS COMPATIBLE LOW INPUT CURRENT HIGH GAIN SPLIT DARLINGTON OPTOCOUPLERS

SINGLE CHANNEL: FOD070L FOD270L
DUAL CHANNEL: FOD073L

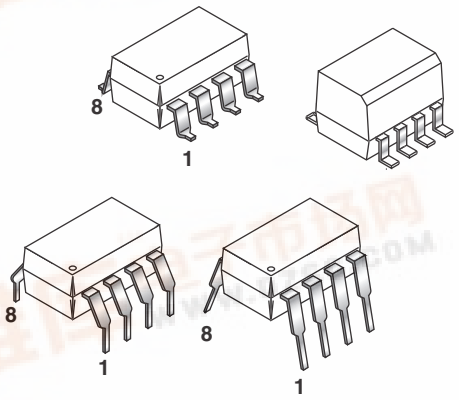
DESCRIPTION

The FOD070L, FOD270L and FOD073L optocouplers consist of an AlGaAs LED optically coupled to a high gain split darlington photodetector. These devices are specified to operate at a 3.3V supply voltage.

The split darlington configuration separating the input photodiode and the first stage gain from the output transistor permits lower output saturation voltage and higher speed operation than possible with conventional darlington phototransistor optocoupler. In the dual channel device FOD073L, an integrated emitter – base resistor provides superior stability over temperature.

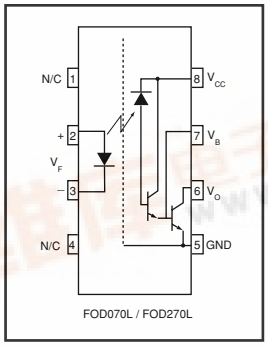
The combination of a very low input current of 0.5 mA and a high current transfer ratio of 2000% makes this family particularly useful for input interface to MOS, CMOS, LSTTL and EIA RS232C, while output compatibility is ensured to LVCMOS as well as high fan-out LVTTL requirements.

An internal noise shield provides exceptional common mode rejection of 10 kV/μs.

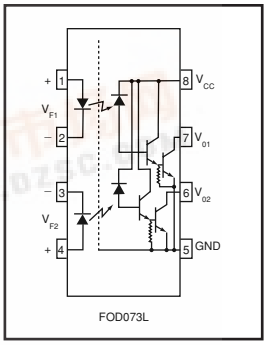


FEATURES

- Low power consumption
- Low input current - 0.5 mA
- Available in single channel 8-pin DIP (FOD270L), 8-pin SOIC (FOD070L) and dual channel 8-pin SOIC
- High CTR-2000%
- High CMR-10 kV/μs
- Guaranteed performance over temperature 0°C to 70°C
- U.L. recognized (File # E90700)
- LVTTL/LVCMOS Compatible output



FOD070L / FOD270L



FOD073L

APPLICATIONS

- Digital logic ground isolation – LVTTL/LVCMOS
- Telephone ring detector
- EIA-RS-232C line receiver
- High common mode noise line receiver
- μP bus isolation
- Current loop receiver

TRUTH TABLE

LED	V_O
ON	LOW
OFF	HIGH

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ABSOLUTE MAXIMUM RATINGS (No derating required up to 85°C)

Parameter		Symbol	Value	Units
Storage Temperature		T_{STG}	-40 to +125	°C
Operating Temperature		T_{OPR}	-40 to +85	°C
Lead Solder Temperature (Wave solder only. See reflow profile for surface mount devices)		T_{SOL}	260 for 10 sec	°C
EMITTER				
DC/Average Forward Input Current	Each Channel	I_F (avg)	20	mA
Peak Forward Input Current (50% duty cycle, 1 ms P.W.)	Each Channel	I_F (pk)	40	mA
Peak Transient Input Current - (≤1 µs P.W., 300 pps)	Each Channel	I_F (trans)	1.0	A
Reverse Input Voltage	Each Channel	V_R	5	V
Input Power Dissipation	Each Channel	P_D	35	mW
DETECTOR				
Average Output Current	Each Channel	I_O (avg)	60	mA
Emitter-Base Reverse Voltage (FOD070L, FOD270L)	Each Channel	V_{EB}	0.5	V
Supply Voltage, Output Voltage	Each Channel	V_{CC}, V_O	-0.5 to 7	V
Output power dissipation	Each Channel	P_D	100	mW

ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C Unless otherwise specified)

INDIVIDUAL COMPONENT CHARACTERISTICS

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
EMITTER	T_A =25°C	V_F	All		1.35	1.7	V
Input Forward Voltage	Each Channel (I_F = 1.6 mA)					1.75	
Input Reverse Breakdown Voltage	(T_A =25°C, I_R = 10 µA) Each Channel	BV_R	All	5.0			V
DETECTOR Logic high output current	(I_F = 0 mA, V_O = V_{CC} = 3.3 V)	I_{OH}	FOD070L FOD270L		0.05	25	µA
	Each Channel		FOD073L				
Logic Low Supply Current	I_F = 1.6 mA, V_O = Open, V_{CC} = 3.3V	I_{CCL}	FOD070L FOD270L		0.5	1.5	mA
	I_{F1} = I_{F2} = 1.6mA V_{O1} = V_{O2} = Open, V_{CC} = 3.3 V		FOD073L		0.8	3	
Logic High Supply Current	I_F = 0 mA, V_O = Open, V_{CC} = 3.3V	I_{CCH}	FOD070L FOD270L		0.01	1	µA
	I_{F1} = I_{F2} = 0mA V_{O1} = V_{O2} = Open, V_{CC} = 3.3 V		FOD073L		0.01	2	

**All typicals at T_A = 25°C

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TRANSFER CHARACTERISTICS (T_A = 0 to 70°C Unless otherwise specified)

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
COUPLED Current transfer ratio (Notes 1,2)	(I_F = 0.5 mA, V_O = 0.4 V, V_{CC} = 3.3V)	CTR	ALL	400		7000	%
Logic low output voltage output voltage (Note 2)	(I_F = 1.6 mA, I_O = 8 mA, V_{CC} = 3.3V)	V_{OL}	ALL		0.07	0.3	V
	(I_F = 5 mA, I_O = 15 mA, V_{CC} = 3.3V)		ALL		0.07	0.4	

**All typicals at T_A = 25°C

SWITCHING CHARACTERISTICS (T_A = 0 to 70°C unless otherwise specified., V_{CC} = 3.3 V)

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
Propagation delay time to logic low	(R_L = 4.7 kΩ, I_F = 0.5 mA) (Note 2) (Fig. 17)	T_{PHL}	FOD070L FOD270L		3	30	µs
			FOD073L		5		
Propagation delay time to logic high	(R_L = 4.7 kΩ, I_F = 0.5 mA) (Note 2) (Fig. 17)	T_{PLH}	FOD070L FOD270L		50	90	µs
			FOD073L		25		
Common mode transient immunity at logic high	(I_F = 0 mA, $\|V_{CM}\|$ = 10 V_{P-P}) T_A = 25°C (R_L = 2.2 kΩ) (Note 3) (Fig. 18)	$\|CM_H\|$	ALL	1,000	10,000		V/µs
Common mode transient immunity at logic low	(I_F = 1.6 mA, $\|V_{CM}\|$ = 10 V_{P-P}, R_L = 2.2 kΩ) T_A = 25°C (Note 3) (Fig. 18)	$\|CM_L\|$	ALL	1,000	10,000		V/µs

** All typicals at TA = 25°C

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ISOLATION CHARACTERISTICS (T_A = 0 to 70°C Unless otherwise specified)

Characteristics	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
Input-output insulation leakage current	(Relative humidity = 45%) (T_A = 25°C, t = 5 s) (V_{I-O} = 3000 VDC) (Note 4)	I_{I-O}	ALL			1.0	µA
Withstand insulation test voltage	($R_H \leq 50\%$, T_A = 25°C) (Note 4) (t = 1 min.)	V_{ISO}	FOD070L FOD073L	2500			V_{RMS}
			FOD270L	5000			
Resistance (input to output)	(Note 4) (V_{I-O} = 500 VDC)	R_{I-O}	ALL		10^{12}		Ω
Capacitance (input to output)	(Note 4,5) (f = 1 MHz)	C_{I-O}	ALL		0.7		pF
Input-Input Insulation leakage current	(RH ≤ 45%, V_{I-I} = 500 VDC (Note 6)	I_{I-I}	FOD073L	0.005			µA
Input-Input Resistance	(V_{I-I} = 500 VDC) (Note 6)	R_{I-I}	FOD073L		10^{11}		Ω
Input-Input Capacitance	(f = 1 MHz) (Note 6)	C_{I-I}	FOD073L		0.03		pF

** All typicals at T_A = 25°C

NOTES

1. Current Transfer Ratio is defined as a ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
2. Pin 7 open. (FOD070L and FOD270L only)
3. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a logic high state (i.e., V_O>2.0 V). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a logic low state (i.e., V_O<0.8 V).
4. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
5. For dual channel devices, CI-O is measured by shorting pins 1 and 2 or pins 3 and 4 together and pins 5 through 8 shorted together.
6. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

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TYPICAL PERFORMANCE CURVES

Fig. 1 Input Forward Current vs Forward Voltage

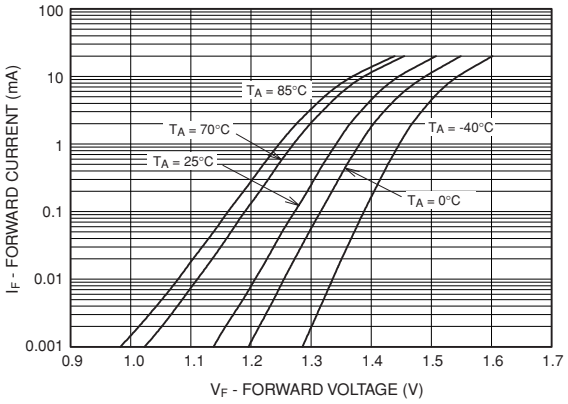


Fig. 2 Current Transfer Ratio vs. Input Forward Current (FOD270L only)

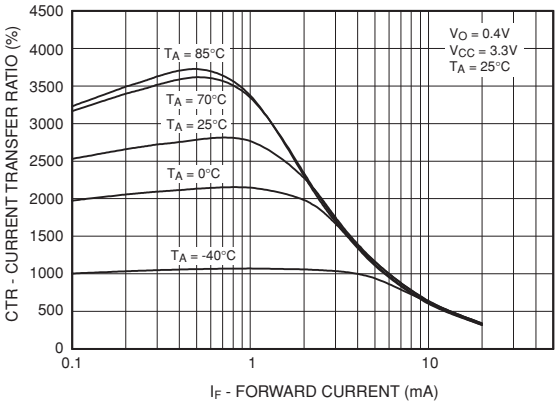


Fig. 3 Current Transfer Ratio vs. Input Forward Current (FOD070L only)

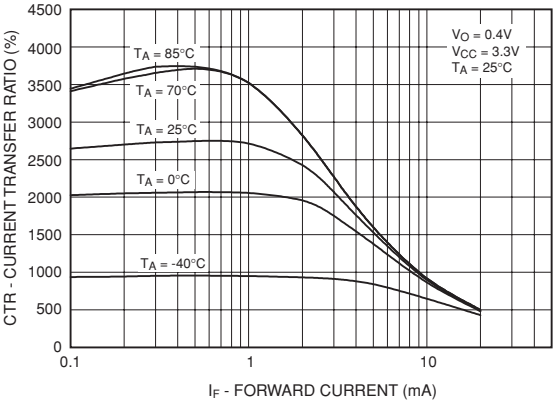


Fig. 4 Current Transfer Ratio vs. Input Forward Current (FOD073L only)

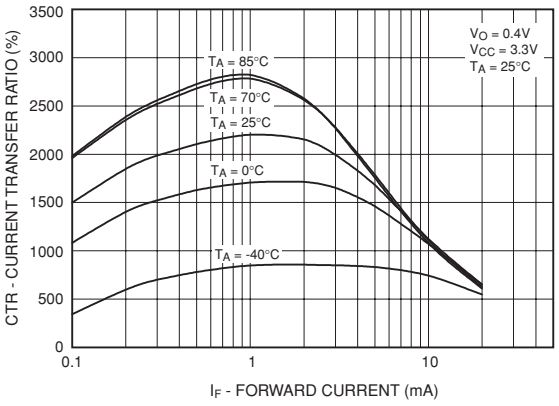


Fig. 5 DC Transfer Charactersitics (FOD070L, FOD270L)

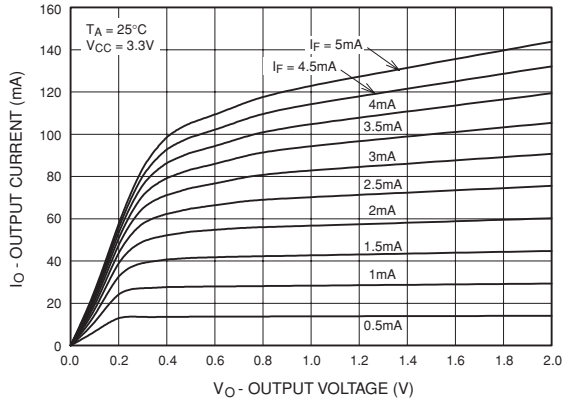
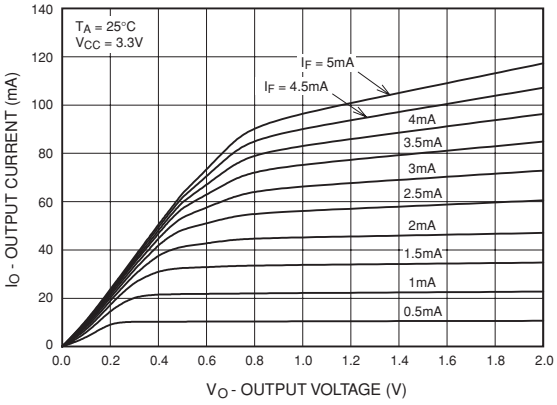


Fig. 6 DC Transfer Characterstics (FOD073L only)



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TYPICAL PERFORMANCE CURVES

Fig. 7 Supply Current vs Input Forward Current (FOD270L, FOD070L, FOD073L)

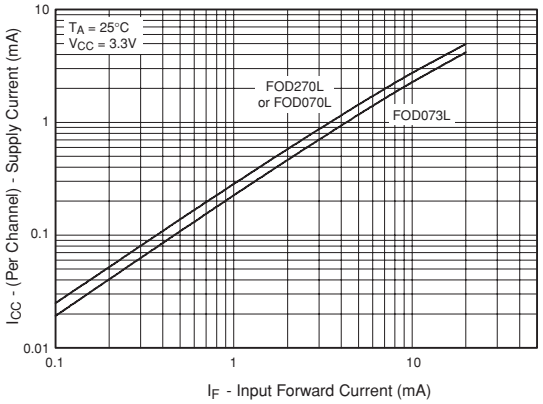


Fig. 8 Output Current vs Input Forward Current (FOD270L only)

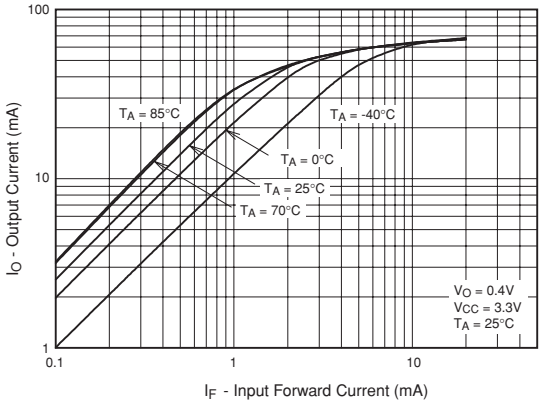


Fig. 9 Output Current vs Input Forward Current (FOD070L only)

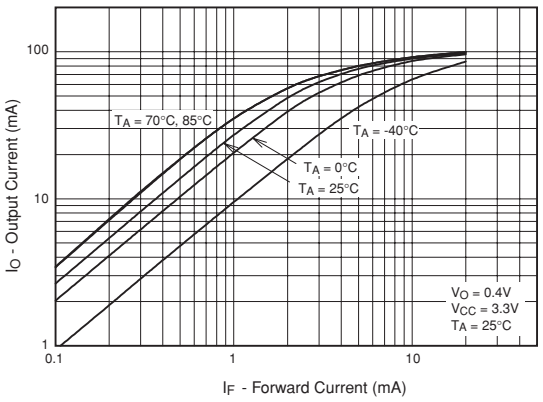


Fig. 10 Output Current vs Input Forward Current (FOD073L only)

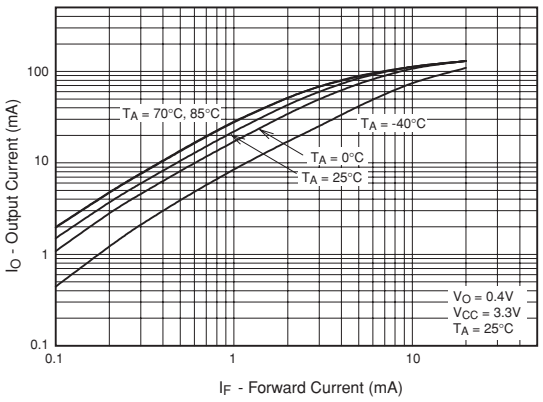


Fig. 11 Propagation Delay vs. Input Forward Current (FOD070L only)

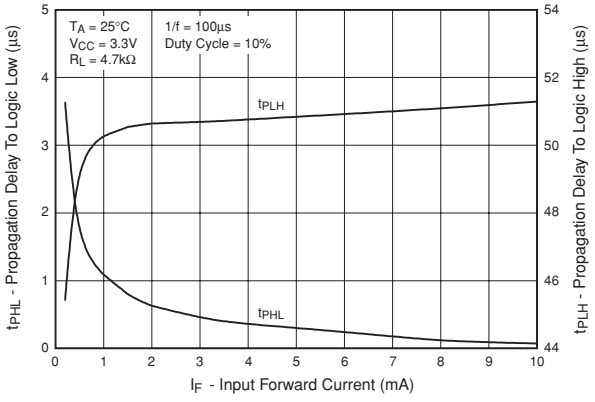
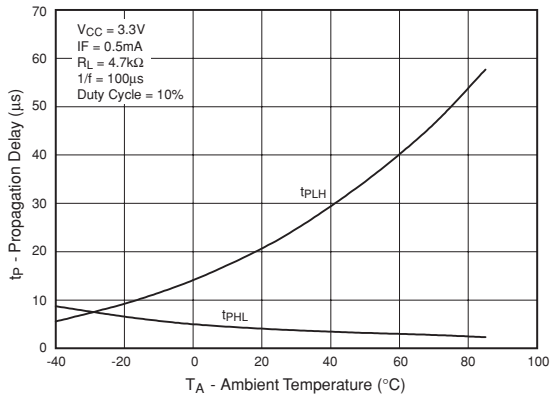


Fig. 12 Propagation Delay vs. Ambient Temperature (FOD073L only)



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TYPICAL PERFORMANCE CURVES

Fig. 13 Propagation Delay vs. Ambient Temperature (FOD070L, FOD270L)

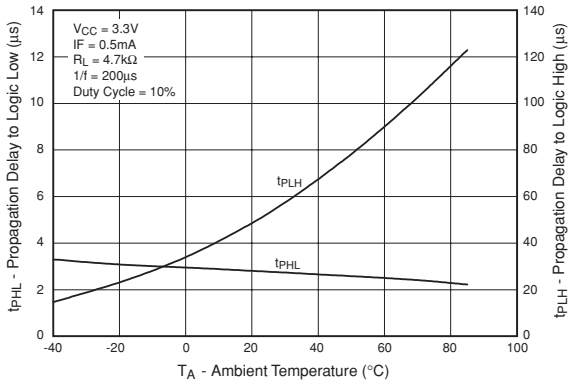


Fig. 14 Propagation Delay To Logic Low vs Pulse Period (FOD073L, FOD070L, FOD270L)

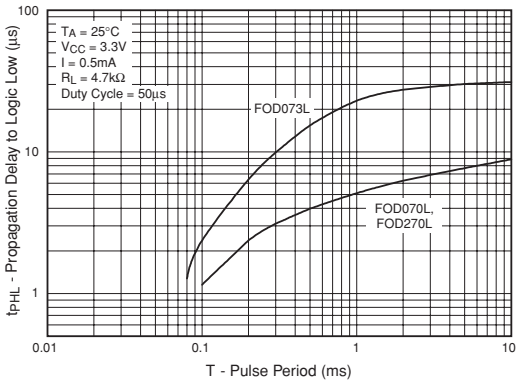


Fig. 15 Propagation Delay vs. Input Forward Current (FOD270L only)

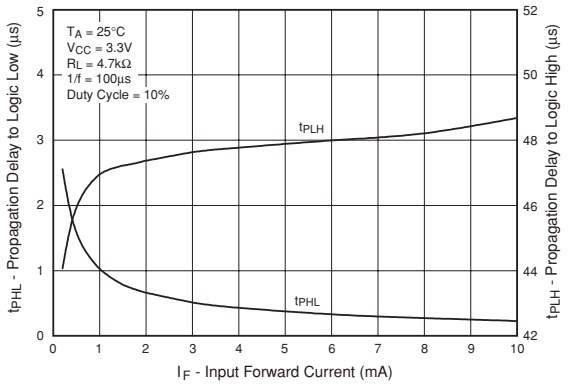
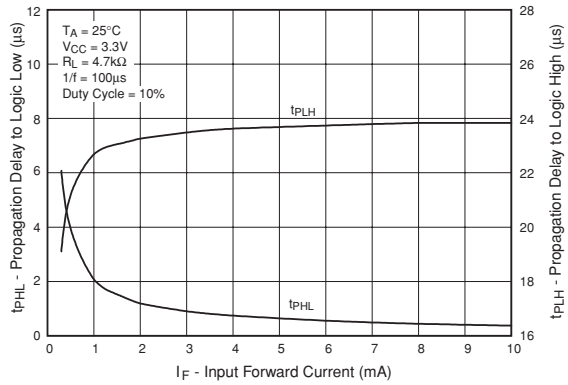


Fig. 16 Propagation Delay vs. Input Forward Current (FOD073L only)



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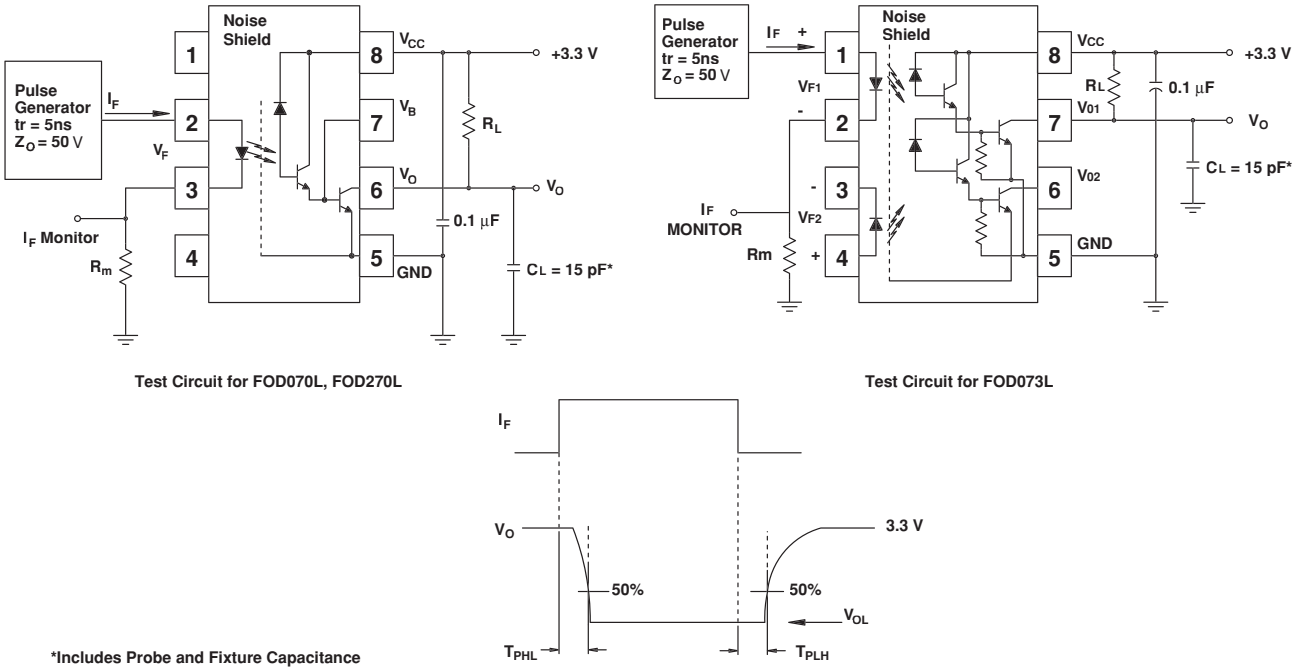

Fig. 17 Switching Time Test Circuit

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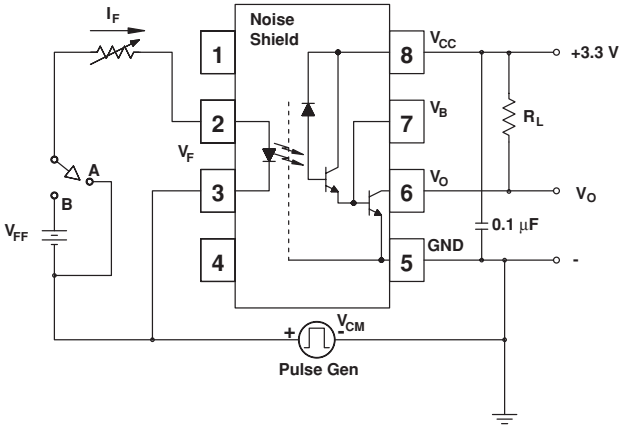
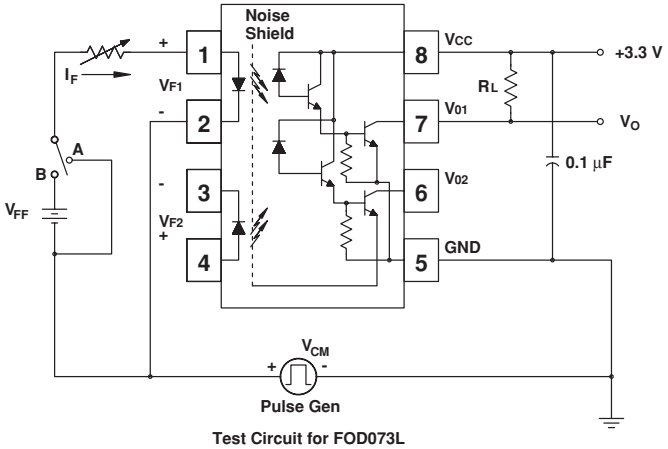


Test Circuit for FOD070L and FOD270L



Test Circuit for FOD073L

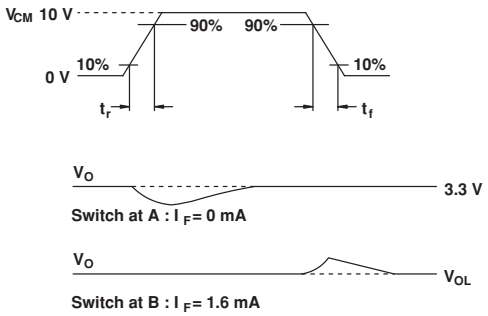


Fig. 18 Common Mode Immunity Test Circuit

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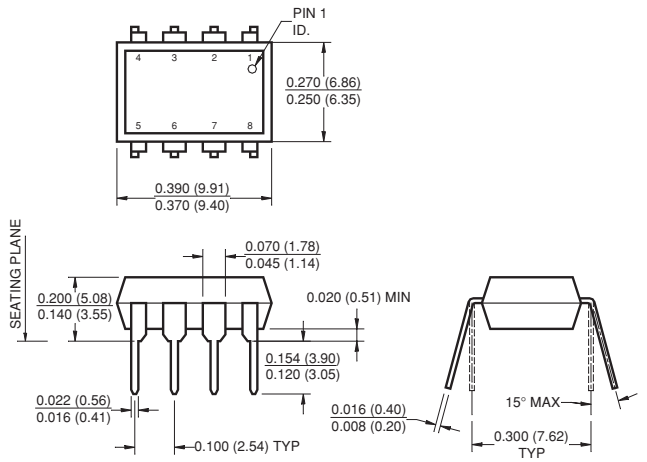
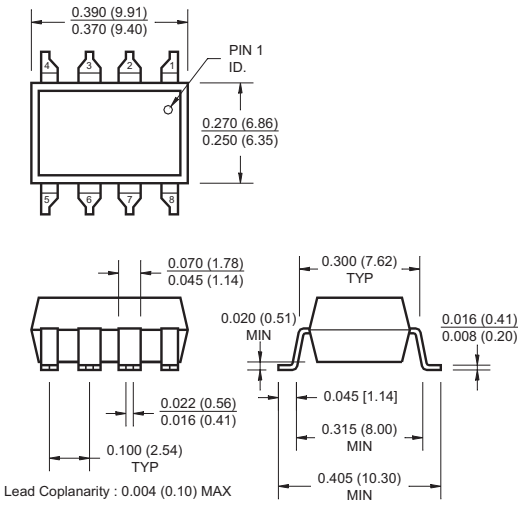
8-Pin DIP

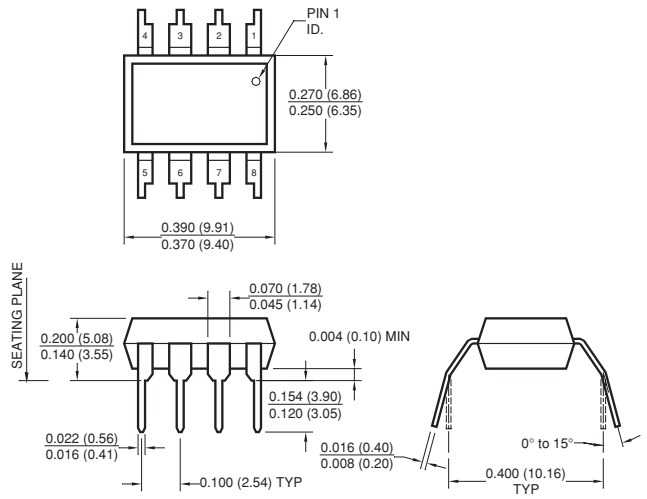
Package Dimensions (Through Hole)



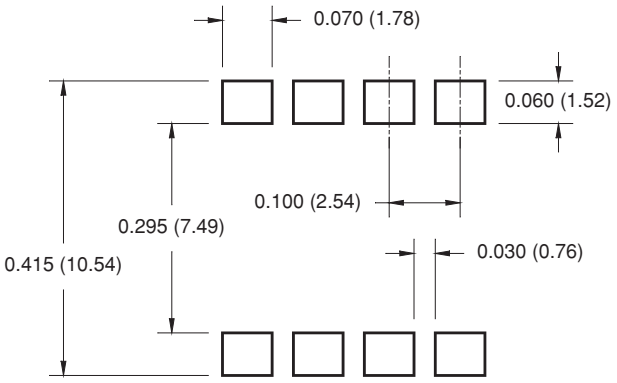
Package Dimensions (Surface Mount)



Package Dimensions (0.4"Lead Spacing)



Recommend Pad Layout for Surface Mount Leadform



NOTE
All dimensions are in inches (millimeters)

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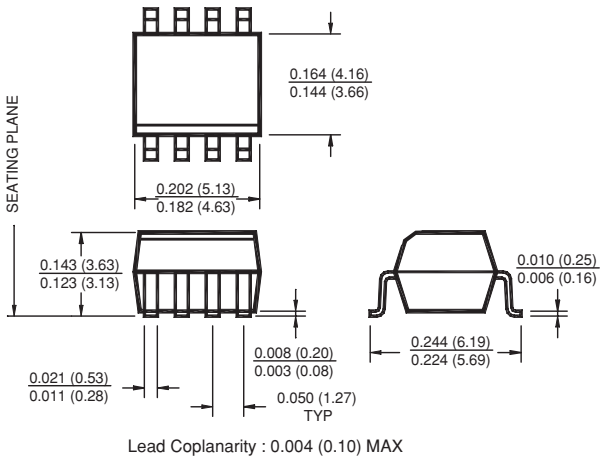
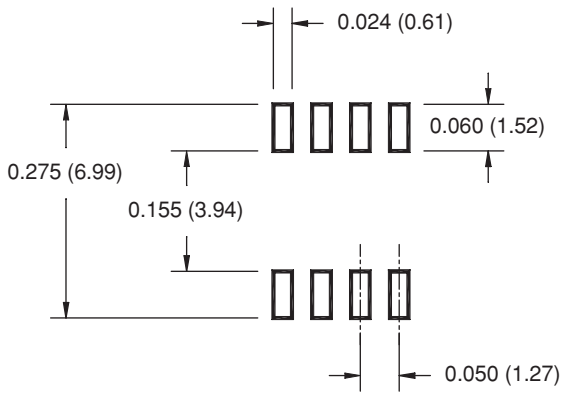
SOIC 8

Package Dimensions (Surface Mount)



Lead Coplanarity : 0.004 (0.10) MAX

Recommend Pad Layout



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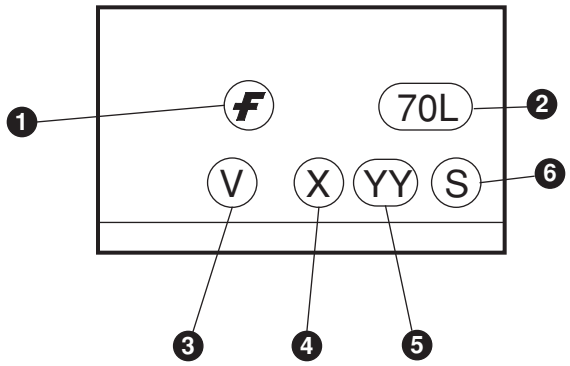
ORDERING INFORMATION

Option	Order Entry Identifier	Description
S	FOD270LS	Surface Mount Lead Bend (DIP Package Only)
SD	FOD270LSD	Surface Mount; Tape and reel (DIP Package Only) (1000 units per reel)
SV	Pending approval	Surface Mount; VDE 0884 (DIP Package Only)
SDV	Pending approval	Surface Mount; Tape and reel (DIP Package Only); VDE 0884 (1000 units per reel)
T	FOD270LT	0.4" lead spacing (DIP Package Only)
TV	Pending approval	0.4" lead spacing, VDE 0884 (DIP Package Only)
R1	FOD070LR1	Tape and reel (500 units per reel) (SOIC 8 Package only)
R1V	Pending approval	VDE, Tape and reel (500 units per reel) (SOIC 8 Package only)
R2	FOD070LR2	Tape and reel (2500 units per reel) (SOIC 8 Package only)
R2V	Pending approval	VDE 0884, Tape and reel (2500 units per reel) (SOIC 8 Package only)
V	Pending approval	VDE 0884

MARKING INFORMATION (FOD070L, FOD073L)



Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	One digit year code, e.g., ‘3’
5	Two digit work week ranging from ‘01’ to ‘53’
6	Assembly package code

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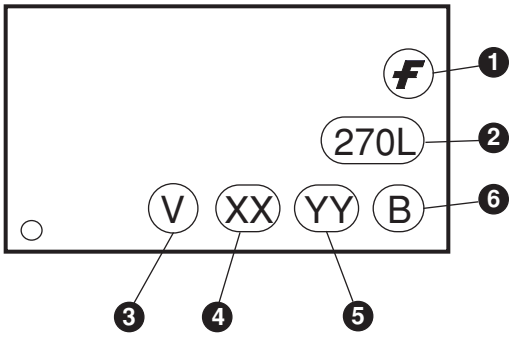
LVTTL/LVCMOS COMPATIBLE LOW INPUT CURRENT HIGH GAIN SPLIT DARLINGTON OPTOCOUPLERS

SINGLE CHANNEL: **FOD070L** **FOD270L**
DUAL CHANNEL: **FOD073L**

MARKING INFORMATION (FOD270L)



Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	Two digit year code, e.g., ‘03’
5	Two digit work week ranging from ‘01’ to ‘53’
6	Assembly package code

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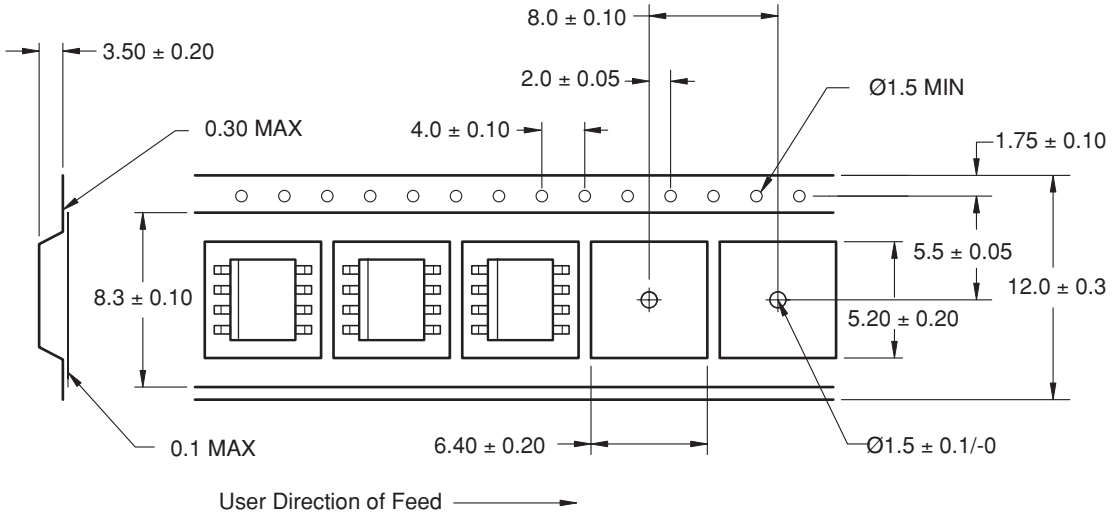
SINGLE CHANNEL: **FOD070L** **FOD270L**
DUAL CHANNEL: **FOD073L**

Carrier Tape Specifications (FOD070L and FOD073L)



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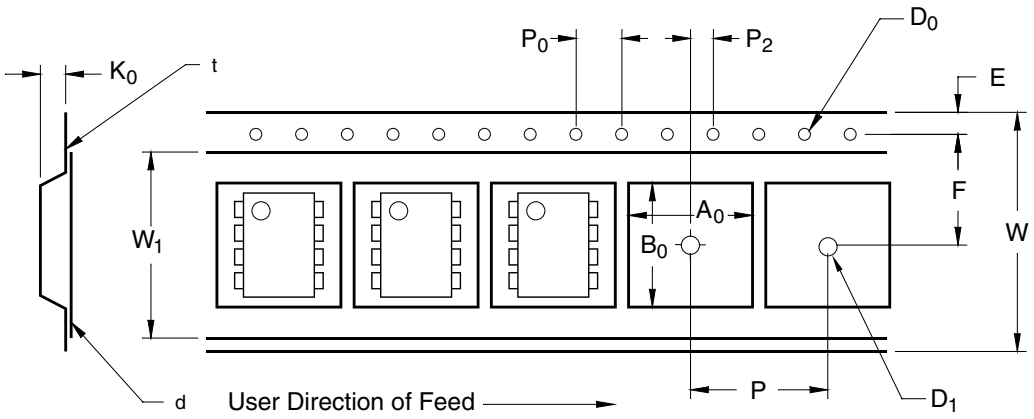
SINGLE CHANNEL: **FOD070L** **FOD270L**
DUAL CHANNEL: **FOD073L**

Carrier Tape Specifications (FOD270L)



Description	Symbol	Dimension in mm
Tape Width	W	16.0 ± 0.3
Tape Thickness	t	0.30 ± 0.05
Sprocket Hole Pitch	P_0	4.0 ± 0.1
Sprocket Hole Diameter	D_0	1.55 ± 0.05
Sprocket Hole Location	E	1.75 ± 0.10
Pocket Location	F	7.5 ± 0.1
	P_2	4.0 ± 0.1
Pocket Pitch	P	12.0 ± 0.1
Pocket Dimensions	A_0	10.30 ±0.20
	B_0	10.30 ±0.20
	K_0	4.90 ±0.20
Cover Tape Width	W_1	1.6 ± 0.1
Cover Tape Thickness	d	0.1 max
Max. Component Rotation or Tilt		10°
Min. Bending Radius	R	30

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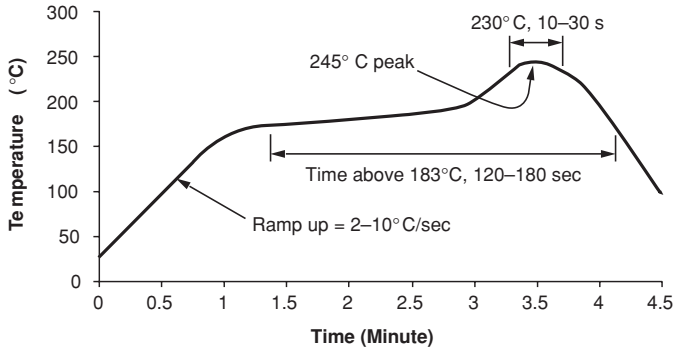
SINGLE CHANNEL: **FOD070L** **FOD270L**
DUAL CHANNEL: **FOD073L**

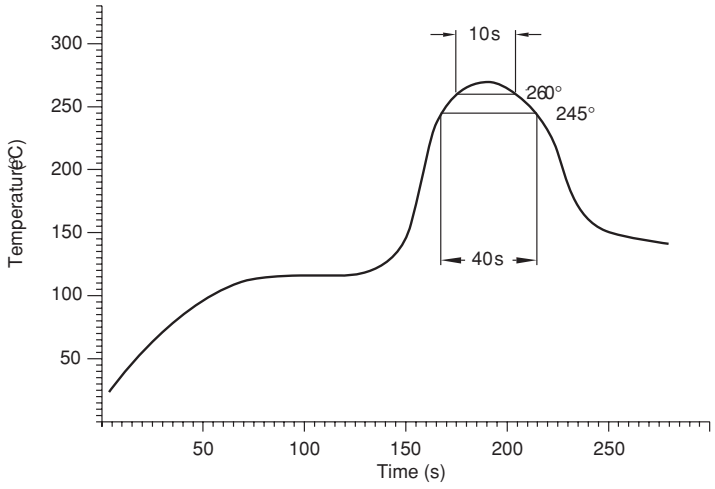
Reflow Profile (FOD070L and FOD073L)



- Peak reflow temperature: 245°C (package surface temperature)
- Time of temperature higher than 183°C for 120–180 seconds
- One time soldering reflow is recommended

Reflow Profile (FOD270L)

• Peak reflow temperature	260° C (package surface temperature)
• Time of temperature higher than 245°C	40 seconds or less
• Number of reflows	Three



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SINGLE CHANNEL: **FOD070L** **FOD270L**
DUAL CHANNEL: **FOD073L**