The MRFIC Line

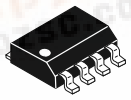
900 MHz Transmit Mixer

MRFIC2002

**900 MHz TX-MIXER
SILICON MONOLITHIC
INTEGRATED CIRCUIT**

The MRFIC2002 is a double-balanced, active mixer designed for transmitters operating in the 800 MHz to 1.0 GHz frequency range. The design utilizes Motorola's advanced MOSAIC 3 silicon bipolar RF process to yield superior performance in a cost effective monolithic device. Applications for the MRFIC2002 include CT1 and CT2 cordless telephones, GSM, remote controls, video and audio short range links, low cost cellular radios, and ISM band transmitters. A power down control is provided to minimize current drain with minimum recovery/turn-on time.

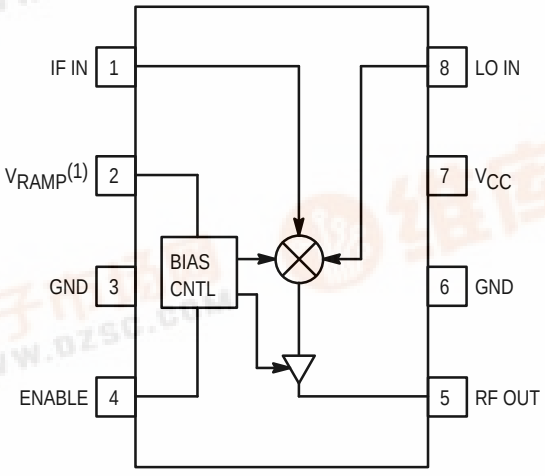
- Conversion Gain = 10 dB (Typ)
- Supply Current = 5.5 mA (Typ)
- Power Down Supply Current = 2.0 μA (Max)
- LO-RF Isolation = 25 dB (Typ)
- Low LO Drive Required = –10 dBm (Typ)
- LO Impedance Insensitive to Power Down
- No Matching Required for RF OUT Port
- All Ports are Single Ended
- Order MRFIC2002R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 12 mm, 13 inch Reel.
- Device Marking = M2002



**CASE 751-05
(SO-8)**

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	5.5	Vdc
Control Voltages	ENABLE, V_{RAMP}	5.0	Vdc
Input Power, LO and IF Ports	P_{LO}, P_{IF}	+10	dBm
Operating Ambient Temperature	T_A	–35 to +85	°C
Storage Temperature	T_{stg}	–65 to +150	°C



(1) For CT2 applications, apply ramp voltage provided in MRFIC2004. For non-CT2, leave open circuited.

Pin Connections and Functional Block Diagram

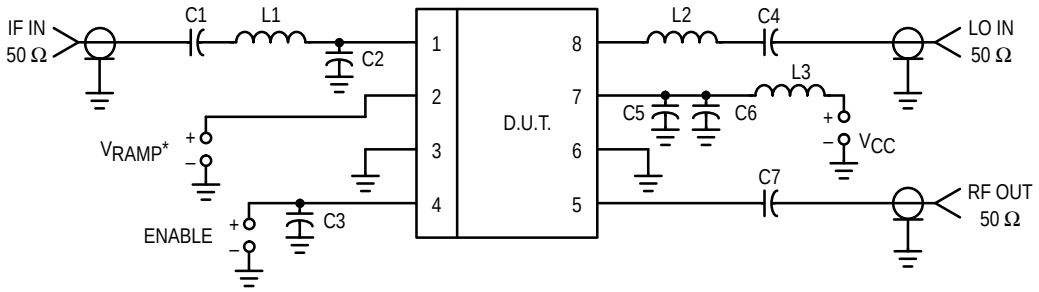
RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	2.7 to 5.0	Vdc
Control Voltage Ranges	ENABLE, V_{RAMP}	0 to 5.0	Vdc
RF Port Frequency Range	f_{RF}	500 to 1000	MHz
IF Port Frequency Range	f_{IF}	0 (dc) to 250	MHz

ELECTRICAL CHARACTERISTICS (V_{CC}, Enable = 3.0 V and V_{Ramp}(1) Open Circuited, P_{LO} = –7.0 dBm, IF @ 100 MHz, LO @ 1.0 GHz, RF @ 900 MHz, T_A = 25°C unless otherwise noted)

Characteristic (2)	Min	Typ	Max	Unit
Supply Current: On-Mode Supply Current: Off-Mode (Enable < 1.0 V)	— —	5.5 0.1	7.0 2.0	mA μA
Enable Response Time	—	1.0	—	μs
Conversion Gain	8.0	10	12	dB
Single Sideband Noise Figure	—	10	—	dB
Output Power at 1.0 dB Gain Compression	—	–18	—	dBm
Output Power at Saturation	–16	–14	—	dBm
LO-RF Isolation (1.0 GHz)	—	25	—	dB
LO-IF Isolation (1.0 GHz)	—	65	—	dB
IF-RF Isolation (100 MHz)	—	18	—	dB
IF-LO Isolation (100 MHz)	—	50	—	dB

NOTES:
1. For CT2 applications, apply ramp voltage provided in MRFIC2004. For non-CT2, leave open circuited.
2. All Electrical Characteristics are measured in test circuit schematic as shown in Figure 1.



C1, C3, C6 — 1000 pF Chip Capacitor
C2 — 6.8 pF Chip Capacitor
C4 — 3.9 pF Chip Capacitor
C5 — 100 pF Chip Capacitor
C7 — 5.6 pF Chip Capacitor
L1 — 270 nH Chip Inductor
L2 — 10 nH Chip Inductor
L3 — 390 nH Chip Inductor
RF Connectors — SMA Type
Board Material — Glass/Epoxy ε_r = 4.5,
Dielectric Thickness = 0.014″ (0.36 mm)

Figure 1. Test Circuit Configuration

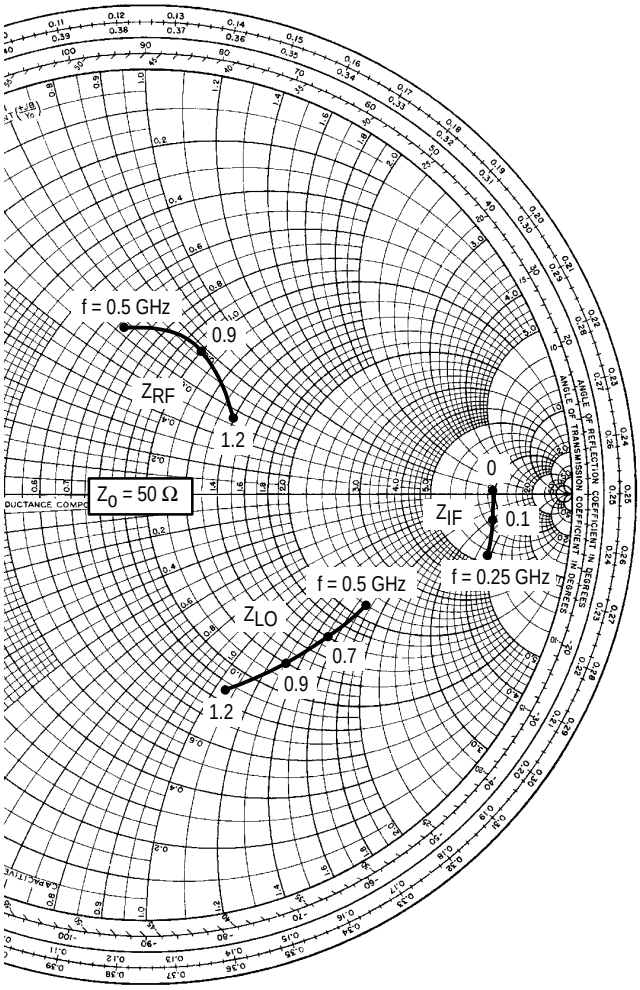


Figure 2. Port Impedances versus Frequency

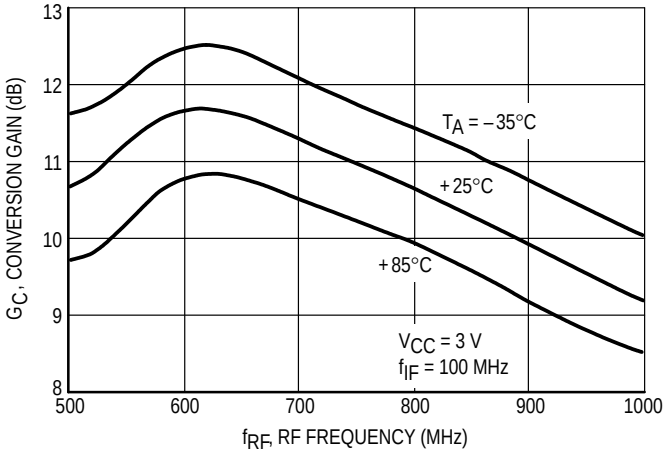


Figure 3. Gain versus RF Frequency

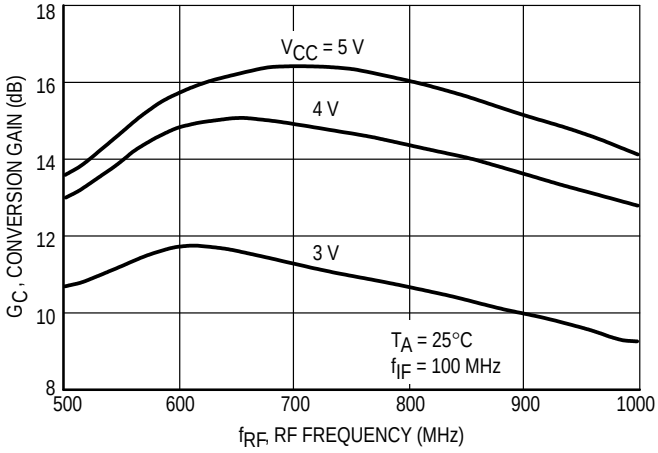


Figure 4. Gain versus RF Frequency

V_{CC} (Volts)	f (MHz)	Γ_{IF}		Γ_{RF}		Γ_{LO}	
		Mag	∠ϕ Degrees	Mag	∠ϕ Degrees	Mag	∠ϕ Degrees
3.0	50	0.83	−2.4	—	—	—	—
	100	0.82	−4.7	—	—	—	—
	150	0.82	−7.1	—	—	—	—
	200	0.81	−9.6	—	—	—	—
	250	0.81	−11.7	—	—	—	—
	500	—	—	0.42	100	0.57	−29
	600	—	—	0.41	94	0.55	−35
	700	—	—	0.40	88	0.54	−41
	800	—	—	0.39	80	0.52	−48
	900	—	—	0.36	71	0.51	−54
	1000	—	—	0.33	63	0.50	−60
	1100	—	—	0.31	55	0.49	−65
	1200	—	—	0.28	45	0.49	−70

Table 1. Deembedded Port Reflection Coefficients
(Enable = 3.0 V, Z_O = 50 Ω, T_A = 25°C)

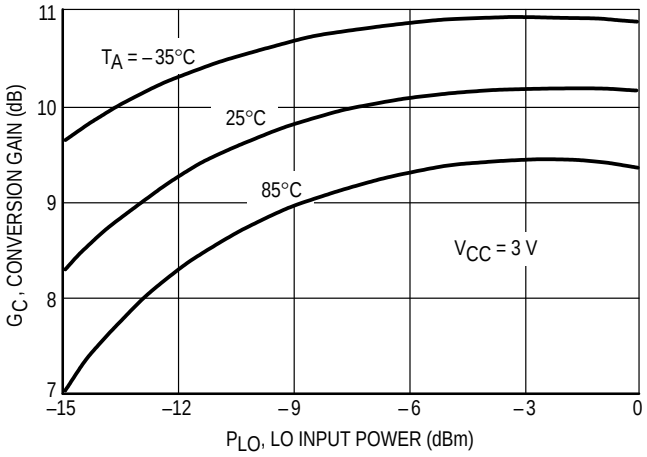


Figure 5. Gain versus LO Input Power

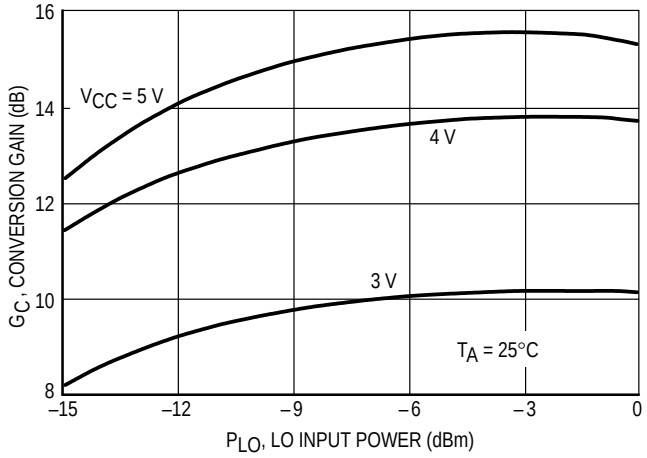


Figure 6. Gain versus LO Input Power

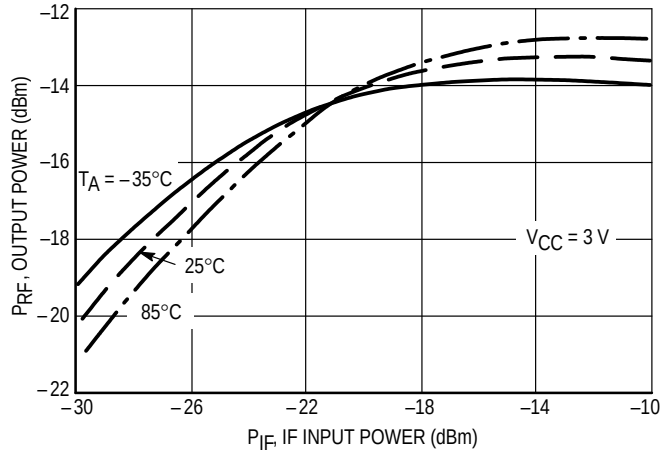


Figure 7. Output Power versus IF Input Power

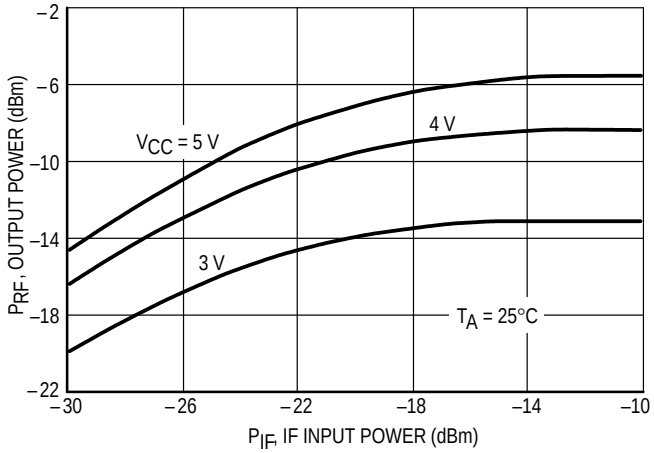


Figure 8. Output Power versus IF Input Power

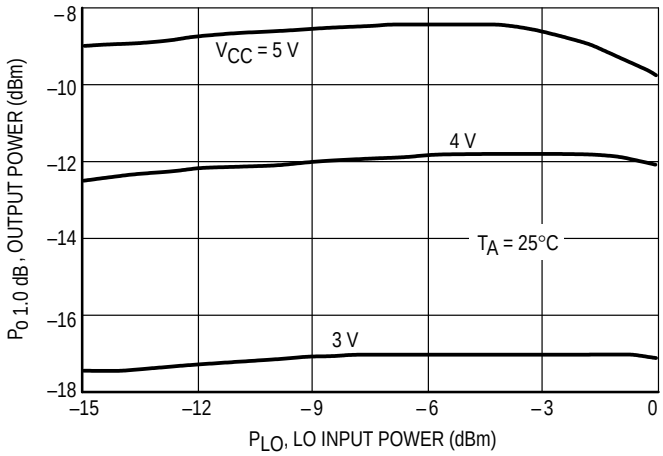


Figure 9. Output Power at 1.0 dB Gain Compression versus LO Input Power

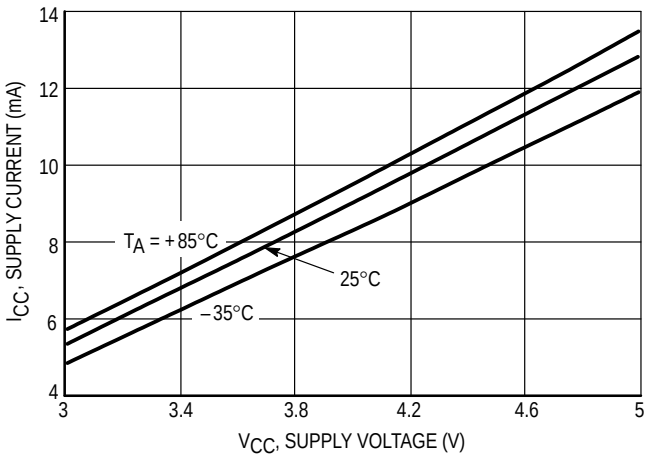


Figure 10. I_{CC} versus V_{CC}

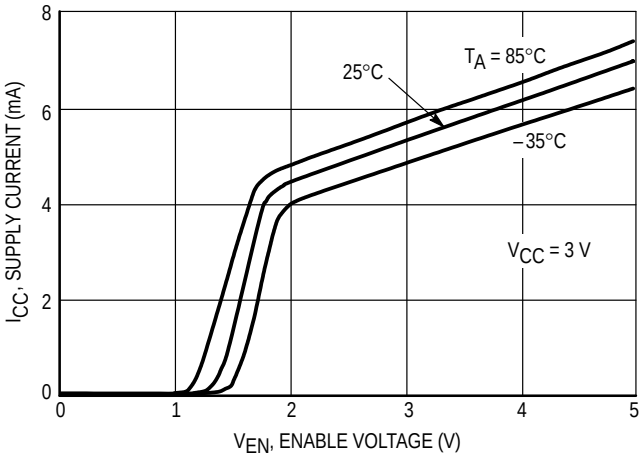


Figure 11. I_{CC} versus Enable Voltage

APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC2002 was designed to have excellent LO and spurious rejection. This is accomplished by using a double-balanced configuration and using a symmetrical die layout.

To eliminate the need for external baluns or decoupling elements, the unused LO and IF ports are decoupled internally. Only one of the RF outputs is used, eliminating the need for an external balun on the RF port as well. Also, the RF port is buffered to provide a 50 ohm output impedance. External matching is required for the LO and IF ports.

To minimize current drain in various TDD/TDMA systems, two methods of enabling/disabling the MRFIC2002 are provided: one that is TTL/CMOS compatible and one that is triggered from a ramp, such as the one provided in the MRFIC2004. The former method must be used if a ramp is not available. The latter method is more desirable since the MRFIC2002 can remain off during guard times and while in idle mode.

THEORY OF OPERATION

Matching the LO port to 50 ohms can be done several ways. The recommended approach is a series inductor as close to the IC as possible. The inductor value is small enough (~8–15 nH depending on LO frequency) to be printed on the board. A DC block is required and should not be placed between the inductor and IC since this will prevent the inductor from being placed close enough to the IC to provide a good match.

The IF port is approximately 500 ohms resistive in parallel with 1.3 pF of capacitance. If 50 ohms is the desired IF port impedance, a shunt capacitor followed by a series inductor will provide the transformation. A DC block is required and can be placed on either side of the matching network.

The RF port is nearly 50 ohms resistive in series with a small amount of inductive reactance, which results in an 8–11 dB return loss. However, a series 5.6 pF capacitor placed as close to the IC as possible will typically provide greater than a 15 dB return loss. The series capacitor also serves as a DC block which is required.

Supply decoupling must be done as close to the IC as possible. A 1000 pF capacitor is recommended. An additional 100 pF capacitor and an RF choke are recommended to keep the RF and LO signals off the supply line.

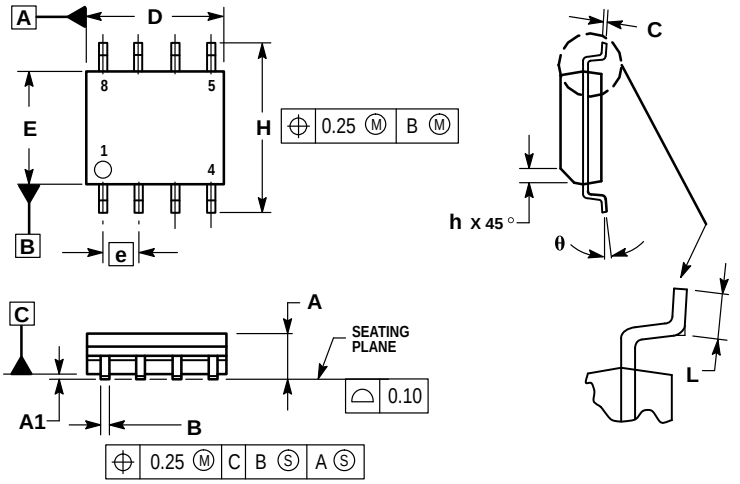
For systems that use a ramp, like the one provided in the MRFIC2004, enabling/disabling can be done by applying the ramp voltage to the V_{RAMP} pin which trips the IC between 0.6 and 1.0 volts. The Enable pin must either be tied high or to the inverse of the receiver enable control line, RXEN. An inverter is provided in the MRFIC2004 to invert RXEN.

For systems that do not use a ramp, the V_{RAMP} pin can be left open circuited and enabling/disabling the MRFIC2002 can be done with its TTL/CMOS compatible Enable pin. The trip point is between 1.0 and 2.0 volts.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a “TF” suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

CASE 751–05
ISSUE S

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