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J111 J112 J113

N-CHANNEL SILICON JUNCTION FIELD EFFECT TRANSISTORS

MICRO ELECTRONICS

J111, J112, J113 are N-channel silicon junction field effect transistors designed for analog switching, choppers and commutators applications.

TO-92

DSG

ABSOLUTE MAXIMUM RATINGS

Gate-Source Voltage	V_{GS}	-35V
Gate Current	I_G	50mA
Total Power Dissipation (T_A=25°C)	P_{tot}	350mW
Power Derating (to 125°C)		3.5mW/°C
Operating Junction & Storage Temperature	Tj, Tstg	-55 to +125°C

ELECTRICAL CHARACTERISTICS (T_A=25°C)

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS	
Gate-Source Breakdown Voltage		BV_{GSS}	-35			V	I_G=-1μA	V_{DS}=0
Gate Reverse Current (note 1)		I_{GSS}			-1	nA	V_{GS}=-15V	V_{DS}=0
Drain Saturation Current	J111	I_{DSS} *	20			mA	V_{DS}=15V	V_{GS}=0
	J112		5			mA	V_{DS}=15V	V_{GS}=0
	J113		2			mA	V_{DS}=15V	V_{GS}=0
Drain Cutoff Current (note 1)		$I_{D(off)}$			-1	nA	V_{DS}=5V	V_{GS}=10V
Gate-Source Pinchoff Voltage		V_p						
	J111		-3		-10	V	I_D=1μA	V_{DS}=5V
	J112		-1		-5	V	I_D=1μA	V_{DS}=5V
	J113		-0.5		-3	V	I_D=1μA	V_{DS}=5V
Drain-Source On Resistance	J111	$r_{DS(on)}$			30	Ω	V_{GS}=-10V	V_{DS}≤0.1V
	J112				50	Ω	V_{GS}=-10V	V_{DS}≤0.1V
	J113				100	Ω	V_{GS}=-10V	V_{DS}≤0.1V
Turn On Delay Time		$t_{d(on)}$		7		ns		
Rise Time		t_r		6		ns		
Turn Off Delay Time		$t_{d(off)}$		20		ns		
Fall Time		t_f		15		ns		

note 1 : Approximately doubles for every 10°C increase in T_A.

* Pulse Test : Pulse Width = 0.3ms, Duty Cycle = 1%

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