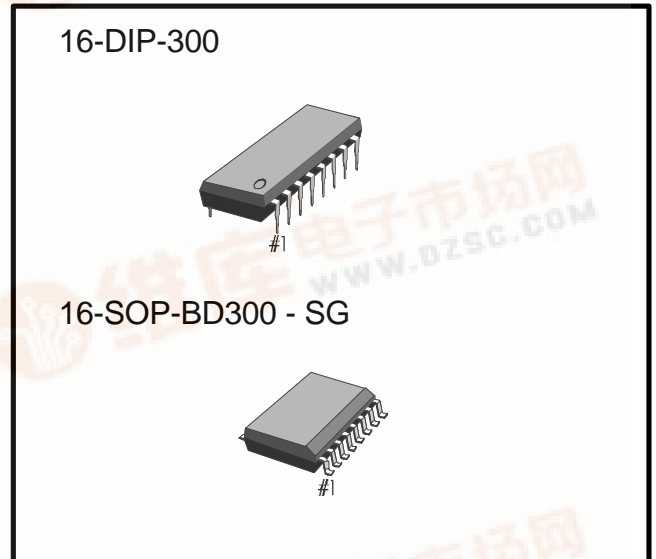


KS8620

1 Chip CODEC for Digital Answering phone

INTRODUCTION

The KS8620 consists of on-chip PCM encoders, decoders (PCM CODECs) and PCM line filter. This device provide all the functions required to interface a full-duplex voice telephone circuit, digital answering phone. This device is designed to perform the transmit encoding and receive decoding as well as the transmit and receive filtering function in PCM system. Also it is intended to be used at the analog termination of a PCM line / trunk. This device provide the Band pass filtering of the analog signals prior to encoding and after decoding. This combination device performs the encoding and decoding of voice and call progress tones as well as the signaling and supervision information.



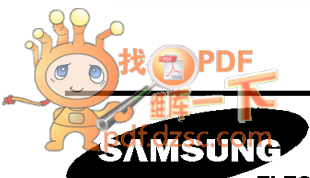
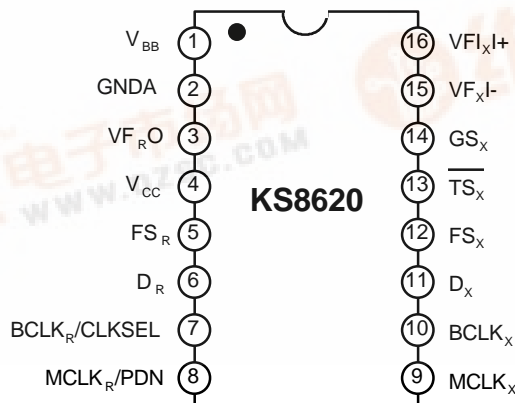
ORDERING INFORMATION

| Device | Package | Operating Temperature |
|---------|--------------------|-----------------------|
| KS8620N | 16-DIP-300 | 0°C ~ + 70°C |
| KS8620D | 16-SOP- BD300 - SG | |

FEATURES

- Complete CODEC and filtering system
- Encoding / Decoding : 8 bits μ -law PCM
- On-chip auto zero, sample and hold, and precision voltage references
- Low power dissipation : 60mW (operating)
3mW (standby)
- $\pm 5V$ operation
- TTL or CMOS compatible
- Automatic power down

PIN CONFIGURATION



BLOCK DIAGRAM

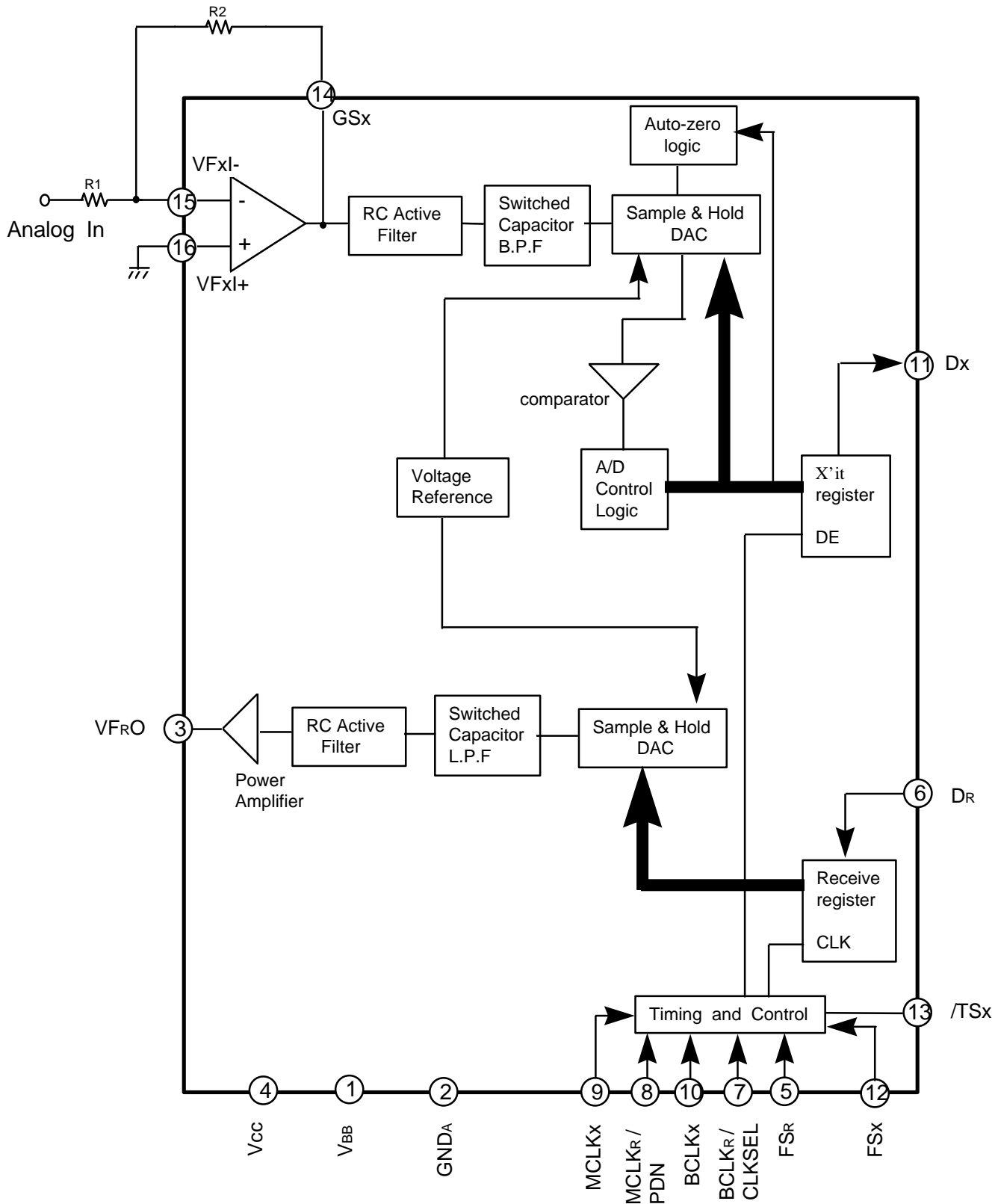


Fig 1. Block Diagram

PIN DESCRIPTION

| Pin No | Symbol | Description |
|--------|-------------------------------|--|
| 1 | V _{BB} | V _{BB} = -5V ± 5% |
| 2 | GND _A | Analog ground |
| 3 | VF _{RO} | Analog output of the receiver filter |
| 4 | V _{CC} | V _{CC} = +5V ± 5% |
| 5 | FS _R | Receive frame sync pulse. 8KHz pulse train. |
| 6 | D _R | PCM data input |
| 7 | BCLK _R / CLKSEL | Logic input which selects either 1.536MHz / 1.544MHz or 2.048MHz for master clock in normal operation and BCLK _x is used for both TX and RX directions. Alternately direct clock input available, vary from 64KHz to 2.048MHz. |
| 8 | MCLK _R / PDN | When MCLK _R is connected continuously high, the device goes powered down. Normally connected continuously low, MCLK _x is selected for all DAC timing. Alternately direct 1.536MHz / 1.544MHz or 2.048MHz clock input is available. |
| 9 | MCLK _X | 1.536MHz / 1.544MHz or 2.048MHz clock input is available |
| 10 | BCLK _X | May be vary from 64KHz 2.048MHz, but BCLK _x is externally tied with MCLK _x in normal operation. |
| 11 | D _X | PCM data output. |
| 12 | FS _X | TX frame sync pulse. 8KHz pulse train. |
| 13 | TS _X | Changed from high to low during the encoder timeslot. Open drain output. |
| 14 | GS _X | Analog output of the TX input amplifier. Used to set gain through external resistor between pin 14 to pin 15. |
| 15 | VF _{XI-} | Inverting input stage of the TX analog signal. |
| 16 | VF _{XI+} | Non-inverting input stage of the TX analog signal. |

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

| Characteristic | Symbol | Value | Unit |
|---|-------------------|---|------|
| Positive Supply Voltage | V _{CC} | +7 | V |
| Negative Supply Voltage | V _{BB} | -7 | V |
| Voltage at any Analog Input or Output | V _{I(A)} | V _{CC} + 0.3 to V _{BB} - 0.3 | V |
| Voltage at any Digital Input or Output | V _{I(D)} | V _{CC} + 0.3 to GND _A - 0.3 | V |
| Operating Temperature Range | T _a | 0 to 70 | °C |
| Storage Temperature Range | T _{STG} | -65 to +150 | °C |
| Lead Temperature Range (soldering , 10 sec) | T _{LEAD} | 300 | °C |

ELECTRICAL CHARACTERISTICS(Unless otherwise specified : Ta = 0°C to 70°C , Vcc = 5V ±5%, VBB = -5V ±5%, GND_A = 0V)

| Characteristic | System | Test Conditions | Min | Typ | Max | Unit |
|--|------------------------|--|--------|------|-----|-------|
| Power Dissipation | | | | | | |
| Power down Current | I _{CC (down)} | No Load | | 0.5 | 3.0 | mA |
| | I _{BB (down)} | No Load | | 0.05 | 1.0 | |
| Active Current | I _{CC (A)} | No Load | | 6.0 | 10 | mA |
| | I _{BB (A)} | No Load | | 6.0 | 10 | |
| Digital Interface | | | | | | |
| Input Low Voltage | V _{IL} | | | | 0.6 | V |
| Input High Voltage | V _{IH} | | 2.2 | | | V |
| Input Low Current | I _{IL} | GND _A < V _{IN} < V _{IL} , all digital input | -15 | | 15 | uA |
| Input High Current | I _{IH} | V _{IH} < V _{IN} < V _{CC} | -15 | | 15 | uA |
| Output Low Voltage | V _{OL} | D _X , I _L = 3.2 mA | | | 0.4 | V |
| | | SIG _R , I _L = 1.0 mA | | | 0.4 | |
| | | /TS _X , I _L = 3.2 mA , open drain | | | 0.4 | |
| Output High Voltage | V _{OH} | D _X , I _H = -3.2 mA | 2.4 | | | V |
| | | SIG _R , I _H = -1.0 mA | 2.4 | | | |
| Output Current in High impedance state (Tri - state) | I _{OH(HZ)} | D _X , GND _A < V _O < V _{CC} | -15 | | 15 | uA |
| Analog Interface with Receiver Filter | | | | | | |
| Output Resistance | R _O | pin VF _{RO} | | 1 | 3 | Ω |
| Load Resistance | R _L | VF _{RO} = + / - 2.5V | 600 | | | Ω |
| Load Capacitance | C _L | | | | 500 | pF |
| Output DC offset voltage | V _{OO(RX)} | | -200 | | 200 | mV |
| Analog Interface with Transmit input Amp | | | | | | |
| Input Leakage Current | I _{LKG} | -2.5V < V < +2.5V , VF _{XI+} or VF _{XI-} | -200 | | 200 | nA |
| Input Resistance | R _I | -2.5V < V < +2.5V , VF _{XI+} or VF _{XI-} | 10 | | | MΩ |
| Output Resistance | R _O | closed loop , unity gain | | 1 | 3 | Ω |
| Load Resistance | R _L | GS _X | 10 | | | KΩ |
| Load Capacitance | C _L | GS _X | | | 50 | pF |
| Output Dynamic Range | V _{OD(TX)} | GS _X , R _L < 10KΩ | +/-2.8 | | | V |
| Voltage Gain | G _V | VF _{XI+} to GS _X | 5,000 | | | V / V |
| Unity Gain bandwidth | B _W | | 1 | 2 | | MHz |
| Offset Voltage | V _{IO(TX)} | | -20 | | 20 | mV |
| Common - mode Voltage | V _{CM(TX)} | CMRR _{XA} > 60dB | -2.5 | | 2.5 | V |
| Common mode rejection ratio | CMRR | DC test | 55 | | | dB |
| Power supply rejection ratio | PSRR | DC test | 55 | | | dB |

TIMING CHARACTERISTICS(Unless otherwise specified : Ta = 0°C to 70°C, Vcc = 5V ±5%, VBB = -5V ±5%, GND_A = 0V)

| Characteristic | System | Test Conditions | Min | Typ | Max | Unit |
|---|-----------------------|---|-----|-------|--------|------|
| Frequency of Master Clock | f _{MCK} | Depends on the device used and the BCLK _R /CLKSEL pin. MCLK _X and MCLK _R | | 1.536 | | MHz |
| | | | | 1.544 | | |
| | | | | 2.048 | | |
| Rise time of Bit Clock | t _{R(BCK)} | t _{PB} = 488ns | | | 50 | nS |
| Fall Time of Bit Clock | t _{F(BCK)} | t _{PB} = 488ns | | | 50 | nS |
| Hold Time for Bit Clock low to Frame sync | t _{H(LFS)} | Long Frame only | 0 | | | nS |
| Hold Time for Bit Clock High to Frame sync | t _{H(HFS)} | Short Frame only | 0 | | | nS |
| Set-up Time from Frame sync to Bit Clock low | t _{SU(FBCL)} | Long Frame only | 80 | | | nS |
| Delay time from BCLK _X High to data valid | t _{D(HDV)} | Load = 150pF + 2 LSTTL loads | 0 | | 180 | nS |
| Delay time to /TS _X low | t _{D(TSXL)} | Load = 150pF + 2 LSTTL loads | | | 140 | nS |
| Delay time from BCLK _X low to data output disable | t _{D(LDD)} | | 50 | | 165 | nS |
| Delay Time to valid data from FS _X or BCLK _X . | t _{D(VD)} | CL = 0 pF to 150 pF Whichever comes later. | 20 | | 165 | nS |
| Set-up Time from D _R valid to BCLK _{X/R} low | t _{SU(DRBL)} | | 50 | | | nS |
| Hold time from BCLK _{X/R} low to D _R invalid | t _{H(BLDR)} | | 50 | | | nS |
| Set-up time from FS _{X/R} to BCLK _{X/R} low | t _{SU(FBLS)} | Short Frame sync pulse (1 or 2 bit clock periods long) : note1 | 50 | | | nS |
| Width of master clock High | t _{W(MCKH)} | MCLK _X and MCLK _R | 160 | | | nS |
| Width of master clock Low | t _{W(MCKL)} | MCLK _X and MCLK _R | 160 | | | nS |
| Rise Time of Master clock | t _{R(MCK)} | MCLK _X and MCLK _R | | | 50 | nS |
| Fall Time of Master clock | t _{F(MCK)} | MCLK _X and MCLK _R | | | 50 | nS |
| Set-up time from BCLK _X High (FS _X in Long Frame Sync mode) to MCLK _X falling edge | t _{SU(BHMF)} | 1 st bit clock after the leading edge of FS _X | 50 | | | nS |
| Period of Bit Clock | t _{CK} | | 485 | 488 | 15,725 | nS |
| Width of Bit clock High | t _{W(BCKH)} | V _{IH} = 2.2V | 160 | | | nS |
| Width of Bit clock Low | t _{W(BCKL)} | V _{IL} = 0.6V | 160 | | | nS |
| Hold time from BCLK _{X/R} to FS _{X/R} low | t _{H(BLFL)} | Short Frame sync pulse (1 or 2 bit clock periods long) : note1 | 100 | | | nS |

TRANSMISSION CHARACTERISTICS

(Unless otherwise specified : Ta = 0°C to 70°C, Vcc = 5V ±5%, VBB = -5V ±5%, GND_A = 0V, f = 1.02KHz
Vin = 0dBm0, transmit input amplifier connected for unity-gain, non-inverting)

| Characteristic | System | Test Conditions | Min | Typ | Max | Unit |
|--|--------------------------------|--|-----------------------|--------|---|-----------------|
| Amplitude Response | | | | | | |
| Receive Gain, Absolute | $G_{V(ARX)}$ | Ta=25°C, Vcc = 5V, VBB = -5V Input = Digital code sequence for 0dBm0 signal at 1020Hz | -1.5 | | 1.5 | dB |
| Receive Gain, Relative to $G_{V(RRX)}$ | $G_{V(RRX)}$ | f = 0Hz to 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz | -0.6 -0.55 -1.5 | | 0.5 0.5 1.5 | dB |
| Absolute Receive Gain Variations with temperature | $\Delta G_{V(ARX)} / \Delta T$ | Ta = 0°C to 70°C | | | ± 0.1 | dB |
| Receive Gain Variations with level | $\Delta G_{V(RXL)}$ | Sinusoidal test method; reference input PCM code correspond to an ideally encoded -10dBm0 signal PCM level = -40dBm0 to +3dBm0 PCM level = -50dBm0 to -40dBm0 | -0.4 -0.8 | | 0.4 0.8 | dB |
| Receive output drive level | | R _L = 600Ω | -2.5 | | 2.5 | V |
| Absolute level | $V_{O(RX)}$ V_{AL} | Norminal 0dBm0 level is same as 4 dBm (600Ω) | | 1.2276 | | Vrms |
| Max overload level | $V_{OL(MAX)}$ | Max overload level (3.17dBm0) | | 2.501 | | V _{PK} |
| Transmit gain, absolute | $G_{V(ATX)}$ | Ta = 25°C, Vcc = 5V, VBB = -5V Input at GSx = 0dBm0 at 1020Hz | -1.5 | | 1.5 | dB |
| Transmit gain, relative to $G_{V(ATX)}$ | $G_{V(RTX)}$ | f = 16 Hz f = 50 Hz f = 60 Hz f = 200 Hz f = 300 Hz - 3000Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz and above, mesaure response from 0 Hz to 4 KHz | | | -35 -25 -21 -0.5 0.5 0.5 -1.5 -10 -25 | dB |

TRANSMISSION CHARACTERISTICS (Continued)

| Characteristic | System | Test Conditions | Min | Typ | Max | Unit |
|--|--------------------------------|--|--------------|-----|--|--------|
| Absolute transmit gain variations with temperature | $\Delta G_{V(ATX)} / \Delta T$ | Ta = 0°C to 70°C | | | ± 0.1 | dB |
| Transmit gain variations with level | $\Delta G_{V(TXL)}$ | Sinusoidal test method ; Reference level = -10dBm0 VF _X l + = -40dBm0 to +3dB0 VF _X l + = -50dBm0 to -40dB0 | -0.4 -0.8 | | 0.4 0.8 | dB |
| Envelope Delay Distortion with Frequency | | | | | | |
| Receive Delay, Absolute | t _{D(ARX)} | f = 1600Hz | | | 200 | μs |
| Receive Delay, Relative to t _{D(ARX)} | t _{D(RRX)} | f = 500Hz - 1000Hz f = 1000Hz - 1600Hz f = 1600Hz - 2600Hz f = 2600Hz - 2800Hz f = 2800Hz - 3000Hz | -40 -30 | | 90 125 175 | μs |
| Transmit Delay, Absolute | t _{D(ATX)} | f = 1600Hz | | | 315 | μs |
| Transmit Delay, Relative to t _{D(ATX)} | t _{D(RTX)} | f = 500Hz - 600Hz f = 600Hz - 800Hz f = 800Hz - 1000Hz f = 1000Hz - 1600Hz f = 1600Hz - 2600Hz f = 2600Hz - 2800Hz f = 2800Hz - 3000Hz | | | 220 145 75 40 75 105 155 | μs |
| Noise | | | | | | |
| Receive Noise, C Message Weighted | N _{RXC} | PCM code equals alternating positive and negative zero, KS8620 | | | 18 | dBrnC0 |
| Transmit Noise, C Message Weighted | N _{TXC} | KS8620 | | | 15 | dBrnC0 |

TRANSMISSION CHARACTERISTICS (Continued)

| Characteristic | System | Test Conditions | Min | Typ | Max | Unit |
|---|--|--|----------------------|-----|------------|----------|
| Noise, Single Frequency | NSF | f = 0KHz to 100KHz, loop around measurement, VFxl+ = 0Vrms | | | -53 | dBm0 |
| Positive Power Supply Rejection, Transmit | PSRR _(PTX) | VFxl+ = 0 Vrms, V _{CC} = 5.0 V _{DC} + 100mVrms f = 0KHz - 50KHz | 25 | | | dB |
| Negative Power Supply Rejection, Transmit | PSRR _(NTX) | VFxl+ = 0 Vrms, V _{BB} = -5.0 V _{DC} + 100mVrms f = 0KHz - 50KHz | 25 | | | dB |
| Positive Power Supply Rejection, Receive | PSRR _(PRX) | PCM code equals positive zero V _{CC} = 5.0V _{DC} + 100mVrms f = 0Hz - 4000Hz f = 4KHz - 25KHz | 25 25 | | | dB dB |
| Negative Power Supply Rejection, Receive | PSRR _(NRX) | PCM code equals positive zero V _{BB} = -5.0V _{DC} + 100mVrms f = 0Hz - 4000Hz f = 4KHz - 25KHz | 25 25 | | | dB dB |
| Spurious Out-Band Signals at the Channel Output | SOS | Loop around measurement, 0dBm0, 300Hz - 3400Hz input PCM applied to D _R , Measure individual image signals at V _{FRO} 4600Hz -7600Hz 7600Hz - 100,000Hz | | | -28 -35 | dB |
| Distortion | | | | | | |
| Signal to Total Distortion Transmit or Receive Half-Channel | THD _{TX} THD _{RX} | Sinusoidal test method ; level = 3.0dBm0 = 0dBm0 to 30dBm0 = -40dBm0 XMT RCV | 28 30 25 25 | | | dB |

TRANSMISSION CHARACTERISTICS (Continued)

| Characteristic | System | Test Conditions | Min | Typ | Max | Unit |
|---|-----------------------|---|-----|-----|----------------|------|
| Single Frequency Distortion, Transmit | THD _{SF(TX)} | | | | -41 | -dB |
| Single Frequency Distortion, Receive | THD _{SF(RX)} | | | | -41 | -dB |
| Intermodulation Distortion | THD _{IMD} | Loop around measurement, VF _{XI+} = -4dBm0 to -21dBm0, two frequencies in the range 300Hz - 3400Hz | | | -35 | -dB |
| Crosstalk | | | | | | |
| Transmit to Receive Crosstalk, 0dBm0 Transmit level | CT _(TX-RX) | f = 300Hz - 3400Hz D _R = Steady PCM code | | -90 | -75 | dB |
| Receive to Transmit Crosstalk, 0dBm0 Receive level | CT _(RX-TX) | f = 300Hz - 3400Hz, VFXI = 0V | | -90 | -70 (note1) | dB |

Note 1. CT_(RX-TX) is measured with a -40dBm0 activating signal applied at VF_{XI+}

ENCODING FORMAT AT D_X OUTPUT

| | μ -Law PCM : KS8620 |
|---|------------------------------------|
| V _{IN} (at GS _X) = + Full Scale | 1 0 0 0 0 0 0 0 |
| V _{IN} (at GS _X) = 0V | 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 |
| V _{IN} (at GS _X) = - Full Scale | 0 0 0 0 0 0 0 0 |