National Semiconductor

PRELIMINARY
April 1999

LMX5080
PLLatinum™ 2.7 GHz Low Power Dual Modulus Prescaler for RF Personal Communications

General Description

The LMX5080 integrated dual modulus prescaler, is designed to be used in a synthesized local oscillator for 2.5 GHz wireless transceivers. It is fabricated using National's 0.5µ ABiCV silicon BiCMOS process. The LMX5080 contains three dual modulus prescalers. Either a 128/130, 256/158 or a 512/514 prescaler can be selected for up to 2.7 Gz RF input frequencies. The prescaler inputs can be driven either differentially, or single ended with the use of a coupling capacitor on one of the inputs to ground. The LMX5080 CMOS output is optimized to generate very stable, low switching noise output signals. The LMX5080 prescaler can be used in conjunction with a low frequency Phase Lock Loop to form a frequency synthesizer suitable for UHF transceivers. Supply voltage can range from 2.7V to 5.5V. The LMX5080 features low current consumption; typically 7.0 mA at 5V V_{CC}

The LMX5080 is available in a 8-pin Small Outline (SOP) surface mount plastic package.

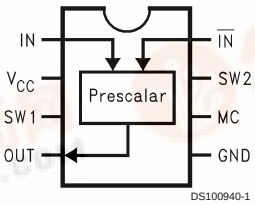
Features

- 2.7V to 5.5V operation
- Low current consumption: 7 mA (typ) @ 5V
- −40˚C to +85˚C low noise CMOS output
- Selectable dual modulus prescaler
  - 128/130
  - 256/258
  - 512/514
- 8-pin small package outline (SOP)

Applications

- 2.5 GHz wireless communications systems (ISM)
- Direct Broadcast Satellite systems (DBS)
- Cable TV tuners (CATV)

Functional Block Diagram



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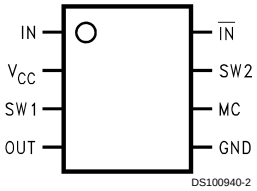
Connection Diagram

Small Outline Package (SOP)



NS Package Number M08A
Order Number LMX5080M, LMX5080MX

Pin Descriptions

Pin No.	Pin Name	I/O	Description
1	IN	I	RF small signal prescaler input. Small signal input from the voltage controlled oscillator
2	V_{CC}	—	Power Supply voltage input may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
3	SW1	I	Divide Ratio Control. CMOS logic input. Pin functionality is described in the Modulus Control Truth Table.
4	OUT	O	Prescaler Output. CMOS level output for connection to low frequency PLL input.
5	GND	—	Ground for analog and digital signals.
6	MC	I	Modulus Control Input. High impedance CMOS logic input. Pin functionality is described in the Modulus Control Truth Table.
7	SW2	I	Divide Ratio Control. High impedance CMOS logic input. Pin functionality is described in the Modulus Control Truth Table.
8	$\overline{IN}$	I	RF small signal prescaler complementary input. In single-ended mode, a bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. The IN and $\overline{IN}$ can be driven differentially when the bypass capacitor is omitted.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Parameter	Symbol	Value Min	Typ	Max	Units
Power Supply Voltage	V_{CC}	−0.3		6.5	V
Voltage on any pin with GND=0V	V_i	−0.3		V_{CC}+0.3	V
Storage Temperature Range	T_S	−65		+1.50	˚C
Lead Temp. (solder 4 sec)	T_L			+2.60	˚C

Recommended Operating Conditions (Note 1)

Parameter	Symbol	Value Min	Typ	Max	Units
Power Supply Voltage	V_{CC}	2.7		5.5	V
Operating Temperature	T_A	−40		+85	˚C

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. Electrical Characteristics document specific minimum and/or maximum performance values at specified test conditions and are guaranteed. Typ or Typical values are for informational purposes only which are based on design parameters or device characterization and are not guaranteed.

Note 2: This device is a high performance RF integrated circuit and is ESD sensitive. Handling and assembly of this device should only be done on ESD-free workstations.

Electrical Characteristics

(V_{CC} = 5.0V, T_A = −40˚C to +85˚C except as specified) (Note 1)

Symbol	Parameter	Condition	Value Min	Typ	Max	Units
I_{CC}	Power Supply Current			7		mA
V_{OH}	Output Amplitude	Z_L = 100 kΩ//10 pF V_{CC} = 2.7V to 5.5V	0.9 x V_{CC}			V
V_{OL}					0.1 x V_{CC}	V
f_{in}	Input Frequency	AC coupled. V_{CC} = 2.7V to 5.5V	100		2700	MHz
Pf_{in}	Operational Input Signal Amplitude	V_{CC} = 2.7V to 5.5V	−15		+4	dBm
f_{out}	Output Frequency		0.1		25	MHz
V_{IH}	High-level Input Voltage (MC, SW1, SW2)		0.7 x V_{CC}			V
V_{IL}	Low-level Input Voltage (MC, SW1, SW2)				0.3 x V_{CC}	V
I_{IH}	High-level Input Current (MC, SW1, SW2)	V_{IH} = 0.7 x V_{CC}		±1		uA
I_{IL}	Low-level Input Current (MC, SW1, SW2)	V_{IL} = 0.3 x V_{CC}		±1		uA
t_{Set}	Modulus Control Set-up time. (Note 3)	SW1=H, SW2=H f_{in} = 2.7 GHz		15	20	ns
IM	Input/Output Intermodulation (Note 4)	−10 dBm / 50Ω AC coupled signal delivered to input. V_{CC}=2.7V to 5.5V. MC=0, MC=1. Fin=2.3 GHz to 2.5 GHz.		−35	−30	dBc

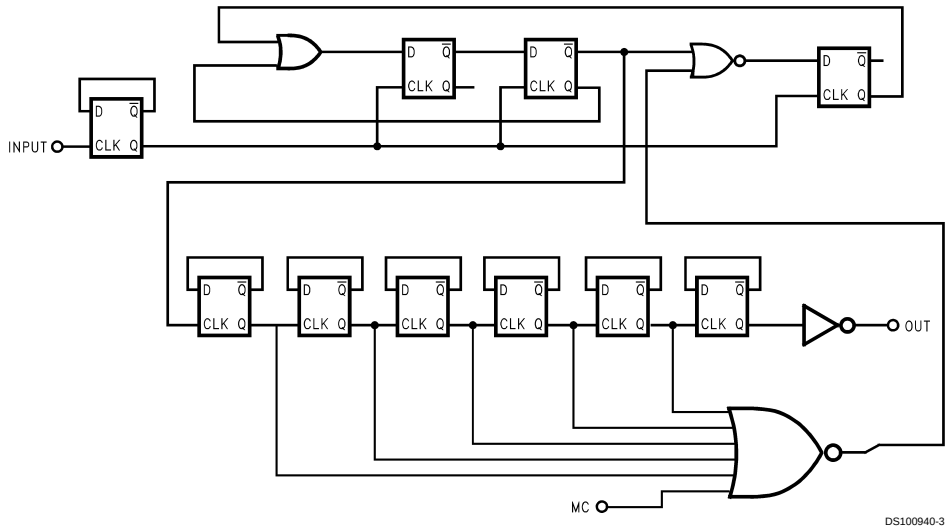
Note 3: See Timing Diagram.

Note 4: Guaranteed by design and characterization, not tested. Output frequency measured at input.

Functional Description

The basic phase-lock-loop (PLL) configuration using an external prescaler consists of a high-stability crystal reference oscillator, a prescaler such as the National Semiconductor LMX5080, a low frequency synthesizer, a voltage controlled oscillator (VCO), and a loop filter. The frequency synthesizer typically includes programmable reference [R] and feedback [N] frequency dividers, a phase detector, as well as a charge pump. The MC signal is fed back to the prescaler from either the low frequency synthesizer, or a controller to set the prescaler divide ratio to N or N+2. The prescaler output frequency is established by dividing the VCO signal down via the prescaler modulus. The RF inputs to the prescalar consist of the Fin and /Fin input pins which are complementary inputs to a differential pair amplifier. This configuration can operate to 2 GHz with an input sensitivity of −15 dBm.

Block Diagram



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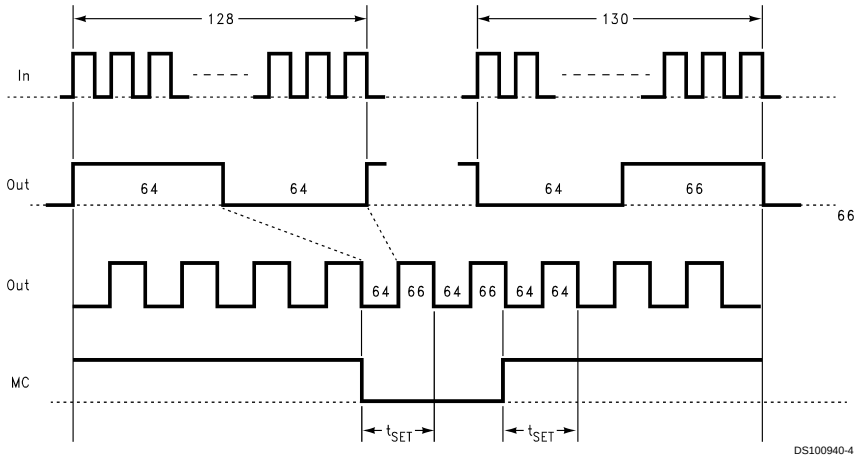
Modulus Control Truth Table

SW1	SW2	MC	Divide Ratio
H	H	H	1/128
H	H	L	1/130
H	L	H	1/256
L	H	H	1/256
H	L	L	1/258
L	H	L	1/258
L	L	H	1/512
L	L	L	1/514

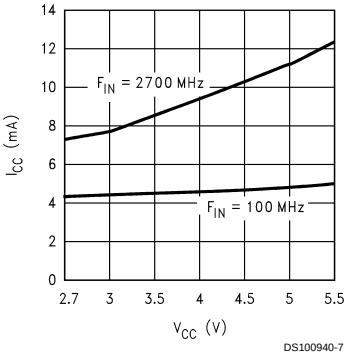
Note: SW1, SW2, MC: H = 0.7 x V_{CC}, L = 0.3 x V_{CC}.

Timing Diagram



Typical Performance Characteristics

I_{CC} vs V_{CC}
N = 1/128, T_A = 25˚C



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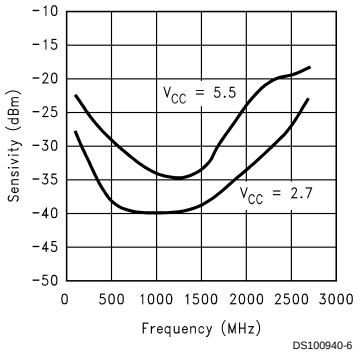
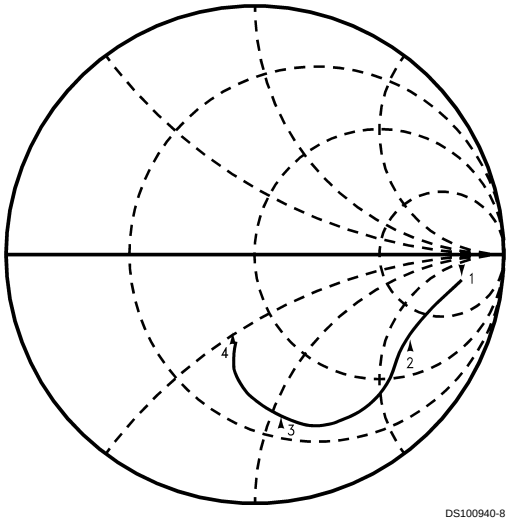
RF Input Sensitivity vs Frequency



DS100940-6

Input Impedance (S11) vs Frequency
V_{CC} = 2.7V to 5.5V, f_{in} = 100 MHz to 2.7 GHz



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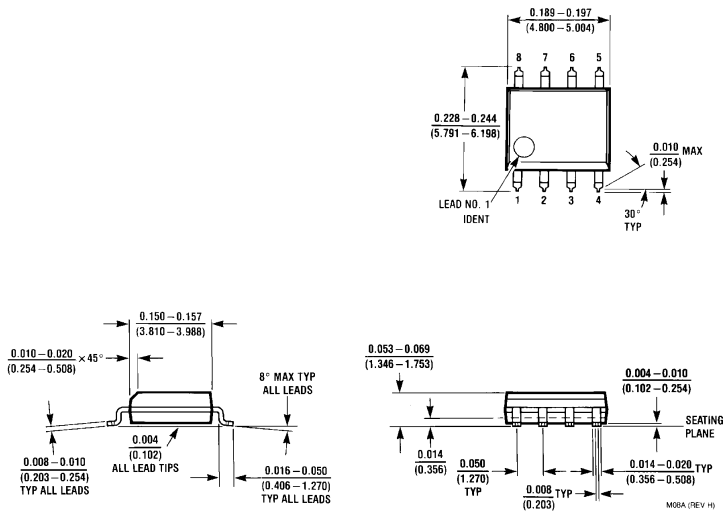
Marker 1 = 100 MHz, Real = 364, I_{mag} = −253
Marker 2 = 1 GHz, Real = 104, I_{mag} = −136
Marker 3 = 2 GHz, Real = 26, I_{mag} = −53
Marker 4 = 2.7 GHz, Real = 36, I_{mag} = −23

Physical Dimensions inches (millimeters) unless otherwise noted



8 Lead (0.150” Wide) Molded Small Outline Package, JEDEC
Order Number LMX5080M
For Tape and Reel
Order Number LMX5080MX
NS Package Number M08A

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National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507