November 1990
Edition 5.0

DATA SHEET

FUJITSU

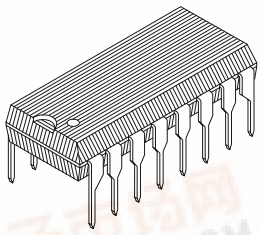
MB1502

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

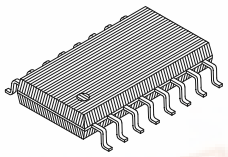
LOW POWER SERIAL INPUT PLL SYNTHESIZER WITH 1.1 GHz PRESCALER

The Fujitsu MB1502, utilizing BI-CMOS technology, is a single chip serial input PLL synthesizer with pulse-swallow function. The MB1502 contains a 1.1GHz two modulus prescaler that can select of either 64/65 or 128/129 divide ratio, control signal generator, 16-bit shift register, 15-bit latch, programmable reference divider (binary 14-bit programmable reference counter), 1-bit switch counter, phase comparator with phase conversion function, charge pump, crystal oscillator, 19-bit shift register, 18-bit latch, programmable divider (binary 7-bit swallow counter and binary 11-bit programmable counter) and analog switch to speed up lock up time.

It operates supply voltage of 5V typ. and achieves very low supply current of 8mA typ. realized through the use of Fujitsu Advanced Process Technology.



Plastic Package
DIP-16P-M04

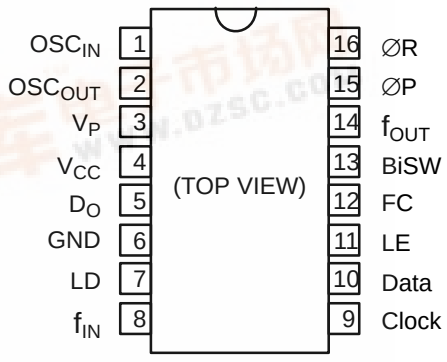


Plastic Package
FPT-16P–M06

FEATURES

- High operating frequency: $f_{IN\ MAX}$=1.1GHz ($V_{IN\ MIN}$=10dBm)
- Pulse swallow function: 64/65 or 128/129
- Low supply current: I_{CC}=8mA typ.
- Serial input 18-bit programmable divider consisting of:
  — Binary 7-bit swallow counter: 0 to 127
  — Binary 11-bit programmable counter: 16 to 2047
- Serial input 15-bit programmable reference divider consisting of:
  — Binary 14-bit programmable reference counter: 8 to 16383
  — 1-bit switch counter (SW) sets divide ratio of prescaler
- On-chip analog switch achieves fast lock up time
- 2 types of phase detector output
  — On-chip charge pump (Bipolar type)
  — Output for external charge pump
- Wide operating temperature: –40°C to +85°C
- 16-pin Plastic DIP Package (Suffix: —P)
  16-pin Plastic Flat Package (Suffix: —PF)

Pin Assignment



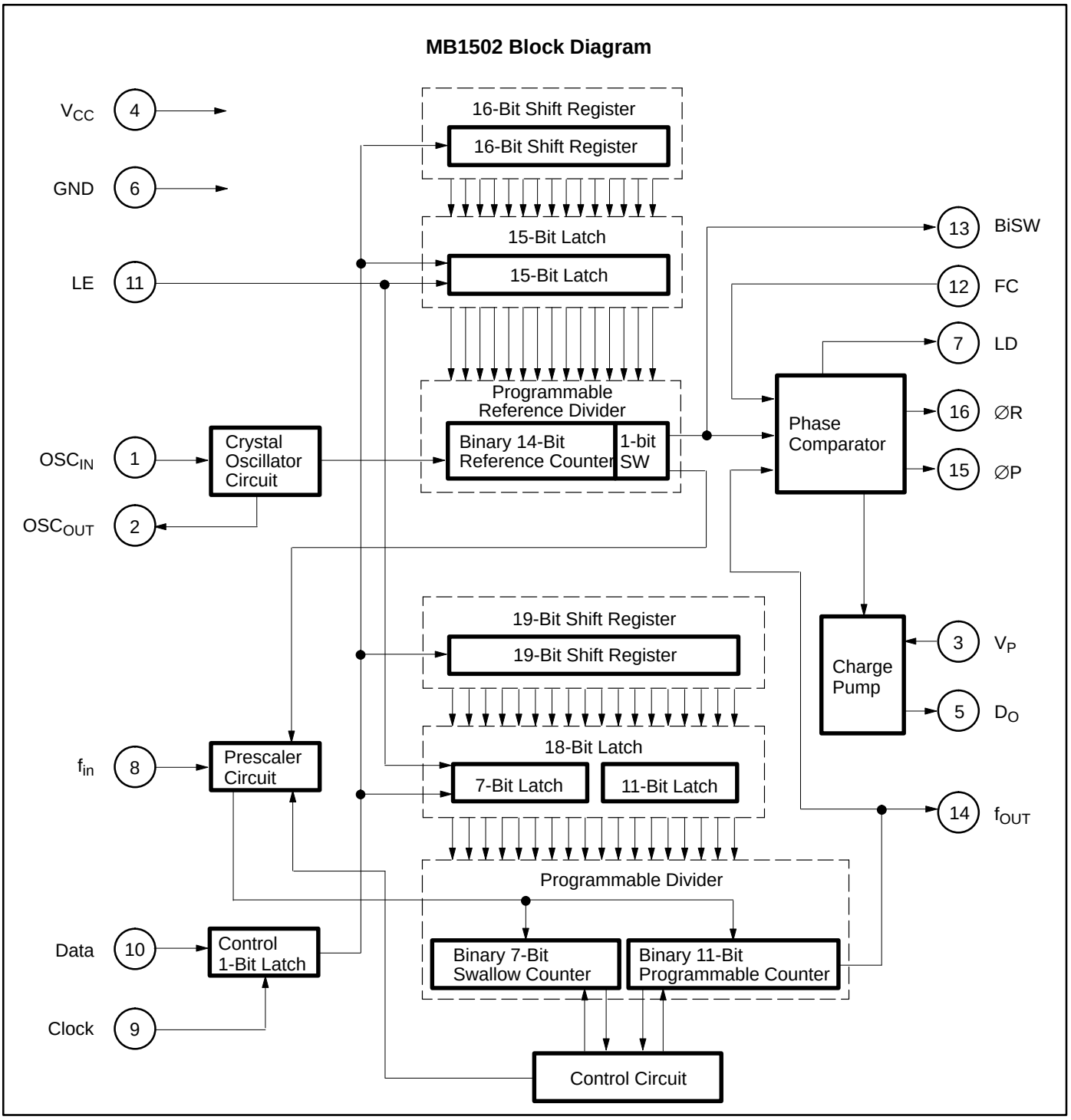
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Ratlng	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
	V_P	V_{CC} to 10.0	V
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Open-drain Voltage	V_{OOP}	–0.5 to 0.8	V
Output Current	I_{OUT}	± 10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratlngs are exceeded.Functional operation should be restricted to the condltions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB1502 Block Diagram



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1 2	OSC_{IN} OSC_{OUT}	I O	Oscillator input. Oscillator output. A crystal is placed between OSC_{IN} and OSC_{OUT}.
3	V_P	—	Power supply input for charge pump and analog switch.
4	V_{CC}	—	Power supply voltage input.
5	D_O	O	Charge pump output. The characteristics of charge pump is reversed depending upon FC input.
6	GND	—	Ground
7	LD	O	Phase comparator output. Normally this pin outputs high level. While the phase difference of f_r, and f_p exists, this pin outputs low level.
8	f_{IN}	I	Prescaler input. The connection with an external VCO should be AC connection.
9	Clock	I	Clock input for 19-bit shift register and 16-bit shift register. On rising edge of the clock shifts one bit of data into the shift registers.
10	Data	I	Binary serial data input. The last bit of the data is a control bit which specified destination of shift registers. When this bit is high level and LE is high level, the data stored in shift register is transferred to 15-bit latch. When this bit is low level and LE is high level, the data is transferred to 18-bit latch.
11	LE	I	Load enable input (with internal pull up resistor). When LE is high or open, the data stored in shift register is transferred into latch depending upon the control bit. At the time, internal charge pump output to be connected to BISW pin because internal analog switch becomes ON state.
12	FC	I	Phase select input of phase comparator (with internal pull up resistor). When FC is low level, the characteristics of charge pump, phase comparator is reversed. FC input signal is also used to control fOUT pin (test pin) output level for f_r or f_p.
13	BISW	O	Analog switch output. Usually BISW pin is set high-impedance state. When internal analog switch is ON (LE pin is high level), this pin outputs internal charge pump state.
14	f_{OUT}	O	Monitor pin of phase comparator input. f_{OUT} pin outputs either programmable reference divider output (f_r) or programmable divider output (f_p) depending upon FC pin input level.
15 16	∅P ∅R	O O	Outputs for external charge pump. The characteristics are reversed according to FC input. ∅P pin is N-channel open drain output.

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data input is achieved by three inputs, such as Data pin, Clock pin and LE pin. Serial data input controls 15-bit programmable reference divider and 18-bit programmable divider, respectively.

Binary serial data is input to Data pin.

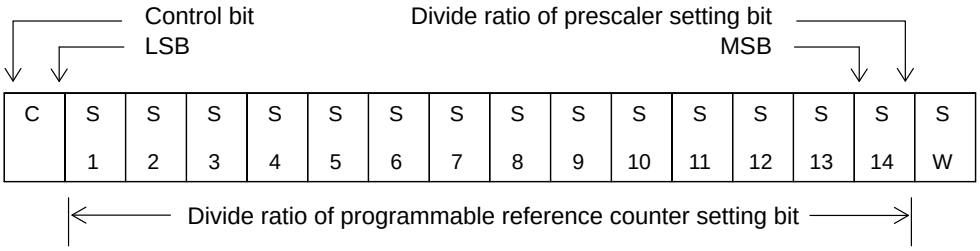
On rising edge of clock shifts one bit of serial data into the internal shift registers and when load enable pin is high level or open, stored data is transferred into latch depending upon the control bit.

Control data “H” data is transferred into 15-bit latch.

Control data “L” data is transferred into 18-bit latch.

PROGRAMMABLE REFERENCE DIVIDER

Programmable reference divider consists of 16-bit shift register, 15-bit latch and 14-bit reference counter. Serial 16-bit data format is shown below.



14-BIT PROGRAMMABLE REFERENCE COUNTER DIVIDE RATIO

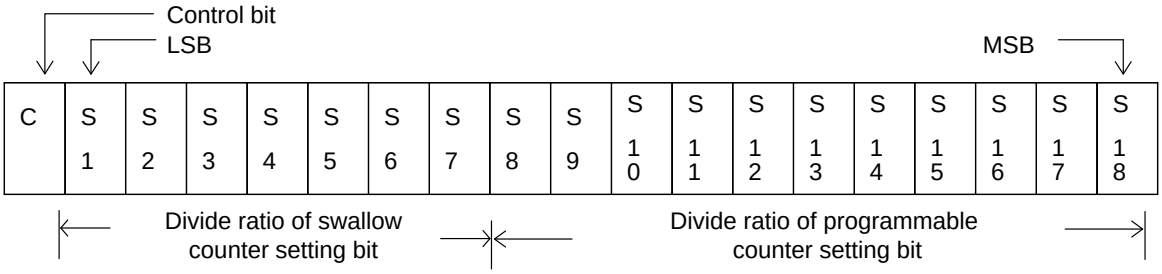
Divide Ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 8 is prohibited.
Divide ratio: 8 to 16383
SW: This bit selects divide ratio of prescaler.
SW=H : 64
SW=L :128
S1 to S14: These bits select divide ratio of programmable reference divider.
C: Control bit (sets as high level).
Data is input from MSB side.

PROGRAMMABLE DIVIDER

Programmable divider consists of 19-bit shift register, 18-bit latch, 7-bit swallow counter and 11-bit programmable counter.

Serial 19-bit data format is shown on following page.



7-BIT SWALLOW COUNTER DIVIDE RATIO

Divide Ratio A	S7	S6	S5	S4	S3	S2	S1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

NOTE: Divide ratio: 0 to 127

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO

Divide Ratio N	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8
16	0	0	0	0	0	0	1	0	0	0	1
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

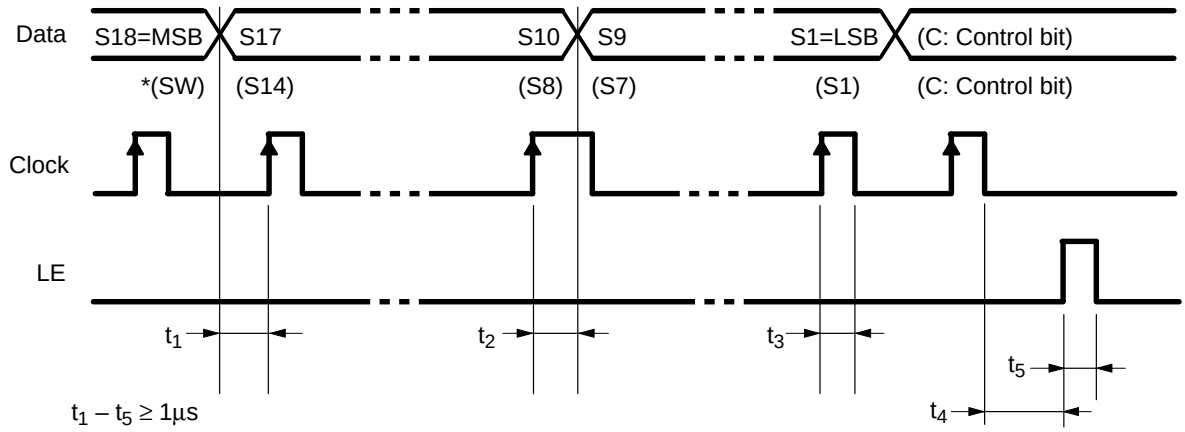
NOTES: Divide ratio less than 16 is prohibited.
Divide ratio: 16 to 2047
S1 to S7: Swallow counter divide ratio setting bit. (0 to 127)
S8 to S18: Programmable counter divide ratio setting bit. (16 to 2047)
C: Control bit (sets as low level).
Data is input from MSB side.

PULSE SWALLOW FUNCTION

$f_{VCO} = [(PxN)+A] \times f_{OSC} \div R$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)
N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$, $A < N$)
f_{OSC}: Output frequency of the external reference frequency oscillator
R: Preset divide ratio of binary 14-bit programmable reference counter (8 to 16383)
P: Preset modulus of external dual modulus prescaler (64 or 128)

Serial Data Input Timing



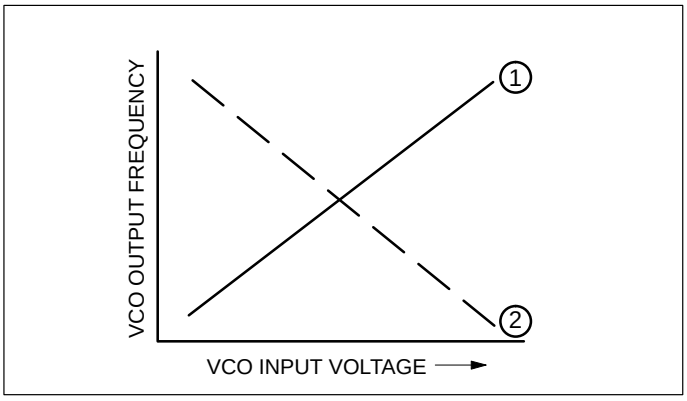
NOTES: Parenthesis data is used for setting divide ratio of programmable reference divider.
On rising edge of clock shifts one bit of data in the shift register.

PHASE CHARACTERISTICS

FC pin is provided to change phase characteristics of phase comparator. Characteristics of internal charge pump output level (D_O), phase comparator output level (∅R, ∅P) are reversed depending upon FC pin input level. Also, monitor pin (f_{OUT}) output level of phase comparator is controlled by FC pin input level. The relation between outputs (D_O, ∅R, ∅P) and FC input level are shown below.

	FC=H or open				FC=L			
	D_O	∅R	∅P	f_{OUT}	D_O	∅R	∅P	f_{OUT}
$f_r > f_p$	H	L	L	(f_r)	L	H	Z	(f_p)
$f_r < f_p$	L	H	Z	(f_r)	H	L	L	(f_p)
$f_r = f_p$	Z	L	Z	(f_r)	Z	L	Z	(f_p)

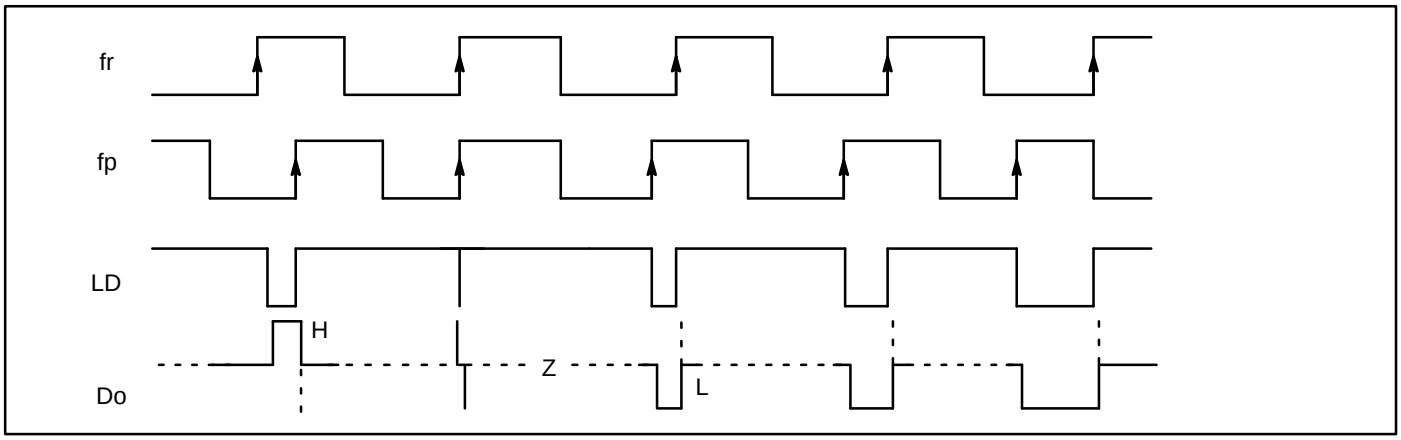
Note: Z = (High impedance)



VCO CHARACTERISTICS
Depending upon VCO characteristics, FC pin should be set accordingly:

— When VCO characteristics are like 1, FC should be set High or open circuit;

— When VCO characteristics are like 2, FC should be set Low.



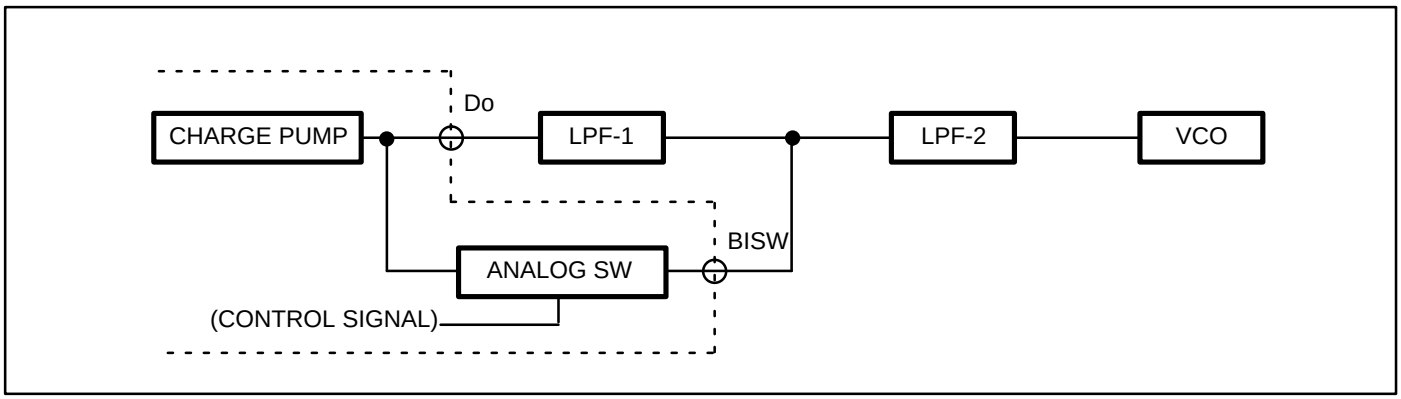
NOTES: Phase difference detection range: –2π to +2π
Spike appearance depends on charge pump characteristics. Also, the spike is output in order to diminish dead band.
When $f_r > f_p$ or $f_r < f_p$, spike might not appear depending upon charge pump characteristics.

ANALOG SWITCH

ON/OFF of analog switch is controlled by LE input signal. When the analog switch is ON, internal charge pump output (D_O) to be connected to BISW pin. When the analog switch is OFF, BISW pin is set to high-impedance state.

LE=H (Changing the divide ratio of internal prescaler) : Analog switch=ON
LE=L (Normal operating mode): Analog switch=OFF

LPF time constant is decreased in order to insert a analog switch between LPF1 and LPF2 when channel of PLL is changing. Thus, lock up time is decreased, that is, fast lock up time is achieved.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_P	V_{CC}	V_P	8.0	V
Input Voltage	V_I	GND		V_{CC}	V
Operating Temperature	T_A	–40		85	°C

ELECTRICAL CHARACTERISTICS

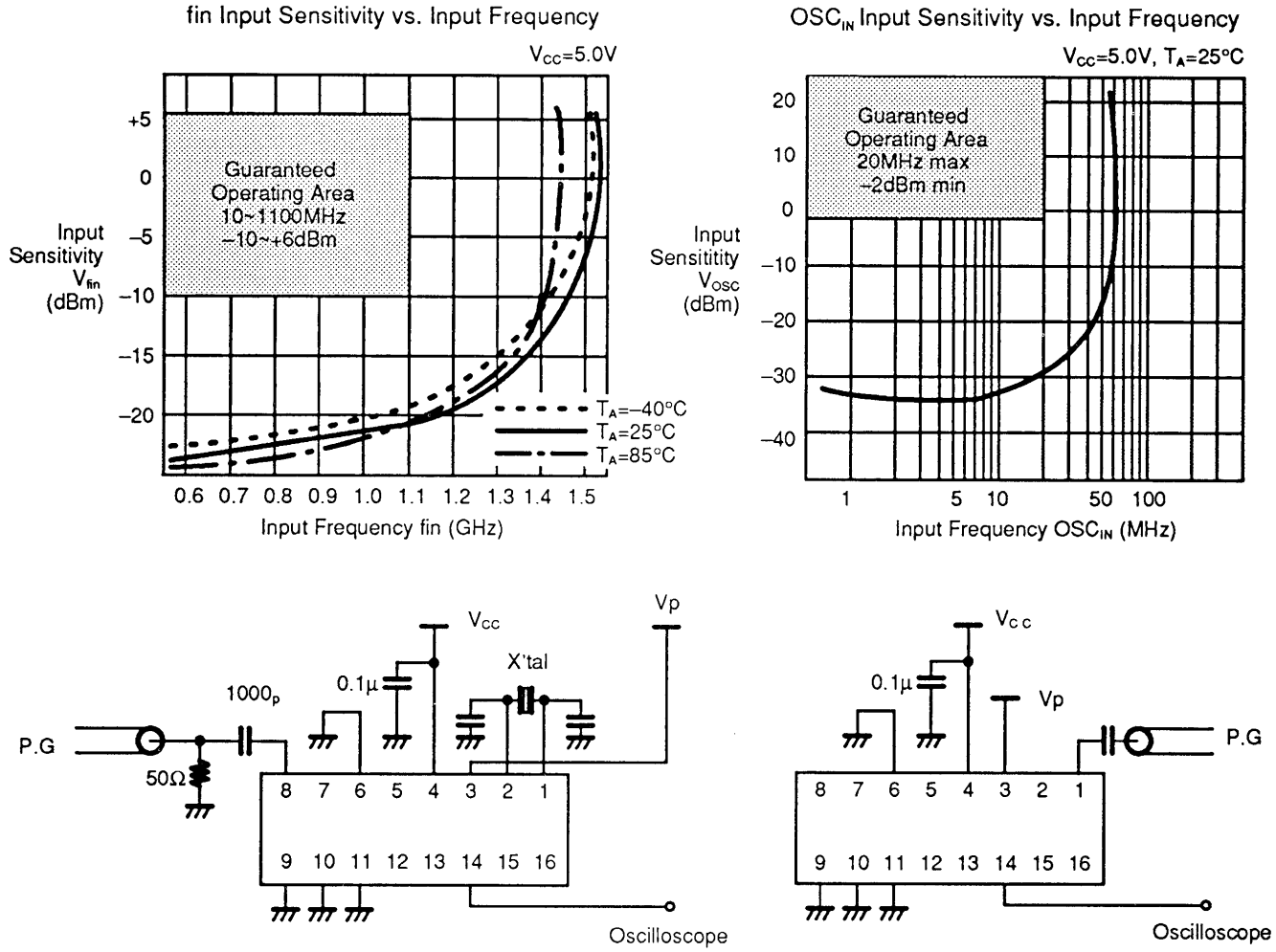
(Vcc=4.5 to 5.5V, T_A=–40 to +85°C, unless otherwise noted.)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current		I_{CC}	Note 1		8.0	12.0	mA
Operating Frequency	f_{in}	f_{in}	Note2	10		1100	MHz
	OSC_{IN}	f_{OSC}			12	20	MHz
Input Sensitivity	f_{in}	V_{fin}		–10		6	dBm
	OSC_{IN}	V_{OSC}		0.5			V_{PP}
High-level Input Voltage	Except f_{in} and OSC_{IN}	V_{IH}		V_{CC}x0.7			V
Low-level Input Voltage		V_{IL}				V_{CC}x0.3	V
High-level Input Current	Data Clock	I_{IH}			1.0		µA
Low-level Input Current		I_{IL}			–1.0		µA
Input Current	OSC_{IN}	I_{OSC}			±50		µA
	LE, FC	I_{LE}			–60		µA
High-level Output Current	Except D_O and OSC_{OUT}	V_{OH}	V_{CC} = 5 V	4.4			V
Low-level Output Current		V_{OL}				0.4	V
N-channel Open Drain Cutoff Current	D_O, ∅P	I_{OFF}	V_P = V_{CC} to 8V V_{OOP}= GND to 8V			1.1	µA
Output Current	Except D_O and OSC_{OUT}	I_{OH}		–1.0			mA
		I_{OL}		1.0			mA
Analog Switch On Resistor		R_{ON}			25		Ω

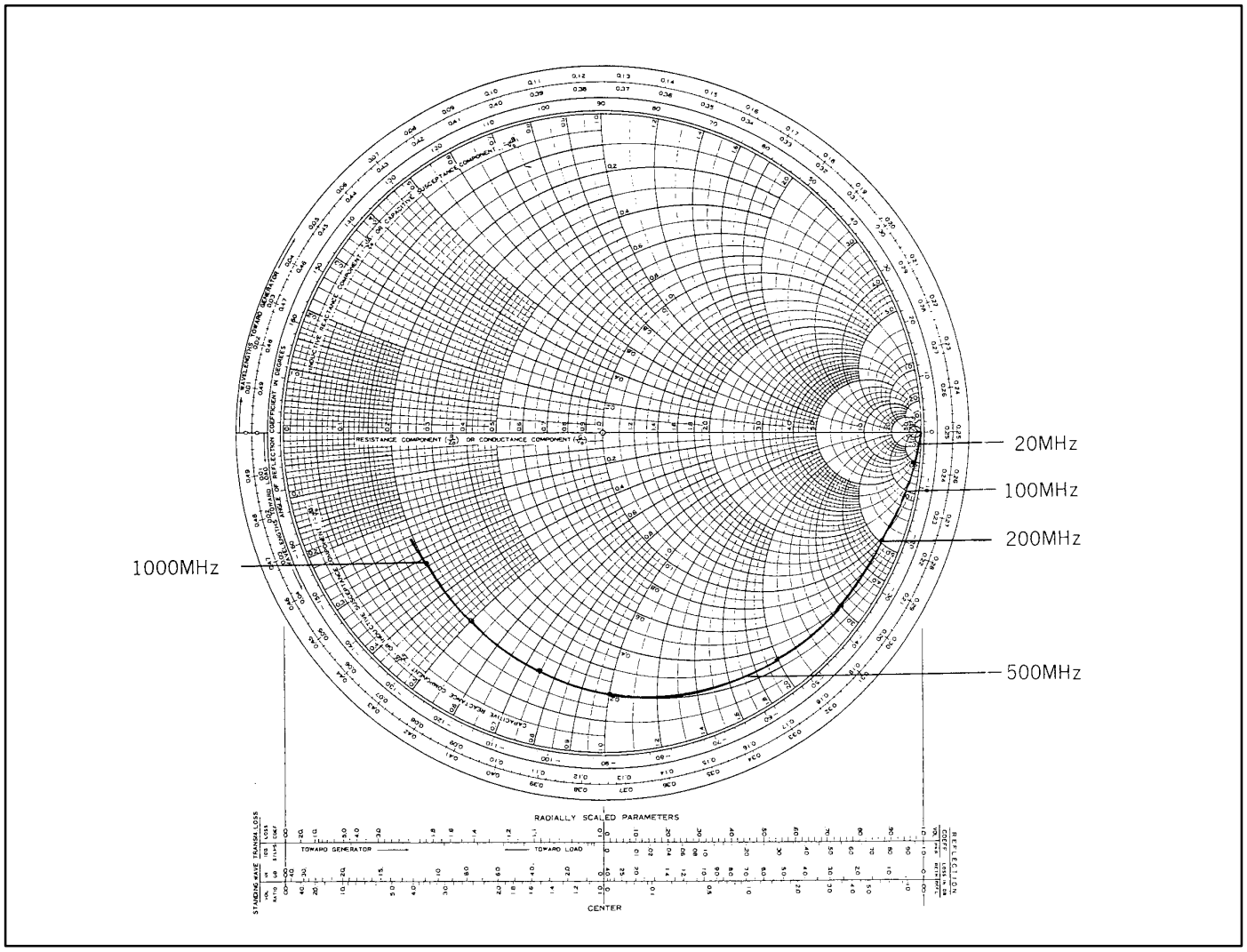
NOTE: 1: f_{in} = 1.1GHz, OSC_{IN}=12MHz, V_{cc}=5V. Inputs are grounded and outputs are open.
2: AC coupling. Minimum operating frequency is measured when a capacitor 1000pF is connected.

TYPICAL CHARACTERISTICS CURVES

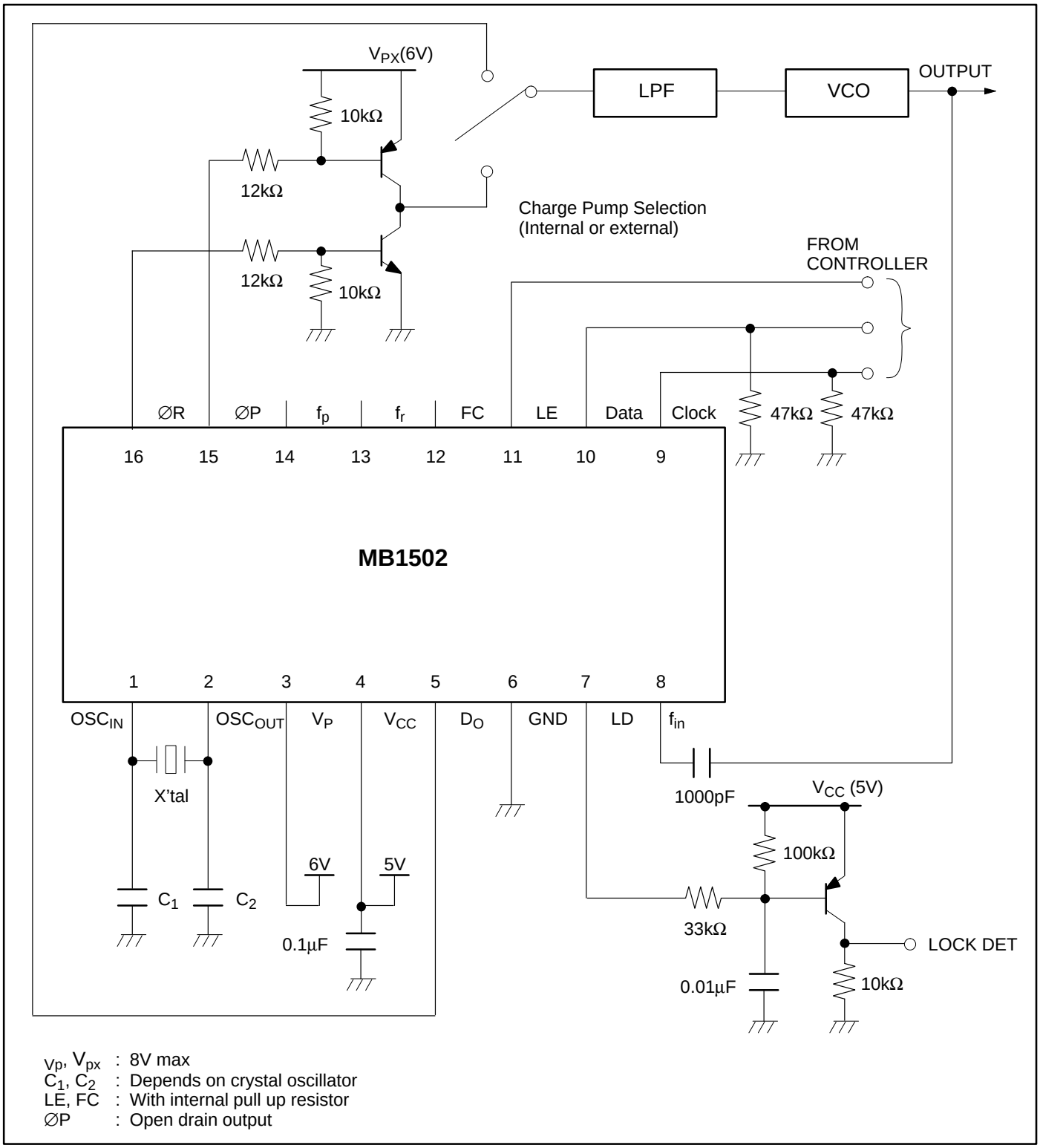
INPUT SENSITIVITY CHARACTERISTICS



INPUT IMPEDANCE CHARACTERISTICS



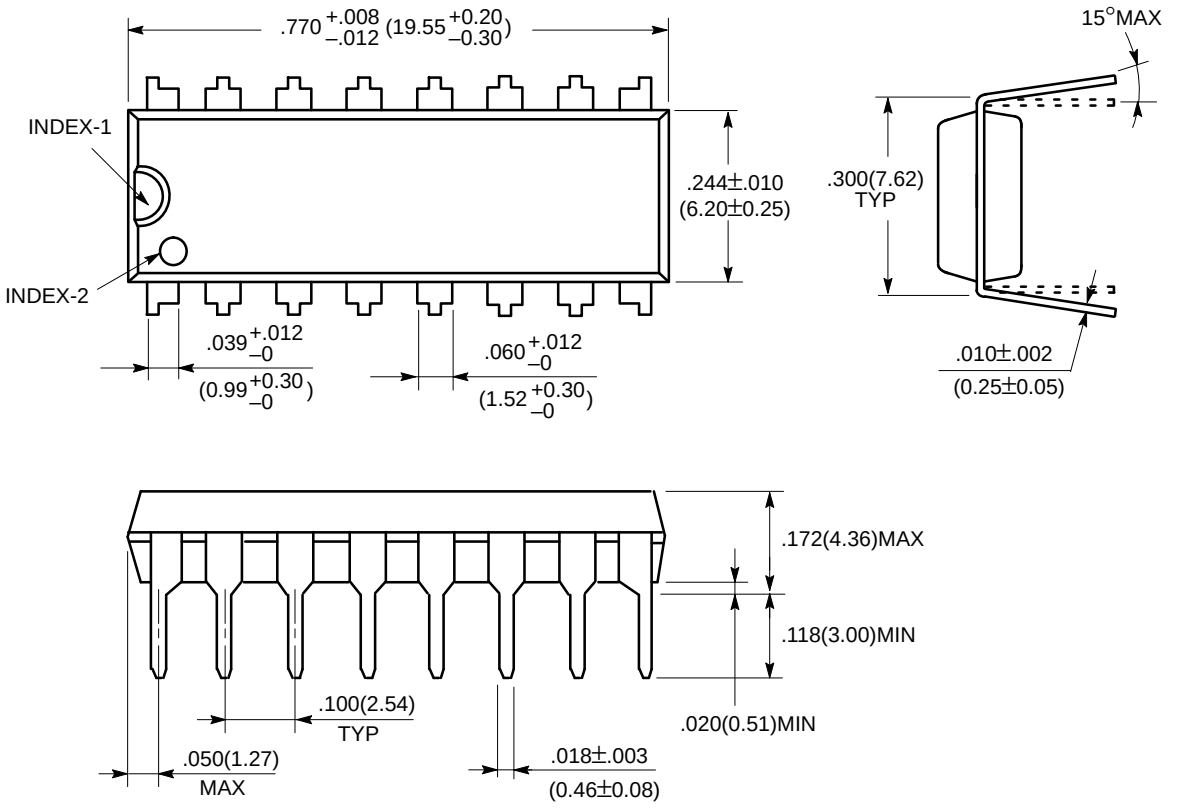
TYPICAL APPLICATION EXAMPLE



V_p, V_{px} : 8V max
C_1, C_2 : Depends on crystal oscillator
LE, FC : With internal pull up resistor
ØP : Open drain output

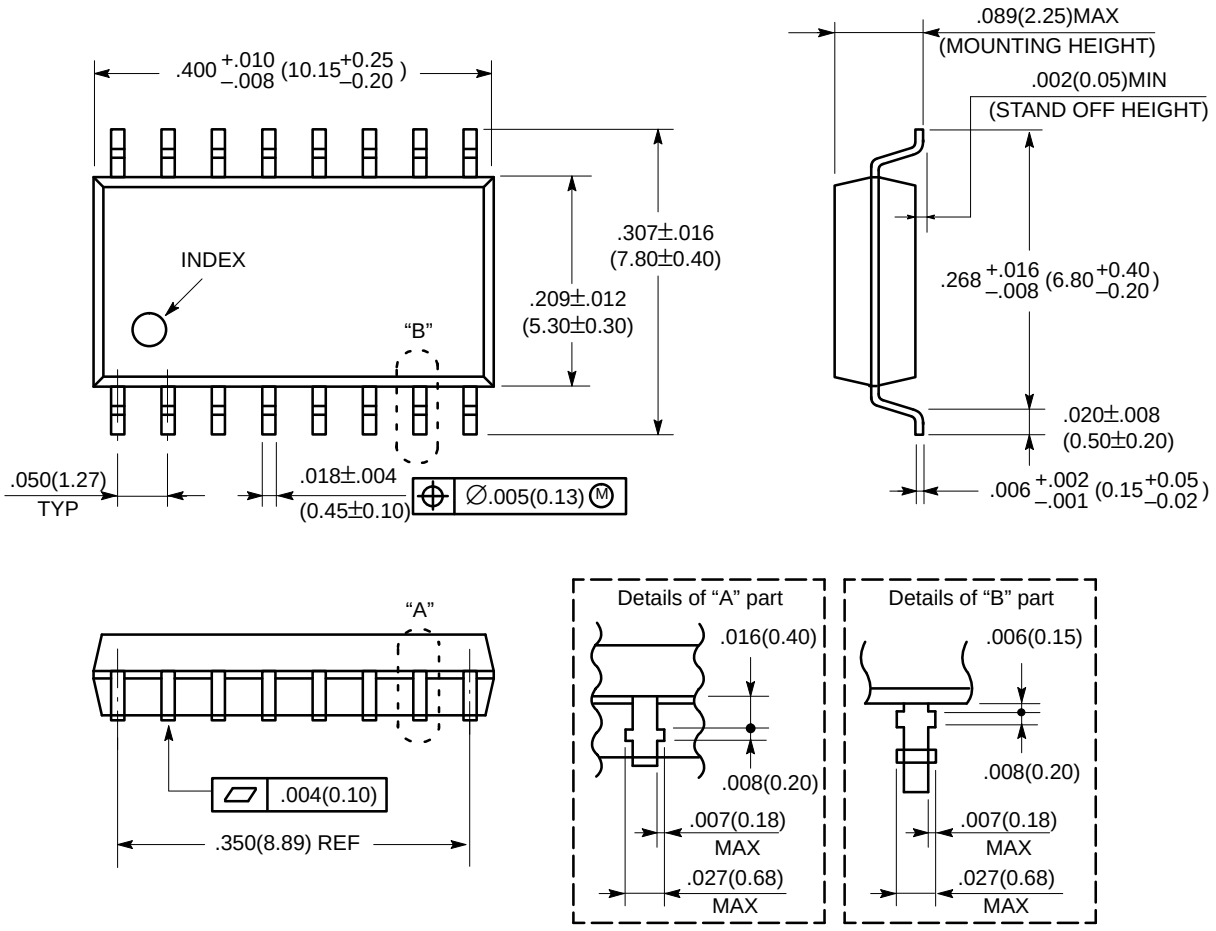
PACKAGE DIMENSIONS

16–Lead Plastic Dual In–Line Package
(Case No.: DIP–16P–M04)



Dimensions in
inches (millimeters)

16–Lead Plastic Flat Package
(Case No.: FPT–16P–M06)



Dimensions in
inches (millimeters)

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