Sept. 1995
Edition 4.0a

FUJITSU

DATA SHEET

MB507

1.6GHz TWO MODULUS PRESCALER

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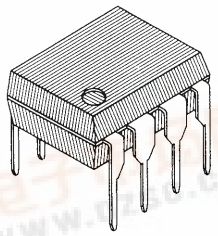
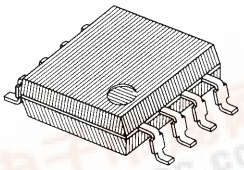
The Fujitsu MB507 is a 1.6GHz two modulus prescaler used with a frequency synthesizer to form a Phase Locked Loop (PLL). It will divide the input frequency by the modulus of 128/129 or 256/257 and has an output level of 1.6V peak to peak on ECL level.



PLASTIC PACKAGE
DIP-08P-M01

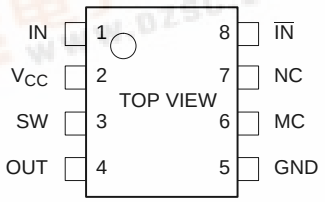


PLASTIC PACKAGE
FPT-08P-M01

FEATURES

- High Frequency Operation 1.6GHz max.
- Power Dissipation 90mW typ.
- Pulse Swallow Function
- Wide Operation Temperature -40°C to +85°C
- Stable Output Amplitude V_{OUT} = 1.6V_{p-p}
- Complete PLL synthesizer circuit with the Fujitsu MB87001A, PLL synthesizer IC
- Package
  Standard 8-pin Dual-In-Line Package (Suffix: –P)
  Standard 8-pin Flat Package (Suffix: –PF)

PIN ASSIGNMENT

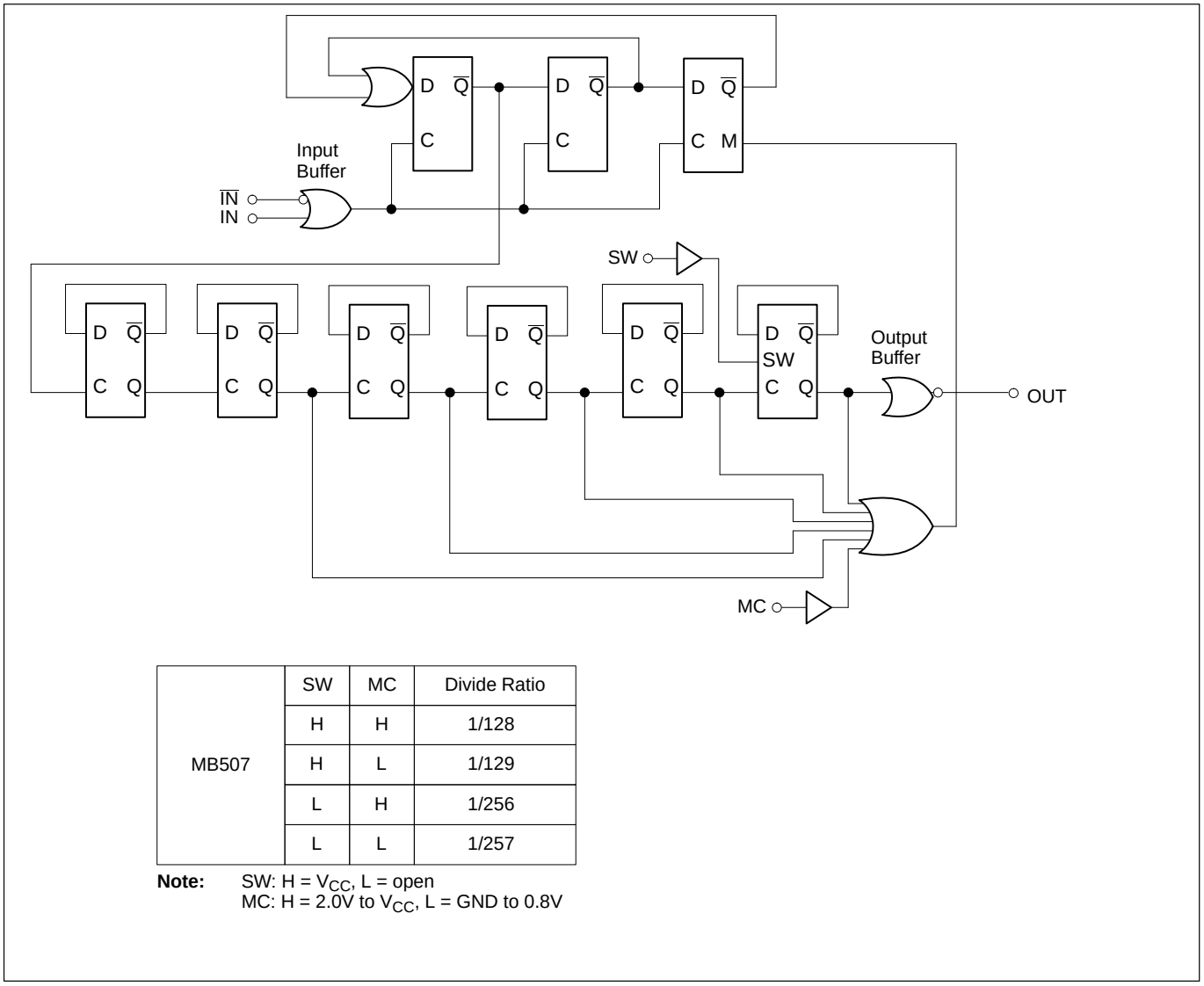


ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–0.5 to V_{CC}	V
Output Current	I_O	10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.



	SW	MC	Divide Ratio
MB507	H	H	1/128
	H	L	1/129
	L	H	1/256
	L	L	1/257

Note: SW: H = V_{CC}, L = open
MC: H = 2.0V to V_{CC}, L = GND to 0.8V

Figure 1. MB507 Block Diagram

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	DC Supply Voltage
3	SW	Divide Ratio Control Input Selecting Divide Ratio (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	NC	No Connection
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Output Current	I_O		1.2		mA
Ambient Temperature	T_A	–40		+85	°C
Load Capacitance	C_L			12	pF

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Supply Curent	I_{CC}			18		mA
Output Amplitude	V_O		1.0	1.6		V_{p-p}
Input Frequency	f_{IN}	with input coupling capacitor 1000pF	100		1600	MHz
Input Signal Amplitude	P_{IN}		–4		10	dBm
High Level Input Voltage for MC Input	V_{IHM}		2.0			V
Low Level Input Voltage for MC Input	V_{ILM}					V
High Level Input Voltage for SW Input	V_{IHS}*		V_{CC} –0.1	V_{CC}	V_{CC} +0.1	V
Low Level Input Voltage for SW Input	V_{ILS}		Open			V
High Level Input Current for MC Input	I_{IHM}	V_{IH} = 2.0V			0.4	mA
Low Level Input Current for MC Input	I_{ILM}	V_{IL} = 0.8V	–0.2			mA
Modulus Set-up Time MC to OUT	t_{SET}	1.6GHz Operation		18	28	ns

Note: *Design Guarantee

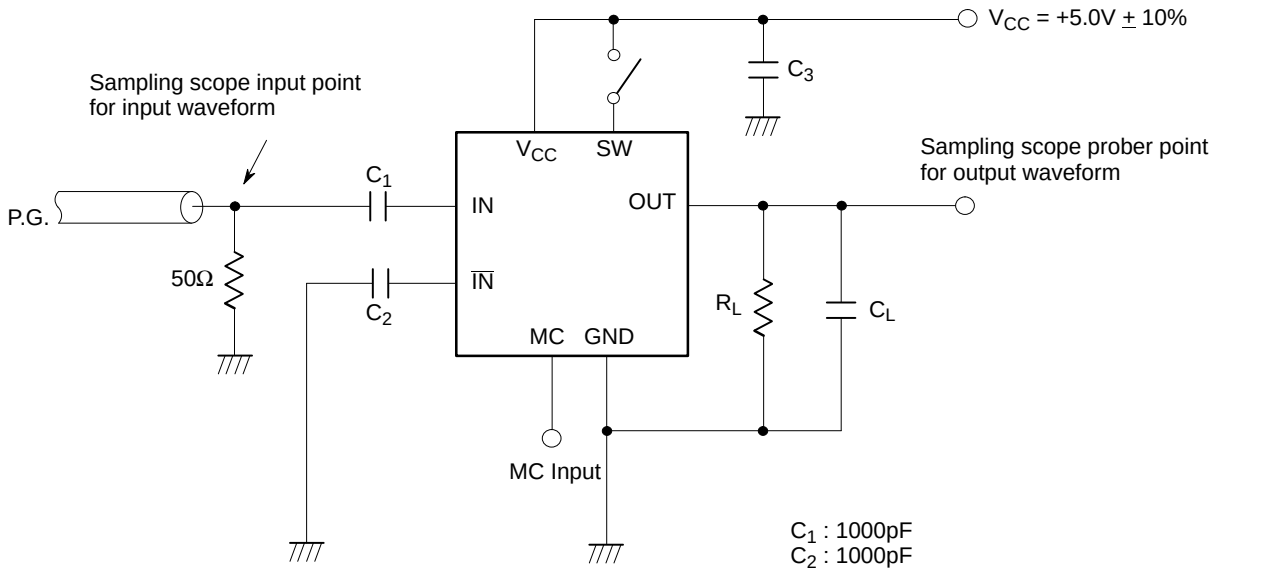
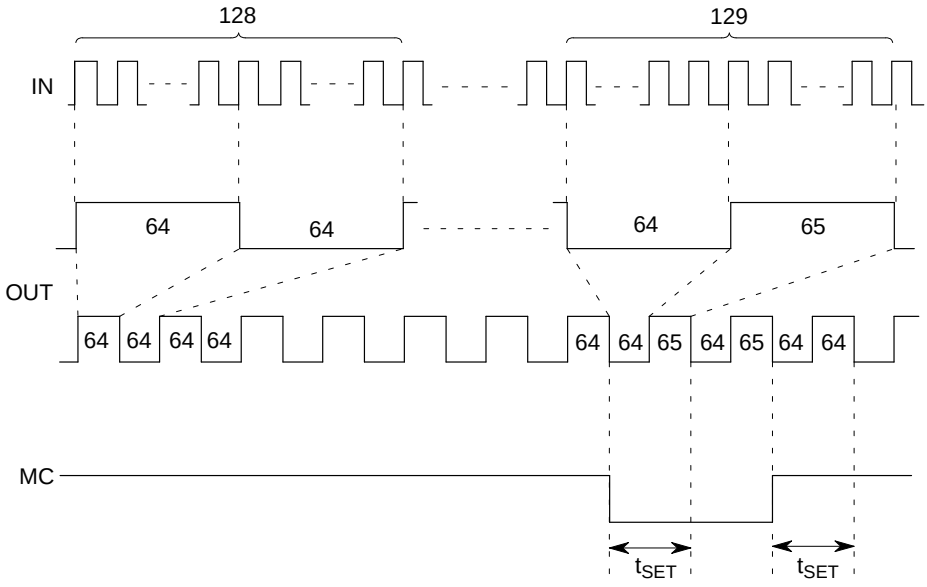


Figure 2. Test Circuit

TIMING CHART (2 MODULUS)

Example: Divide ratio = 128/129



Note: When divide of 129 is selected, positive pulse is applied by one to 65.
The typical set up time is 18 ns from the MC signal input to the timing of change of prescaler divide ratio.

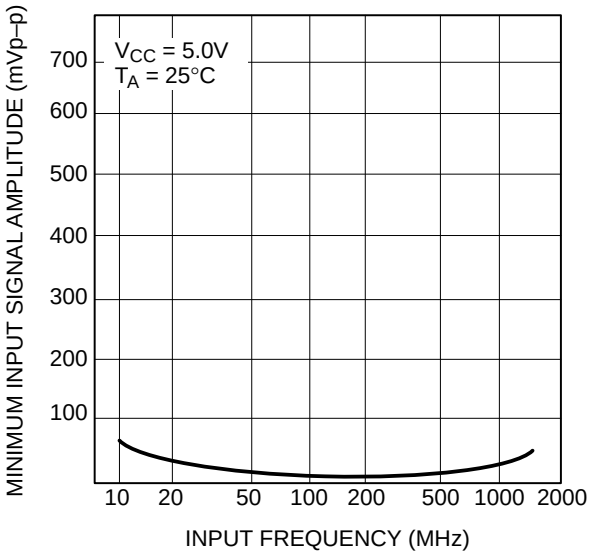


Figure 3. Input Signal Amplitude vs. Input Frequency

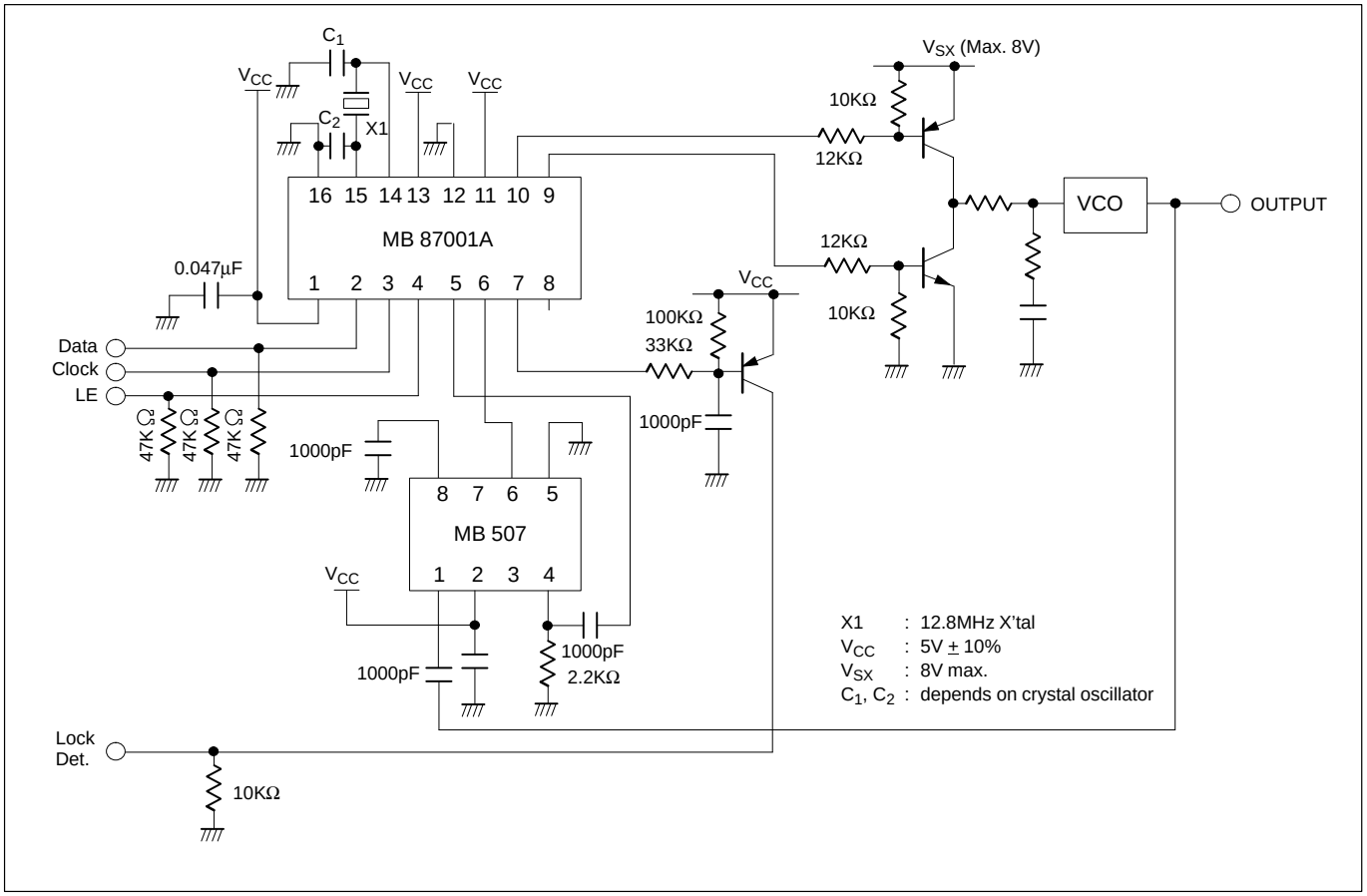
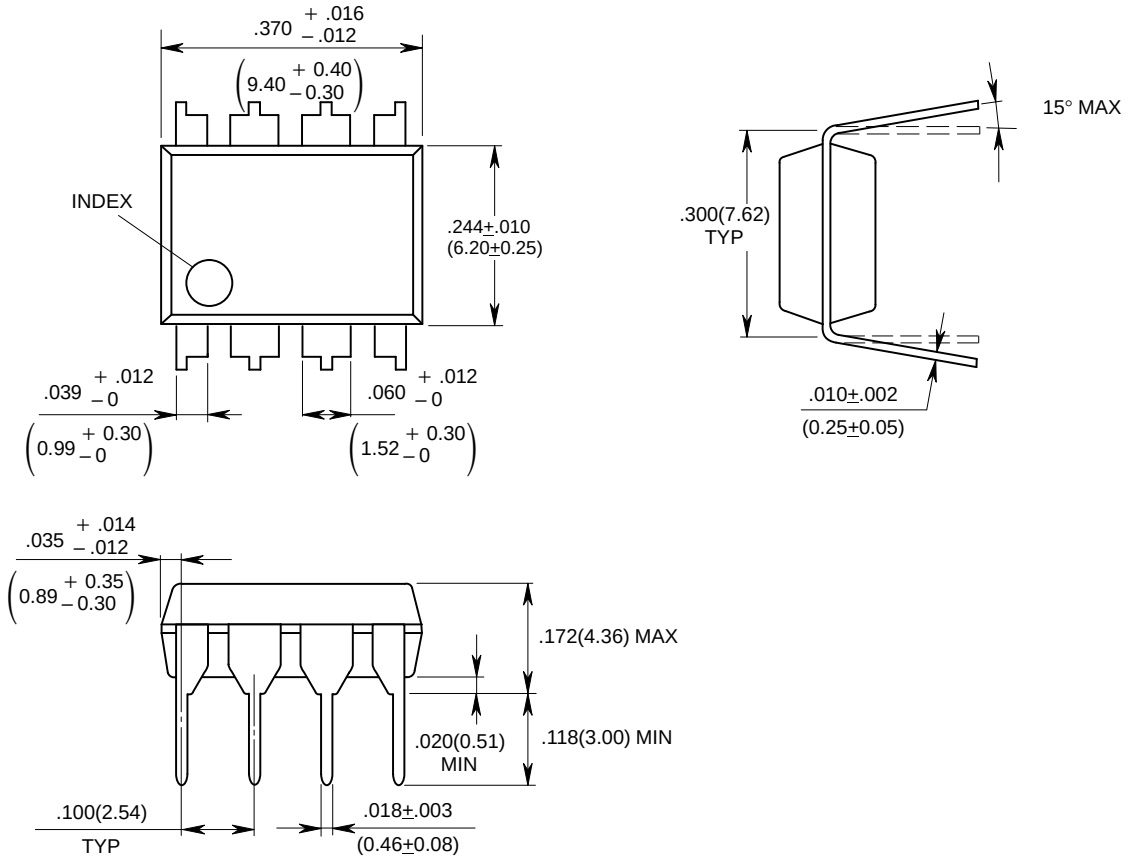


Figure 4. Typical Application Example

PACKAGE DIMENSIONS

(Suffix: P)

8-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No: DIP-08P-M01)

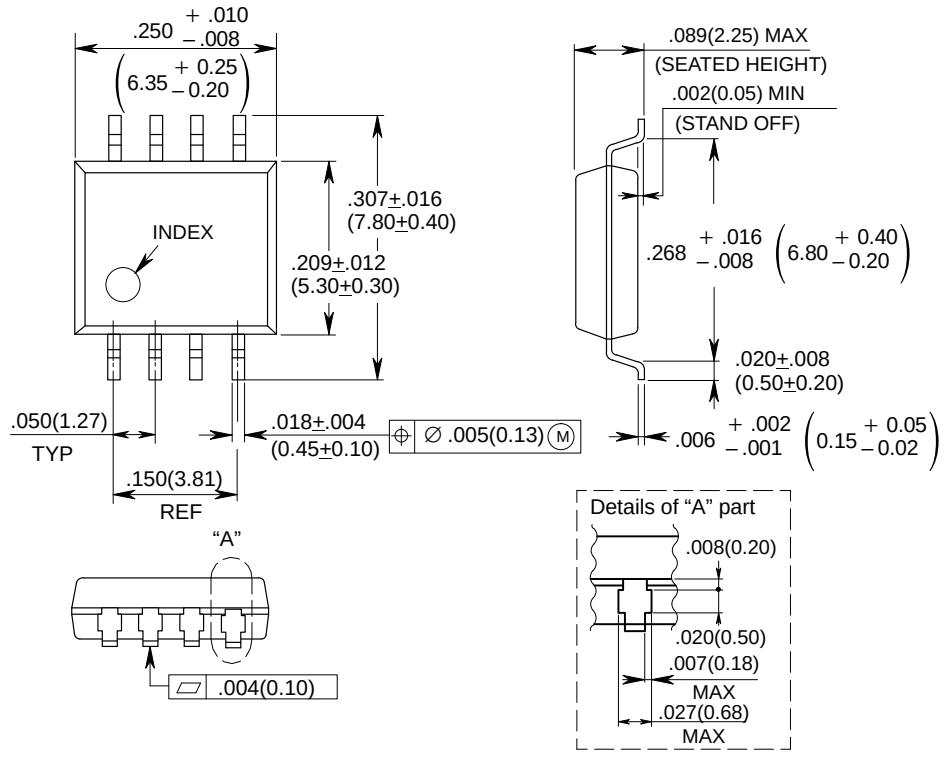


DImensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: PF)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No: FPT-08P-M01)



DImensions in
inches (millimeters)

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