MCP6041/2/3/4

600 nA, Rail-to-Rail Input/Output Op Amps

Features

- Low Quiescent Current: 600 nA/Amplifier (typ)
- Rail-to-Rail Input: -0.3 V to V_{DD}+0.3 V (max)
- Rail-to-Rail Output: V_{SS}+10 mV to V_{DD}-10 mV (max)
- Gain Bandwidth Product: 14 kHz (typ)
- Wide Supply Voltage Range: 1.4 V to 5.5 V (max)
- Unity Gain Stable
- Available in Single, Dual and Quad
- Chip Select ($\overline{CS}$) with MCP6043
- 5-lead SOT-23 package (MCP6041 only)

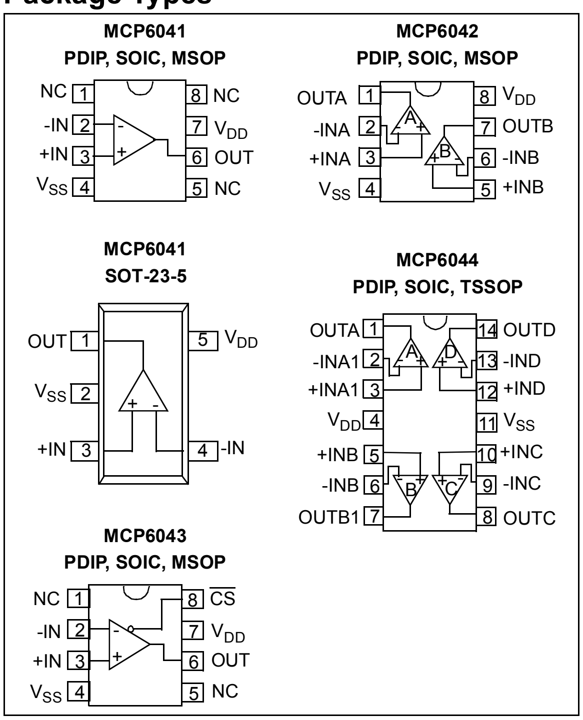
Applications

- Toll Booth Tags
- Wearable Products
- Temperature Measurement
- Battery Powered

Available Tools

- Spice macro models (at www.microchip.com)
- FilterLab® Software (at www.microchip.com)

Package Types



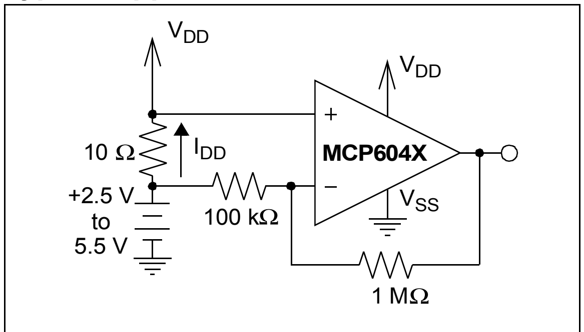
Description

The MCP6041/2/3/4 family of operational amplifiers from Microchip Technology, Inc. operate with a single supply voltage as low as 1.4 V, while drawing less than 1 µA (max) of quiescent current per amplifier. These devices are also designed to support rail-to-rail input and output operation. This combination of features supports battery-powered and portable applications.

The MCP6041/2/3/4 amplifiers have a typical gain bandwidth product of 14 kHz (typ) and are unity gain stable. These specs make these operational amplifiers appropriate for low frequency applications, such as battery current monitoring and sensor conditioning.

The MCP6041/2/3/4 family operational amplifiers are offered in single (MCP6041), single with a Chip Select ($\overline{CS}$) feature (MCP6043), dual (MCP6042) and quad (MCP6044) configurations. The MCP6041 device is available in the 5-lead SOT-23 package.

Typical Application



High Side Battery Current Sensor

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{DD} - V_{SS} ....7.0 V
All inputs and outputs.................... V_{SS} –0.3 V to V_{DD} +0.3 V
Difference Input voltage .... $|V_{DD} - V_{SS}|$
Output Short Circuit Current ....continuous
Current at Input Pins ....±2 mA
Current at Output and Supply Pins ....±30 mA
Storage temperature ....-65°C to +150°C
Ambient temp. with power applied ....-55°C to +125°C
ESD protection on all pins (HBM)....................≥ 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
+IN/+INA/+INB/+INC/+IND	Non-inverting Inputs
-IN/-INA/-INB/-INC/-IND	Inverting Inputs
V_{DD}	Positive Power Supply
V_{SS}	Negative Power Supply
OUT/OUTA/OUTB/OUTC/OUTD	Outputs
$\overline{CS}$	Chip Select
NC	No internal connection to IC

MCP6041/2/3/4 DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, all limits are specified for V_{DD} = +1.4 V to +5.5 V, V_{SS} = GND, T_A = 25 °C, $V_{CM} = V_{DD}/2$, R_L = 1 MΩ to $V_{DD}/2$, and $V_{OUT} \sim V_{DD}/2$

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset:						$V_{CM} = V_{SS}$
Input Offset Voltage	V_{OS}	-3.0	—	+3.0	mV	
Drift with Temperature	$\Delta V_{OS}/\Delta T$	—	±1.5	—	µV/°C	T_A= -40°C to+85°C
Power Supply Rejection	PSRR	70	85	—	dB	
Input Bias Current and Impedance:						
Input Bias Current	I_B	—	1.0	—	pA	
Input Bias Current Over Temperature	I_B	—	—	100	pA	T_A= -40°C to+85°
Input Offset Current	I_{OS}	—	1.0	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||6	—	Ω||pF	
Common Mode:						
Common-Mode Input Range	VCMR	V_{SS}–0.3	—	V_{DD}+0.3	V	
Common-Mode Rejection Ratio	CMRR	62	80	—	dB	V_{DD} = 5 V, V_{CM} = -0.3 V to 5.3 V
		60	75	—	dB	V_{DD} = 5 V, V_{CM} = 2.5 V to 5.3 V
		60	80	—	dB	V_{DD} = 5 V, V_{CM} = -0.3 V to 2.5 V
Open Loop Gain:						
DC Open Loop Gain (large signal)	A_{OL}	95	115	—	dB	R_L = 50 kΩ to $V_{DD}/2$, 100 mV < V_{OUT} < (V_{DD} – 100 mV)
Output:						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 10	—	V_{DD} – 10	mV	R_L = 50 kΩ to $V_{DD}/2$
Linear Region Output Voltage Swing	V_{OVR}	V_{SS} + 100	—	V_{DD} – 100	mV	R_L = 50 kΩ to $V_{DD}/2$, A_{OL} ≥ 95 dB
Output Short Circuit Current	I_O	—	21	—	mA	V_{OUT} = 2.5 V, V_{DD} = 5 V
Power Supply:						
Supply Voltage	V_{DD}	1.4	—	5.5	V	
Quiescent Current per amplifier	I_Q	0.3	0.6	1.0	µA	I_O = 0

MCP6041/2/3/4 AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, all limits are specified for V_{DD} = +5 V, V_{SS} = GND, T_A = 25 °C, $V_{CM} = V_{DD}/2$, R_L = 1 MΩ to $V_{DD}/2$, C_L = 60 pF, and $V_{OUT} \sim V_{DD}/2$

Parameters	Sym	Min	Typ	Max	Units	Conditions
Gain Bandwidth Product	GBWP	—	14	—	kHz	
Slew Rate	SR	—	3.0	—	V/ms	
Phase Margin	PM	—	65	—	°	G = +1
Input Voltage Noise	E_n	—	5.0	—	µVp-p	f = 0.1 Hz to 10 Hz
Input Voltage Noise Density	e_n	—	170	—	nV/√Hz	f = 1 kHz
Input Current Noise Density	i_n	—	0.6	—	fA/√Hz	f = 1 kHz

SPECIFICATIONS FOR MCP6043 CHIP SELECT FEATURE

Electrical Characteristics: Unless otherwise indicated, all limits are specified for V_{DD} = +1.4 V to +5.5 V, V_{SS} = GND, T_A = 25 °C, $V_{CM} = V_{DD}/2$, R_L = 1 MΩ to $V_{DD}/2$, C_L = 60 pF, and $V_{OUT} \sim V_{DD}/2$

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Specifications:						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	V_{SS} + 0.3	V	For entire V_{DD} range
$\overline{CS}$ Input Current, Low	I_{CSL}	—	5.0	—	pA	$\overline{CS} = V_{SS}$
$\overline{CS}$ High Specifications:						
$\overline{CS}$ Logic Threshold, High	V_{IH}	V_{DD} - 0.3	—	V_{DD}	V	For entire V_{DD} range
$\overline{CS}$ Input Current, High	I_{CSH}	—	5.0	—	pA	$\overline{CS} = V_{DD}$
$\overline{CS}$ Input High, GND Current	I_Q	—	20	—	pA	$\overline{CS} = V_{DD}$
Amplifier Output Leakage, $\overline{CS}$ High		—	20	—	pA	$\overline{CS} = V_{DD}$
Dynamic Specifications:						
$\overline{CS}$ Low to Amplifier Output High Turn-on Time	t_{ON}	—	2.0	50	ms	$\overline{CS}$ low = V_{SS} + 0.3 V, G = +1 V/V, $V_{OUT} = 0.9\ V_{DD}/2$
$\overline{CS}$ High to Amplifier Output High Z	t_{OFF}	—	10	—	µs	$\overline{CS}$ high = V_{DD} - 0.3 V, G = +1 V/V $V_{OUT} = 0.1\ V_{DD}/2$
Hysteresis	V_{HYST}	—	0.6	—	V	V_{DD} = 5 V

MCP6041/2/3/4 TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, all limits are specified for V_{DD} = +1.4 V to +5.5 V, V_{SS} = GND

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Temperature Ranges:						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances:						
Thermal Resistance, 5L-SOT23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note 1: The MCP6041/2/3/4 family of op amps operates over this extended range, but with reduced performance.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{DD} = +5 V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, R_L = 1 MΩ to V_{DD}/2, C_L = 60 pF, and V_{OUT} ~ V_{DD}/2.

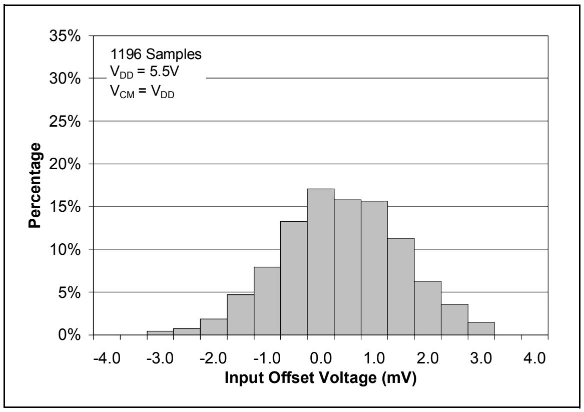


FIGURE 2-1: Histogram of Input Offset Voltage with V_{DD} = 5.5 V, V_{CM} = V_{DD}.

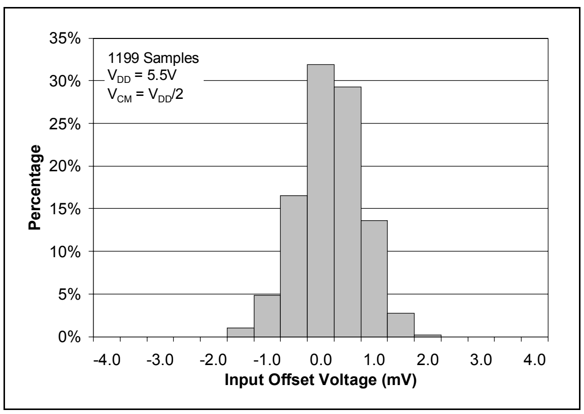


FIGURE 2-2: Histogram of Input Offset Voltage with V_{DD} = 5.5 V, V_{CM} = V_{DD}/2.

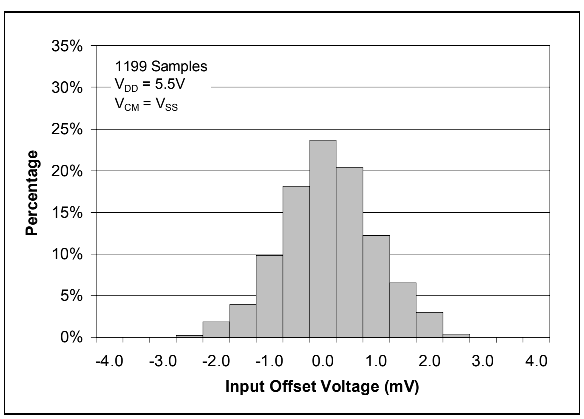


FIGURE 2-3: Histogram of Input Offset Voltage with V_{DD} = 5.5 V, V_{CM} = V_{SS}.

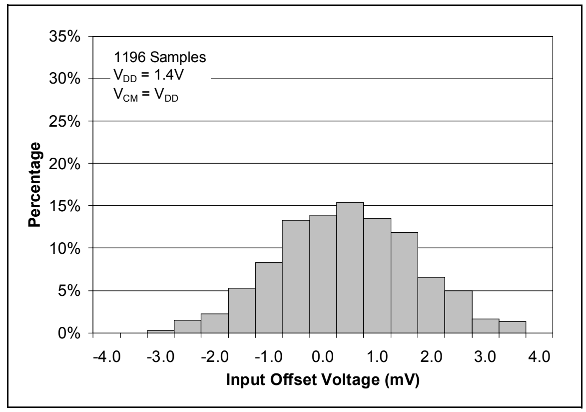


FIGURE 2-4: Histogram of Input Offset Voltage with V_{DD} = 1.4 V, V_{CM} = V_{DD}.

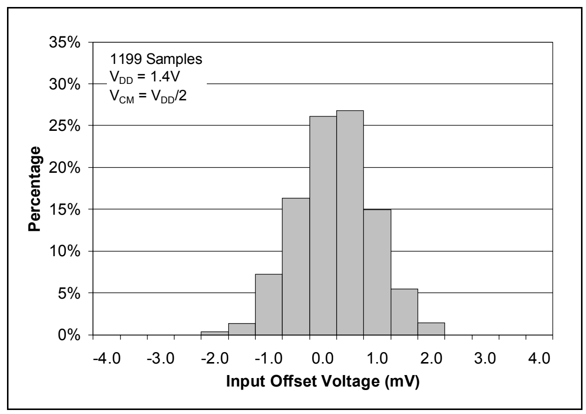


FIGURE 2-5: Histogram of Input Offset Voltage with V_{DD} = 1.4 V, V_{CM} = V_{DD}/2.

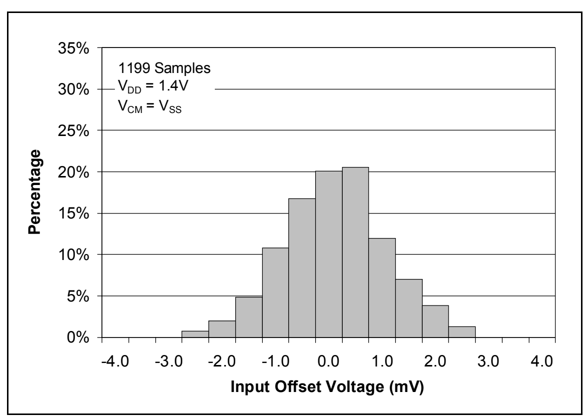


FIGURE 2-6: Histogram of Input Offset Voltage with V_{DD} = 1.4 V, V_{CM} = V_{SS}.

Note: Unless otherwise indicated, V_{DD} = +5 V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, R_L = 1 MΩ to V_{DD}/2, C_L = 60 pF, and V_{OUT} ~ V_{DD}/2.

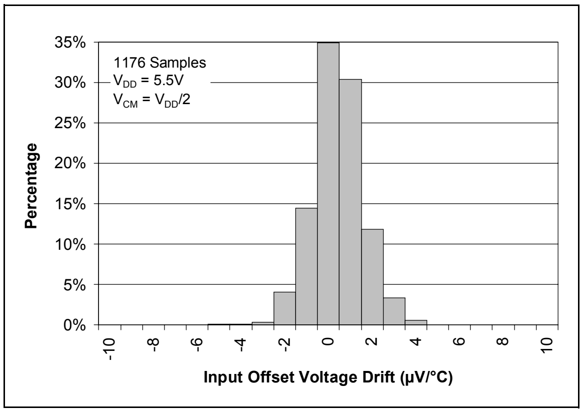


FIGURE 2-7: *Histogram of Input Offset Voltage Drift with V_{DD} = 5.5 V, V_{CM} = V_{DD}/2.*

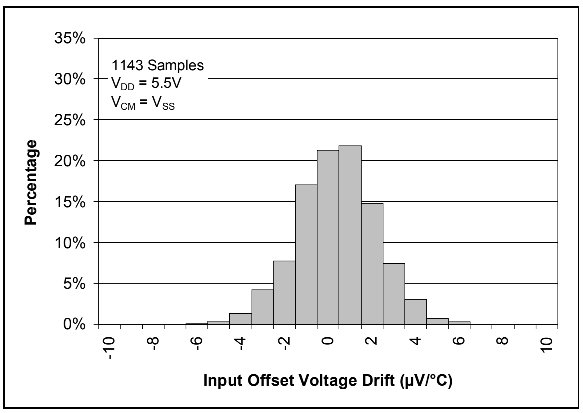


FIGURE 2-8: *Histogram of Input Offset Voltage Drift with V_{DD} = 5.5 V, V_{CM} = V_{SS}.*

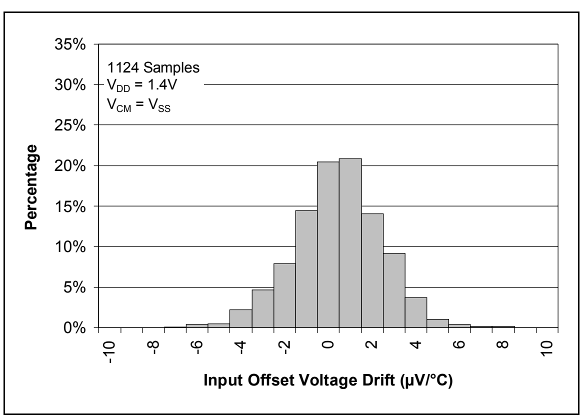


FIGURE 2-9: *Histogram of Input Offset Voltage Drift with V_{DD} = 1.4 V, V_{CM} = V_{SS}.*

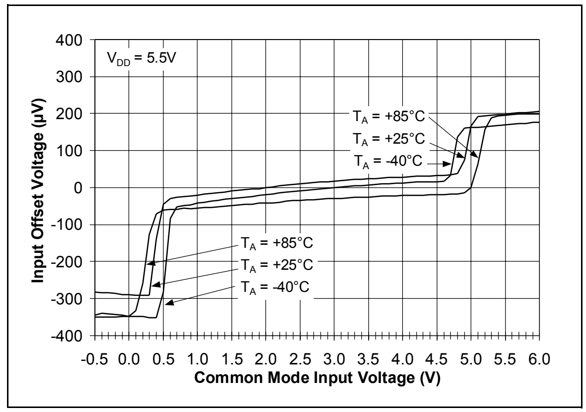


FIGURE 2-10: *Input Offset Voltage vs. Common Mode Input Voltage vs. Temperature with V_{DD} = 5.5 V.*

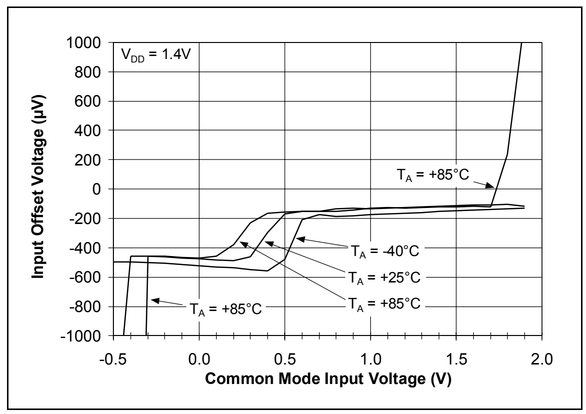


FIGURE 2-11: *Input Offset Voltage vs. Common Mode Input Voltage vs. Temperature with V_{DD} = 1.4 V.*

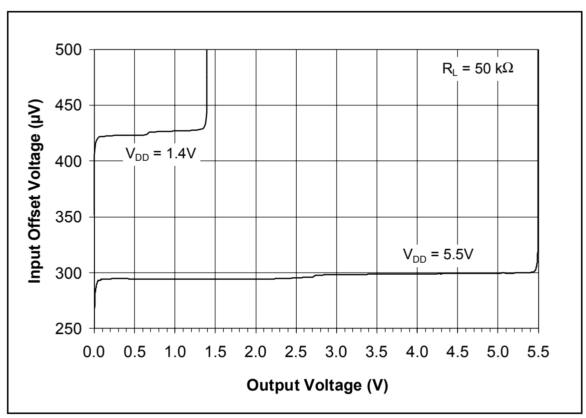


FIGURE 2-12: *Input Offset Voltage vs. Output Voltage vs. Power Supply Voltage.*

Note: Unless otherwise indicated, V_{DD} = +5 V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, R_L = 1 MΩ to V_{DD}/2, C_L = 60 pF, and V_{OUT} ~ V_{DD}/2.

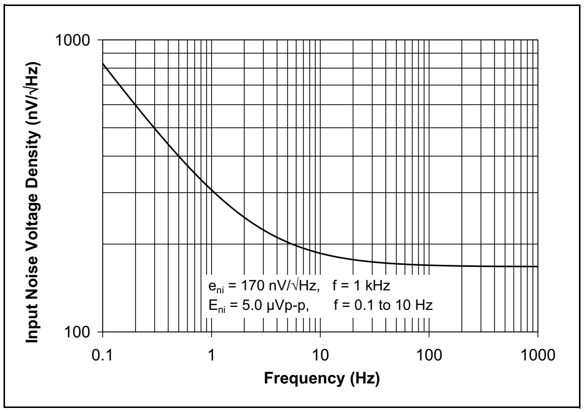


FIGURE 2-13: *Input Noise Voltage Density vs. Frequency.*

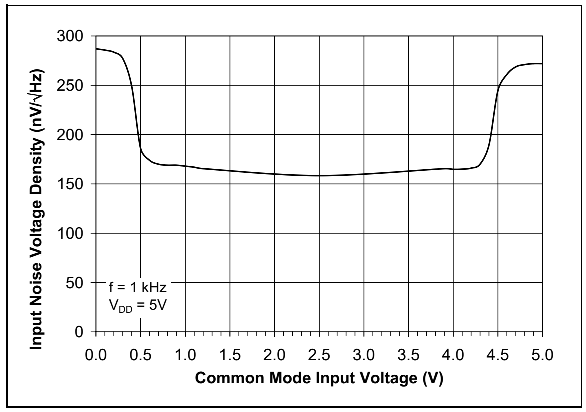


FIGURE 2-16: *Input Noise Voltage Density vs. Common Mode Input Voltage.*

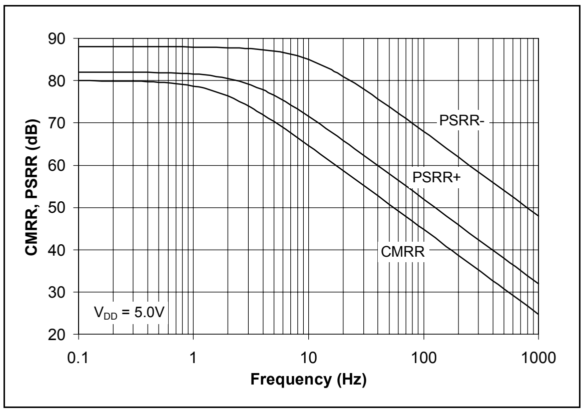


FIGURE 2-14: *Common Mode Rejection Ratio, Power Supply Rejection Ratio vs. Frequency.*

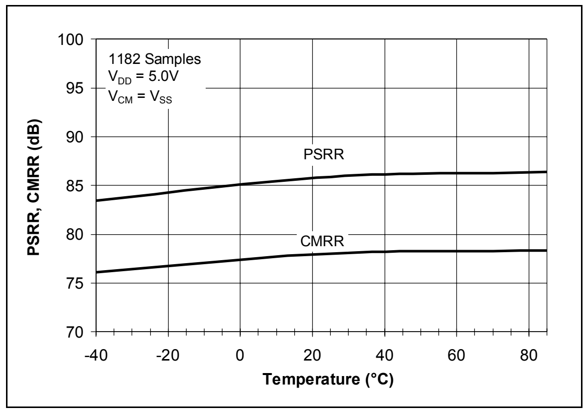


FIGURE 2-17: *Common Mode Rejection Ratio, Power Supply Rejection Ratio vs. Temperature.*

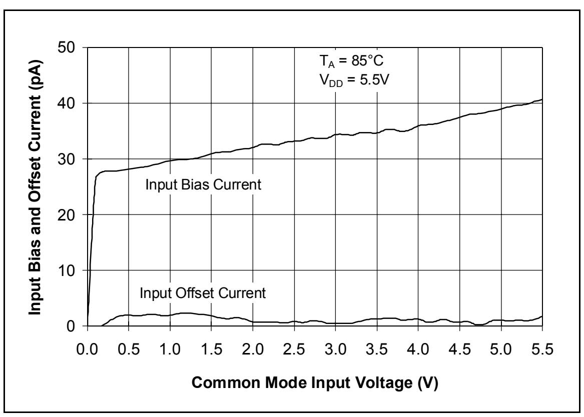


FIGURE 2-15: *Input Bias, Offset Currents vs. Common Mode Input Voltage with Temperature = 85°C.*

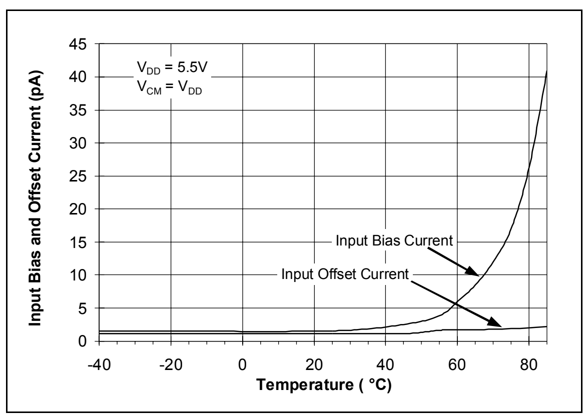


FIGURE 2-18: *Input Bias, Offset Currents vs. Temperature.*

Note: Unless otherwise indicated, V_{DD} = +5 V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, R_L = 1 MΩ to V_{DD}/2, C_L = 60 pF, and V_{OUT} ~ V_{DD}/2.

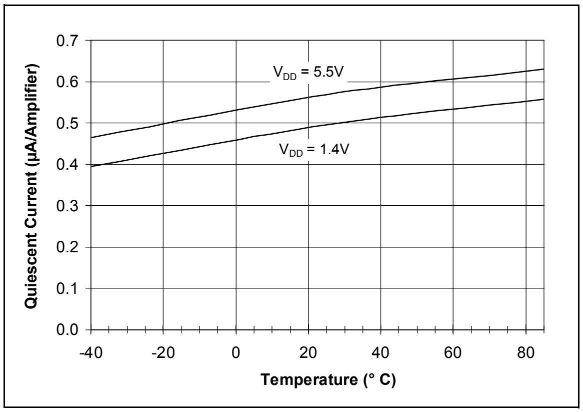


FIGURE 2-19: *Quiescent Current vs. Temperature vs. Power Supply Voltage.*

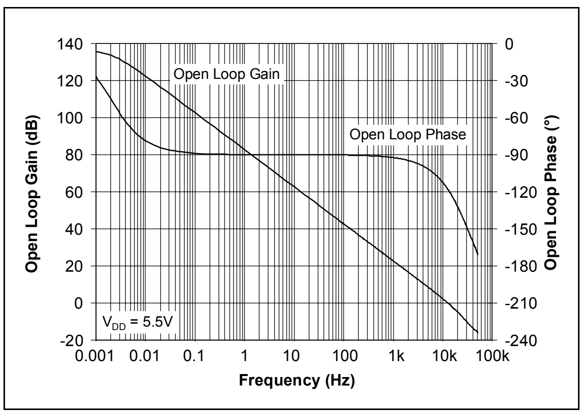


FIGURE 2-20: *Open Loop Gain, Phase vs. Frequency with V_{DD} = 5.5 V.*

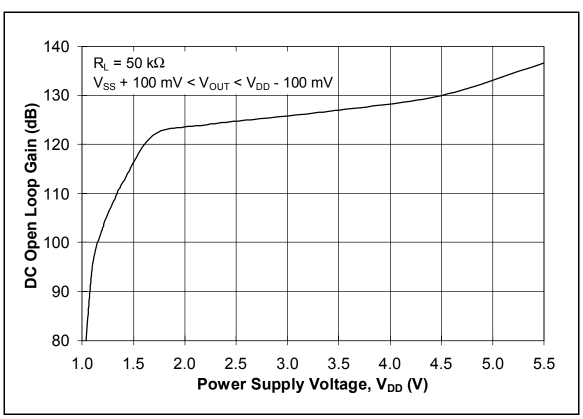


FIGURE 2-21: *Open Loop Gain vs. Power Supply Voltage.*

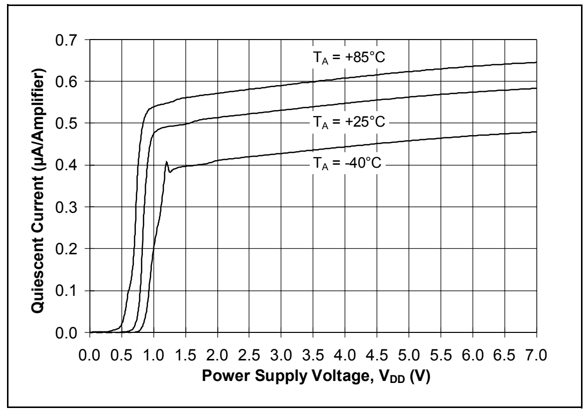


FIGURE 2-22: *Quiescent Current Vs. Power Supply Voltage vs. Temperature.*

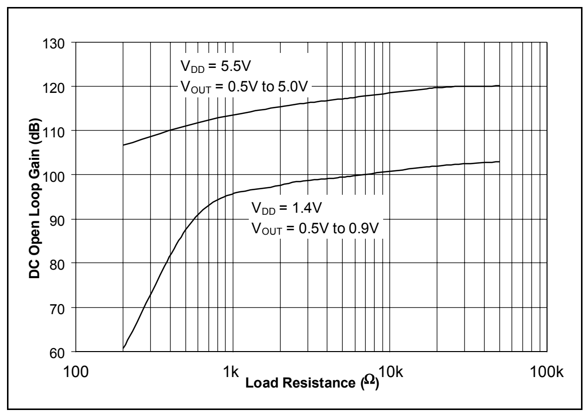


FIGURE 2-23: *Open Loop Gain vs. Load Resistance vs. Power Supply Voltage.*

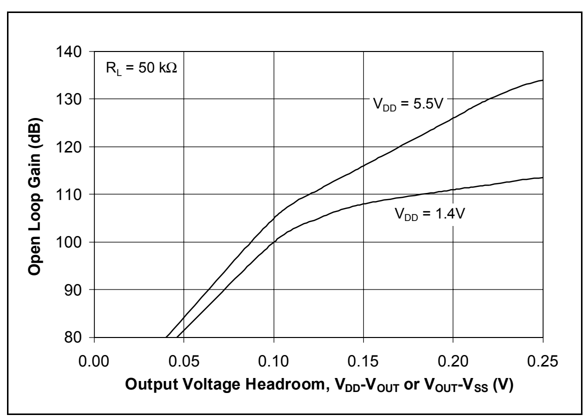


FIGURE 2-24: *Open Loop Gain vs. Output Voltage Headroom vs. Power Supply Voltage.*

Note: Unless otherwise indicated, V_{DD} = +5 V, V_{SS} = GND, T_A = 25°C, $V_{CM} = V_{DD}/2$, R_L = 1 MΩ to $V_{DD}/2$, C_L = 60 pF, and $V_{OUT} \sim V_{DD}/2$.

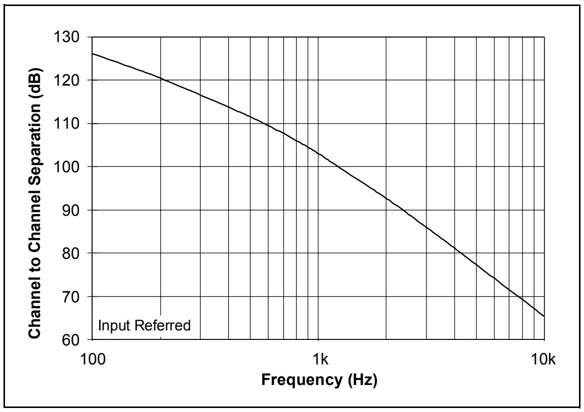


FIGURE 2-25: *Channel to Channel Separation vs. Frequency (MCP6042 and MCP6044 only).*

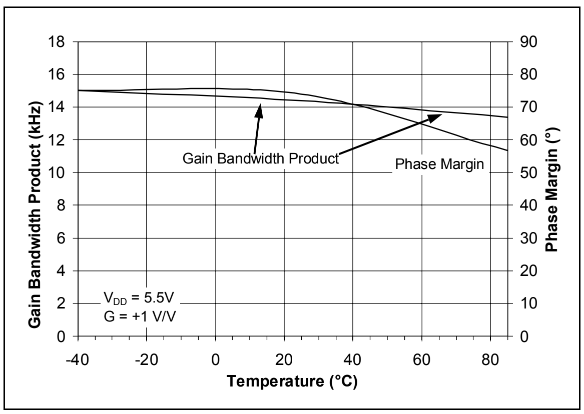


FIGURE 2-26: *Gain Bandwidth Product, Phase Margin vs. Temperature with V_{DD} = 5.5 V, Unity Gain.*

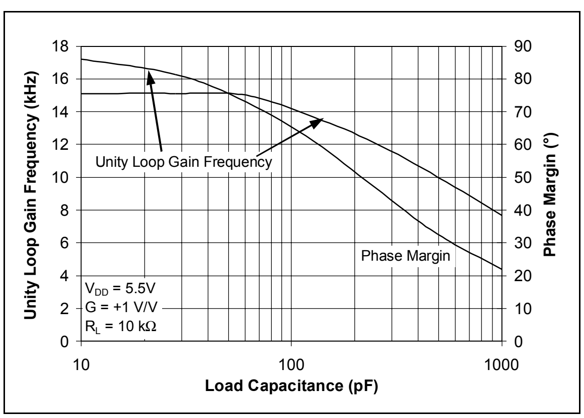


FIGURE 2-27: *Unity Loop Gain Frequency, Phase Margin vs. Load Capacitance.*

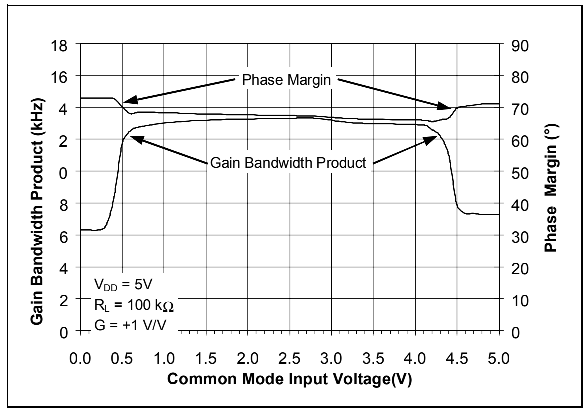


FIGURE 2-28: *Gain Bandwidth Product, Phase Margin vs. Common Mode Input Voltage with Unity Gain.*

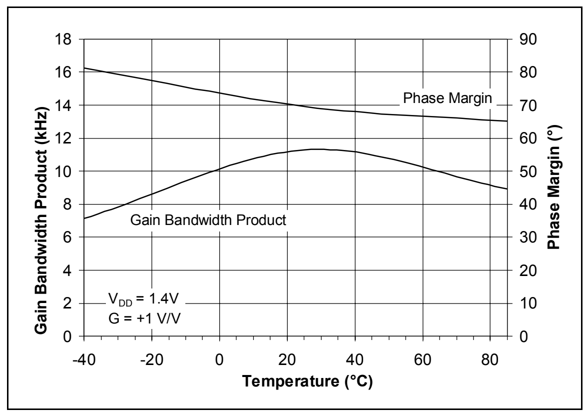


FIGURE 2-29: *Gain Bandwidth Product, Phase Margin vs. Temperature with V_{DD} = 1.4 V, Unity Gain.*

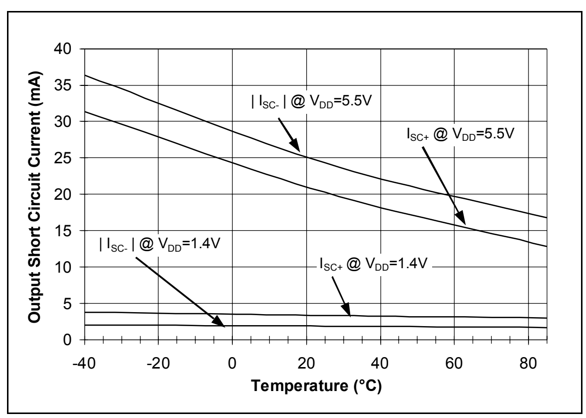


FIGURE 2-30: *Output Short Circuit Current vs. Temperature vs. Power Supply Voltage.*

Note: Unless otherwise indicated, V_{DD} = +5 V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, R_L = 1 MΩ to V_{DD}/2, C_L = 60 pF, and V_{OUT} ~ V_{DD}/2.

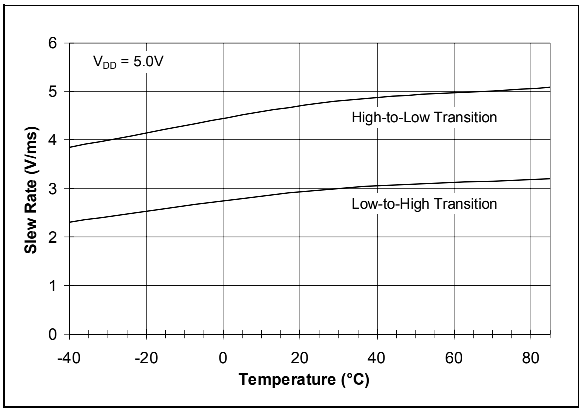


FIGURE 2-31: *Slew Rate vs. Temperature.*

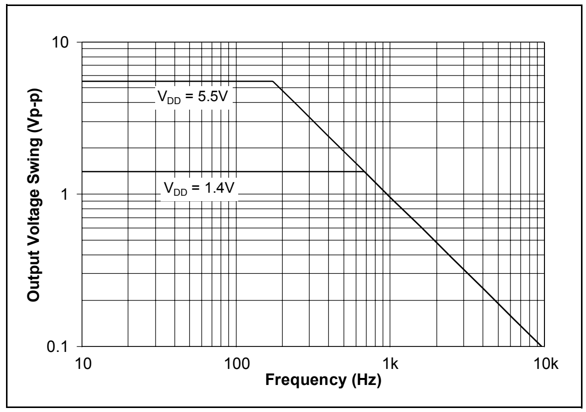


FIGURE 2-34: *Output Voltage Swing vs. Frequency vs. Power Supply Voltage.*

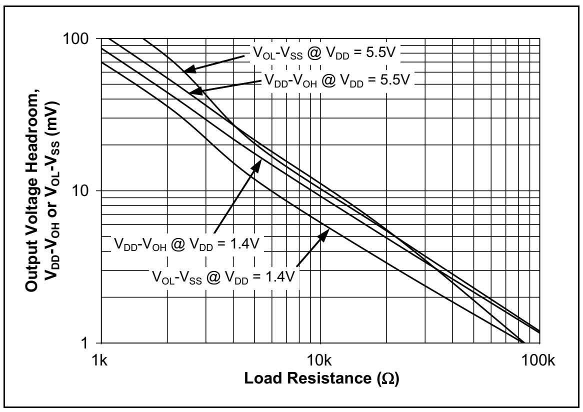


FIGURE 2-32: *Output Voltage Headroom vs. Load Resistance vs. Power Supply Voltage.*

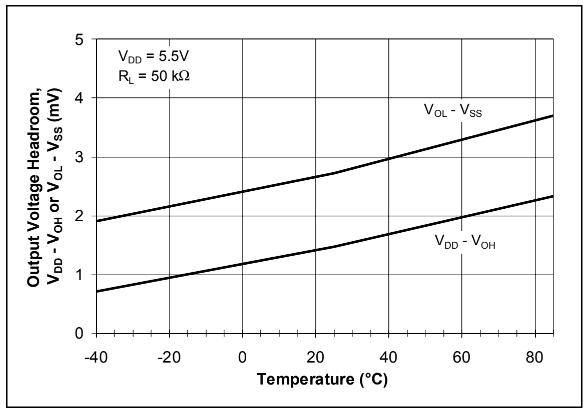


FIGURE 2-35: *Output Voltage Headroom vs. Temperature.*

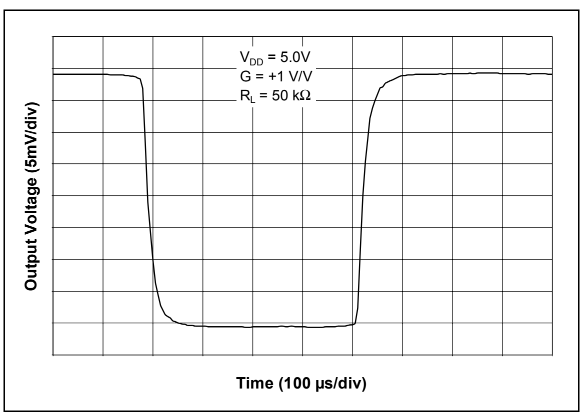


FIGURE 2-33: *Small Signal Non-Inverting Pulse Response.*

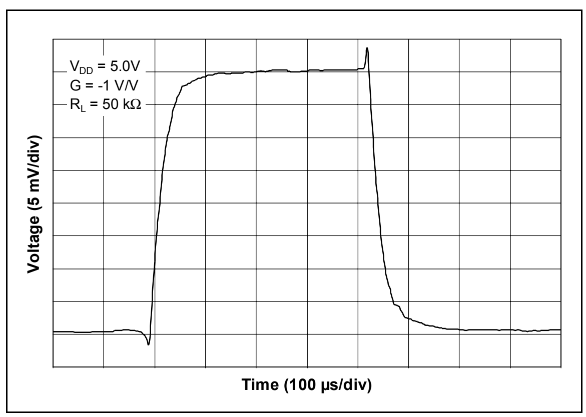


FIGURE 2-36: *Small Signal Inverting Pulse Response.*

Note: Unless otherwise indicated, V_{DD} = +5 V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, R_L = 1 MΩ to V_{DD}/2, C_L = 60 pF, and V_{OUT} ~ V_{DD}/2.

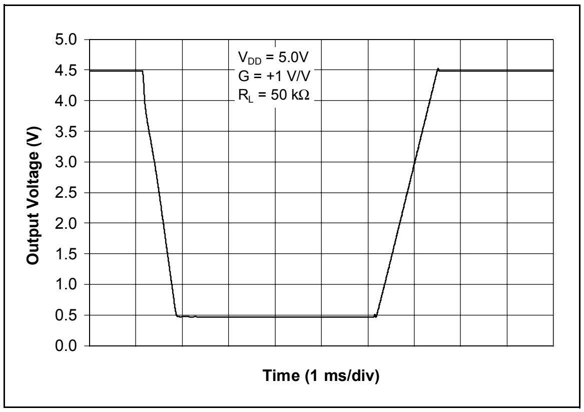


FIGURE 2-37: *Large Signal Non-Inverting Pulse Response.*

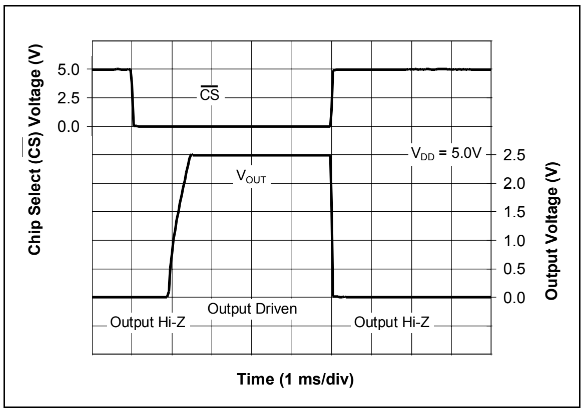


FIGURE 2-38: *Chip Select ($\overline{CS}$) to Amplifier Output Response Time (MCP6043 only).*

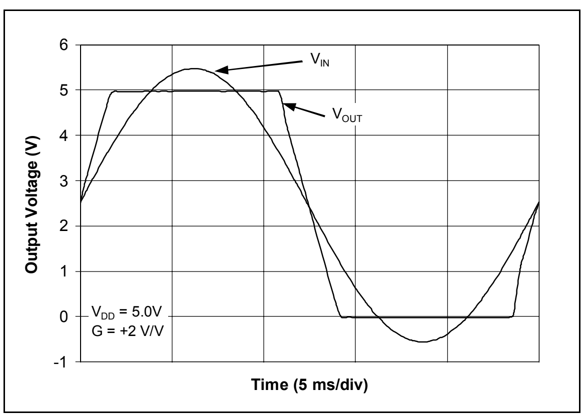


FIGURE 2-39: *The MCP6041/2/3/4 family shows no phase reversal (for information only– the Maximum Absolute Input Voltage is still V_{SS}-0.3 V and V_{DD}+0.3 V).*

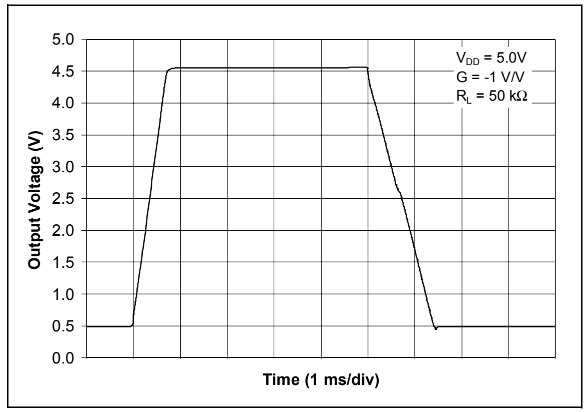


FIGURE 2-40: *Large Signal Inverting Pulse Response.*

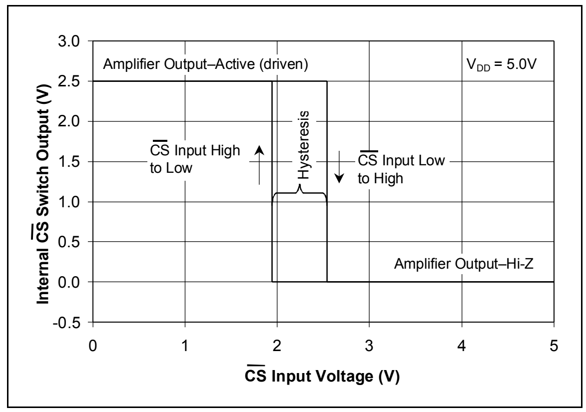


FIGURE 2-41: *Chip Select ($\overline{CS}$) Hysteresis (MCP6043 only).*

3.0 APPLICATIONS INFORMATION

The MCP6041/2/3/4 family of operational amplifiers are fabricated on Microchip's state-of-the-art CMOS process. They are unity gain stable and suitable for a wide range of applications requiring very low power consumption. With these op amps, the power supply pin needs to be by-passed with a 0.1 µF capacitor.

3.1 Rail to Rail Input

The input stage of the family of devices uses two differential input stages in parallel; one operates at low V_{CM} (common mode input voltage) and the other at high V_{CM}. With this topology, the MCP6041/2/3/4 family operates with V_{CM} up to 300 mV past either supply rail. The Input Offset Voltage is measured at both $V_{CM} = V_{SS}$ - 0.3 V and V_{DD} + 0.3 V to ensure proper operation.

3.2 Output Loads and Battery Life

The MCP6041/2/3/4 op amp family has outstanding quiescent current, which supports battery-powered applications. There is minimal quiescent current glitching when chip select ($\overline{CS}$) is raised or lowered. This prevents excessive current draw and reduced battery life, when the part is turned off or on.

Heavy resistive loads at the output can cause excessive battery drain. Driving a DC voltage of 2.5 V across a 100 kΩ load resistor will cause the supply current to increase by 25 µA, depleting the battery 43 times as fast as I_Q (0.6 µA typ) alone.

High frequency signals (fast edge rate) across capacitive loads will also significantly increase supply current. For instance, a 0.1 µF capacitor at the output presents an AC impedance of 15.9 kΩ (1/2πfC) to a 100 Hz sinewave. It can be shown that the average power drawn from the battery by a 5.0 Vp-p sinewave (1.77 Vrms), under these conditions, is:

EQUATION

$$\begin{aligned} P_{SUPPLY} &= (V_{DD} - V_{SS})(I_Q + V_{L(p-p)} f C_L) \\ &= (5V)(0.6\mu A + 5.0V_{p-p} \bullet 100Hz \bullet 0.1\mu F) \\ &= 3.0\mu W + 50\mu W \end{aligned}$$

This will drain the battery 18 times as fast as I_Q alone.

3.3 Rail to Rail Output

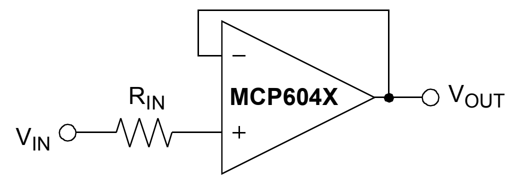
The output voltage range of the MCP6041/2/3/4 family is specified two ways. The first specification, Maximum Output Voltage Swing, defines the maximum swing possible under a particular output load. According to the spec table, the output can reach ≤ 10 mV of either supply rail when R_L = 50 kΩ. See Figure 2-32 for information on Maximum Output Voltage Swing vs. load resistance.

The second specification, Linear Region Output Voltage Swing, details the output voltage range that supports the specified Open Loop Gain (A_{OL} ≥ 95 dB with R_L = 50 kΩ).

3.4 Input Voltage and Phase Reversal

The MCP6041/2/3/4 op amp family uses CMOS transistors at the input. It is designed to not exhibit phase inversion when the input pins exceed the supply voltages. Figure 2-39 shows an input voltage exceeding both supplies with no resulting phase inversion.

The maximum operating V_{CM} (common mode input voltage) that can be applied to the inputs is V_{SS} -0.3 V and V_{DD} +0.3 V. Voltage on the input that exceed this absolute maximum rating can cause excessive current to flow in or out of the input pins. Current beyond ±2 mA can cause possible reliability problems. Applications that exceed this rating must be externally limited with an input resistor as shown in Figure 3-1.



$$R_{IN} \geq \frac{(Maximum\ expected\ V_{IN}) - V_{DD}}{2\ mA}$$

$$R_{IN} \geq \frac{V_{SS} - (Minimum\ expected\ V_{IN})}{2\ mA}$$

FIGURE 3-1: *An input resistor, R_{IN}, should be used to limit excessive input current if the inputs exceed the Absolute Maximum specification.*

3.5 Capacitive Load and Stability

Driving capacitive loads can cause stability problems with voltage feedback op amps. A buffer configuration (G = +1) is the most sensitive to capacitive loads. Figure 2-27 shows how increasing the load capacitance will decrease the phase margin. While a phase margin above 60° is ideal, 45° is sufficient. As can be seen, up to C_L = 150 pF can be placed on the MCP6041/2/3/4 op amp outputs without any problems, while 250 pF is usable with a 45° phase margin.

When the op amp is required to drive large capacitive loads (C_L >150 pF), a small series resistor (R_{ISO} in Figure 3-2) at the output of the amplifier improves the phase margin. This resistor makes the output load resistive at higher frequencies, which improves the phase margin. The bandwidth reduction caused by the capacitive load, however, is not changed. To select R_{ISO}, start with 1 kΩ, then use the MCP6041 SPICE macro model and bench testing to adjust R_{ISO} until the frequency response peaking is reasonable. Use the smallest reasonable value.

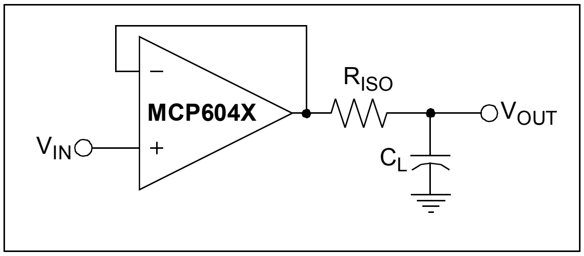


FIGURE 3-2: *Amplifier circuit for heavy capacitive loads.*

3.6 The MCP6043 Chip Select ($\overline{CS}$) Option

The MCP6043 is a single amplifier with a chip select ($\overline{CS}$) option. When $\overline{CS}$ is pulled high, the supply current drops to 20 pA (typ) and goes through the $\overline{CS}$ pin to V_{SS}. When this happens, the amplifier is put into a high impedance state. By pulling $\overline{CS}$ low, the amplifier is enabled. If the $\overline{CS}$ pin is left floating, the amplifier will not operate properly. Figure 3-3 shows the output voltage and supply current response to a $\overline{CS}$ pulse.

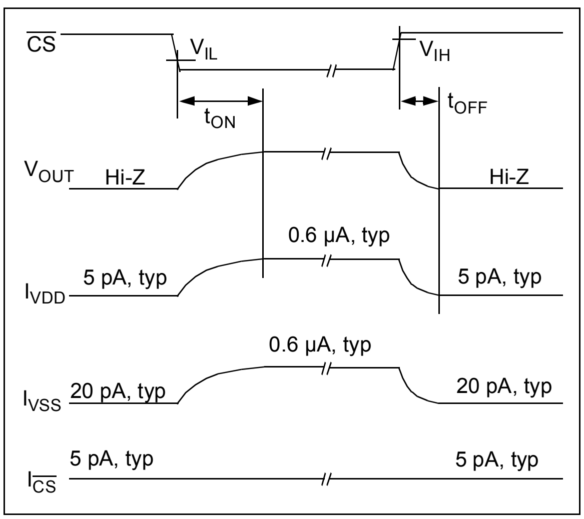


FIGURE 3-3: *Timing Diagram for the $\overline{CS}$ function on the MCP6043 op amp.*

3.7 Layout Considerations

Good PC board layout techniques will help you achieve the performance shown in the specs and Typical Performance Curves. It will also assist in minimizing Electro-Magnetic Compatibility (EMC) issues.

3.7.1 SURFACE LEAKAGE

In applications where low input bias current is critical, PC board surface leakage effects and signal coupling from trace to trace need to be considered.

Surface leakage is caused by a difference in voltage between traces, combined with high humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5 V difference would cause 5 pA of current to flow; this is greater than the input current of the MCP6041/2/3/4 family at 25°C (1 pA, typ).

The simplest technique to reduce surface leakage is using a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin or trace. Figure 3-4 shows an example of a typical layout.

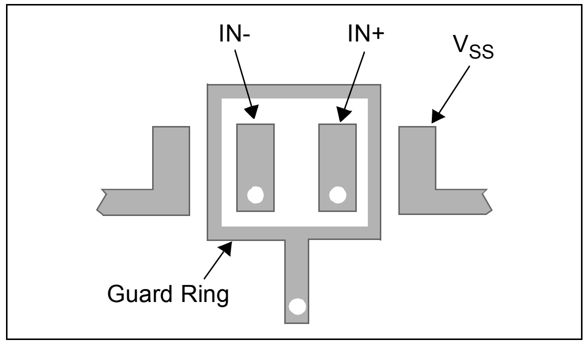


FIGURE 3-4: *Example of Guard Ring layout.*

Circuit schematics for different guard ring implementations are shown in Figure 3-5. Figure 3-5A biases the guard ring to the input common mode voltage, which is most effective for non-inverting gains, including unity gain. Figure 3-5B biases the guard ring to a reference voltage (V_{REF}, which can be ground). This is useful for inverting gains and precision photo sensing circuits.

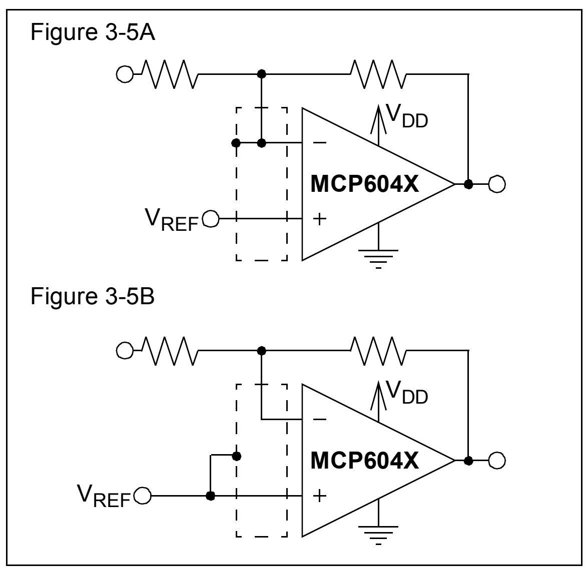


FIGURE 3-5: *Two possible guard ring connection strategies to reduce surface leakage effects.*

3.7.2 COMPONENT PLACEMENT

Separate digital from analog and low speed from high speed. This helps prevent crosstalk.

Keep sensitive traces short and straight. Separate them from interfering components and traces. This is especially important for high frequency (low rise time) signals.

Use a 0.1 µF supply bypass capacitor within 0.1" (2.5 mm) of the V_{DD} pin. It must connect directly to the ground plane.

3.7.3 SIGNAL COUPLING

The input pins of the MCP6041/2/3/4 family of op amps are high impedance, which allows noise injection. This noise can be capacitively or magnetically coupled. In either case, using a ground plane helps reduce noise injection.

When noise is coupled capacitively, the ground plane provides shunt capacitance to ground for high frequency signals. Figure 3-6 shows the equivalent circuit. The coupled current, I_M, produces a lower voltage ($V_{TRACE\ 2}$) on the victim trace when the trace to ground plane capacitance (C_{SH2}) is large and the terminating resistor (R_{T2}) is small. Increasing the distance between traces, and using wider traces, also helps.

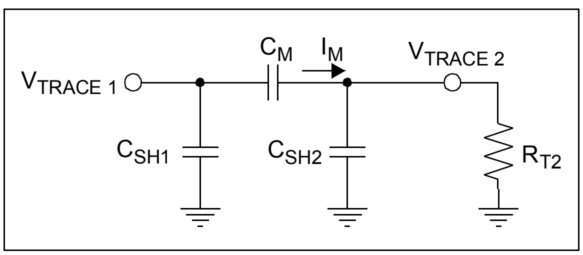


FIGURE 3-6: *Equivalent circuit for capacitive coupling between traces on a PC board (with ground plane).*

When noise is coupled magnetically, ground plane reduces the mutual inductance between traces. This occurs because the ground return current at high frequencies will follow a path directly beneath the signal trace. Increasing the separation between traces makes a significant difference. Changing the direction of one of the traces can also reduce magnetic coupling.

If these techniques are not enough, it may help to place guard traces next to the victim trace. They should be on both sides of the victim trace and be as close as possible. Connect the guard traces to ground plane at both ends, and in the middle, for long traces.

3.8 Typical Applications

3.8.1 BATTERY CURRENT SENSING

The MCP6041/2/3/4 op amps' Common Mode Input Range, which goes 300 mV beyond both supply rails, supports their use in high side and low side battery current sensing applications. The very low quiescent current (0.6 µA, typ) help prolong battery life while the rail-to-rail output allows you to detect low currents.

Figure 3-7 shows a high side battery current sensor circuit. The 10 Ω resistors are sized to minimize power losses. The battery current (I_{DD}) through the 10 Ω resistor causes its top terminal to be more negative than the bottom terminal. This keeps the common mode input voltage of the op amp ≤ V_{DD}, which is within its allowed range. The output of the op amp can reach V_{DD} - 0.1 mV (see Figure 2-32), which is a smaller error than the offset voltage.

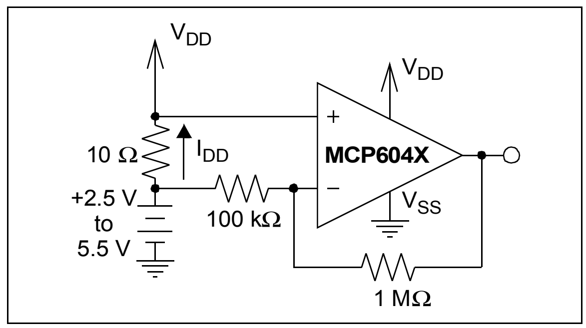
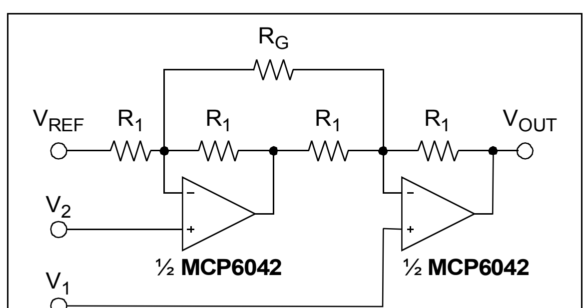


FIGURE 3-7: *High Side Battery Current Sensor.*

3.8.2 INSTRUMENTATION AMPLIFIER

The MCP6041/2/3/4 op amp is well suited for conditioning sensor signals in battery-powered applications. Figure 3-8 shows a two op amp instrumentation amplifier, using the MCP6042, that works well for applications requiring rejection of common mode noise at higher gains. The reference voltage (V_{REF}) is supplied by a low impedance source. In single supply applications, V_{REF} is typically $V_{DD}/2$.



$$V_{OUT} = (V_1 - V_2)\left(1 + \frac{R_1}{R_2} + \frac{2R_1}{R_G}\right) + V_{REF}$$

FIGURE 3-8: *Two Op Amp Instrumentation Amplifier.*

4.0 SPICE MACRO MODEL

The Spice macro model for the MCP6041, MCP6042, MCP6043 and MCP6044 simulates the typical amplifier performance of: offset voltage, DC power supply rejection, input capacitance, DC common mode rejection, open loop gain over frequency, phase margin, output swing, DC power supply current, power supply current change with supply voltage, input common mode range, output voltage range vs. load and input voltage noise.

The characteristics of the MCP6041, MCP6042, MCP6043 and MCP6044 amplifiers are similar in terms of performance and behavior. This single op amp macro model supports all four devices with the exception of the chip select function of the MCP6043, which is not modeled.

The listing for this macro model is shown on the next page. The most recent revision of the model can be downloaded from Microchip's web site at www.microchip.com.

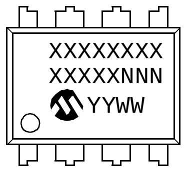

```
.SUBCKT MCP6041 1 2 3 4 5
*               | | | | |
*               | | | | Output
*               | | | Negative Supply
*               | | Positive Supply
*               | Inverting Input
*               Non-inverting Input
*
* Macromodel for the MCP6041/2/3/4 op amp
family:
*   MCP6041 (single)
*   MCP6042 (dual)
*   MCP6043 (single w/ CS; chip select is not
modeled)
*   MCP6044 (quad)
*
* Revision History:
*   REV A: 7-9-01 created KEB
*
* Recommendations:
*   Use PSPICE (other simulators may require
translation)
*   For a quick, effective design, use a com-
bination of: data sheet
*     specs, bench testing, and simulations
with this macromodel
*   For high impedance circuits, set
GMIN=100F in the.OPTIONS
*     statement
*
* Supported:
*   Typical performance at room temperature
(25 degrees C)
*   DC, AC, Transient, and Noise analyses.
*   Most specs, including: offsets, PSRR,
CMRR, input impedance,
*     open loop gain, voltage ranges, supply
current,..., etc.
*
* Not Supported:
*   Chip Select (MCP6043)
*   Variation in specs vs. Power Supply Volt-
age
*   Distortion (detailed non-linear behavior)
*   Temperature analysis
*   Process variation
*   Behavior outside normal operating region
*
* Input Stage
V10  3 10 -0.3
R10 10 11 78K
R11 10 12 78K
C11 11 12 4.9P
C12  1  0 6P
E12  1 14 POLY(4) 20 0 21 0 26 0 27 0   1M 1 1
1 1
G12 14  0 POLY(2) 22 0 23 0   1.5P 1U 1U
M12 11 14 15 15 NMI
C13 14  2 3P
M14 12  2 15 15 NMI
G14  2  0 POLY(2) 24 0 25 0   0.5P 1U 1U
C14  2  0 6P
I15 15  4 500N
V16 16  4 0.18
D16 16 15 DL
V13  3 13 0.00
D13 14 13 DL
*
* Noise Sources
I20 21 20 17.2N
D20 20  0 DN1
D21  0 21 DN1
I22 23 22 588U
D22 22  0 DN23
D23  0 23 DN23
I24 25 24 588U
D24 24  0 DN23
D25  0 25 DN23
*
* PSRR and CMRR
G26  0 26 POLY(1) 3 4   110U -20U
R26 26  0 1
G27  0 27 POLY(2) 1 3 2 4   -275U 50U 50U
R27 27  0 1
*
* Open Loop Gain, Slew Rate
G30  0 30 POLY(1) 12 11   0 1MEG
R30 30  0 1
C30 30  0 11.4
G31  0 31 POLY(1) 30 0   0 1
R31 31  0 1
C31 31  0 775N
*
* Output Stage
G40  0 40 POLY(1) 45 5   0 22.7M
D41 40 41 DL
R41 41  0 1K
D42 42 40 DL
R42 42  0 1K
G43  3  0 POLY(1) 41 0   100N  1M
G47  0  4 POLY(1) 42 0   100N -1M
E43 43  0 POLY(1) 3 0   0 1
```

```
E47 47  0 POLY(1) 4 0   0 1
V44 43 44 1M
D44 45 44 DLS
D46 46 45 DLS
V46 46 47 1M
G45 47 45 POLY(2) 31 0 3 4   0 8U 4U
R45 45 47 125K
R48 45  5 44
C48  5  0 2P
*
* Models
.MODEL NMI NMOS L=2 W=42
.MODEL DL   D N=1   IS=1F
.MODEL DLS  D N=1M  IS=1F
.MODEL DN1  D IS=1F KF=1.13E-18 AF=1
.MODEL DN23 D IS=1F KF=3E-20    AF=1
*
.ENDS MCP6041
```

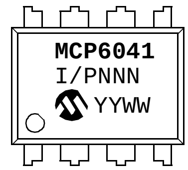
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

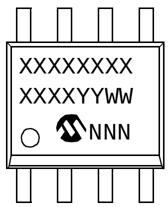
8-Lead PDIP (300 mil)



Example:



8-Lead SOIC (150 mil)



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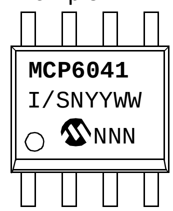
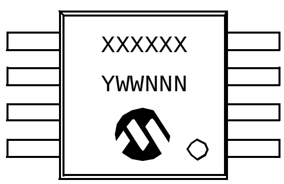
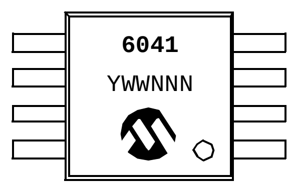


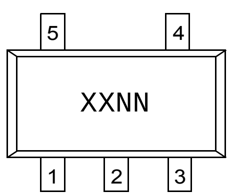
8-Lead MSOP



Example:



5-Lead SOT-23 (MCP6041 only)



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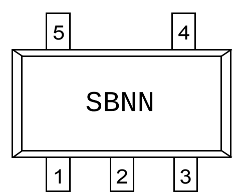


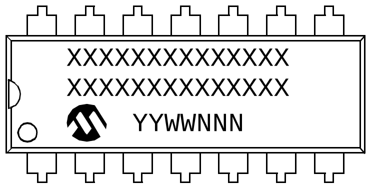
Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

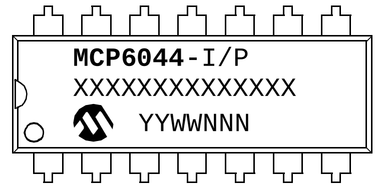
* Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

5.1 Package Marking Information (Continued)

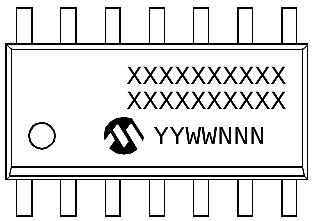
14-Lead PDIP (300 mil) (MCP6044)



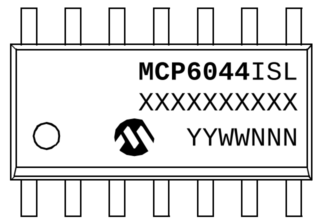
Example:



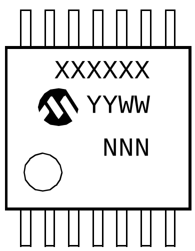
14-Lead SOIC (150 mil) (MCP6044)



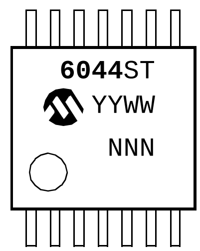
Example:



14-Lead TSSOP (MCP6044)



Example:

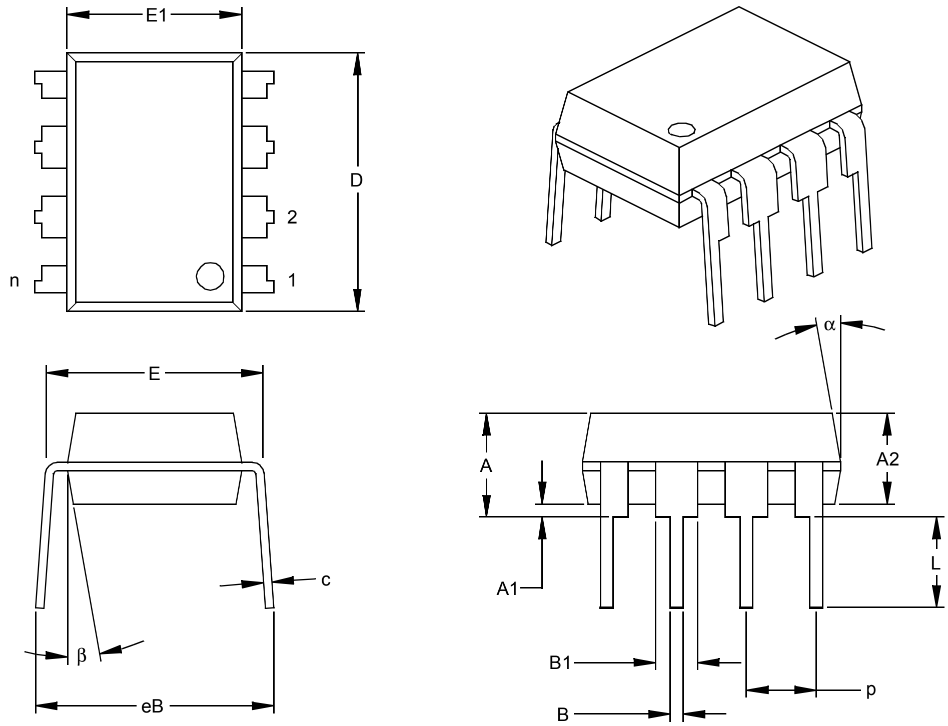


Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

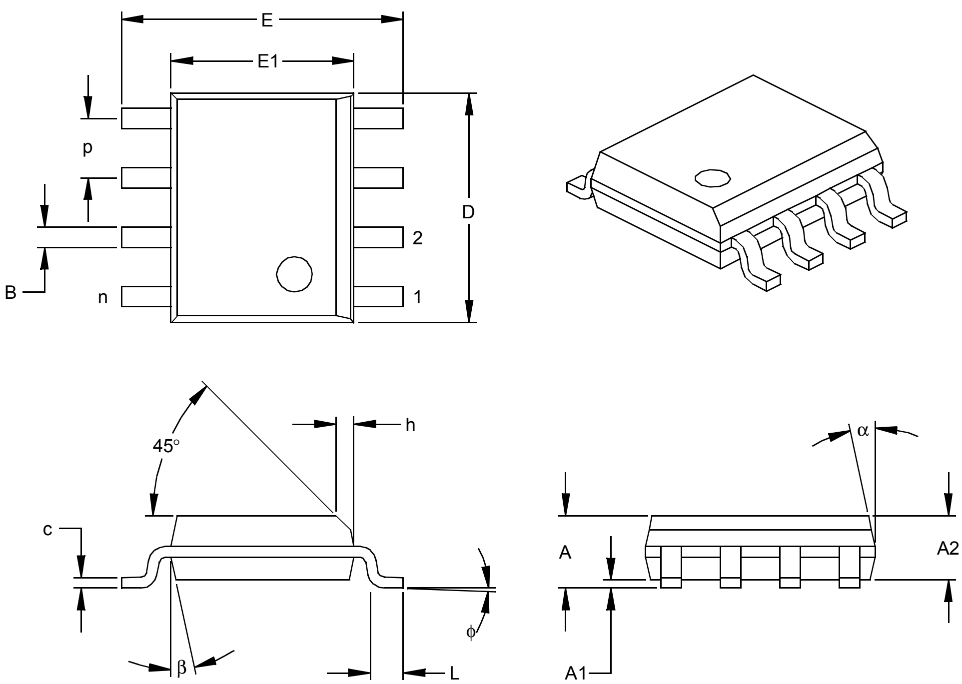


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

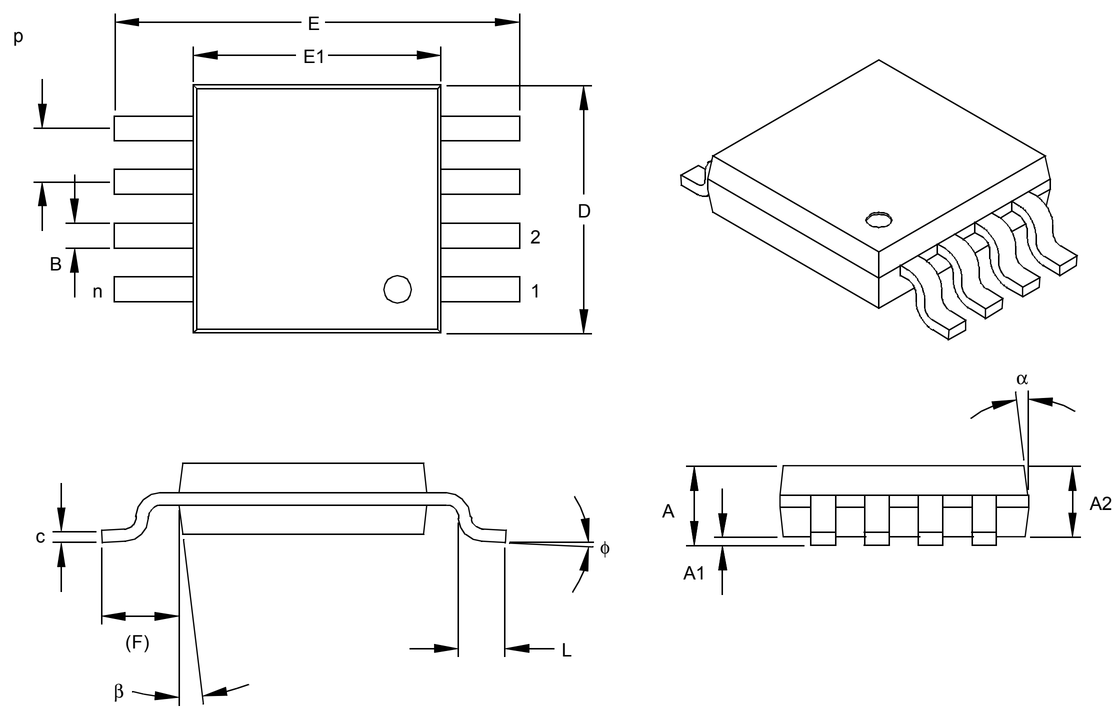


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8				8
Pitch	p		.026			0.65	
Overall Height	A			.044			1.18
Molded Package Thickness	A2	.030	.034	.038	0.76	0.86	0.97
Standoff §	A1	.002		.006	0.05		0.15
Overall Width	E	.184	.193	.200	4.67	4.90	.5.08
Molded Package Width	E1	.114	.118	.122	2.90	3.00	3.10
Overall Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.016	.022	.028	0.40	0.55	0.70
Footprint (Reference)	F	.035	.037	.039	0.90	0.95	1.00
Foot Angle	φ	0		6	0		6
Lead Thickness	c	.004	.006	.008	0.10	0.15	0.20
Lead Width	B	.010	.012	.016	0.25	0.30	0.40
Mold Draft Angle Top	α		7			7	
Mold Draft Angle Bottom	β		7			7	

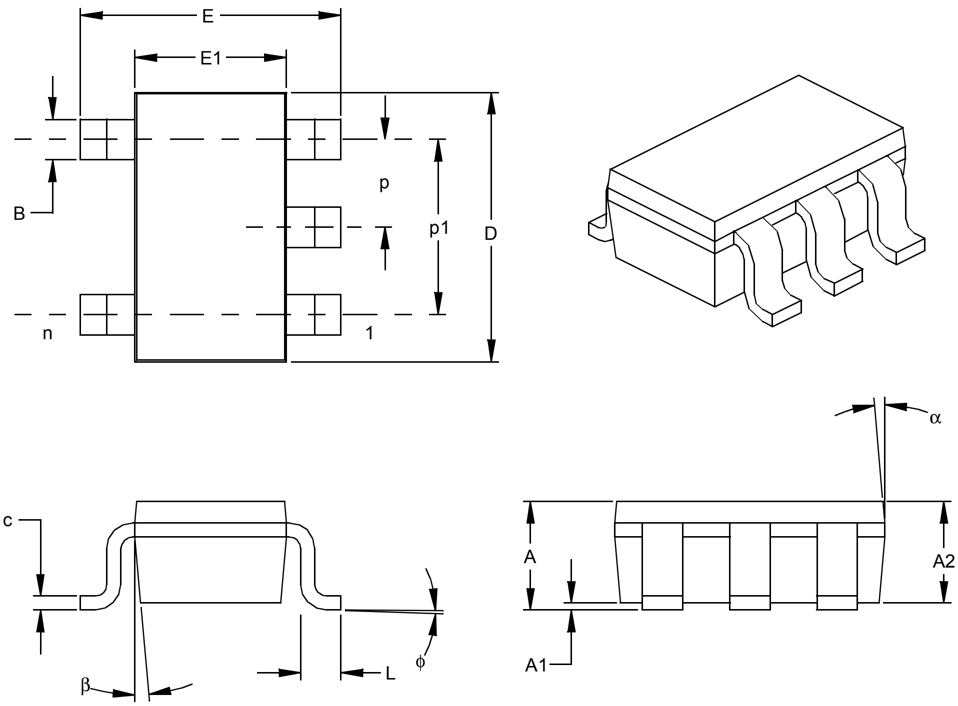
*Controlling Parameter
§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

Drawing No. C04-111

5-Lead Plastic Small Outline Transistor (OT) (SOT23)

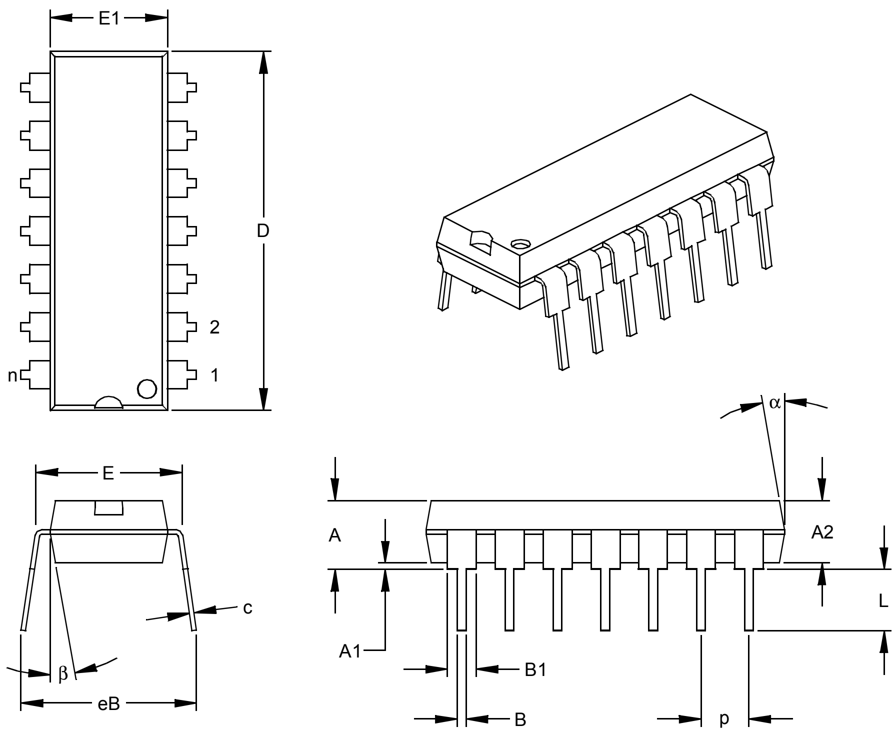


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		5			5	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff §	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	φ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MO-178
Drawing No. C04-091

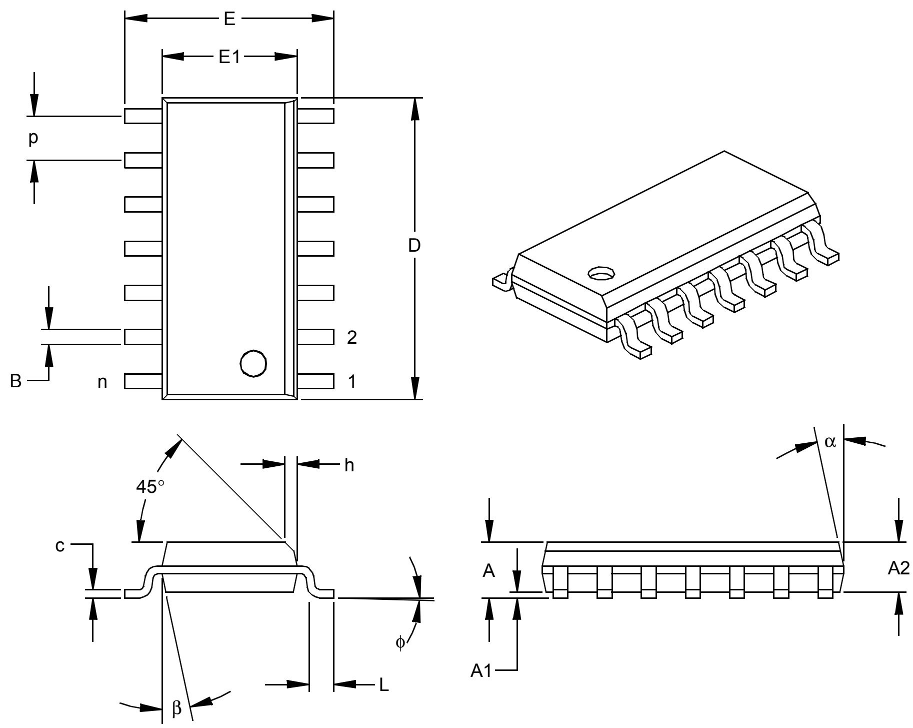
14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-005

14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)

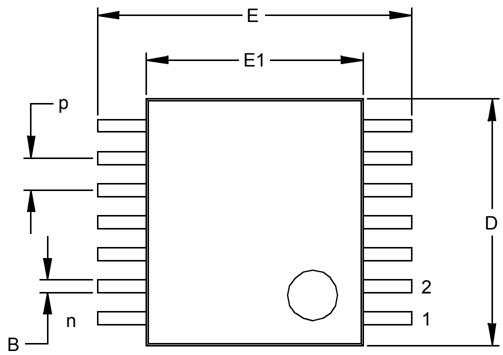


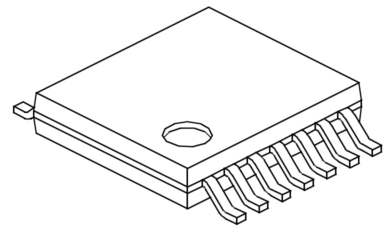
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

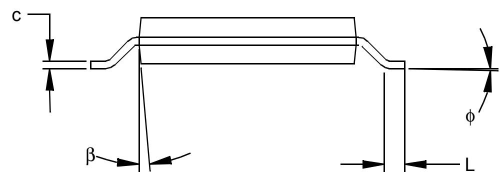
* Controlling Parameter
§ Significant Characteristic

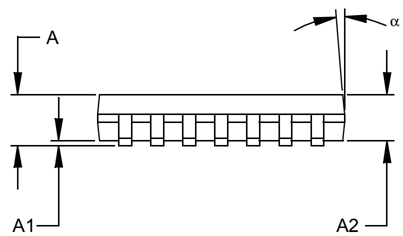
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-065

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)









Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B1	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-087

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013001

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PART NO.	X	/XX
Device	Temperature Range	Package

Device:	MCP6041:	CMOS Single Op Amp
	MCP6041T:	CMOS Single Op Amp (Tape and Reel for SOT-23, SOIC, MSOP)
	MCP6042:	CMOS Dual Op Amp
	MCP6042T:	CMOS Dual Op Amp (Tape and Reel for SOIC and TSSOP)
	MCP6043:	CMOS Single Op Amp w/$\overline{CS}$ Function
	MCP6043T:	CMOS Single Op Amp w/$\overline{CS}$ Function (Tape and Reel for SOIC and MSOP)
	MCP6044:	CMOS Quad Op Amp
	MCP6044T:	CMOS Quad Op Amp (Tape and Reel for SOIC and TSSOP)
Temperature Range:	I =	-40°C to +85°C
Package:	MS =	Plastic MSOP, 8-lead
	P =	Plastic DIP (300 mil Body), 8-lead, 14-lead
	SN =	Plastic SOIC (150 mil Body), 8-lead
	OT =	Plastic Small Outline Transistor (SOT-23), 5-lead (Tape and Reel - MCP6041 only)
	SL =	Plastic SOIC (150 mil Body), 14-lead
	ST =	Plastic TSSOP (4.4mm Body), 14-lead

Examples:

a) MCP6041-I/P: Industrial temperature, PDIP package.
b) MCP6041T-I/OT: Tape and Reel, Industrial temperature, SOT-23 package.
c) MCP6042-I/SN: Industrial temperature, SOIC package.
d) MCP6043-I/MS: Industrial temperature, MSOP package.
e) MCP6044-I/SL: Industrial temperature, SIOC package.
f) MCP6044-I/ST: Industrial temperature, TSSOP package.

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