MP7652

EXAR

4-Channel Voltage Output 15 MHz, Input Bandwidth, 8-Bit Multiplying DACs with 3-Wire Serial Digital Port and Independent References

FEATURES

- **Independent References**
- **4 Independent 2-Quadrant Multiplying 8-Bit DACs**
- **Dual Positive (+10 V and +5 V) Supplies or Dual (±5 V) Supplies Capability**
- **High Speed:**
  - **12.5 MHz Digital Clock Rate**
  - **V_{REF} to V_{OUT} Settling Time: 150ns to 8–bit (typ)**
  - **Voltage Reference Input Bandwidth: 15 MHz**
- **Low Power: 80mW**
- **Low AC Voltage Reference Feedthrough**
- **Excellent Channel-to-Channel Isolation**
- **DNL = ±0.5 LSB, INL = ±1 LSB (typ)**
- **DACs Matched to ±0.5% (typ)**
- **Very Low Noise**
- **Low Harmonic Distortion: 0.25% typical with V_{REF} = 1 V p-p @ 1 MHz**
- **V_{REF}/2 Output Preset Level**
- **Latch-Up Free**
- **ESD Protection: 2000 V Minimum**

APPLICATIONS

- **Direct High-Frequency Automatic Gain Control**
- **Video AGC & CCD Level AGC**
- **Convergence Adjustment for High-Resolution Monitors (Workstations)**

GENERAL DESCRIPTION

The MP7652 is ideal for digital gain control of high frequency analog signals such as video, composite video, CCD and others. The device includes 4-channels of high speed, wide bandwidth, two quadrant multiplying, 8-bit accurate digital-to-analog converter. It includes an output drive buffer per channel capable of driving a ±1mA (typ) load. DNL of better than ±0.5 LSB is achieved with a channel-to-channel matching of typically 0.5%. Stability, matching, and precision of the DACs are achieved by using MPS' thin film technology. Also, excellent channel-to-channel isolation is achieved with EXAR's BiCMOS process which cannot be achieved using a typical CMOS technology.

An open loop architecture (patent pending) provides wide small signal bandwidth from V_{REF} to output up to 15 MHz (typ), fast output settling time of 150 ns, and excellent V_{REF} feedthrough isolation. The bottom of each DAC reference string is brought out separately for totally isolated operation. In addition, low distortion in the order of 0.25% with a 1 V p-p, 1 MHz signal is achieved.

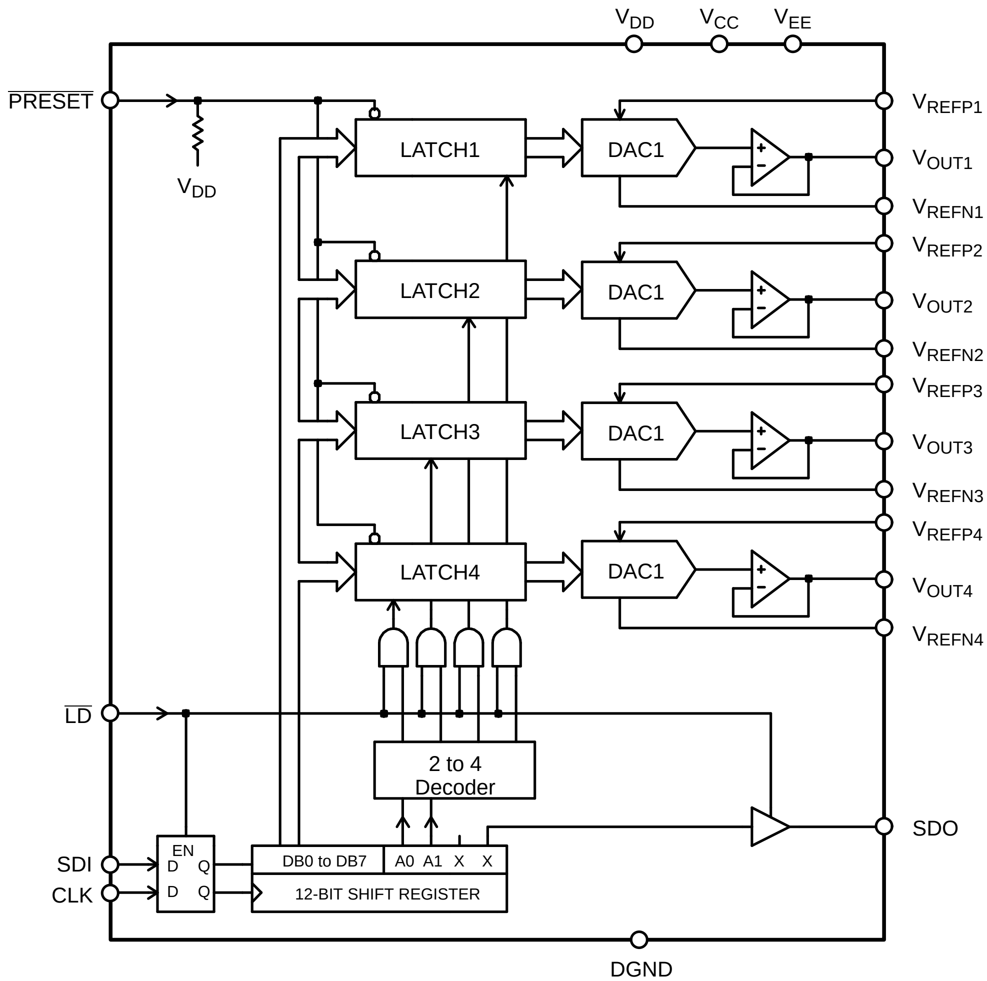
The combination of a constant input Z and the ability to vary V_{REFN} within V_{CC} –1.8 and V_{EE} +1.5 V allows flexibility for optimum system design.

The MP7652 is fabricated on a junction isolated, high speed BiCMOS (BiCMOS IV^{TM}) process with thin film resistors. This process enables precision high speed analog/digital (mixed-mode) circuits to be fabricated on the same chip.

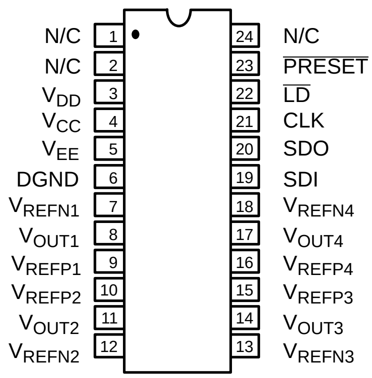
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
SOIC	–40 to +85°C	MP7652AS	±1	±0.5	±1.5
Plastic Dip	–40 to +85°C	MP7652AN	±1	±0.5	±1.5

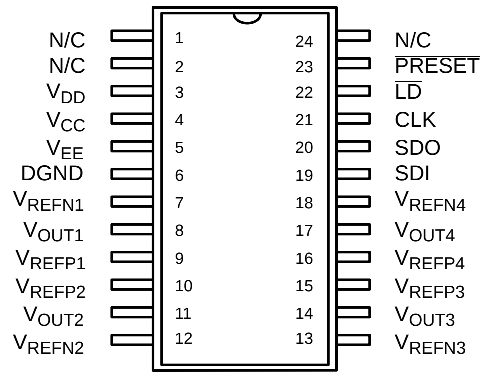
SIMPLIFIED BLOCK DIAGRAM



PIN CONFIGURATIONS



24 Pin PDIP (0.300”)
NN24



24 Pin SOIC (Jedec, 0.300”)
S24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	N/C	No Connection
2	N/C	No Connection
3	V_{DD}	Digital Positive Supply
4	V_{CC}	Analog Positive Supply
5	V_{EE}	Analog Negative Supply
6	DGND	Digital Ground
7	V_{REFN1}	DAC 1 Negative Reference Input
8	V_{OUT1}	DAC 1 Output
9	V_{REFP1}	DAC 1 Positive Reference Input
10	V_{REFP2}	DAC 2 Positive Reference Input
11	V_{OUT2}	DAC 2 Output
12	V_{REFN2}	DAC 2 Negative Reference Input
13	V_{REFN3}	DAC 3 Negative Reference Input

PIN NO.	NAME	DESCRIPTION
14	V_{OUT3}	DAC 3 Output
15	V_{REFP3}	DAC 3 Positive Reference Input
16	V_{REFP4}	DAC 4 Positive Reference Input
17	V_{OUT4}	DAC 4 Output
18	V_{REFN4}	DAC 4 Negative Reference Input
19	SDI	Serial Data and Address Input
20	SDO	Serial Data Output
21	CLK	Shift Register Clock Input
22	$\overline{LD}$	Load Data to Selected DAC
23	$\overline{PRESET}$	Preset all DACs to 1/2 $(V_{REF} – V_{REFN})$. $\overline{PRESET}$ is internally connected to V_{DD} through 300 kΩ.
24	N/C	No Connection

ELECTRICAL CHARACTERISTICS TABLE FOR DUAL SUPPLIES

Unless Otherwise Noted: V_{DD} = 5 V, V_{CC} = +5 V, V_{EE} = –5 V, V_{REFP} = 3 V and –3 V, T = 25°C, Output Load = Open, DGND=V_{REFN} = 0 V

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DC CHARACTERISTICS						
Resolution (All Grades)	N	8			Bits	
Differential Non-Linearity	DNL			±0.8	LSB	
Integral Non-Linearity	INL			±1	LSB	
Monotonicity			Guaranteed			
Gain Error	GE			±1.5	% FSR	FSR = Full Scale Range[1]
Zero Scale Offset	Z_{OFS}			±50	mV	
Output Drive Capability	I_O		±1		mA	
REFERENCE/INV INPUTS						
Impedance of V_{REF}	REF	6		18	kΩ	
Voltage Range	V_R	V_{EE} +1.5		V_{CC} –1.8	V	V_{REFP} Max Swing is V_{REFN} ±3 V
V_{REFN} DC Voltage Range	INV Pos.		V_O		V	
	INV Neg.		V_{EE} ± 1		V	
DYNAMIC CHARACTERISTICS[2]						R_L = 5 kΩ, C_L = 20 pF
Input to Output Bandwidth			15		MHz	V_{REFP}=1.6 Vp–p, R_L =5kΩ, to V_{EE}
Input to Output Settling Time[6]			150		ns	V_{REFP}=1.6Vp–p, R_L =5kΩ, to V_{EE}
Small Signal Voltage Reference Input to Output Bandwidth	ft_r		15		MHz	V_{OUT}=50mV p-p above code 16
Small Signal Voltage Reference Input to Output Bandwidth	ft_r		15		MHz	V_{OUT}=50mV p-p for all codes
Voltage Settling from V_{REF} to V_{DAC} Out	t_{sr}		275		ns	V_{REFP}=0 to V_{REFP} = 3V Step[6] to 1 LSB
Voltage Settling from Digital Code to V_{DAC} Out	t_{sd}		275		ns	ZS to FS to 1 LSB
V_{REF} Feedthrough	F_{DT}		TBD		dB	Codes=0 @ 1 MHz
Group Delay	GD		TBD		ns	
Harmonic Distortion	T_{HD}		TBD		%	V_{REFP}=1MHz Sine 3V p-p
Channel-to-Channel Crosstalk	C_T		TBD		dB	@ 1 MHz, single channel
Digital Feedthrough	Q		TBD		nVs	CLK to V_{OUT}
Power Supply Rejection Ratio	PSRR		±0.5		%/%	ΔV=±5%
POWER CONSUMPTION						
Positive Supply Current	I_{CC}		12		mA	V_{REFP} = 0 V
Negative Supply Current	I_{EE}		12		mA	V_{REFP} = 0 V
Power Dissipation	P_{DISS}		80		mW	V_{REFP} = 0 V, Codes = all 1
DIGITAL INPUT CHACTERISTICS						
Logic High[3]	V_{IH}	2.4			V	
Logic Low[3]	V_{IL}			0.8	V	
Input Current	I_L			±10	µA	
Input Capacitance[2]	C_L			8	pF	

ELECTRICAL CHARACTERISTICS TABLE

Description	Symbol	25°C Min	25°C Typ	25°C Max	Units	Conditions
DIGITAL TIMING SPECIFICATIONS[2, 4]						
Input Clock Pulse Width	t_{CH}, t_{CL}	60			ns	
Data Setup Time	t_{DS}	70			ns	
Data Hold Time	t_{DH}	0			ns	
CLK to SDO Propagation Delay	t_{PD}			150	ns	
DAC Register Load Pulse Width	t_{LD}	100			ns	
$\overline{\text{PRESET}}$ Pulse Width	t_{PR}	50			ns	
Clock Edge to Load Rising Edge	t_{CKLD1}	100			ns	
Clock Edge to Load Falling Edge	t_{CKLD2}	0			ns	
Load Falling Edge to SDO Tri-state Enable	t_{HZ1}	80			ns	
Load Rising Edge to SDO Tri-state Disable	t_{HZ2}	40			ns	
Load Falling Edge to CLK Disable	t_{LDCK1}	30			ns	
Load Rising Edge to CLK Enable	t_{LDCK2}	60			ns	
LD Set-up Time with Respect to CLK	t_{LDSU}	20			ns	

NOTES

1 Full Scale Range (FSR) is 3V.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 *See Figures 1 and 2.*
5 For reference input pulse: $t_R = t_F \geq 100$ ns.

Specifications are subject to change without notice

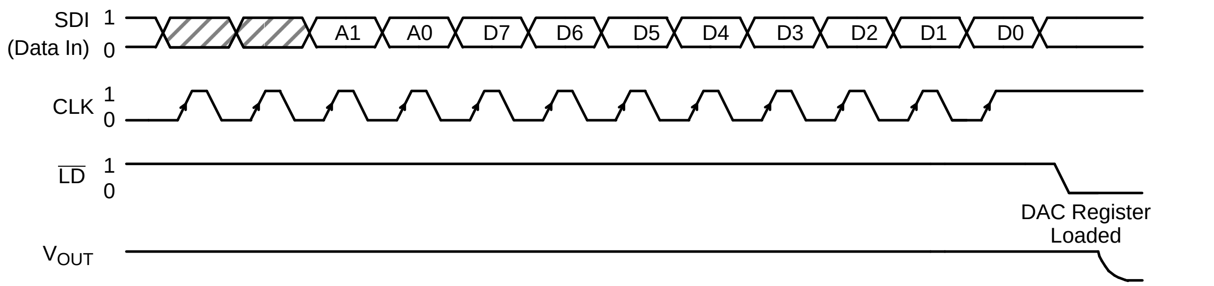
ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)[1, 2]

V_{CC} to V_{REFN} . . . . +6.5 V
V_{EE} to V_{REFN} . . . . –6.5 V
V_{CC} to DGND . . . . +13.0 V
V_{EE} to DGND . . . . –6.5 V
V_{REFP} 1-4 to DGND, V_{REFN} . . . . V_{CC} to V_{EE}
Digital Input & Output Voltage to DGND –0.5 to V_{DD} +0.5 V
Operating Temperature Range
Extended Industrial . . . . –40°C to +85°C

Maximum Junction Temperature . . . . –65°C to 150°C
Storage Temperature . . . . 150°C
Lead Temperature (Soldering, 10 sec) . . . . +300°C
Package Power Dissipation Rating @ 75°C
PDIP, SOIC 1000mW
Derates above 75°C . . . . 6mW/°C

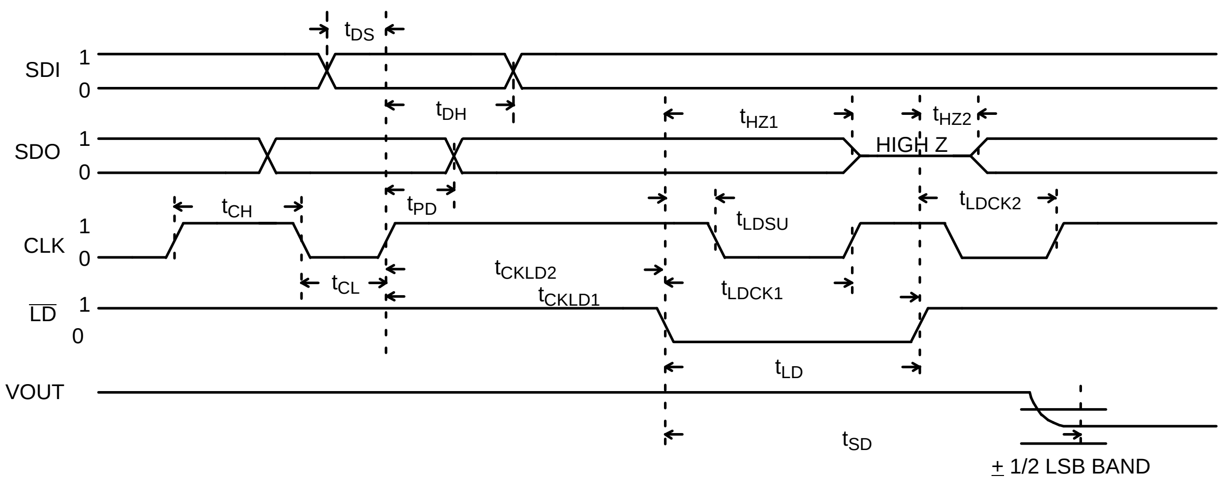
NOTES:

1 Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.



(PRESET = "High" or open)

Figure 1. Serial Data Timing and Loading



(PRESET = "High" or open)

Figure 2. Detail Serial Data Input Timing

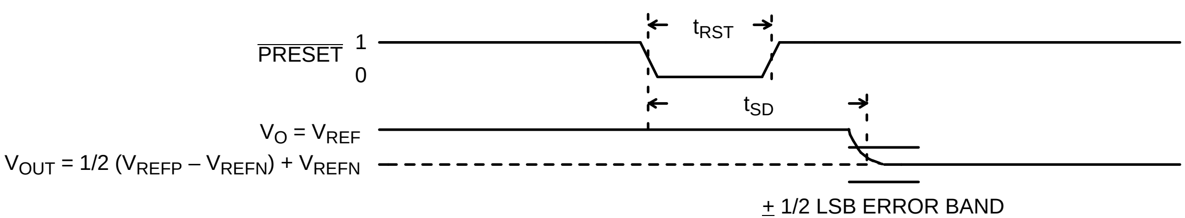


Figure 3. PRESET Operation

THEORY OF OPERATION

The MP7652 is a 4-channel multiplying D/A converter that incorporates a novel open loop architecture invented by MPS. The design produces the widest bandwidth, fastest settling time, most constant group delay, and a very low noise operation compared to the conventional R-2R based architectures (given an equal technology platform). This device is particularly useful in applications where analog multipliers are used to perform the gain adjustment function for high frequency analog signal conditioning. Analog multipliers produce much higher noise and. This design allows for digital control of gain with constant and very low noise for all gain settings.

Linearity Characteristics

Each DAC achieves DNL $\leq \pm$0.5 LSB (typ), INL $\leq \pm$1 LSB (typ), and gain error $\leq \pm$1.5%. Since all 4 channel D/A converters are fabricated on the same IC, the linearity matching and gain matching of $\pm$0.5% (typ) is achieved.

AC and Low Noise Performance

The novel subranging architecture delivers a 15 MHz (type) –3 dB bandwidth. A constant group delay of 70 ns (typ) is achieved to frequencies up to 8 MHz. Analog output settling time for a code change of FS to ZS and ZS to FS with V_{REFP} = 3 V, is typically 150 ns (with R_L = 5 k to V_{EE}). Also, with all codes set to FS (all 1s) and a V_{REFP} 3 V step, the analog output will settle to 8 bits in less than 110 ns (typ). Note that the AC performance specifications also match to between all 4 channels. The above AC and transient performance is achieved with each channel consuming only 20 mW (typ) with 10 V p-p supplies.

Serial Port

MP7652 is equipped with a serial data 3-wire standard µ-processor logic interface to reduce pin count, package size, and board wire (space). This interface consists of $\overline{LD}$ which controls the transfer of data to the selected DAC channel, SDI (serial data/address input), CLK (shift register clock) and SDO (serial data output). When the $\overline{LD}$ signal is high, CLK signal loads the digital input bits (SDI) into the 12-bit shift register. The $\overline{LD}$ signal going low loads this data into the selected DAC. The $\overline{LD}$ signal going low also disables the serial data input (SDI), output (SDO tri-stated) and the CLK input. This design tremendously reduces digital noise, and glitch transients into the DACs due to free running CLK and SDI. Also, tri-stating the SDO output with $\overline{LD}$ signal would allow read back of pre-stored digital data of the selected package using one SDO wire for all DAC ICs on the board. When the $\overline{PRESET}$ signal is low, the output of all DACs are 1/2 of (V_{REFP} + V_{REFN}), regardless of any digital inputs. Note that V_{REFP} is referenced to V_{REFN}.

Power Supplies and Voltage Reference DC Voltage Ranges

For the single supply operation, V_{CC} = +10 V, V_{DD} = +5 V, and V_{EE} = DGND = 0 V. The V_O 1-4 and V_{REFP} 1-4 range would be V_{CC} –1.8 V (10 – 1.8 = 8.2 V) to V_{EE} +1.5 V (0 + 1.5 = 1.5 V). V_{REFN} is the equivalent of AGND for this DAC. In this mode V_{REFN} can be set at (V_{CC} + V_{EE})/2 = (10 + 0)/2 = 5 V. V_{REFN} 1-4 DC range can also be set from V_{EE} +1.5 = 1.5 V to V_{CC} – 1.5 = 8.2 V. Refer to *Table 2.* for the relationship equations.

For the dual supply operation, V_{CC} = +5, V_{DD} = +5, and V_{EE} = –5 V. The V_{OUT} 1-4 and V_{REFP} 1-4 range would be V_{CC} –1.8 V (–1.8 = 3.2 V) to V_{EE} +1.5 V (–5 + 1.5 = –3.5 V). In this mode V_{REFN} can be set to (V_{CC} + V_{EE})/2 = (5 – 5)/2 = 0 V. Similarly, V_{REFN} 1-4 DC range can be set from V_{EE} +1.5 V = 3.5 V to V_{CC} –1.8 = +3.2 V. Refer to *Table 2.* for the relationship equations.

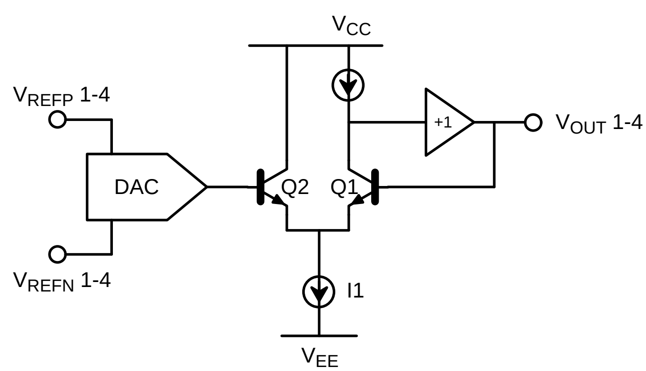


Figure 4. Simplified Block Diagram

Inputs				Internal Address		Output	
$\overline{PRESET}$	SDI	CLK	$\overline{LD}$	A1	A0	SDO	Operation
0	X	X	X	X	X	X	Preset all DACs to 1/2 (V_{REFP} + V_{REFN})
1	Data In	0→1	1	X	X	Last bit of shift reg.	Shift data in and out
1	X	X	0	0	0	Hi-Z	DAC 1 Transparent
1	X	X	0→1	0	0	Last bit of shift reg.	DAC 1 Latched
1	X	X	0	0	1	Hi-Z	DAC 2 Transparent
1	X	X	0→1	0	1	Last bit of shift reg.	DAC 2 Latched
1	X	X	0	1	0	Hi-Z	DAC 3 Transparent
1	X	X	0→1	1	0	Last bit of shift reg.	DAC 3 Latched
1	X	X	0	1	1	Hi-Z	DAC 4 Transparent
1	X	X	0→1	1	1	Last bit of shift reg.	DAC 4 Latched

Table 1. Digital Function Truth Table
Serial In/Serial Out

D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DAC Output Voltage $V_{OUTi} = V_{REFNi} + (V_{REFPi} - V_{REFNi})\left(\frac{D}{256}\right)$
0	0	0	0	0	0	0	0	V_{REFN}
0	0	0	0	0	0	0	1	$(V_{REFP} - V_{REFN})\left(\frac{1}{256}\right) + V_{REFN}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	$(V_{REFP} - V_{REFN})\left(\frac{254}{256}\right) + V_{REFN}$
1	1	1	1	1	1	1	1	$(V_{REFP} - V_{REFN})\left(\frac{255}{256}\right) + V_{REFN}$

Table 2. DAC Transfer Function
Analog Output vs. Digital Code

OPERATION WITH DUAL POSITIVE POWER SUPPLIES

For the dual positive supplies operation, V_{CC} = +10 V, V_{DD} = 5 V, V_{EE} = 0 V and analog output zero level is to be referenced to (V_{CC} + V_{EE}) /2 by setting the AGND pin to 5 V.

MICROPROCESSOR INTERFACE

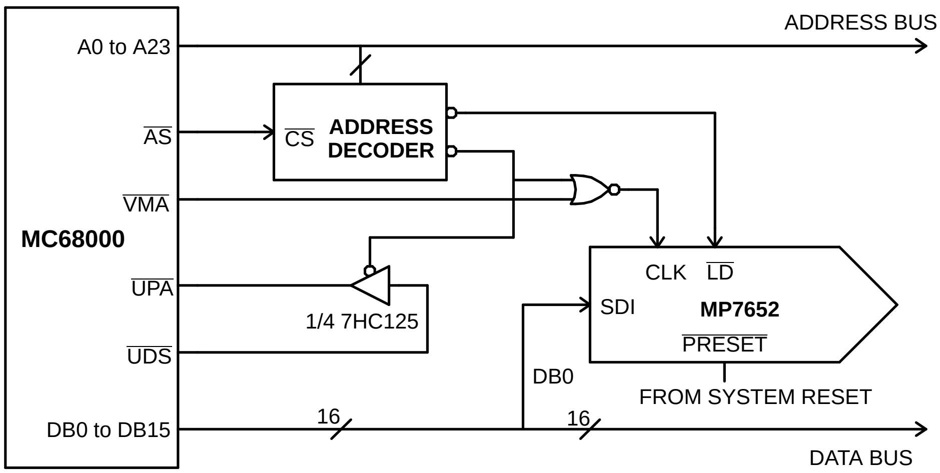
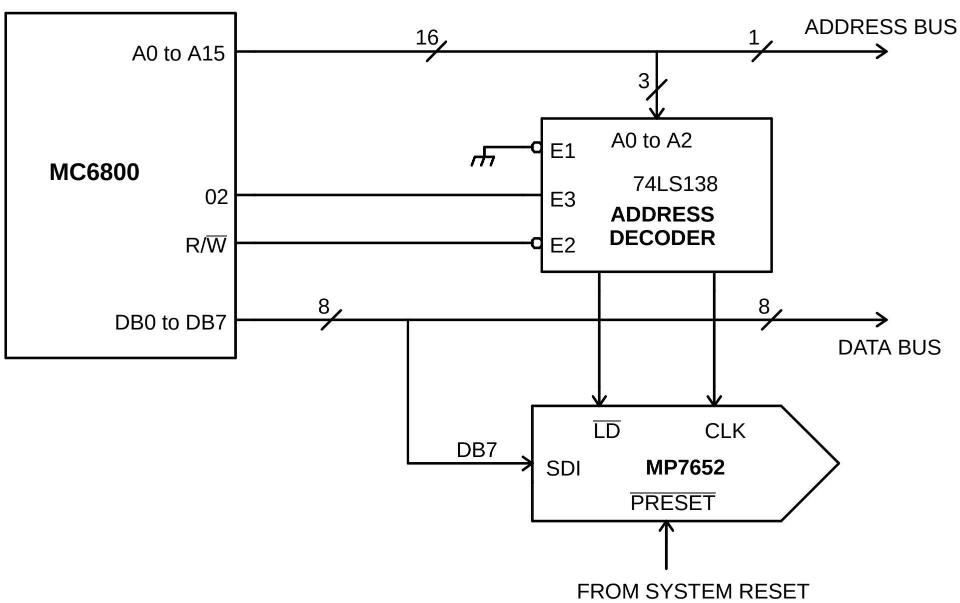


Figure 5. MC68000 Interface (Simplified Diagram)



NOTES:
1. Execute consecutive memory write instructions while manipulating the data between WRITEs so that each WRITE presents the next bit
2. The serial data loading is triggered by the CLK pulse which is asserted by a decoded memory WRITE location 2000, R/W, and 02. A WRITE to address 4000 transfers data from the input shift register to the DAC register.

Figure 6. MC6800 Interface (Simplified Diagram)

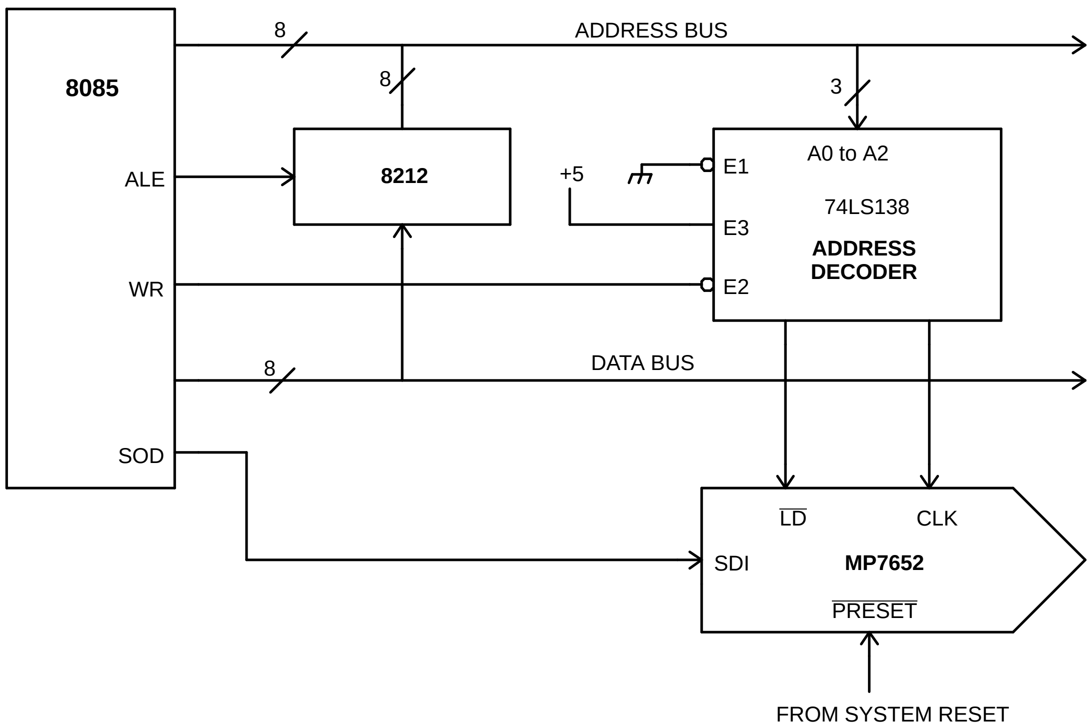


Figure 7. 8085 Interface (Simplified Diagram)

NOTES:

1. Clock generated by $\overline{WR}$ and decoding address 8000
2. Data is clocked into the DAC shift register by executing memory write instructions. the clock input is generated by decoding address 8000 and $\overline{WR}$. Data is then loaded into the DAC register with a memory write instruction to address 4000.
3. Serial data must be present in the right justified format in registers H & L of the microprocessor.

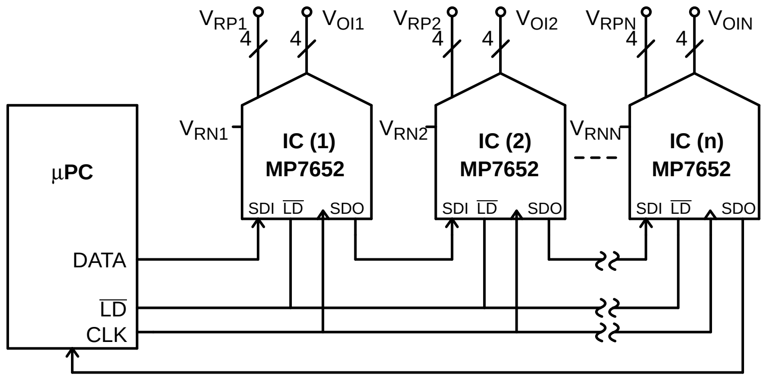


Figure 8. Simplified Diagram
Configuration A

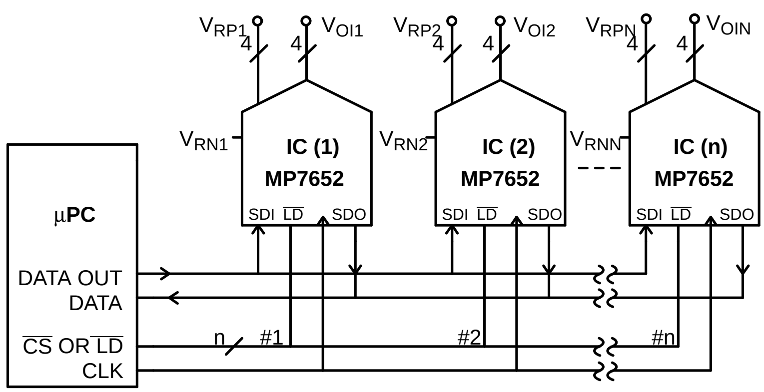


Figure 9. Simplified Diagram
Configuration B

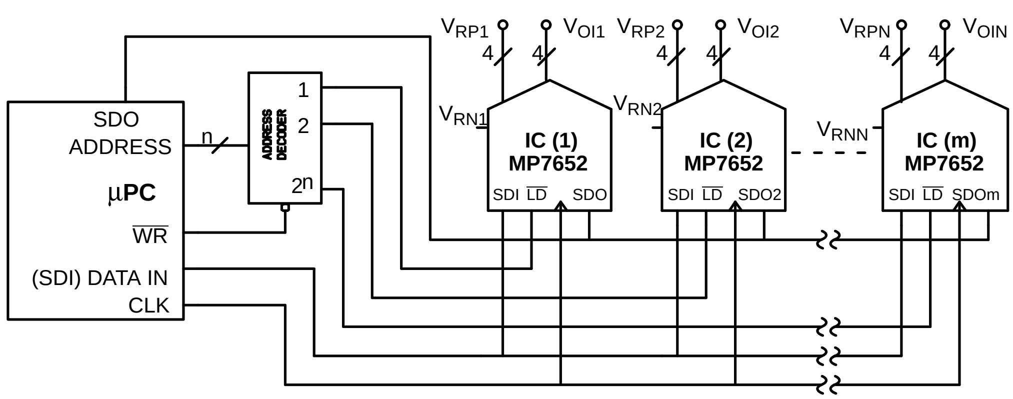
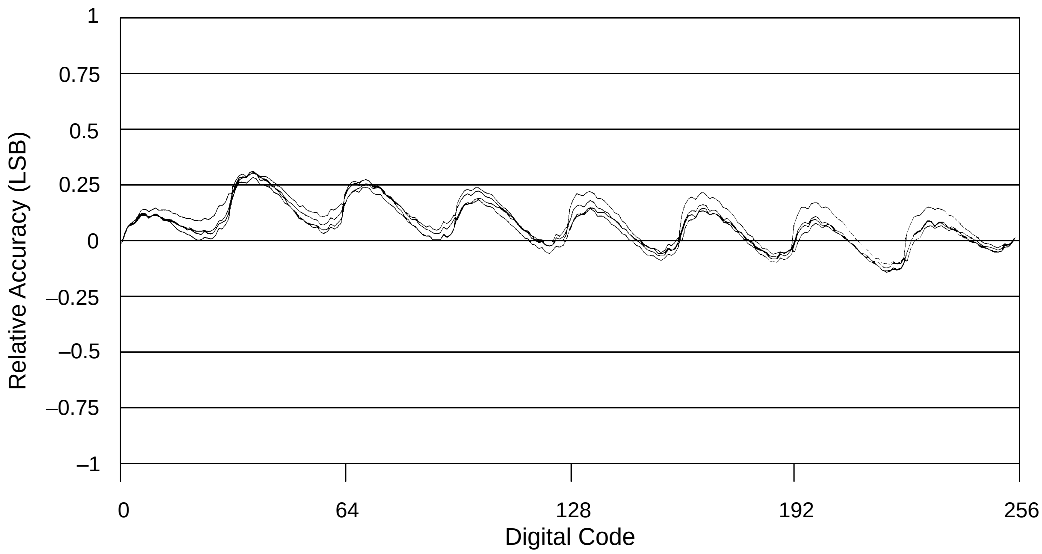
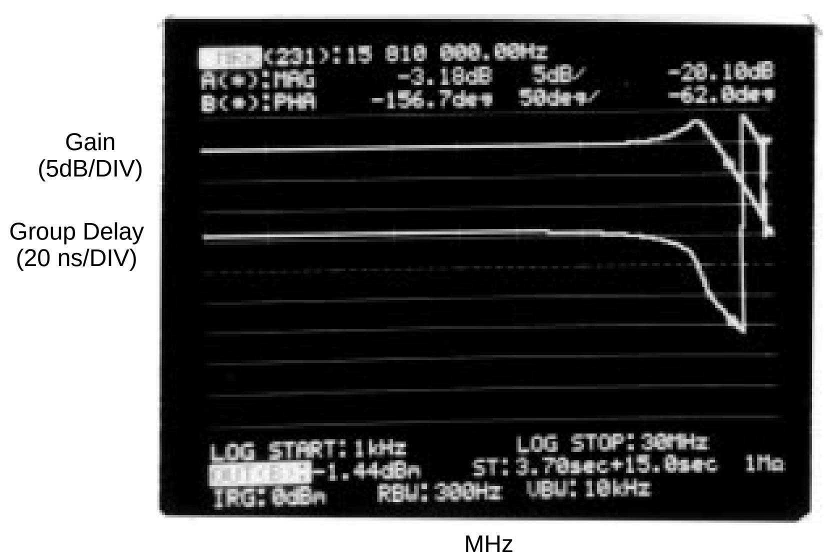


Figure 10. Simplified Diagram
Configuration C

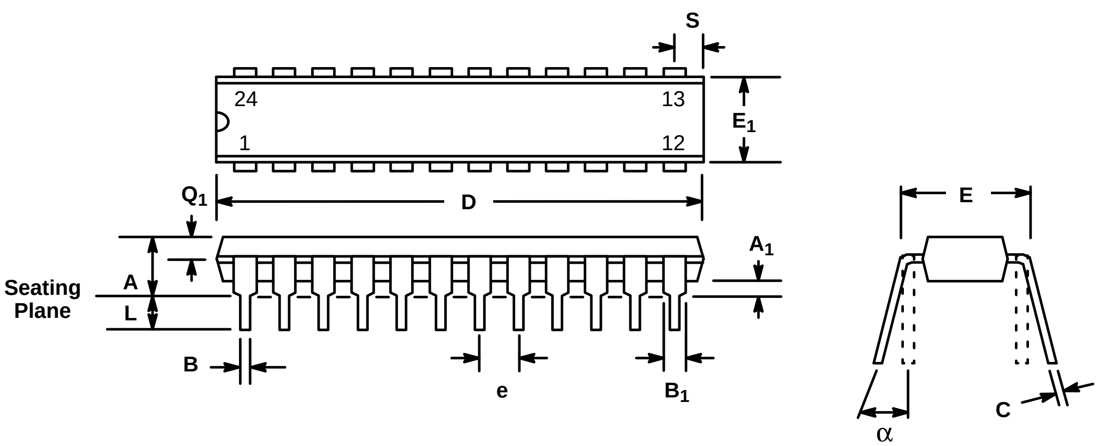


Graph 1. Relative Accuracy vs. Digital Code
DACs 1 to 4



Graph 2. Typical Gain and Group Delay vs. Frequency
(with 5K Resistor Across Output to V_{EE})

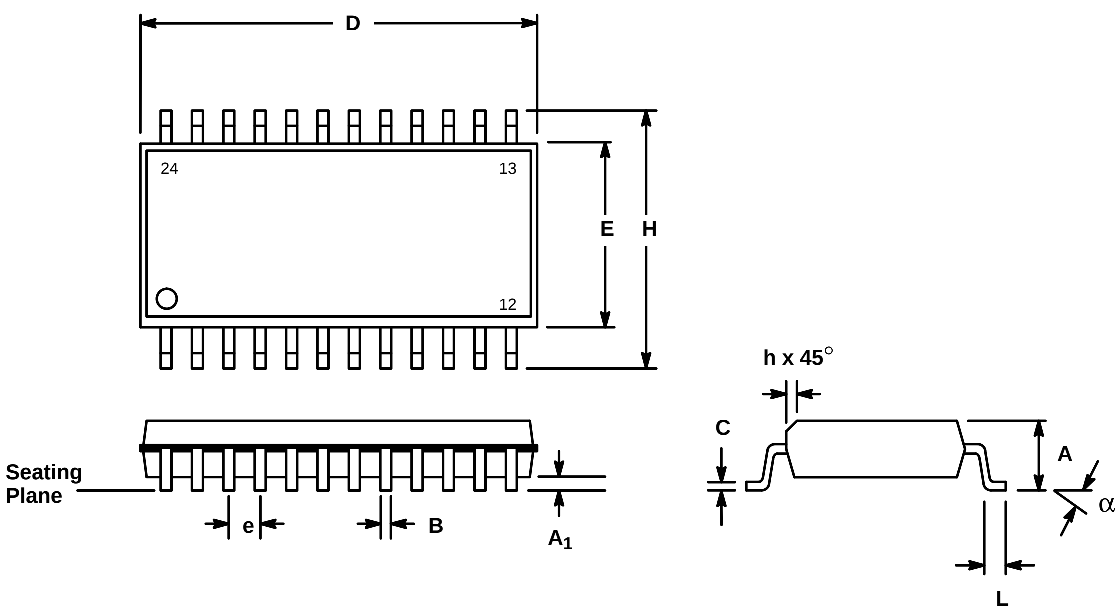
24 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
NN24



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.16	1.280	29.46	32.51
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.028	0.098	0.711	2.49

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

24 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S24



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.097	0.104	2.464	2.642
A1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.483
C	0.0091	0.0125	0.231	0.318
D	0.602	0.612	15.29	15.54
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

Notes

NOTICE

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