MYSON TECHNOLOGY

MTV021

Enhanced Super On-Screen Display

FEATURES

- Horizontal SYNC input up to 130 KHz.
- On-chip PLL circuitry up to 96 MHz.
- Programmable horizontal resolutions up to 1524 dots per display row.
- Full-screen display consists of 15 (rows) by 30 (columns) characters.
- 12 x 18 dot matrices per character.
- Total of 272 characters and graphic fonts, including 256 standard and 16 multi-color mask ROM fonts.
- 8 color-selectable maximum per display character.
- 7 color-selectable maximum for character background.
- Double character height and/or width control.
- Programmable positioning for display screen center.
- Bordering, shadowing and blinking effect.
- Programmable character height (18 to 71 lines) control.
- Row to row spacing register to manipulate the constant display height.
- 4 programmable background windows with multi-level operation and shadowing on window effect.
- Software clears bit for full-screen erasing.
- Half tone and fast blanking output.
- Fade-in/fade-out effect.
- 8-channel/8-bit PWM D/A converter output.
- Compatible with SPI bus or I^2C interface with slave address 7AH (slave address is mask option).
- 16-pin, 20-pin or 24-pin PDIP package.

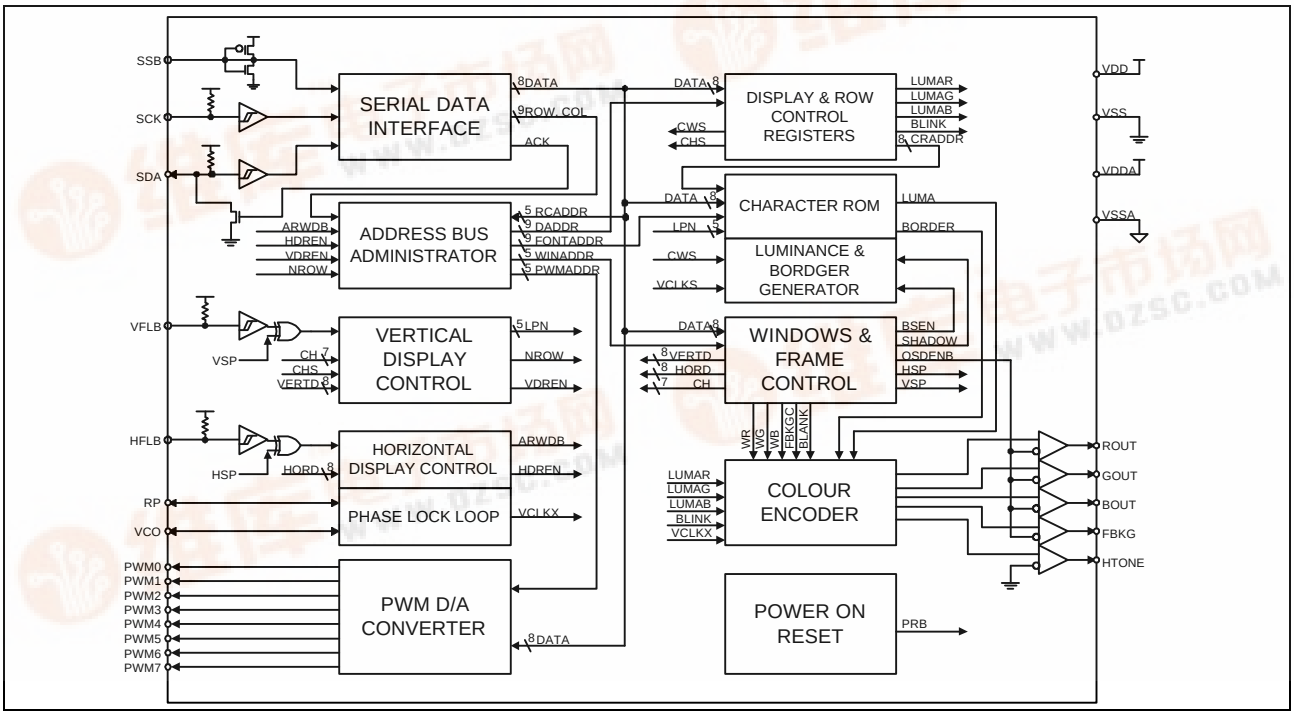
GENERAL DESCRIPTION

MTV021 is designed for monitor applications to display built-in characters or fonts onto monitor screens. The display operation occurs by transferring data and control information from the micro-controller to RAM through a serial data interface. It can execute full-screen display automatically, as well as specific functions such as character background color, bordering, shadowing, blinking, double height and width, font by font color control, frame positioning, frame size control by character height and row-to-row spacing, horizontal display resolution, full-screen erasing, fade-in/fade-out effect, windowing effect and shadowing on window.

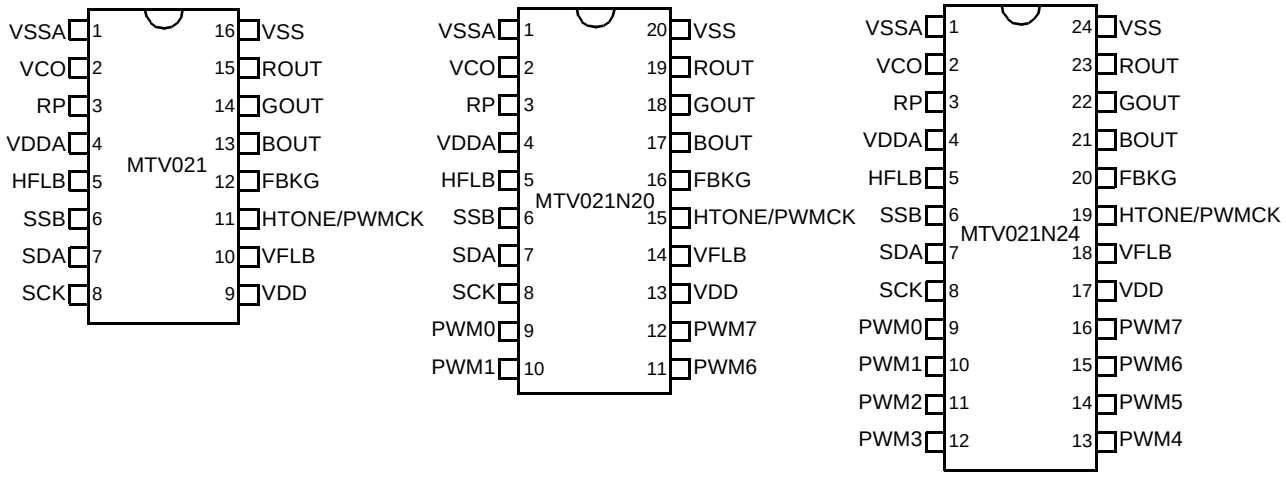
MTV021 provides 256 standard and 16 multi-color characters and graphic fonts for more efficacious applications. The full OSD menu is formed by 15 rows x 30 columns, which can be positioned anywhere on the monitor screen by changing vertical or horizontal delay.

Moreover, MTV021 also provides 8 PWM DAC channels with 8-bit resolution and a PWM clock output for external digital-to-analog control.

BLOCK DIAGRAM



1.0 PIN CONNECTION



2.0 PIN DESCRIPTIONS

Name	I/O	Pin No.			Descriptions
		N16	N20	N24	
VSSA	-	1	1	1	**Analog ground.** This ground pin is used to internal analog circuitry.
VCO	I/O	2	2	2	**Voltage Control Oscillator.** This pin is used to control the internal oscillator frequency by DC voltage input from external low pass filter.
RP	I/O	3	3	3	**Bias Resistor.** The bias resistor is used to regulate the appropriate bias current for internal oscillator to resonate at specific dot frequency.
VDDA	-	4	4	4	**Analog power supply.** Positive 5 V DC supply for internal analog circuitry. And a 0.1uF decoupling capacitor should be connected across to VDDA and VSSA.
HFLB	I	5	5	5	**Horizontal input.** This pin is used to input the horizontal synchronizing signal. It is a leading edge triggered and has an internal pull-up resistor.
SSB	I	6	6	6	**Serial interface enable.** It is used to enable the serial data and is also used to select the operation of I²C or SPI bus. If this pin is left floating, I²C bus is enabled, otherwise the SPI bus is enabled.
SDA	I	7	7	7	**Serial data input.** The external data transfer through this pin to internal display registers and control registers. It has an internal pull-up resistor.
SCK	I	8	8	8	**Serial clock input.** The clock-input pin is used to synchronize the data transfer. It has an internal pull-up resistor.
PWM0	O	-	9	9	**Open-Drain PWM D/A converter 0.** The output pulse width is programmable by the register of Row 15, Column 23.
PWM1	O	-	10	10	**Open-Drain PWM D/A converter 1.** The output pulse width is programmable by the register of Row 15, Column 24.
PWM2	O	-	-	11	**Open-Drain PWM D/A converter 2.** The output pulse width is programmable by the register of Row 15, Column 25.
PWM3	O	-	-	12	**Open-Drain PWM D/A converter 3.** The output pulse width is programmable by the register of Row 15, Column 26.

Name	I/O	Pin No.			Descriptions
		N16	N20	N24	
PWM4	O	-	-	13	**Open-Drain PWM D/A converter 4.** The output pulse width is programmable by the register of Row 15, Column 27.
PWM5	O	-	-	14	**Open-Drain PWM D/A converter 5.** The output pulse width is programmable by the register of Row 15, Column 28.
PWM6	O	-	11	15	**Open-Drain PWM D/A converter 6.** The output pulse width is programmable by the register of Row 15, Column 29.
PWM7	O	-	12	16	**Open-Drain PWM D/A converter 7.** The output pulse width is programmable by the register of Row 15, Column 30.
VDD	-	9	13	17	**Digital power supply.** Positive 5 V DC supply for internal digital circuitry and a 0.1uF decoupling capacitor should be connected across to VDD and VSS.
VFLB	I	10	14	18	**Vertical input.** This pin is used to input the vertical synchronizing signal. It is leading triggered and has an internal pull-up resistor.
HTONE / PWMCK	O	11	15	19	**Half tone output / PWM clock output.** This is a multiplexed pin selected by PWMCK bit. This pin can be a PWM clock or used to attenuate R, G, B gain of VGA for the transparent windowing effect.
FBKG	O	12	16	20	**Fast Blanking output.** It is used to cut off external R, G, B signals of VGA while this chip is displaying characters or windows.
BOUT	O	13	17	21	**Blue color output.** It is a blue color video signal output.
GOUT	O	14	18	22	**Green color output.** It is a green color video signal output.
ROUT	O	15	19	23	**Red color output.** It is a red color video signal output.
VSS	-	16	20	24	**Digital ground.** This ground pin is used to internal digital circuitry.

3.0 FUNCTIONAL DESCRIPTIONS

3.1 SERIAL DATA INTERFACE

The serial data interface receives data transmitted from an external controller. And there are 2 types of bus can be accessed through the serial data interface, one is SPI bus and other is I^2C bus.

3.1.1 SPI bus

While SSB pin is pulled to "high" or "low" level, the SPI bus operation is selected. And a valid transmission should be starting from pulling SSB to "low" level, enabling MTV021 to receiving mode, and retain "low" level until the last cycle for a complete data packet transfer. The protocol is shown in Figure 1.

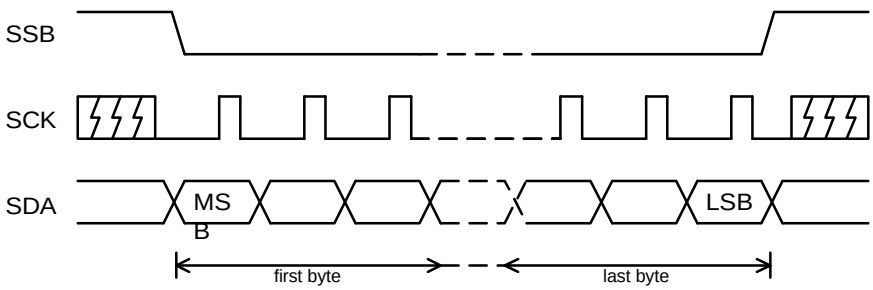


FIGURE 1. Data Transmission Protocol (SPI)

There are three transmission formats shown as below:
Format (a) R - C - D → R - C - D → R - C - D
Format (b) R - C - D → C - D → C - D → C - D
Format (c) R - C - D → D → D → D → D → D
Where R=Row address, C=Column address, D=Display data

3.1.2 I²C bus

I²C bus operation is only selected when SSB pin is left floating. And a valid transmission should be starting from writing the slave address 7AH, which is mask option, to MTV021. The protocol is shown in Figure 2.

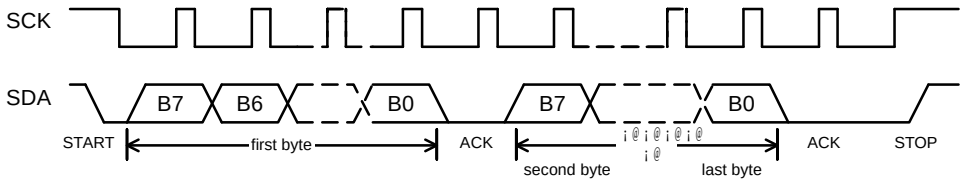


FIGURE 2. Data Transmission Protocol (I²C)

There are three transmission formats shown as below:
Format (a) S - R - C - D → R - C - D → R - C - D
Format (b) S - R - C - D → C - D → C - D → C - D
Format (c) S - R - C - D → D → D → D → D → D
Where S=Slave address, R=Row address, C=Column address, D=Display data

Each arbitrary length of data packet consists of 3 portions viz, Row address (R), Column address (C), and Display data (D). Format (a) is suitable for updating small amount of data which will be allocated with different row address and column address. Format (b) is recommended for updating data that has same row address but different column address. Massive data updating or full screen data change should use format (c) to increase transmission efficiency. The row and column address will be incremented automatically when the format (c) is applied. Furthermore, the undefined locations in display or fonts RAM should be filled with dummy data.

TABLE 1. The configuration of transmission formats.

	Address	b7	b6	b5	b4	b3	b2	b1	b0	Format
Address Bytes of Display Reg.	Row	1	0	0	x	R3	R2	R1	R0	a,b,c
	$Column_{ab}$	0	0	x	C4	C3	C2	C1	C0	a,b
	$Column_{c}$	0	1	x	C4	C3	C2	C1	C0	c
Attribute Bytes of Display Reg.	Row	1	0	1	x	R3	R2	R1	R0	a,b,c
	$Column_{ab}$	0	0	x	C4	C3	C2	C1	C0	a,b
	$Column_{c}$	0	1	x	C4	C3	C2	C1	C0	c

There are 2 types of data should be accessed through the serial data interface, one is ADDRESS bytes of display registers, and other is ATTRIBUTE bytes of display registers, the protocol are same for all except the bit5 of row address. The MSB(b7) is used to distinguish row and column addresses when transferring data from external controller. The bit6 of column address is used to differentiate the column address for format (a), (b) and format (c) respectively. Bit5 of row address for display register is used to distinguish ADDRESS byte when it is set to "0" and ATTRIBUTE byte when it is set to "1". See Table 1 on page 4.

The data transmission is permitted to change from format (a) to format (b) and (c), or from format (b) to format (a), but not from format (c) back to format (a) and (b). The alternation between transmission formats is configured as the state diagram shown in Figure 3.

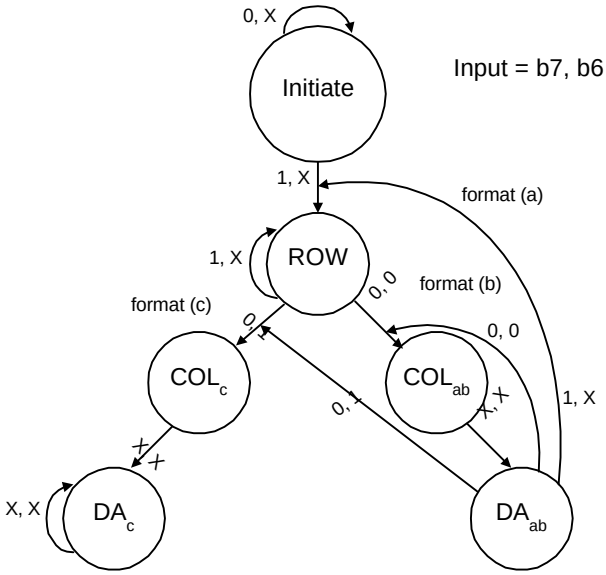


FIGURE 3. Transmission State Diagram

3.2 Address bus administrator

The administrator manages bus address arbitration of internal registers or user fonts RAM during external data write in. The external data write through serial data interface to registers must be synchronized by internal display timing. In addition, the administrator also provides automatic increment to address bus when external write using format (c).

3.3 Vertical display control

The vertical display control can generates different vertical display sizes for most display standards in current monitors. The vertical display size is calculated with the information of double character height bit(CHS), vertical display height control register(CH6-CH0).The algorithm of repeating character line display are shown as Table 2 and Table 3. The programmable vertical size range is 270 lines to maximum 2130 lines.

The vertical display center for full screen display could be figured out according to the information of vertical starting position register (VERTD) and VFLB input. The vertical delay starting from the leading edge of VFLB, is calculated with the following equation:

Vertical delay time = (VERTD * 4 + 1) * H Where H = one horizontal line display time

TABLE 2. Repeat line weight of character

CH6 - CH0	Repeat Line Weight
CH6,CH5=11	+18*3
CH6,CH5=10	+18*2
CH6,CH5=0x	+18
CH4=1	+16

TABLE 2. Repeat line weight of character

CH6 - CH0	Repeat Line Weight
CH3=1	+8
CH2=1	+4
CH1=1	+2
CH0=1	+1

TABLE 3. Repeat line number of character

Repeat Line Weight	Repeat Line #																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
+1	-	-	-	-	-	-	-	-	v	-	-	-	-	-	-	-	-	-
+2	-	-	-	-	v	-	-	-	-	-	-	-	v	-	-	-	-	-
+4	-	-	v	-	-	-	v	-	-	-	v	-	-	-	v	-	-	-
+8	-	v	-	v	-	v	-	v	-	v	-	v	-	v	-	v	-	-
+16	-	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	-
+17	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	-
+18	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v

Note:" v " means the nth line in the character would be repeated once, while " - " means the nth line in the character would not be repeated.

3.4 Horizontal display control

The horizontal display control is used to generate control timing for horizontal display based on double character width bit (CWS), horizontal positioning register (HORD), horizontal resolution register (HORR), and HFLB input. A horizontal display line consists of (HORR*12) dots which include 360 dots for 30 display characters and the remaining dots for blank region. The horizontal delay starting from HFLB leading edge is calculated with the following equation,

Horizontal delay time = (HORD * 6 + 49) * P - phase error detection pulse width
Where P = One pixel display time = One horizontal line display time / (HORR*12)

3.5 Phase lock loop (PLL)

On-chip PLL generates system clock timing (VCLK) by tracking the input HFLB and horizontal resolution register (HORR). The frequency of VCLK is determined by the following equation:

VCLK Freq = HFLB Freq * HORR * 12

The VCLK frequency ranges from 6MHz to 96MHz selected by (VCO1, VCO0). In addition, when HFLB input is not present to MTV021, the PLL will generate a specific system clock, approximately 2.5MHz, by a built-in oscillator to ensure data integrity.

3.6 Display & Row control registers

The internal RAM contains display and row control registers. The display registers have 450 locations which are allocated between (row 0, column 0) to (row 14, column 29), as shown in Figure 4. Each display register has its corresponding character address on ADDRESS byte, its corresponding background color, 1 blink bit and its corresponding color bits on ATTRIBUTE bytes. The row control register is allocated at column 30 for

row 0 to row 14, it is used to set character size to each respective row. If double width character is chosen, only even column characters could be displayed on screen and the odd column characters will be hidden.

ROW #	COLUMN #		
	0 1 ... 28 29	30	31
0 1 13 14	DISPLAY REGISTERS	ROW CTRL REG	R E S E R V E D

ROW 15	COLUMN#					
	0 2	3 5	6 8	9 11	12 22	23 30
	WINDOW1	WINDOW2	WINDOW3	WINDOW4	FRAME CRTL REG	PWM D/A CRTL REG

FIGURE 4. Memory Map

ADDRESS BYTE

b7	b6	b5	b4	b3	b2	b1	b0
CRADDR							
MSB							LSB

CRADDR - Define ROM character address.

ATTRIBUTE BYTE

b7	b6	b5	b4	b3	b2	b1	b0
-	BGR	BGG	BGB	BLINK	R	G	B

BGR, BGG, BGB - These three bits define the color of the background for its relative address character. If all three bits are clear, no background will be shown(transparent). Therefore, total 7 background color can be selected.

BLINK - Enable blinking effect while this bit is set to " 1 ". And the blinking is alternate per 32 vertical frames.

R, G, B - These three bits are used to specify its relative address character color.

1. Row Control Registers, (Row 0 - 14)

COLN 30	b7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	-	-	CHS	CWS

CHS - Define double height character to the respective row.

CWS - Define double width character to the respective row.

3.7 Character ROM

MTV021 character ROM contains 272 built-in characters and symbols including 256 standard fonts and 16 multi-color fonts. The 256 standard fonts are located from address 0 to 255. And the 16 multi-color fonts are located from address 240 to 255 while CFONT bit is set to "1". Each character and symbol consists of 12x18 dots matrix. The detail pattern structures for each character and symbols are shown in "CHARACTERS AND SYMBOLS PATTERN" on page 17.

3.8 Multi-Color Font

The color fonts comprises three different R, G, B fonts. When the code of color font is accessed, the separate R/G/B dot pattern is output to corresponding R/G/B output. See Figure for the sample displayed color font. Note: No black color can defined in color font, black window underline the color font can make the dots become black in color. The detail pattern structures for each character and symbols are shown in "CHARACTERS AND SYMBOLS PATTERN" on page 17.

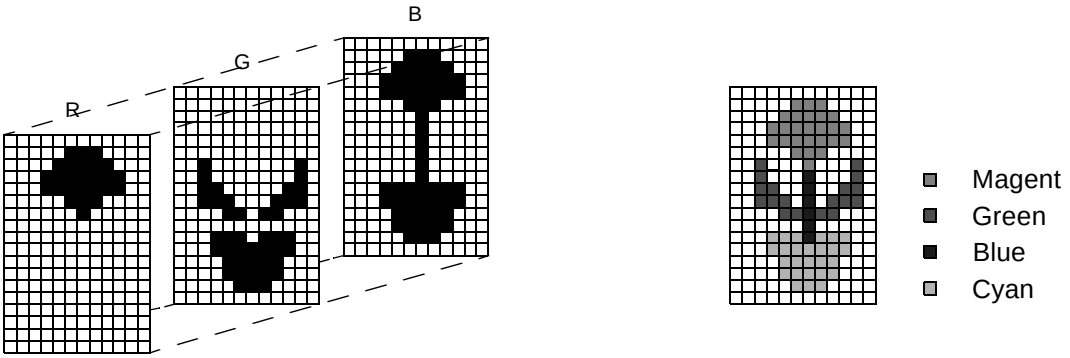


FIGURE 5. Example of Multi-Color Font

TABLE 4. The Multi-Color Font Color Selection

	R	G	B
Background Color	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Magent	1	0	1
Yellow	1	1	0
White	1	1	1

3.9 Luminance & border generator

There are 2 shift registers included in the design which can shift out of luminance and border dots to color encoder. The bordering and shadowing feature is configured in this block. For bordering effect, the character will be enveloped with blackedge on four sides. For shadowing effect, the character is enveloped with blackedge for right and bottom sides only.

3.10 Window and frame control

The display frame position is completely controlled by the contents of VERTD and HORD. The window size and position control are specified in column 0 to 11 on row 15 of memory map, as shown in Figure 4. Window 1 has the highest priority, and window 4 is the least, when two windows are overlapping. More detailed information is described as follows:

1. Window control registers,
ROW 15

	b7	b6	b5	b4	b3	b2	b1	b0
Column 0,3,6,OR 9	ROW START ADDR MSB LSB				ROW END ADDR MSB LSB			

	b7	b6	b5	b4	b3	b2	b1	b0
Column 1,4,7,OR 10	COL START ADDR MSB LSB					WEN	-	WSHD

	b7	b6	b5	b4	b3	b2	b1	b0
Column 2,5,8,OR 11	COL END ADDR MSB LSB					R	G	B

START(END) ADDR - These addresses are used to specify the window size. It should be noted that when the start address is greater than the end address, the window will be disabled.

WEN - Enable the window display.

WSHD - Enable shadowing on the window.

R, G, B - Specify the color of the relative background window.

2. Frame control registers,
ROW 15

	b7	b6	b5	b4	b3	b2	b1	b0
Column 12	VERTD MSB LSB							

VERTD - Specify the starting position for vertical display. The total steps are 256, and the increment of each step is 4 Horizontal display lines. The initial value is 4 after power up.

	b7	b6	b5	b4	b3	b2	b1	b0
Column 13	HORD MSB LSB							

HORD - Define the starting position for horizontal display. The total steps are 256, and the increment of each step is 6 dots. The initial value is 15 after power up.

	b7	b6	b5	b4	b3	b2	b1	b0
Column 14	-	CH6	CH5	CH4	CH3	CH2	CH1	CH0

CH6-CH0 - Define the character vertical height, the height is programmable from 18 to 71 lines. The character vertical height is at least 18 lines if the contents of CH6-CH0 is less than 18. For example, when the contents is " 2 ", the character vertical height is regarded as equal to 20 lines. And if the con-

tents of CH4-CH0 is greater than or equal to 18, it will be regarded as equal to 17. See Table 2 and Table 3 for detail description of this operation.

	b7	b6	b5	b4	b3	b2	b1	b0
Column 15	-	HORR						
		MSB						LSB

HORR - Specify the resolution of a horizontal display line, and the increment of each step is 12 dots. That is, the pixels' number per H line equal to HORR*12. It is recommended that HORR should be greater than or equal to 36 and smaller than 96M / (Hfreq*12). The initial value is 40 after power up.

	b7	b6	b5	b4	b3	b2	b1	b0
Column 16	-	-	-	RSPACE				
				MSB				LSB

RSPACE - Define the row to row spacing in unit of horizontal line. That is, extra RSPACE horizontal lines will be appended below each display row, and the maximum space is 31 lines. The initial value is 0 after power up.

	b7	b6	b5	b4	b3	b2	b1	b0
Column 17	OSDEN	BSEN	SHADOW	FAN	BLANK	WENCLR	RAMCLR	FBKGC

OSDEN - Activate the OSD operation when this bit is set to "1". The initial value is 0 after power up.

BSEN - Enable the bordering and shadowing effect.

SHADOW - Activate the shadowing effect if this bit is set, otherwise the bordering is chosen.

FAN - Enable the fade-in/fade-out function when OSD is turned on from off state or vice verca. The function roughly takes about one second to fully display the whole menu or to disappear completely.

BLANK - Force the FBKG pin output to high while this bit is set to "1".

WENCLR - Clear all WEN bits of window control registers when this bit is set to "1". The initial value is 0 after power up.

RAMCLR - Clear all ADDRESS bytes, BGR, BGG, BGB and BLINK bits of display registers when this bit is set to "1". The initial value is 0 after power up.

FBKGC - Define the output configuration for FBKG pin. When it is set to "0", the FBKG outputs during the displaying of characters or windows, otherwise, it outputs only during the displaying of character.

	B7	b6	b5	b4	b3	b2	b1	b0
Column 18	TRIC	FBKGP	PWMCK	SELVCL	HSP	VSP	VCO1	VCO0

TRIC - Define the driving state of output pins ROUT, GOUT, BOUT and FBKG when OSD is disabled. That is, while OSD is disabled, these four pins will drive low if this bit is set to 1, otherwise these four pins are in high impedance state. The initial value is 0 after power up.

FBKGP - Select the polarity of the output pin FBKG

= 1 ⇒Positive polarity FBKG output is selected.

= 0 ⇒Negative polarity FBKG output is selected.

The initial value is 1 after power up.

PWMCK - Select the output options to HTONE/PWMCK pin.
= 0 ⇒ HTONE option is selected.
= 1 ⇒ PWMCK option is selected with 50/50 duty cycle and synchronous with the input HFLB.
The frequency is selected by (VCO1, VCO0) shown as Table 5.
The initial value is 0 after power up.

SELVCL - Enable auto detection for horizontal and vertical syncs input edge distorition to avoid unstable Vsync leading mismatch with Hsync signal while the bit is set to "1". The initial value is 0 after power up.

HSP - = 1 ⇒ Accept positive polarity Hsync input.
= 0 ⇒ Accept negative polarity Hsync input.

VSP - = 1 ⇒ Accept positive polarity Vsync input.
= 0 ⇒ Accept negative polarity Vsync input.

VCO1, VCO0 - Select the appropriate curve partitions of VCO frequency to voltage based on HFLB input and horizontal resolution register (HORR). And there are different curve partitions based on different application resister value on pin 3 (pin RP) as belows:
(i) 12K ohm:
= (0, 0) ⇒ 6MHz < Pixel rate ≤ 12MHz
= (0, 1) ⇒ 12MHz < Pixel rate ≤ 24MHz
= (1, 0) ⇒ 24MHz < Pixel rate ≤ 48MHz
= (1, 1) ⇒ 48MHz < Pixel rate ≤ 96MHz
(ii) 11K ohm:
= (0, 0) ⇒ 6.5MHz < Pixel rate ≤ 13MHz
= (0, 1) ⇒ 13MHz < Pixel rate ≤ 26MHz
= (1, 0) ⇒ 26MHz < Pixel rate ≤ 52MHz
= (1, 1) ⇒ 52MHz < Pixel rate ≤ 96MHz
(iii)10K ohm:
= (0, 0) ⇒ 7MHz < Pixel rate ≤ 14MHz
= (0, 1) ⇒ 14MHz < Pixel rate ≤ 28MHz
= (1, 0) ⇒ 28MHz < Pixel rate ≤ 56MHz
= (1, 1) ⇒ 56MHz < Pixel rate ≤ 96MHz
(iv)9.1K ohm:
= (0, 0) ⇒ 7.5MHz < Pixel rate ≤ 15MHz
= (0, 1) ⇒ 15MHz < Pixel rate ≤ 30MHz
= (1, 0) ⇒ 30MHz < Pixel rate ≤ 60MHz
= (1, 1) ⇒ 60MHz < Pixel rate ≤ 96MHz
(v)8.2K ohm:
= (0, 0) ⇒ 8MHz < Pixel rate ≤ 16MHz
= (0, 1) ⇒ 16MHz < Pixel rate ≤ 32MHz
= (1, 0) ⇒ 32MHz < Pixel rate ≤ 64MHz
= (1, 1) ⇒ 64MHz < Pixel rate ≤ 96MHz
(vi)7.5K ohm:
= (0, 0) ⇒ 8.5MHz < Pixel rate ≤ 17MHz
= (0, 1) ⇒ 17MHz < Pixel rate ≤ 34MHz
= (1, 0) ⇒ 34MHz < Pixel rate ≤ 68MHz
= (1, 1) ⇒ 68MHz < Pixel rate ≤ 96MHz
(vii)under or equal to 6.2K ohm:
= (0, 0) ⇒ 9.5MHz < Pixel rate ≤ 19MHz
= (0, 1) ⇒ 19MHz < Pixel rate ≤ 38MHz
= (1, 0) ⇒ 38MHz < Pixel rate ≤ 76MHz

= (1, 1) ⇒ 76MHz < Pixel rate ≤ 96MHz

where Pixel rate = VCLK Freq = HFLB Freq * HORR * 12
The initial value is (0, 0) after power up.

Notes :

1. That is, if HORR is specified and RP resister = 12K ohm, then (VCO1, VCO0)
   = (0, 0) if 6000/(HORR * 12) < HFLB Freq (KHz) ≤ 12000/(HORR * 12)
   = (0, 1) if 12000/(HORR * 12) < HFLB Freq (KHZ) ≤ 24000/(HORR * 12)
   = (1, 0) if 24000/(HORR * 12) < HFLB Freq (KHZ) ≤ 48000/(HORR * 12)
   = (1, 1) if 48000/(HORR * 12) < HFLB Freq (KHZ) ≤ 96000/(HORR * 12)
2. It is necessary to wait for the PLL to become stable while (i) the HORR register is changed; (ii) the (VCO1, VCO0) bits is changed; (iii) the horizontal signal (HFLB) is changed.
3. When PLL is unstable, don't write data in any address except Column 15,17,18 of Row 15. If data is written in any other address, a malfunction may occur.

TABLE 5. PWMCK Frequency and PWMDA sampling rate

(VCO1, VCO0)	PWMCK Freq (6M ~ 12MHz)	PWMDA sampling rate (23K ~ 47KHz)
(0, 0)	HFLB Freq * HORR * 12	HFLB Freq * HORR * 12 / 256
(0, 1)	HFLB Freq * HORR * 6	HFLB Freq * HORR * 6 / 256
(1, 0)	HFLB Freq * HORR * 3	HFLB Freq * HORR * 3 / 256
(1 ,1)	HFLB Freq * HORR * 3 / 2	HFLB Freq * HORR * 3 / 512

Column 19	B7	b6	b5	b4	b3	b2	b1	b0
	-	WSR	WSG	WSB	-	CSR	CSG	CSB

WSR, WSG, WSB - Define the color of shadowing on windows. The initial value is (0, 0, 0) after power up.

CSR, CSG, CSB - Define the color of bordering or shadowing on characters. The initial value is (0, 0, 0) after power up.

Column 20	B7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	-	-	-	CFONT

CFONT - Enable 16 multi-color fonts.
= 0 ⇒ Character address 240 to 255 are connected to standard ROM fonts.
= 1 ⇒ Character address 240 to 255 are connected to 16 multi-color ROM fonts.
The initial value is 0 after power up.

Column 21	B7	b6	b5	b4	b3	b2	b1	b0
	WW41	WW40	WW31	WW30	WW21	WW20	WW11	WW10

WW41, WW40 - Determines the shadow width of the window 4 when WSHD bit of th window 4 is enabled. Please refer to the Table 6 for more details.

TABLE 6. Shadow Width Setting

(WW41, WW40)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Shadow Width (unit in Pixel)	2	4	6	8

WW31, WW30 - Determines the shadow width of the window 3 when WSHD bit of th window 3 is enabled.

WW21, WW20 - Determines the shadow width of the window 2 when WSHD bit of th window 2 is enabled.

WW11, WW10 - Determines the shadow width of the window 1 when WSHD bit of th window 1 is enabled.

Column 22	B7	b6	b5	b4	b3	b2	b1	b0
	WH41	WH40	WH31	WH30	WH21	WH20	WH11	WH10

WH41, WH40 - Determines the shadow height of the window 4 when WSHD bit of th window 4 is enabled. Please refer to the Table 7 for more details.

TABLE 7. Shadow Height Setting

(WH41, WH40)	**(0, 0)**	**(0, 1)**	**(1, 0)**	**(1, 1)**
Shadow Height (unit in Line)	2	4	6	8

WH31, WH30 - Determines the shadow height of the window 3 when WSHD bit of th window 3 is enabled.
WH21, WH20 - Determines the shadow height of the window 2 when WSHD bit of th window 2 is enabled.
WH11, WH10 - Determines the shadow height of the window 1 when WSHD bit of th window 1 is enabled.

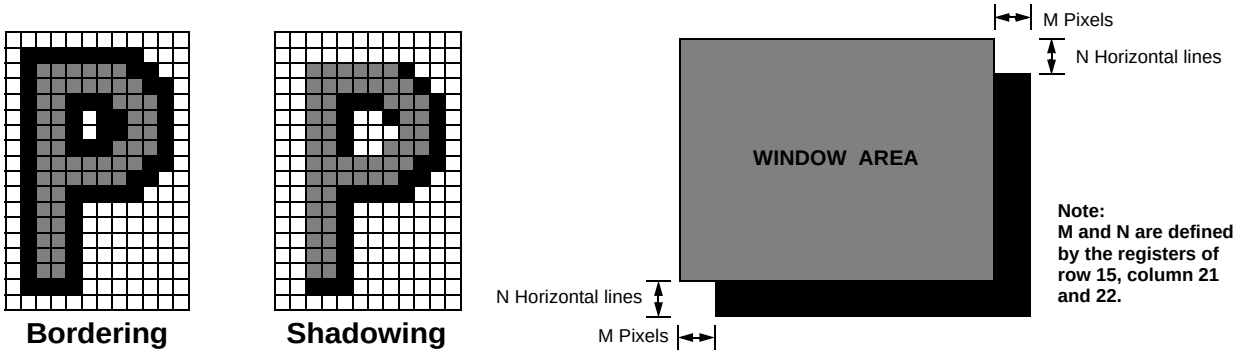


FIGURE 6. Character Bordering and Shadowing and Shadowing on Window

3.11 Color encoder

The decoder generates the video output to ROUT, GOUT and BOUT by integrating window color, border blackedge, luminance output and color selection output (R, G, B) to form the desired video outputs.

3.12 PWM D/A converter

There are 8 open-drain PWM D/A outputs (PWM0 to PWM7). These PWM D/A converter outputs pulse width are programmable by writing data to Column 19 to 26 registers of Row 15 with 8-bit resolution to control the pulse width duration from 0/256 to 255/256. And the sampling rate is selected by (VCO1, VCO0) shown as table 5. In applications, all open-drain output pins should be pulled-up by external resistors to supply voltage (5V to 9V) for desired output range.

	b7	b6	b5	b4	b3	b2	b1	b0
Column 23 | Column 30	PWMDA0 | PWMDA7							
	MSB							LSB

PWMDA0 - PWMDA7 - Define the output pulse width of pin PWM0 to PWM7.

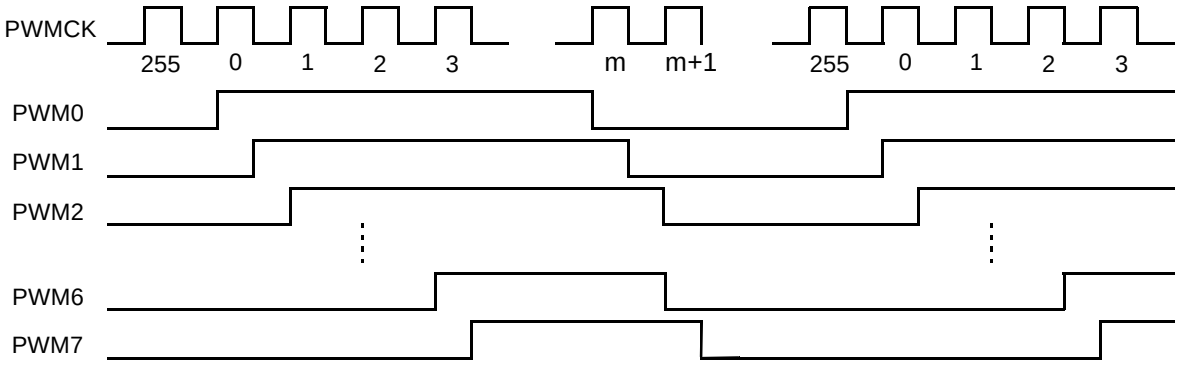


FIGURE 7. 8 Channel PWM Output Rising Edges Are Separated by Half PWMCK

	B7	b6	b5	b4	b3	b2	b1	b0
Column 31	0	0	0	0	0	0	0	0

Note: The byte is reserved for the testing. Write " Ax " will enter into test mode and write " 00 " in normal operation.

4.0 ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage(VDD,VDDA)	-0.3 to +7 V
Voltage with respect to Ground	-0.3 to VDD+0.3 V
Storage Temperature	-65 to +150 ^{o}C
Ambient Operating Temperature	0 to +70 ^{o}C

5.0 OPERATING CONDITIONS

DC Supply Voltage(VDD,VDDA)	+4.75 to +5.25 V
Operating Temperature	0 to +70 ^{o}C

6.0 ELECTRICAL CHARACTERISTICS (Under Operating Conditions)

Symbol	Parameter	Conditions (Notes)	Min.	Max.	Units
V_{IH}	Input High Voltage	-	0.7 * VDD	VDD+0.3	V
V_{IL}	Input Low Voltage	-	VSS-0.3	0.3 * VDD (0.2 * VDD for SSB pin)	V

Symbol	Parameter	Conditions (Notes)	Min.	Max.	Units
V_{OH}	Output High Voltage	$I_{OH} \geq$ -5 mA	VDD-0.8	-	V
V_{OL}	Output Low Voltage	$I_{OL} \leq$ 5 mA	-	0.5	V
V_{ODH}	Open Drain Output High Voltage	- (For all OD pins, and pulled up by external 5 to 9V power supply)	5	9	V
V_{ODL}	Open Drain Output Low Voltage	5 mA $\geq I_{DOL}$ (For all OD pins)	-	0.5	V
I_{CC}	Operating Current	Pixel rate=96MHz I_{load} = 0uA	-	25	mA
I_{SB}	Standby Current	Vin = VDD, I_{load} = 0uA	-	12	mA

7.0 SWITCHING CHARACTERISTIC (Under Operating Conditions)

Symbol	Parameter	Min.	Typ.	Max.	Units
f_{HFLB}	HFLB input frequency	15	-	130	KHz
T_r	Output rise time	-	-	5	ns
T_f	Output fall time	-	-	5	ns
t_{BCSU}	SSB to SCK set up time	200	-	-	ns
t_{BCH}	SSB to SCK hold time	100	-	-	ns
t_{DCSU}	SDA to SCK set up time	200	-	-	ns
t_{DCH}	SDA to SCK hold time	100	-	-	ns
t_{SCKH}	SCK high time	500	-	-	ns
t_{SCKL}	SCK low time	500	-	-	ns
$t_{SU:STA}$	START condition setup time	500	-	-	ns
$t_{HD:STA}$	START condition hold time	500	-	-	ns
$t_{SU:STO}$	STOP condition setup time	500	-	-	ns
$t_{HD:STO}$	STOP condition hold time	500	-	-	ns

8.0 TIMING DIAGRAMS

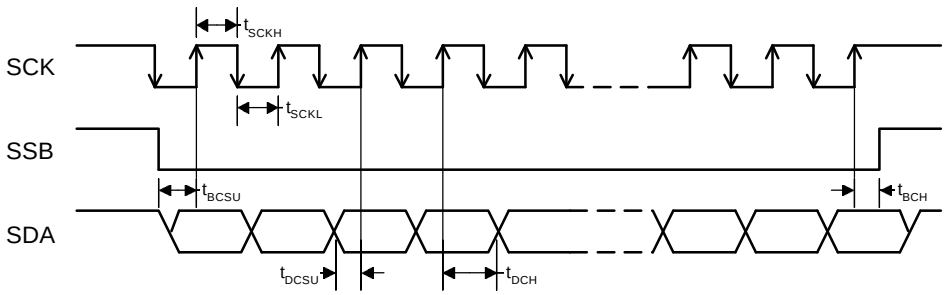


FIGURE 8. Data interface timing(SPI)

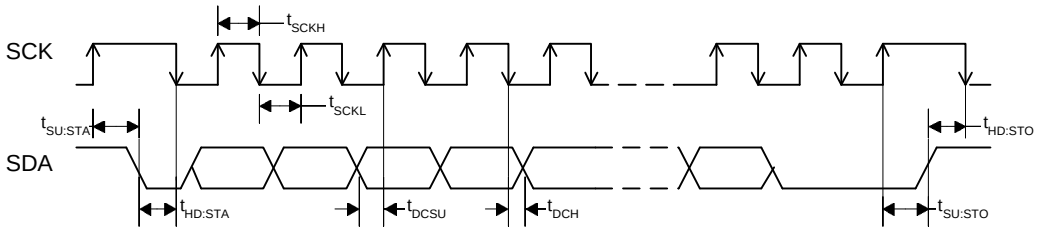
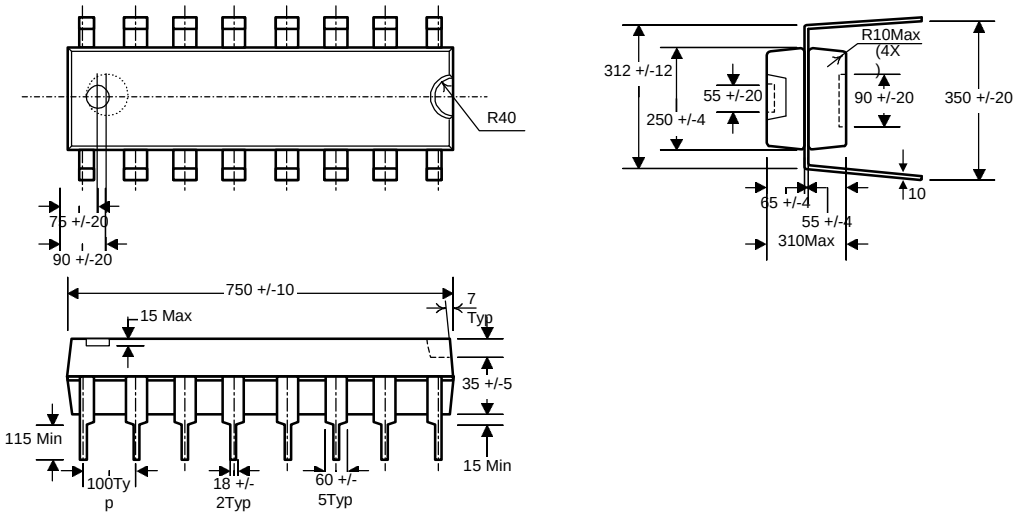


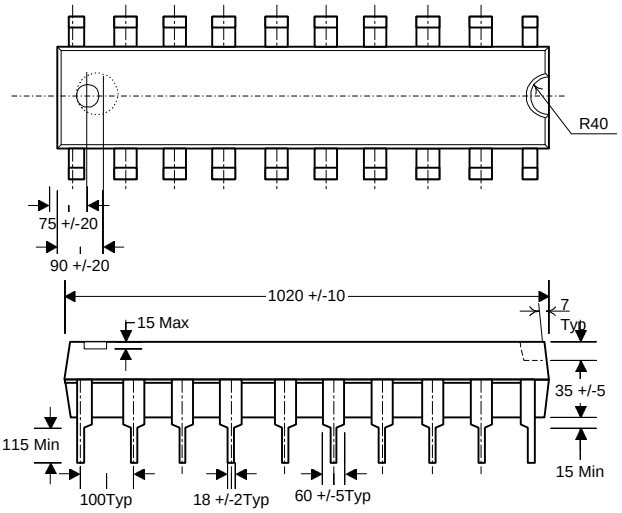
FIGURE 9. Data interface timing(I²C)

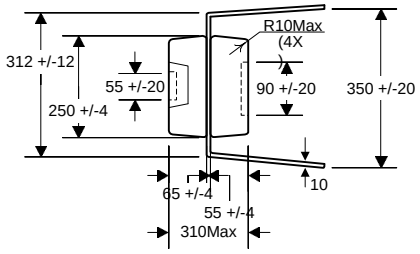
9.0 PACKAGE DIMENSION

9.1 16 Pin 300mil

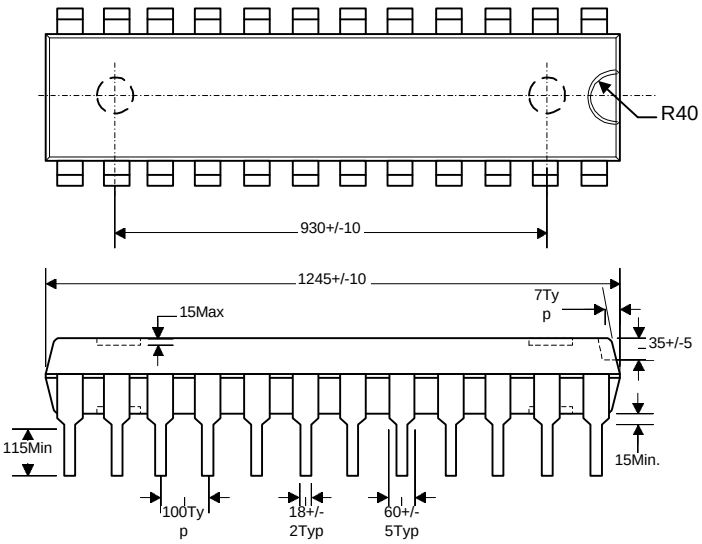


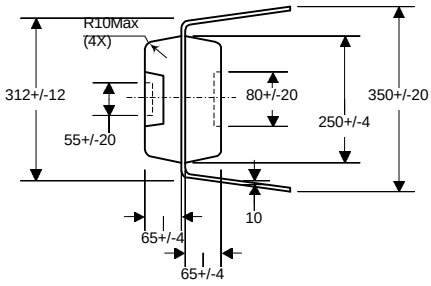
9.2 20 Pin 300mil





9.3 24 Pin 300mil





10.0 CHARACTERS AND SYMBOLS PATTERN

Please see the attachment.

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