# MX98728EC

## GMAC
## SINGLE CHIP 10/100 FAST ETHERNET CONTROLLER FOR GENERIC APPLICATION

### 1.0 Features

- 32 bits general purpose asynchronous bus architecture up to 33Mhz for easy system application
- Single chip solution integrating 10/100 TP transceiver to reduce overall cost
- Optional MII interface for external tranceiver.
- Fully compliant with the IEEE 802.3u spec.
- Supports 32/16 bits x1, x2, x4 burst read transfers for the receive packet buffer
- Packet buffer access through an IO mapped port or host DMA for a wide variety of bus applications
- Programmable bus integrity check timer and interrupt assertion scheme
- Supports 16/8 bits packet buffer data width and 32/16 bits host bus data width
- Separated TX and RX FIFOs to support the full duplex mode, independent TX and RX channel
- Rich on-chip registers to support a wide variety of network management functions
- 1.6KB TX FIFO to support maximum network throughput in the full duplex mode
- 16/8 bits SRAM interface of the packet buffer supporting burst DMA for on-chip FIFOs
- Flexible packet buffer partition and addressing space for up to 1MB
- NWAY autonegotiation function to automatically set up network speed and protocol
- 3 loop back modes for system level diagnosis
- Supports 64 bits hash table for multicast addressing, broadcast control.
- Optional EEPROM configuration, supports 1K bits and 4K bits EEPROM interface
- Supports software EEPROM interface for easy upgrade of EEPROM contents
- 5V CMOS in an 160 PQFP package

### 1.1 Introduction

MX98728EC ( GMAC ) is a general purpose single chip 10/100 Fast Ethernet controller. With no glue logic or very little extra logic, it can be used in a variety of system applications through its host bus interface. Single chip solution will help reduce system cost, not only on the IC count but also on the board size. Full NWAY function with 10/100 transceiver will ease the field installation. Simply plug the chip in and it will connect itself with the best protocol available.

A data cache is also used on the host bus to deliver the 32 /16 bits burst read on the host data port up to 4 data transfers in a single cycle. Two hand shake signals to communicate to the host bus interface during the data port transfer are simple and fast for the system integrator. An intelligent built-in SRAM bus arbiter will manage all SRAM access requests from the host bus access, the transmit local DMA and the receive local DMA.

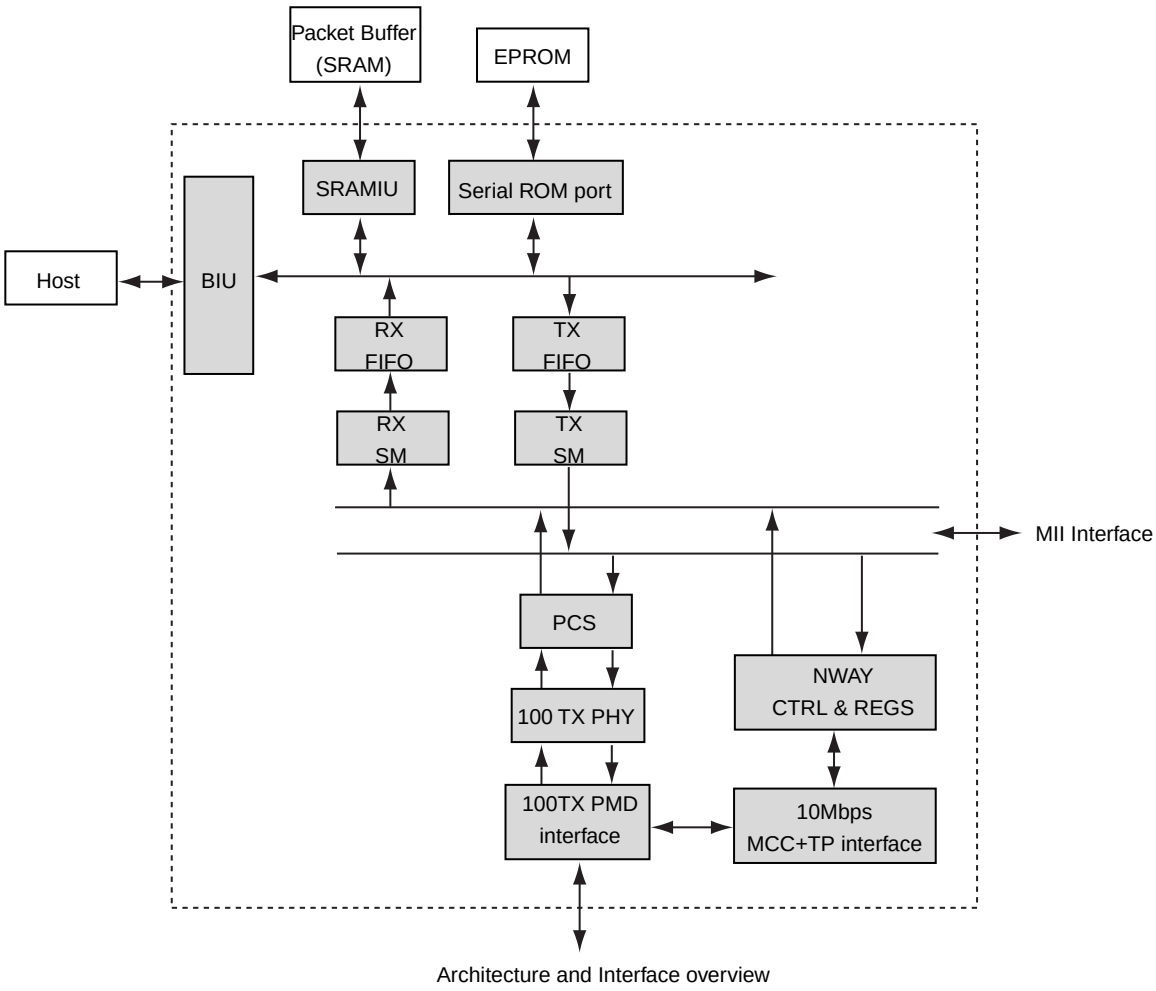
The 16/8 bit SRAM interface with local DMAs help system developers to optimize the performance. The behavior of these local DMAs can be easily adjusted by the optional bits on the chip. (The term "packet buffer" and "packet memory" are used interchangeably in this document).

A programmable receive packet interrupt scheme using a timer (RXINTT) and a packet counter (RXINTC) allows system developers to adjust the interrupt traffic. The receive interrupt assertion timing is also programmable for different system applications. A general purpose host receive packet counter (HRPKTCNT) is also provided to the host for the buffer management purpose.

Bus integrity check feature allows the system to recover from a bus hang or an excessively long bus access. BICT ( Bus integrity check timer ) can be programmed to abort any bus access that runs abnormally long. Based multicast and broadcast frame filtering is supported to minimize the unnecessary network traffic.

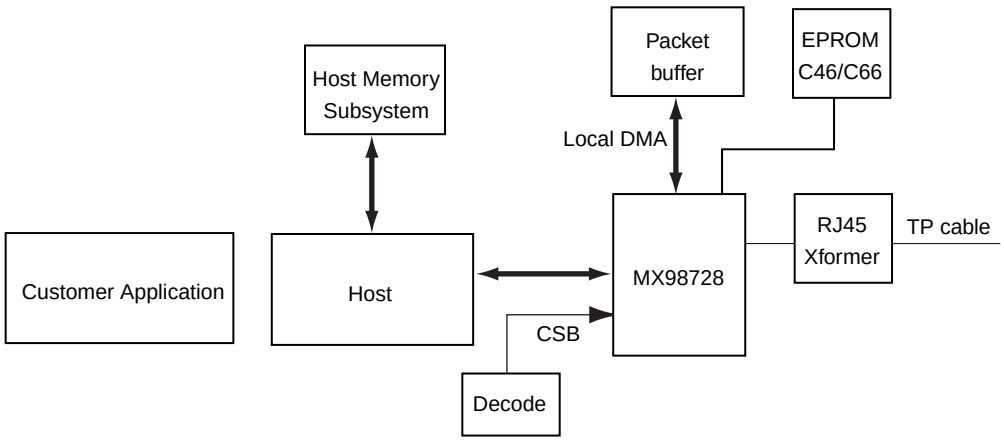
MX98728EC is also equipped with the back-to-back transmit capability which allows the software to fire as many transmit packets as needed in a single command. The receive FIFO also allows the back-to-back reception. Optional EEPROM can be used to store the MAC ID and the other configuration information. All options including MAC ID can be programmed through the host interface.

### 1.2 Internal Block Diagram



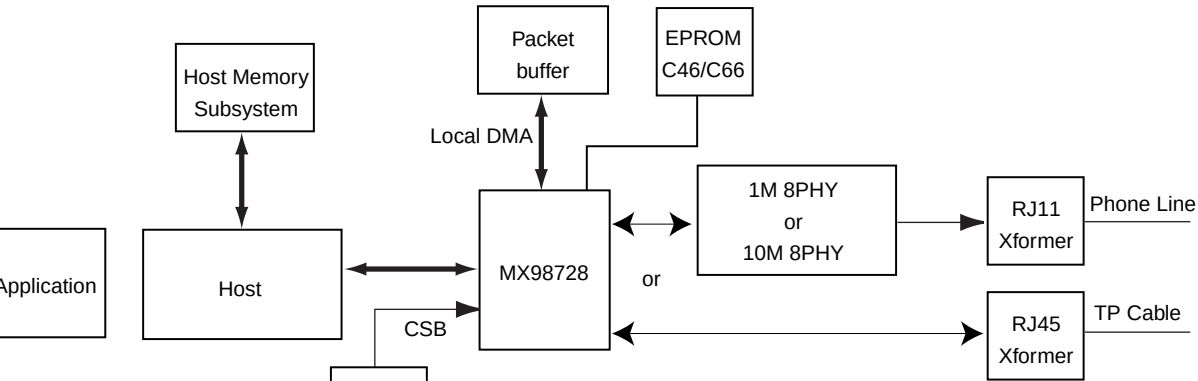

Architecture and Interface overview

### 1.3 Typical Application



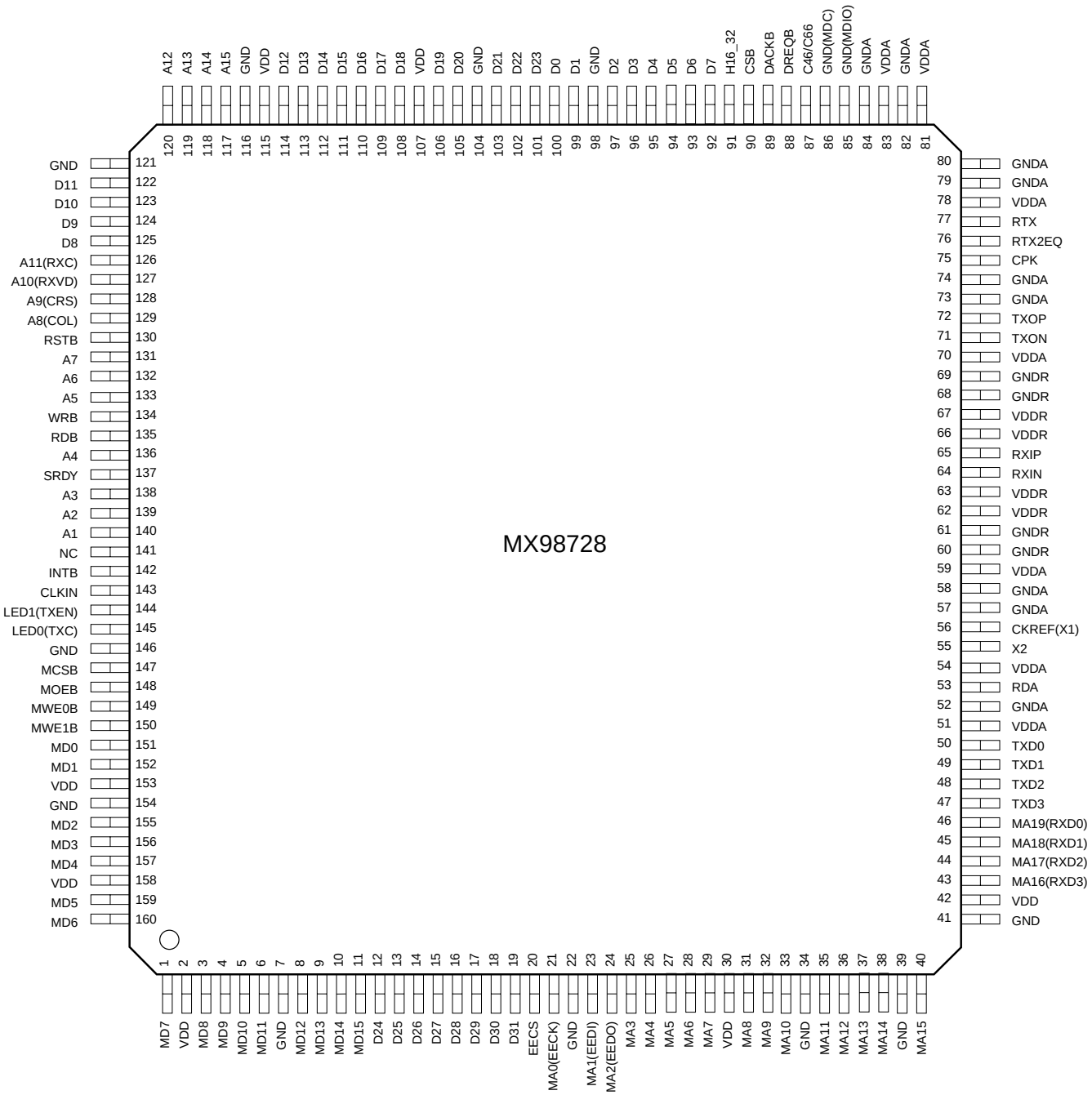

TYPICAL APPLICATION

### 1.4 Combo Application




COMBO APPLICATION

## 2.0 Pin Configuration and Description :



**2.1 Pin Description: ( all internal pull-up is 168K ohm, pull-down is 70K ohm )**

**Host Bus Interface**

| PIN# | Pin Name | Type | Description |
|---|---|---|---|
| 143 | CLKIN | I, TTL | Not used, NC pin. |
| 19-12,<br>101-103,<br>105-106,<br>108-114,<br>122-125,<br>92-97,<br>99, 100 | D[31:0] | I/O, 4ma | Host Data Bit [31:0]: |
| 117-120,<br>126-129,<br>131-133,<br>136,138-140 | A[15:1] | I, 4ma | Host Bus Address Bit [15:1] : In 32 bit mode, H16_32=0, all host accesses are 32 bit wide. When H16_32=1, all host accesses are 16 bit wide. (Internal pull-up).<br>A11, A10, A9, A8 has other definition in MII mode. |
| 126 | A11(RXC) | I, TTL | Host Bus Address Bit11, when on-chip tranceiver is used, it is used in A[15:1], when in MII mode, it is defined as receive clock RXC (25MHz or 2.5MHz) When this pin is used as address bit, it is internally grounded until Reg50.6 (A11A8EN bit) is set to enable decoding of this pin as address bit. |
| 127 | A10(RXDV) | I,TTL | Host Bus Address Bit10, when on-chip tranceiver is used, it is used in A[15:1], when in MII mode, it is defined as receive data valid RXDV signal. When this pin is used as address bit, it is internally grounded until Reg50.6 (A11A8EN bit) is set to enable decoding of this pin as address bit. |
| 128 | A9(CRS) | I,TTL | Host Bus Address Bit9, when on-chip tranceiver is used, it is used in A[15:1], when in MII mode, it is defined as carrier same CRS signal. When this pin is used as address bit, it is internally grounded until Reg50.6 (A11A8EN bit) is set to enable decoding of this pin as address bit. |
| 129 | A8(COL) | I,TTL | Host Bus Address Bit8, when on-chip tranceiver is used, it is used in A[15:1], when in MII mode, it is defined as collision COL signal. When this pin is used as address bit, it is internally grounded until Reg50.6 (A11A8EN bit) is set to enable decoding of this pin as address bit. |
| 141 | NC | | NC pin : Not connected. |
| 137 | SRDY | O, 4ma | Synchronous Ready : Active high for the write cycle to indicate the data is secured and the cycle can be finished. |

| | | | |
|---|---|---|---|
| 135 | RDB | I, TTL | Host Bus Read Indicator : Active low. (Internal pull-up) |
| 134 | WRB | I, TTL | Host Bus Write Indicator : Active low. (Internal pull-up) |
| 142 | INTB | O/D, 4ma | Host Bus Interrupt Output : Active low. |
| 88 | DREQB | O, 4ma | DMA Burst Read Request : Active low to request a burst read transfer. |
| 89 | DACKB | I, TTL | DMA Read Acknowledge : Active low during the burst read cycle. |
| 130 | RSTB | I,TTL | Host Bus Reset Input : Active low. (Schmidt trigger input, Internal pull-up) Input delay is typically 7ns, minimum RSTB pulse width must be 5 Tclk,Tclk=1/50MHz. |
| 90 | CSB | I,TTL | Host Bus Chip Select Input : Active low to enable access to GMAC, set to disable access to GMAC. But the network activity is independent of this signal. (Internal pull-down) |
| 91 | H16_32 | I,TTL | Host Bus Width 16 bit / 32 bit select : Set for the 16 bit host bus, reset for the 32 bit host bus. |

**Packet Memory Interface**

| PIN# | Pin Name | Type | Description |
|---|---|---|---|
| 46-43, 40, 38-35, 33-31, 29-25 | MA[19:3] | O,4ma | Memory Address Bits 19-3: |
| 46 | MA19(RXD0) | I/O, 4ma | Memory Address Bit19, when on-chip tranceiver is used, it is defined as MA19, while in MII mode, it is used as receive data bit RXD0 pin. |
| 45 | MA18(RXD1) | I/O, 4ma | Memory Address Bit18, when on-chip tranceiver is used, it is defined as MA18, while in MII mode, it is used as receive data bit RXD1 pin. |
| 44 | MA17(RXD2) | I/O, 4ma | Memory Address Bit17, when on-chip tranceiver is used, it is defined as MA17, while in MII mode, it is used as receive data bit RXD2 pin. |
| 43 | MA16(RXD3) | I/O, 4ma | Memory Address Bit16, when on-chip tranceiver is used, it is defined as MA16, while in MII mode, it is used as receive data bit RXD3 pin. |
| 24 | MA2(EEDO) | I/O,4ma | Memory Address Bit 2 or EEPROM Data Out bit: Right after the host reset, GMAC automatically load the configuration information from the external EEPROM. During this period, MA2 pin acts as an EEDO pin that reads in the output data stream from the EEPROM. After the EEPROM auto load sequence is done, this pin becomes MA2. Together with MA[19:3], they form the packet buffer address lines 19 - 0. |

| | | | |
|---|---|---|---|
| 23 | MA1(EEDI) | I/O,4ma | Memory Address Bit 1 or EEPROM Data In bit: During the EEPROM auto load sequence, the MA1 pin acts as the EEDI pin that writes the data stream into the EEPROM. After the EEPROM auto load sequence is done, this pin becomes MA1. Together with MA[19:2], they form the packet buffer address lines. |
| 21 | MA0(EECK) | I/O,4ma | Memory Address Bit 0 or EEPROM Clock Input : During the EEPROM auto load sequence, MA0 pin acts as the EECK pin that provides clock to the EEPROM. After the EEPROM autoload sequence is done, this pin becomes MA0. Together with MA[19:1], they form the packet buffer address lines. MA0 is don't care when packet memory is in word mode. |
| 11-8,<br>6-3,<br>1,<br>160, 159,<br>157-155,<br>152,151 | MD[15:0] | I/O,4ma | Packet Memory Data Bits 15-0: (Internal pull-down) |
| 148 | MOEB | O,4ma | Memory Output Enable: Active low during packet buffer read accesses. |
| 147 | MCSB | O,4ma | Memory Chip Select: Active low during packet buffer accesses. |
| 150,149 | MWEB[1:0] | O,4ma | Byte Write Enable: Active low during the packet buffer write cycle. MWEB1 for the high byte and MWEB0 for the low byte. |

**10/100 Transceiver interface**

| PAD# | Pin Name | Type | Description |
|---|---|---|---|
| 53 | RDA | O | RDA external resistor to ground: 10K ohm, 5% |
| 56 | CKREF(X1) | I,TTL | 25Mhz , 30 PPM external osc./crystal input : |
| 55 | X2 | O | 25Mhz , 30 PPM external crystal output : |
| 64 | RXIN | I | Twisted pair receive differential input: supports both 10/100 Mbps speeds. |
| 65 | RXIP | I | Twisted pair receive differential input: supports both 10/100 Mbps speeds. |
| 71 | TXON | O | Twisted pair transmit differential output: supports both 10/100 Mbps speeds, 802.3 AOI spec. |
| 72 | TXOP | O | Twisted pair transmit differential output: supports both 10/100 Mbps speeds, 802.3 AOI spec. |
| 75 | CPK | O | NC pin : used in the test mode only. |
| 76 | RTX2EQ | O | RTX2EQ external resistor to ground: 1.4K ohm, 5% |
| 77 | RTX | O | RTX external resistor to ground: 560 ohm, 5% |

**Miscellaneous**

| PIN# | Pin Name | Type | Description |
|---|---|---|---|
| 20 | EECS | O,2ma | EEPROM Chip Select Signal |
| 87 | C46/C66 | I,TTL | EEPROM Size Select : 1 for C46, 0 for C66. Default is 1.(Internal pull-up) |
| 145 | LED0(TXC) | I/O,16ma | LED0 (TXC in MII mode) : When on-chip tranceiver is used, it is defined as SPEED LED. When the light is on, it indicates the 100 Mbps speed. When off, it indicates the 10 Mbps speed. When both LED0 and LED1 are flashing identically, it means the bus integrity error. (Internal pull-up). When in MII mode, this pin is defined as transmit clock TXC (25 MHz or 2.5 MHz) input. |
| 144 | LED1(TXEN) | O,16ma | LED1 (TXEN in MII mode) :When on-chip tranceiver is used, it is defined as Link/Activity LED. When the light is stable and on, it indicates a good link. When flashing, it indicates TX and RX activities. When off, it means a bad link. (Internal pull-up). When in MII mode, this pin is defined as transmit enable TXEN pin. |
| 47-50 | TXD[3:0] | O, 4ma | MII Test port TXD[3:0] : Used only in the test mode as part of the MII interface. (Internal pull-down) |

**VDD/GND Pins**

| PIN# | Pin Name | Type | Description |
|---|---|---|---|
| 51,54,59,70,78,81,83 | VDDA | | Analog Vdd Pins : Must be carefully isolated in the separated Vdd plane. |
| 52,57,58,73,74,79,80, 82,84 | GNDA | | Analog Ground Pins : Must be carefully isolated in the seperated GND plane. |
| 62,63,66,67 | VDDR | | RX Vdd Pins : Must be carefully isolated in the separated Vdd plane. |
| 60,61,68,69 | GNDR | | RX Ground Pins : Must be carefully isolated in the separated ground plane. |
| 42,30,2,153,115,107 158 | VDD | | Digital Vdd Pins : Must be carefully isolated in the separated Vdd plane. |
| 41,39,34,22,7,154, 146,121,116,104,98, | GND | | Digital Ground Pins : Must be carefully isolated in the separated ground plane. |
| 85 | GND(MDIO) | I/O, 4ma | Normally grounded when on-chip tranceiver is used, while in MII mode, it is defined as MDIO pin. |
| 86 | GND(MDC) | I/O, 4ma | Normally grounded when on-chip tranceiver is used, while in MII mode, it is defined as MDC clock pin. |

## 3.0 Register (Default value is defined after the hardware/power-up reset)

**Reset logic : All register bits are cleared by the hardware reset, while the register bit with an "*" in its symbol name is also cleared by the software reset.**

**Network Control Register A : NCRA (Reg0h), R/W, default=00h**

| Bit | Symbol | Description |
|---|---|---|
| 0.0 | RESET | Reset : Software reset. After hardware reset, this bit is 0 meaning normal operation. To reset GMAC by software, software must write a 1 to this bit first, then followed by writing a 0 to this bit. After writing a 0 to this bit, GMAC starts normal operation. |
| 0.1<br>0.2 | ST0*<br>ST1* | Start Transmit Command/Status : Write to issue commands. When done, both bits are cleared automatically.<br><br>Transmit command : ST1 ST0<br>IDLE state 0 0 Read to indicate TX DMA idle state, write has no effect.<br>TX DMA Poll 0 1 Start TX DMA, send packets stored in packet memory.<br>TX FIFO Send 1 0 Immediately send the packet stored in the TX FIFO.<br>TX DMA Poll 1 1 Start TX DMA, send packets stored in packet memory.<br><br>All transmit commands are cleared to 00 when the operation is done to indicate idle state. When the TX DMA poll and the TX FIFO Send can not be used at the same time. New packet can be written to the FIFO directly only when ST1, ST0=IDLE and TXDMA[3:0]=1h. The TX DMA poll and the TX FIFO Send commands can be issued only when ST1, ST0=IDLE and TXDMA[3:0]=1h, regardless of any error status in previous transmission. |
| 0.3 | SR* | Start Receive : Enable the MAC to receive packets. Default is disabled. |
| 0.4, 0.5 | LB0*,LB1* | Loop Back Mode: LB1 LB0<br>Mode0 0 0 Normal mode<br>Mode1 0 1 Internal FIFO Loopback<br>Mode2 1 0 Internal NWAY Loopback<br>Mode3 1 1 Internal PMD Loopback<br><br>Mode 2 and 3 are reserved for the IC test purpose. Only mode 1 can be used on the bench. External loopback for the bench can be done by the full duplex normal mode with the real cable hooked up from the TX port to the RX port. |
| 0.6 | INTMODE | Interrupt Mode: Set for the active high interrupt, reset for the active low interrupt case. |
| 0.7 | INTCLK | must be 0 for normal operation. |

**Network Control Register B : NCRB (Reg1h),R/W, default=01h**

| Bit | Symbol | Description |
|---|---|---|
| 1.0 | PR* | Promiscuous mode: Set to receive any incoming valid frames received, regardless of its destination address. Default is set. |
| 1.1 | CA* | CApture Effect Mode: Set to enable an enhanced pick-off algorithm to avoid the network capture effect. |
| 1.2 | PM* | Pass Multicast: Set to accept all multicast packets (not including the broadcast address). Default is reset which directs all multicast address to hash table for further filtering . |
| 1.3 | PB* | Pass Bad Frame: Set to enable GMAC to accept Runt frames defined by register 50.2 ( RUNTSIZE). Default is reset. When PB=1, runt frame is accepted reguardless of Reg32.3 (ARXERRB). |
| 1.4 | AB* | Accept Broadcast: Default is reset which yields control of all the broadcast addresses to the check logic defined by register 32h bit 7, register 38h and 39h. Set to accept all broadcast packets without any further address filtering. |
| 1.5 | HBD* | Reserved for test purpose. Default is 0. |
| 1.7-6 | RXINTC[1:0]* | Receive Interrupt Counter : Receive interrupt RI or REI assertion depends on the number of packets received defined by these two bits or the RXINTT timer ( Reg.15/14h ) timeout, whichever comes first.<br><br>Default is 00h after reset, meaning the normal receive interrupt operation which asserts RI or REI after a single packet is received and no RXINTT timer is used. Non-zero value in these two bits will enable this special receive interrupt operation.<br>RXINTC1 RXINTC0 Interrupt received packet count<br>0 0 1 ( default )<br>0 1 2<br>1 0 4<br>1 1 8 |

**GMAC Test Register A : TRA (Reg02h),R/W, default=00h**

| Bit | Symbol | Description |
|---|---|---|
| 2.0 | TEST | Test mode enable: Set to enable test modes defined by TMODE[2:0]. Default is reset for the normal operation, |
| 2.1-2.3 | TMODE[2:0] | Test Mode Select bits[2:0]: Reserved for GMAC's internal tests, only meaningful when the TEST bit is set, except when TMODE [2:0] = "110" which is also used as normal mode with EEPROM interface disabled. When TMODE [2:0] = "110" & Test =0, then MA19~MA16 are still SRAM address bit19~16, while Test = 1, MA19~MA16 are defined as test pins reserved for debug purpose. |
| 2.4 | RWR | Receive Watchdog Release : When set, the receive watchdog is released 40 to 48 bit times from the last carrier deassertion. When reset, the receive watchdog is released 16 to 24 bits times from the last carrier deassertion. |
| 2.5 | RWD | Receive Watchdog Disable : When set, the receive watchdog is disabled. When reset, receive carriers longer than 2560 bytes are guaranteed to cause the watchdog time-out. Packets shorted than 2048 bytes are guaranteed to pass. |
| 2.6 | FC | Forced Collision : Set to force collision at every transmit packet. This bit works only in the internal FIFO loopback mode, i.e. LB0=1, LB1=0, to test the excessive collision. Default is reset. |
| 2.7 | SB | Start/Stop Back-off counter: When set, indicates the internal back-off counter stops counting when any carrier is detected. The counter resumes when the carrier drops. When reset, the internal back-off counter is not affected by the carrier activity. Default is reset. |

**GMAC Test Register B : TRB (Reg03h),R/W, default=00h**

| Bit | Symbol | Description |
|---|---|---|
| 3.0 | FKD* | Flaky Oscillator Disable: When set, indicates that the internal flaky oscillator is disabled. Pseudo random numbers are chosen instead of fully random numbers, used for the internal diagnostic purpose. Set to disable the normal clocking scheme in the timer's test. Reset to enable the timer test. Default is reset. |
| 3.1 | RDNCNTCB* | Reserved for test |
| 3.2 | RDNCNTSB* | Reserved for test |
| 3.3 | COLCNTCB* | Reserved for test |
| 3.4 | BFS0*(MDC) | Normally used as BFS0 pin for test purpose, while in MII mode, it is defined as MII management clock signal (MDC) to be used as a timing reference of MDIO pin. |
| 3.5 | BKCNTLB*(MDIOEN) | Normally used as BKCNTLB pin for test purpose, while in MII mode, it is used to control the direction of MDIO pin. Set MDIOEN = 1 will make MDIO pin as input pin, the value can be read from MDI bit.<br>Set MDIOEN = 0 will make MDIO pin as output pin, the value of MDO bit is driven out to MDIO pin. |

| | | |
|---|---|---|
| 3.6 | BFS1*(MDO) | Normally used as BFS1 pin for test purpose, while in MII mode, it is used as MII management write data (MDO) for MDIO pin's output data. |
| 3.7 | BFSTATUS*(MDI) | Normally used as BFSTATUS pin for test purpose, while in MII mode, it is used as MII management read data (MDI) for MDIO pin's input data. |

**Last Transmitted Packet Status: LTPS ( Reg4h), RO, default=00h**

| Bit | Symbol | Description |
|---|---|---|
| 4.0 | CC0* | Collision Count Bit 0 : |
| 4.1 | CC1* | Collision Count Bit 1 : |
| 4.2 | CC2* | Collision Count Bit 2 : |
| 4.3 | CC3* | Collision Count Bit 3 : When CC[3:0] = 1111 and a new collision is detected, it is called the excessive collision error which will abort the current packet. The TEI interrupt bit will be set. |
| 4.4 | CRSLOST* | Carrier Sense Lost : Set to indicate CRS was lost during the transmission. Default is reset for the normal packet transmission. |
| 4.5 | UF* | TX FIFO Underflow : Set to indicate a underflow problem in the TX FIFO. An FIFOEI interrupt is generated for the driver to resolve this problem. |
| 4.6 | OWC* | Out of Window Collision : Set to indicate a collision occurred after 64 bytes of data has been transmitted. No retransmission will be issued. |
| 4.7 | TERR* | Transmit Error: Set to indicate the packet transmitted with error. Reset for the normal packet transmission. |

**Last Received Packet Status: LRPS ( Reg5h), RO**

| Bit | Symbol | Description |
|---|---|---|
| 5.0 | BF* | RX Packet Buffer Full Error : 1 indicates the RX packet buffer is full. |
| 5.1 | CRC* | CRC error : The calculation is based on the integer multiple of bytes. Set to indicate the CRC error for the received packet. |
| 5.2 | FAE* | Frame Alignment Error : Set to indicate an extra nibble is received which is not at the octet boundary. This error is independent of the CRC detection. |
| 5.3 | FO* | FIFO Overrun : When set, an interrupt is generated. The driver must resolve this error. |
| 5.4 | RW* | Receive Watchdog : Set to indicate the frame length exceeds 2048 bytes. An interrupt will be generated to the driver. |
| 5.5 | MF* | Multicast Frame address : Set to indicate the current frame has the multicast address. |
| 5.6 | RF* | Runt Frame : Set to indicate a frame length less than 64 or 60 bytes depending on register 50.2 ( RUNTSIZE ), only meaningful when the Reg01h.3 PB bit is set. When PB=1, a runt frame will be accepted & RI is set for receive interrupt. When PB=0, a runt frame is rejected. |
| 5.7 | RERR* | Receive Error : Set to indicate a packet received with errors including CRC, FAE, FO, RW error. |

Notes : This LRPS register contains the same status byte as in the description field of the last received packet in the packet memory.

**Missed Packet Counter: MPCL (Reg07/06h), R/W, default=0000h**

| Bit | Symbol | Description |
|---|---|---|
| 6.7-0 | MISSCNT[7:0]* | Miss Packet Counter Bits [7:0]: Lower byte of the Miss packet counter. |
| 7.7-0 | MISSCNT[15:8]* | Miss Packet Counter Bits [15:8]: Upper byte of the Miss packet counter. |

**Interrupt Mask Register: IMR (Reg.08h), R/W, default=00h**

| Bit | Symbol | Description |
|---|---|---|
| 8.0 | FRAGIM | Fragment Counter Interrupt Mask: Set to enable the host DMA Fragment counter ( FRAGI) interrupt. Default is reset which disable the FRAGI interrupt.When AUTORCVR is set, this bit should be reset. |
| 8.1 | RIM | Received Interrupt Mask: Set to enable the Packet Received Interrupt. Default is reset which disables the RI interrupt. |
| 8.2 | TIM | Transmit Interrupt Mask: Set to enable the Packet transmit OK interrupt. Default is reset which disables the TI interrupt. |
| 8.3 | REIM | Receive Error Interrupt Mask: Set to enable the Receive Error interrupt. Default is reset which disables the REI interrupt. |
| 8.4 | TEIM | Transmit Error Interrupt Mask: Set to enable transmit error interrupt. Default is reset which disables the TEI interrupt. |
| 8.5 | FIFOEIM | FIFO Error Interrupt Mask: Set to enable the FIFO Error interrupt. Default is reset which disables the FIFOEI interrupt. When AUTORCVR is set, this bit should be reset. |
| 8.6 | BUSEIM | Bus Error Interrupt Mask: Set to enable the Bus Error interrupt. Default is reset which disables the BUSEI interrupt. |
| 8.7 | RBFIM | RX Buffer Full Interrupt Mask: Set to enable the RX Buffer full interrupt. Default is reset which disables the BFI interrupt. |

**Interrupt Register: IR (Reg09h), R/W, default=00h**

| Bit | Symbol | Description |
|---|---|---|
| 9.0 | FRAGI* | Fragment Counter Interrupt : Set to assert the interrupt when the host DMA Fragment Counter is less than current received packet length. Writing 1 to this bit will clear the bit and the interrupt. Writing 0 has no effect. |
| 9.1 | RI* | Receive OK Interrupt : Set to assert the interrupt. Writing 1 to this bit will clear the bit and the interrupt. Writing 0 has no effect. The assertion timing of RI can be programmed through the Reg50.4 bit (RINTSEL) for either the completion of the host receive DMA activity or the completion of the receive local DMA activity. |
| 9.2 | TI* | Transmit OK Interrupt: Set to assert the interrupt. Writing 1 to this bit will clear the bit and the interrupt. Writing 0 has no effect. |
| 9.3 | REI* | Receive Error Interrupt: Set to assert the interrupt when the packet is received with error . Writing 1 to this bit will clear the bit and the interrupt. Writing 0 has no effect. The assertion timing of RI can be programmed through the Reg50.4 bit (RINTSEL) for either the completion of the host receive DMA activity or the completion of the receive local DMA activity. |
| 9.4 | TEI* | Transmit Error Interrupt : Set to assert the interrupt when the packet is transmitted with error. Writing 1 to this bit will clear the bit and the interrupt. Writing 0 has no effect. |
| 9.5 | FIFOEI* | FIFO Error Interrupt: Set to assert the interrupt when either the TX FIFO is overrun or the RX FIFO is overrun. Writing 1 to this bit will clear the bit and the interrupt. Writing 0 has no effect. |
| 9.6 | BUSEI* | Bus Error Interrupt: Set to assert the interrupt when the Bus integrity check is enabled and failed. Writing 1 to this bit will clear the bit and the interrupt. Writing 0 has no effect. |
| 9.7 | RBFI* | RX Buffer Full Interrupt: Set to assert the interrupt when the RX buffer area is being overwritten by new received packets. Writing 1 to this bit will clear the bit and the interrupt. Writing 0 has no effect. |

Note : All page pointer bits [11:0] are mapped to MA[19:8] with the same bit ordering.

**Boundary Page Pointer Register: BP (Reg.0Bh/0Ah), R/W, default=x000h**

| Bit | Symbol | Description |
|---|---|---|
| 0A.7-0, 0B.3-0 | BP[11:0] | Boundary Page Pointer between the tx/rx buffers: page TLBP[11:0] to page BP[11:0] is the tx buffer. Page BP[11:0] to page RHBP[11:0] is the rx buffer. BP[11:0] is mapped to MA[19:8]. The MSB is the Reg0BH.3 bit. The LSB is the Reg0AH.0 bit. |

**TX Low Boundary Page Pointer Register: TLBP (Reg.0Dh/0Ch), R/W, default=x000h**

| Bit | Symbol | Description |
|---|---|---|
| 0D.3-0, | TLBP[11:0] | TX Low Boundary Page Pointer : The TX packet buffer is defined as between TLBP [11:0] and BP [11:0]. The MSB is the Reg0Dh.3 bit. The LSB is the Reg0Ch.0 bit. |

**Transmit Buffer Write Page Pointer Register: TWP (Reg.0Fh/0Eh), R/W, default=x000h**

| Bit | Symbol | Description |
|---|---|---|
| 0E.7-0, 0F.3-0 | TWP[11:0] | Transmit Buffer Write Page Pointer: TWP[11:0] are mapped to MA[19:8] with the same bit ordering. The MSB is the Reg0Fh.3 bit. The LSB is the Reg0Eh.0 bit. TWP is normally controlled by the device driver. An internal Byte Counter (TWPBC) is associated with this page register. |

**Reserved Register: (Reg11h/10h), default=x000h**

| Bit | Symbol | Description |
|---|---|---|
| reserved | | not used |

**Transmit Buffer Read Page Pointer Register: TRP (Reg.13h/12h), R/W, default=x000h**

| Bit | Symbol | Description |
|---|---|---|
| 12.7-0, 13.3-0 | TRP[11:0] | The Page Index of the Transmit Buffer Read Pointer: Current transmit read page pointer. The MSB is the Reg13h.3 bit. The LSB is the Reg12h.0 bit. TRP is controlled by GMAC only. An internal Byte Counter (TRPBC) is associated with this page register. |

**Receive Interrupt Timer: RXINTT (Reg15h/14h), R/W, default=0000h**

| Bit | Symbol | Description |
|---|---|---|
| 14.7-0, 15.7-0 | RXINTT[7:0], RXINTT[15:8] | Receive Interrupt Timer: Default is 0000h, meaning no time-out is used on the RI or the REI interrupt assertion. Reg15h.7 is the RXINTT.15 bit. Reg14h.0 is the RXINTT.0 bit. Any non-zero value enables the time out function if RXINTC[1:0] (Reg01h.[7:6] ) > 0. The time unit of this counter is 40ns per count. The possible timeout period ranges from 40ns to 2622 us. When the RXINTT times out, if the received packet count has not reached the RXINTC [1:0], an interrupt will be generated (which is caused by the RXINTT timeout alone). Depending on the Reg50.4 bit, RXINTT will start counting after the end of the last receive packet of either the host DMA or the RX local DMA. See waveform diagram about "RXINTT start time definifion." |

**Receive Buffer Write Page Pointer Register: RWP (Reg17h/16h), R/W, default=x000h**

| Bit | Symbol | Description |
|---|---|---|
| 16.7-0, 17.3-0 | RWP[11:0] | Receive Buffer Write Page Pointer: Current receive write page pointer. The MSB is the Reg17h.3 bit. The LSB is the Reg16h.0 bit. This register is controlled by GMAC only. An internal Byte Counter (RWPBC) is associated with this page register. |

**Receive Buffer Read Page Pointer Register: RRP ( Reg19h/18h), R/W, default=0000h**

| Bit | Symbol | Description |
|---|---|---|
| 18.7-0, 19.3-0 | RRP[11:0] | Receive buffer Read Page Pointer: Current receive read page pointer. RRP[11:0] is mapped to MA[19:8]. The MSB is the Reg19h.3 bit. The LSB is the Reg18h.0 bit. This register is normally controlled by the device driver. An internal Byte Counter (RRPBC) is associated with this page register. |

**RX High Boundary Page Pointer Register: RHBP Reg.1Bh/1Ah, R/W, default=x000h**

| Bit | Symbol | Description |
|---|---|---|
| 1A.7-0. 1B.3-0 | RHBP[11:0] | Receive High Boundary Page Pointer : The RX packet buffer is defined as between RHBP [11:0] and BP[11:0]. The MSB is the Reg1Bh.3 bit. The LSB is Reg1Ah.0 bit. |

**EEPROM Interface Register: Reg1Ch, R/W, default=00h**

| Bit | Symbol | Description |
|---|---|---|
| 1C.0 | EECS* | Chip Select output to the external EEPROM clock device |
| 1C.1 | EECK* | Serial Clock output to the external EEPROM clock device, <1MHz. |
| 1C.2 | EEDI* | Serial Data Input to the external EEPROM clock device |
| 1C.3 | EEDO* | Serial Data Output from the external EEPROM clock device |
| 1C.4 | EESEL* | Set to enable the external EEPROM write operation(write Select). Default 0 is read. |
| 1C.5 | EELD* | Set to enable reloading the entire contents of the EEPROM just like the power-on reset or the hardware reset. When the loading is done, this bit will be set by GMAC automatically. |
| 1C.6 | HOLDREQ | Reserved, default = 0. |
| 1C.7 | HLDAACK | Reserved, Read only. |

**Bus Integrity Check Timer: BICT (Reg1Dh), R/W, default=00h**

| Bit | Symbol | Description |
|---|---|---|
| 1D.7-0 | BICT[7:0]* | Bus Integrity Check Timer: Default is 00h, meaning no bus integrity check is enabled. The time unit of this counter is 40ns. Value in this counter other than zero will enable the bus integrity check. Any bus cycle longer than the timeout period will cause the "termination of the current bus cycle", which can avoid the abnormal bus hang and the bus dead lock. The BUSEI interrupt will be issued. LED0 and LED1 will both be flashing identically in 12.5Hz. The possible timeout period ranges from 40ns to a maximum of 10.24us. This counter can be used to warn long cycles so that the driver can tune the local DMA performance. |

**IO Data Port Page Pointer Register: IORDP (Reg.1Fh/1Eh), R/E, default=x000h**

| Bit | Symbol | Description |
|---|---|---|
| 1E.7-0, 1F.3-0 | IORDP[11:0] | IO Read Data Port Page Pointer [11:0] : Any read to IORD (Reg4C-4F) will be mapped to the packet buffer address which consists of IORDP and the current content of the internal byte counter (IORDPBC). IORDP can be pointed to any page within the packet buffer space. IORDP[11:0] are mapped to MA[19:8] during the data port access. IORDP can be increment automatically when the current page is exhausted and if AUTOPUB is 0. This page pointer is usually used by the driver to read multiple TX packets status in the packet memory. Bit 3A.1 ( STIORD/RRDYB ) is with IORDP and IORD if the SRDY pin is not available on the system application. |

**Network Address Filtering Registers : Reg20h~25h (R/W), 26h~2Dh (R/W), default=00h**

| Bit | Symbol | Description |
|---|---|---|
| 20.[7:0] | PAR0 | Physical Address Register Byte 0: PAR [7:0] |
| 21.[7:0] | PAR1 | Physical Address Register Byte 1: PAR [15:8] |
| 22.[7:0] | PAR2 | Physical Address Register Byte 2 : PAR [23:16] |
| 23.[7:0] | PAR3 | Physical Address Register Byte 3 : PAR [31:24] |
| 24.[7:0] | PAR4 | Physical Address Register Byte 4 : PAR [39:32] |
| 25.[7:0] | PAR5 | Physical Address Register Byte 5 : PAR [47:40] |
| 26.[7:0] | MAR0 | Hash Table Register Byte 0 : MAR [7:0] |
| 27.[7:0] | MAR1 | Hash Table Register Byte 1 : MAR [15:8] |
| 28.[7:0] | MAR2 | Hash Table Register Byte 2 : MAR [23:16] |
| 29.[7:0] | MAR3 | Hash Table Register Byte 3 : MAR [31:24] |
| 2A.[7:0] | MAR4 | Hash Table Register Byte 4 : MAR [39:32] |
| 2B.[7:0] | MAR5 | Hash Table Register Byte 5 : MAR [47:40] |
| 2C.[7:0] | MAR6 | Hash Table Register Byte 6 : MAR [56:48] |
| 2D.[7:0] | MAR7 | Hash Table Register Byte 7 : MAR [63:57] |

**Transceiver Control Register : ANALOG (Reg 2Eh), R/W, default=07h**

| Bit | Symbol | Description |
|---|---|---|
| 2E.0 | DS120 | Must be 1 for NORMAL mode with auto-compensation. |
| 2E.1 | DS130 | Must be 1 for NORMAL mode with auto-compensation |
| 2E.2 | PWD10B | Set for NORMAL mode, write 0 followed by write 1 will power down 10 Base-T analog circuit. |
| 2E.3 | PWD100 | Reset for NORMAL mode, write 1 followed by write 0 will power down 100 Base-T analog circuit. |
| 2E.4 | RSQ | Reduced SQuelch Enable : Set to enable the reduced squelch circuit in the 10 Base-T mode for the receive channel. This can help the reception in a long cable application. Default is reset, meaning the normal CAT-5 cable is used. |
| 2E.5 | RST100 | Reset for NORMAL mode, write 1 followed by write 0 will reset 100 Bare-T analog circuit. |
| 2E.6-7 | Reserved | must be zero. |

**DMA Interval Timer : DINTVAL (Reg 2Fh), R/W, default=00h**

| Bit | Symbol | Description |
|---|---|---|
| 2F.7-0 | DINTVAL | DMA Interval Timer : Used to control the latency between the two consecutive DMA read burst cycles. Default is all zero, meaning this function is disabled. A non-zero value tells GMAC to prepare the next host DMA read close to the timer's expiration. This timer will improve the Host DMA read access priority. The timer's time base is 0.5Mhz, which gives a maximum of 512us. |

**NWAY Configuration Register : NWAYC (Reg 30h), R/W, default=84h**

| Bit | Symbol | Description |
|---|---|---|
| 30.0 | FD | Full Duplex Mode: Set 1 to force the full duplex mode. The default is 0, meaning the half duplex mode. This bit is meaningful only if ANE = 0 |
| 30.1 | PS100/10 | Port Select 100/10 bit : Default is 0, meaning the 10 Base-T mode. |
| 30.2 | ANE | Autonegotiation Enable: Set to enable the NWAY function. Default is set. ANS[2:0] should be written 001 to restart the autonegotiation sequence after ANE is set. |
| 30.[5:3] | ANS[2:0] | Autonegotiation status bits: Read only for the NWAY status, except when write 001 will restart the autonegotiation sequence. The MSB is the Reg30h.5 bit when Nway settles down in one network mode, one bit of Reg31.4~Reg 31.7 will be set to indicate the chosen network mode.<br>Autonegotiation Arbitration State, arbitration states are defined<br>000 = Autonegotiation disable<br>001 = Transmit disable<br>010 = ability detect<br>011 = Acknowledge detect<br>100 = Complete acknowledge detect<br>101 = FLP link good; autonegotiation complete<br>110 = Link check |
| 30.6 | NTTEST | Reserved |
| 30.7 | LTE | Link Test Enable : Default is high, meaning the link check is always enabled. Reset forces a good link in the 10 Base-T mode for the testing purpose. |

**NWAY Status Register : NWAYS (Reg 31h), RO, default=00h**

| Bit | Symbol | Description |
|---|---|---|
| 31.0 | LS10 | Physical Link Status of 10 Mbps TP : Set for a good link in 10 Base-T. |
| 31.1 | LS100 | Physical Link Status of 100 Mbps TP : Set for a good link in 100 Base-TX. |
| 31.2 | LPNWAY | Link Partner NWAY Status : 1 to indicate the link partner is capable of NWAY support. Reset for the non-NWAY link partner. |
| 31.3 | ANCLPT | Auto-negotiation Completion : Set to indicate that a normal NWAY state machine completion. Reset for incomplete state. |
| 31.4 | 100TXF | NWAY 100 TX Full_duplex Mode : Set to indicate NWAY is settled down in the 100 TX full duplex mode. |
| 31.5 | 100TXH | NWAY 100 TX Half_dulpex Mode : Set to indicate NWAY is settled down in the 100 Base-T half duplex mode. |
| 31.6 | 10TXF | NWAY 10 TX Full_duplex Mode : Set to indicate NWAY is settled down in the 10 Base-T full duplex mode. |
| 31.7 | 10TXH | NWAY 10 TX Half_duplex Mode : Set to indicate NWAY is settled down in the 10 Base-T half duplex mode. |

**GMAC Configuration A Register: GCA (Reg 32h), R/W, default=00h**

| Bit | Symbol | Description |
|---|---|---|
| 32.0 | BPSCRM | Bypass Scrambler: Default is 0, meaning enable the 100 TX scrambler. Set to disable the scrambler for the 100 TX mode. |
| 32.1 | PBW | Packet Buffer Data Width : Default is 0, meaning the packet buffer data width is byte. Set when the packet buffer data width is 16 bits. |
| 32.2 | SLOWSRAM | Normally reset, SRAM Taa must be less than 25ns, set to use -70ns SRAM or better |
| 32.3 | ARXERRB | Accept RX packet with error : Default is reset to receive packets with error, set to reject packets with error, packet memory will not contain packet with RW, FO, CRC errors. |
| 32.4 | MIISEL | Default = 0 after reset, on-chip tranceiver is used. Set by software to enable MII interface. |
| 32.5 | AUTOPUB | Auto Page Update option :<br>Set to disable the automatic host page update during the host DMAs. Reset to enable the host page update for the RRP, TWP registers. Default is reset. |
| 32.6 | TXFIFOCNTEN | Default=0, after rest which means Reg 3E & 3F (TXFIFOCNT) are not used. This option is only good for a byte-base host transfer. For host which do word/double word transfer, this bit must be set to 1 to force TXFIFO use actual packet length for transmission. |
| 32.7 | RESERVED | Default = 0. |

**GMAC Configuration B Register: GCB (Reg33h), R/W, default=00h**

| Bit | Symbol | Description | | | |
|---|---|---|---|---|---|
| 33.1-0 | TTHD[1:0] | Transmit FIFO Threshold : Default is 00 | | | |
| | | TTHD1 | TTHD0 | FIFO depth | aggressiveness |
| | | 0 | 0 | 1/2 | medium |
| | | 0 | 1 | 1/4 | least |
| | | 1 | 0 | 3/4 | more |
| | | 1 | 1 | reserved | reserved |
| 33.3-2 | RTHD[1:0] | Receive FIFO Threshold : Default is 00 | | | |
| | | RTHD1 | RTHD0 | FIFO depth | aggressiveness |
| | | 0 | 0 | 1/2 | medium |
| | | 0 | 1 | 1/4 | most |
| | | 1 | 0 | 3/4 | least |
| | | 1 | 1 | reserved | |
| 33.4 | SRAMELEN | SRAM Early Latch Enable : Default = 0. Set to enable. | | | |
| 33.5 | X4ELEN | X4 FIFO Early Latch Enable : Defautl = 0. Set to enable. | | | |
| 33.6 | DREQB2EN | DREQB NEW Timing Enable : Default = 0. Set to enable. | | | |
| 33.7 | reserved | | | | |

**IO Mapped Data port: TWD (Reg34h/35h/36h/37h), WO**

| Bit | Symbol | Description |
|---|---|---|
| 34.7-0<br>35.7-0<br>36.7-0<br>37.7-0 | TWD[31:0] | Transmit Write Data Port : The 32 bit data port is used for writing the packet data into the transmit buffer ring. In the 32 bit mode, i.e. H16_32=0, reg37h is the MSB byte (byte3), and reg34h is the LSB byte (byte 0). In the 16 bit mode, i.e. H16_32=1, reg35h is the MSB byte (byte 1) and reg34h is the LSB byte (Byte 0). Access to this port will be mapped to the packet buffer pointed to by the TWP page pointer and the internal byte counter TWPBC. No burst is supported for either read or write. Any access to this port will increment the TWPBC by either 2 or 4 depending on H16_32. This is usually used by the driver to prepare TX packets. If host system does not support SRDY pin, then register 3A bit 0 ( WRDYB ) can be used to handshake with GMAC during the data port write cycle. |

**Reserved Register : RESERVED (Reg39h/38h), R/W, default=0000h**

| Bit | Symbol | Description |
|---|---|---|
| 38.7-0 | RESERVED | Default = 00h |
| 39.7-0 | RESERVED | Default = 00h |

**Host Interface Protocol Register: Reg3Ah, R/W, default=00h**

| Bit | Symbol | Description |
|---|---|---|
| 3A.0 | WRDYB | Write Packet Memory Ready Bar Status Indication : It is used to indicate whether the TWD port is ready for the next write. Read only. 1 indicates the host can not issue a new write cycle into the TWD data port. 0 indicates the host can issue a new write cycle into the TWD port. This bit is primarily used by the host who does not use the SRDY pin. |
| 3A.1 | STIORD/RRDYB | Start IORD read/Read Ready Bar : Write 1 to start the IORD port read. When data is ready for the host in the IORD port, this bit becomes 0 indicating a "read ready". So the host needs to poll this bit for 0 before he can issue a read to the IORD port. Reading a 1 indicates data is not ready in the IORD port yet. This bit is primarily used by the host who does not use the SRDY pin. |
| 3A.2 | DREQB | DREQB pin status bit : A direct reflection of the DREQB pin which can be read to inquire whether there are any RX packet data available in the RRD port. This bit is primarily used by the host who does not use the DREQB pin. |

**Link Partner Link Code Register : LPC, Reg3Bh, RO**

| Bit | Symbol | Description |
|---|---|---|
| 3B.0 | LPC[0] | Link Partner Link Code A0 : 10 Base-T half duplex ability |
| 3B.1 | LPC[1] | Link Partner Link Code A1 : 10 Base-T full duplex ability |
| 3B.2 | LPC[2] | Link Partner Link Code A2 : 100 Base-TX half duplex ability |
| 3B.3 | LPC[3] | Link Partner Link Code A3 : 100 Base-TX full duplex ability |
| 3B.4 | LPC[4] | Link Partner Link Code A4 : 100 Base-T4 ability |
| 3B.5 | LPC[5] | Link Partner Link Code RF bit : Remote Fault bit |
| 3B.6 | LPC[6] | Link Partner Link Code Ack bit : Acknowledge bit |
| 3B.7 | LPC[7] | Link Partner Link Code NP bit : Next Page bit |

**TX/RX DMA Status Register: Reg3Ch, R/W, default=00h**

| Bit | Symbol | Description |
|---|---|---|
| 3C.7-4 | TXDMA[3:0]* | TX DMA State Indicators : For internal diagnostic purpose indicating TX DMA's current status.<br>TXDMA3 is TX status error bit, set to indicate error during transmission.<br>TXDMA2 is TX FIFO underflow error. |
| 3C.3-0 | RXDMA[3:0]* | RX DMA State Indicators : For internal diagnostic purpose indicating RX DMA's current status.<br>RXDMA3 is RX status error bit, set to indicate error during receive.<br>RXDMA2 is RX FIFO overflow error. |

| TXDMA[1:0] | State Description |
|---|---|
| 00 | Idle |
| 01 | Read TX Description |
| 10 | Transmit Current Packet |
| 11 | Write TX Description |

| RXDMA[1:0] | State Description |
|---|---|
| 00 | Idle |
| 01 | Receive Current Packet |
| 10 | Write TX Description |
| 11 | Run Frame/Reset RX FIFO |

**MISC Control Register : MISC1, Reg3Dh, R/W, default=3Ch**

| Bit | Symbol | Description |
|---|---|---|
| 3D.0 | BURSTDMA | reserved for internal DMA burst control, default = 0 after reset. |
| 3D.1 | DISLDMA* | Disable Local DMA arbitration : Default is 0 after reset, meaning local DMAs are enabled in the SRAM bus arbitration. Set to disable the local DMA arbitration only when the Reg02h.0 TEST bit is also set. It is used to force the overrun or the underrun error for the test purpose. |
| 3D.2 | TPF | 10 Base-T Port Full Duplex capability bit in the linkcode word : Default is set to enable advertising the 10 Base-T Full duplex capability. Reset to disable advertising this capability in the outgoing NWAY's linkcode word. |
| 3D.3 | TPH | 10 Base-T Port Half Duplex capability bit in the linkcode word : Default is set to enable advertising the 10 Base-T Half duplex capability. Reset to disable advertising this capability in the outgoing NWAY's linkcode word. |
| 3D.4 | TXF | 100 Base-TX Full Duplex capability bit in the linkcode word : Default is set to enable advertising the 100 Base-TX Full duplex capability. Reset to disable advertising this capability in the outgoing NWAY's linkcode word. |
| 3D.5 | TXH | 100 Base-TX Half Duplex capability bit in the linkcode word ; Default is set to enable advertising the 100 Base-TX Half duplex capability. Reset to disable advertising this capability in the outgoing NWAY's linkcode word. |
| 3D.6 | TXFIFORST | TX FIFO Reset control : Writing a 1 to this bit will clear the TX FIFO, reset all the current TX FIFO's internal pointers and related byte counters and bring the TX DMA back to the idle state. After reset this bit to 0, GMAC starts normal operation. If current transmission takes too long due to collisions, the software can use this bit to abort "current transmission" and bring GMAC's TX DMA back to idle state for a fresh new transmission. |
| 3D.7 | RXFIFORST | RX FIFO Reset control : Writing a 1 to this bit will clear the RX FIFO, reset all the current RX FIFO's internal pointers and related byte counters and bring the RX DMA back to the idle state. After reset this bit to 0, GMAC starts normal operation. |

**TX FIFO Byte Counter (Direct FIFO Mode) : TXFIFOCNT, Reg3F/3Eh, R/W**

| Bit | Symbol | Description |
|---|---|---|
| 3E.7-0 | TXFIFOCNT[7:0] | TX FIFO Send Byte Count bits [7:0]: Together with TXFIFOCNT[11:8] forms a 12 bits TX FIFO byte count for the direct FIFO mode. |
| 3F.3-0 | TXFIFOCNT[11:8] | TX FIFO Send Byte Count bits [11:8]: Together with TXFIFOCNT[7:0] forms a 12 bits TX FIFO byte count for the direct FIFO mode. Software must program TXFIFOCNT[11:0] with exact packet length in bytes before command GMAC to start transmit ( ST0, ST1 ). Since host bus is either word or double word mode. A exact byte count must be programmed for TX channel to send out data and CRC correctly. |

**RX Burst Read Data Port : RRD[31:0] (Reg40h~43h), RO, default=XXXXXXXXh**

| Bit | Symbol | Description |
|---|---|---|
| 40.7-0,<br>41.7-0<br>42.7-0<br>43.7-0 | RRD[31:0] | RX Read Data Port : The 32 bit read only data port for the RX buffer ring. The MSB byte (byte 3) is Reg43h and The LSB byte (byte 0) is Reg40h if H16_32=0. Reg41h is the MSB byte (byte 1 ) and Reg40h is the LSB 43.7-0 byte (Byte 0) if H16_32=1.The RX buffer ring accessed by this port is pointed to by RRP and RRPBC. When 4 consecutive double words (4x4 bytes if H16_32=0, or 4x2 bytes if H16_32=1) are ready inside GMAC, DREQB will be asserted and burst transfers can be issued through the use of DACKB. GMAC will maintain the burst read buffer's integrity in both cases. This port is used to fetch RX packets. |

**ID1 (Reg45h/44h), RO, default="MX"**

| Bit | Symbol | Description |
|---|---|---|
| 44.7-0,<br>45.7-0 | ID1[15:0] | ID1 16 bit code : Reg45h is the MSB byte, which is set to "M". Reg44h is the LSB byte, which is set to "X". |

**ID2 (Reg46h/47h), RO, default="0001"**

| Bit | Symbol | Description |
|---|---|---|
| 46.7-0,<br>47.7-0 | ID2[15:0] | ID2 16 bit code : Reg47h is the MSB byte, which is set to 00h. Reg46h is the LSB byte, which is set to 01h. |

**Write TX FIFO Data Port Register : WRTXFIFOD[31:0] ( reg 4B-48h ), WO**

| Bit | Symbol | Description |
|---|---|---|
| 48.7-0, 49.7-0 4A.7-0 4B.7-0 | WRTXFIFOD[31:0] | Write TX FIFO Data Port : The 32 bit write only data port for the TX on-chip FIFO in the direct FIFO mode. In the 32 bit mode, H16_32=0, the MSB byte (byte 3) is Reg4Bh and the LSB byte (Byte 0) is Reg48h. In the 16 bit mode, H16_32=1, Reg49h is the MSB byte (byte 1) and Reg48h is the LSB byte (byte 0). An internal counter (TXFIFOBC) is used to keep track of the total number of bytes written to the FIFO through this port before the host issues reg00h.ST1=1, ST0=0 (the TX FIFO send command). Do not write to this port when the TX local DMA is still active. |

**IO Read Data Port Register : IORD[31:0] ( reg 4C-4Fh ), RO**

| | | |
|---|---|---|
| 4C.7-0, 4D.7-0 4E.7-0 4F.7-0 | IORD[31:0] | IO Read Data Port : The 32 bit read only data port that works with the IORDP page pointer. In the 32 bit mode, H16_32=0, the MSB byte (byte 3) is Reg4Fh and the LSB byte (byte 0) is Reg4Ch. In the 16 bit mode, H16_32=1, Reg4Dh is the MSB byte (byte 1) and Reg4Ch is the LSB byte (byte 0). An internal counter (IORDPBC) is used to keep track of the current location within a particular page . For the system that does not support the SRDY pin, the Register 3A.1 bit (STIORD/RRDYB ) can be used to read this port in a hand shaking manner. To use register 3A.1 ,first write 1 to register 3A.1. When the data is ready in this IORD port, register 3A.1 bit will be internally cleared to 0. So the host can read the register 3A.1 bit for 0 in order to know whether the data is ready or not. This IORD can be used to fetch TX descriptors in a multiple packets send operation. |

**MISC Control Register 2 : MISC2, Reg50h, R/W, default=00h.**

| Bit | Symbol | Description |
|---|---|---|
| 50.0 | HBRLEN0 | Host Burst Read Length control bit 0 : Together with HBRLEN1 define the length of the burst read access. |
| 50.1 | HBRLEN1 | Host Burst Read Length control bit 1 : Together with HBRLEN0 define the length of the burst read access.<br>HBRLEN1 HBRLEN0 burst length<br>0 0 x4<br>0 1 x1<br>1 0 x2<br>1 1 x4 |
| 50.2 | RUNTSIZE | Runt Frame Size Select bit : Default is 0, meaning the runt frame is defined as less than 64 bytes. Set to define the runt frame as less than 60 bytes. |
| 50.3 | DREQBCTRL | DREQB timing Control : Default is 0, meaning DREQB is deasserted after the data transfer. If set, DREQB deassertion is earlier than the end of the data transfer. See the timing diagram for details. |
| 50.4 | RINTSEL | Receive Interrupt timing Select : Default is 0, which asserts RI and REI at the end of the receive local DMA. If set, assert RI and REI at the end of the host receive DMA. It also defines the RXINTT's & RXINTC's counting timing. See the timing diagram for details. |
| 50.5 | ITPSEL | reserved for internal test probing select. |
| 50.6 | A11A8EN | Default=0, A11 to A8 are internally grounded. set this bit to enable A11 to A8 decoding. This bit is ignored if MIISEL = 1 in MII mode. |
| 50.7 | AUTORCVR | Auto RX Full Recovery: Default is reset meaning when RX buffer full and RX FIFO overflow happen at the same time, GMAC will stop receiving until host clear up RX FIFO and RX full condition. Set to enable GMAC to recover from such error automatically , the last packet with such error will be discarded in the packet memory and RX FIFO will be cleared at the end of current receiving, and then receiving is resumed for next packet. |

**Host Receive Packet Counter : HRPKTCNT, Reg53/52h, RO**

| Bit | Symbol | Description |
|---|---|---|
| 52.7-0 | HRPKTCNT[7:0] | Host Receive Packet Count [7:0] : Together with HRPKTCNT[15:8] forms a 16 bits counter. Cleared after a read access to this register. |
| 53.7-0 | HRPKTCNT[15:8] | Host Receive Packet Count [15:8] : Together with HRPKTCNT[7:0] forms a 16 bits counter. Counter is increment only at the beginning of a received packet's last host DMA cycle. A read access to this register will clear the counter to 0 right at the end of this read cycle. This counter records the total receive packet count since previous read access to this counter. |

**Host DMA Fragment Counter : FRAGCNT, Reg56/55/54h, RW**

| Bit | Symbol | Description |
|---|---|---|
| 54.7-0 | FRAGCNT[7:0] | Host DMA Fragment [23:0] : Used as a down counter to track word count in all packet memory read by the host. The largest count value can be programmed is 16MB, and is decrement by 2 at every word transferred for 16bit host bus or decrement by 4 at every word transferred for 32bit host bus from packet memory to host. When the remaining count value is less than current receive packet length then reg 9h. 0 bit ( FRAGI ) will be set , DREQB will be disabled and an interrupt to host bus will be issued if reg 8h.0 ( FRAGIM ) is also set by software. Initial counter value must be non-zero to enable this Fragment counter function with interrupt and DREQB control. When interrupt is asserted and DREQB is disabled, this counter must be re-programmed and write 1 to FRAGI bit to clear up interrupt flag in order to resume pending host DMA activities to the receive channel. |
| 55.7-0 | FRAGCNT[15:8] | |
| 56.7-0 | FRAGCNT[23:16] | |

## Descriptor structure

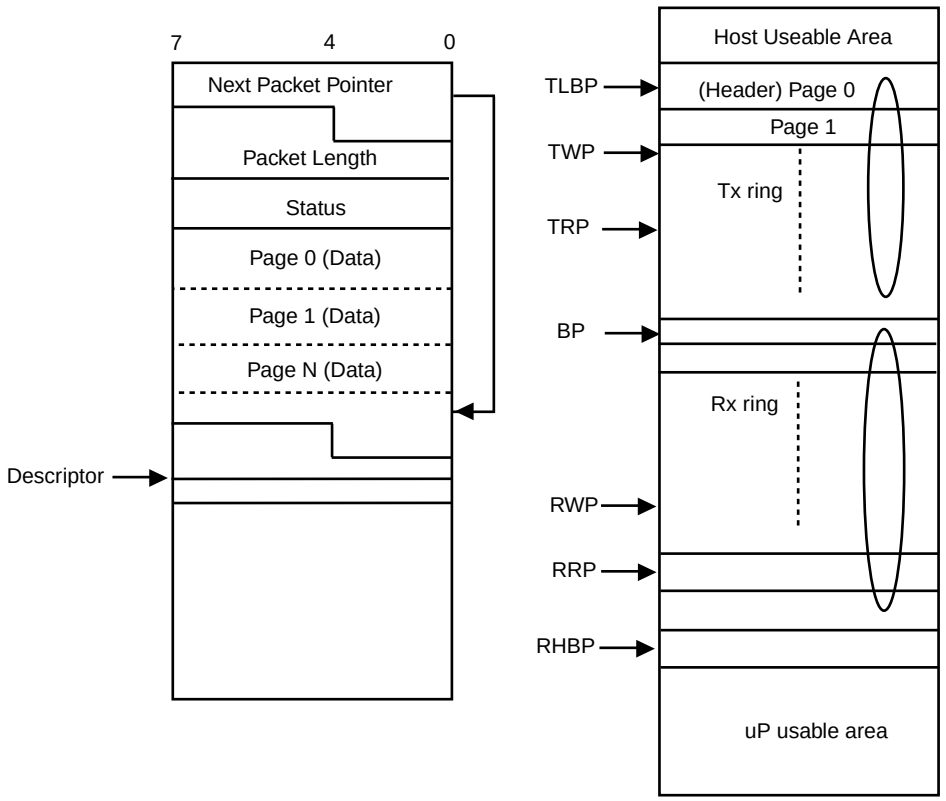



Figure 4.0 Packet Buffer Data Structures

## 4.0 Host Communication

GMAC and the device driver communicate through three data structures :

* On chip registers described in Chapter 3.
* Descriptors and data buffers resides in the packet memory.
* Direct data port with on the chip TX FIFO for the direct packet transmission.

GMAC moves received data frames to the receive buffer in the local packet memory and transmits data from the transmit buffers in the local packet memory. All the page pointers in the registers together with the descriptors acts as pointers to these buffers in the packet memory. Figure 4.0 depicts the general data structure of the packet memory and page pointers.

There are two data buffers inside the packet memory, i.e. the transmit buffer and the receive buffer. Packet memory is partitioned into pages. Each page contains exactly 256 bytes. A page pointer defined by registers acts as the base address of the corresponding page. By programming these page pointers, the size and the area of the transmit buffer and the receive buffer can be individually set to the desirable size and area.

The transmit and receive buffers must be contiguous and separated by the BP ( Boundary Page pointer ) defined in registers 0Ah and 0Bh. TLBP ( Transmit Low Boundary Pointer ) defines the start page of the transmit buffer. BP- 1 defines the end page of the transmit buffer. If the current transmit process exceeds the end of the BP- 1 page, it will be set to the start page pointed to by TLBP, thus forms a "ring buffer" that logically links the end page back to the start page of the transmit buffer.

The receive buffer has a similar structure as the transmit buffer. The start page of the receive buffer is pointed to by BP while the end page is pointed to by RHBP ( Receive High Boundary Page Pointer ). If the current receive process exceeds the end of the end page pointed to by RHBP, then it will be set to the start page pointed to by BP, thus forms a "ring buffer" that logically links the end page and the start page of the receive buffer.

A 1.6K bytes TX FIFO can also be used to send out a packet directly from the FIFO. The register port WRTXFIFOD ( 4Bh-48h ) can be used by the host to write the packet data directly into the TX FIFO. After moving one complete packet into the TX FIFO, the host can issue a command (called the TX FIFO send command) to send out the packet stored in the TX FIFO. This function can be used alternately with the other transmission method that uses the TX buffer ring.

All incoming and outgoing packets are stored in these buffers. A long packet may occupy multiple pages that are contiguous. The descriptor is located at the beginning of the first page of the packet. Normally there might be some free space left in the last page of a multiple-page packet which is called the fragment page. A new packet must start from an empty page. The free space inside those fragment pages can not be used.

### 4.1 Packet Transmission

GMAC supports two ways to prepare packet(s) for transmission. One way is the host can write a packet directly into the TX FIFO through an IO port and send the packet directly from the FIFO. This is called the direct FIFO mode. The other way is to write packet(s) into the TX buffer ring in the packet memory and activate the TX local DMA to send out packet(s). Using the direct FIFO mode can eliminate the TX local DMA completely, which will leave the packet memory's total bandwidth to the RX local DMA and the host. Therefore, receiving at the full line speed is more achievable this way. The disadvantage is that only one packet is prepared and sent out at a time. The next packet must wait until the current packet is sent out and the FIFO is empty before it can be moved into the TX FIFO. In another word, you can not issue the multiple packet transmission with a single command. But you still can prepare new packet(s) in the TX buffer ring while a packet in the direct FIFO mode is still active. Once the packet in the direct FIFO mode is finished, you can active the TX DMA right away.

The TX local DMA mode is used between GMAC and the packet memory during the transmission of the packet. TRP ( Transmit Read Page pointer ) is used by the local DMA to fetch the first page of the desired packet in the packet memory. When GMAC receives a TX DMA send command ( register 00h.ST1=0, ST0=1 ), data in the packet memory will be moved into the GMAC's transmit FIFO. GMAC will append preamble, sync and CRC fields during the actual transmission. The advantage of this mode is the multiple packets can be processed with a single command. New packet(s) to the packet memory can be prepared while the TX local DMA is active. Therefore, potential higher throughout of the TX channel can be achieved. The disadvantage is the packet memory bandwidth is now shared by the host, the TX channel and the RX channel. This means the bandwidth might not be enough for all three to run at their full speeds which may result in the TX FIFO underrun, or the RX FIFO overrun and slow host accesses, especially in a system where you only have an 8 bit packet memory.

It may be desirable to mix both the direct FIFO mode and the TX local DMA mode so that the bandwidth of the packet memory and the convenience of the concurrent processing of multiple packets can be compromised to achieve the best system performance. Cautions should be taken when you use the mixed mode. Do not write directly to the FIFO while the TX local DMA is active, because such write will interfere with whichever packet being transmitted in the FIFO. Do not activate the TX local DMA while the direct FIFO send has not been finished for the current packet transmission. Register 00h.ST1 and ST0 bits are both command and status, before the host issues any new packet send command (the TX DMA poll or the TX FIFO send ). Always read these two bits and make sure they are both 0, which indicate a transmit channel IDLE ( the FIFO is also empty ). The rule of the mixed modes is always activating one mode at a time. ST1 and ST0 must both be 0 before the other mode is used.

**Prior to the transmission in the direct FIFO mode**

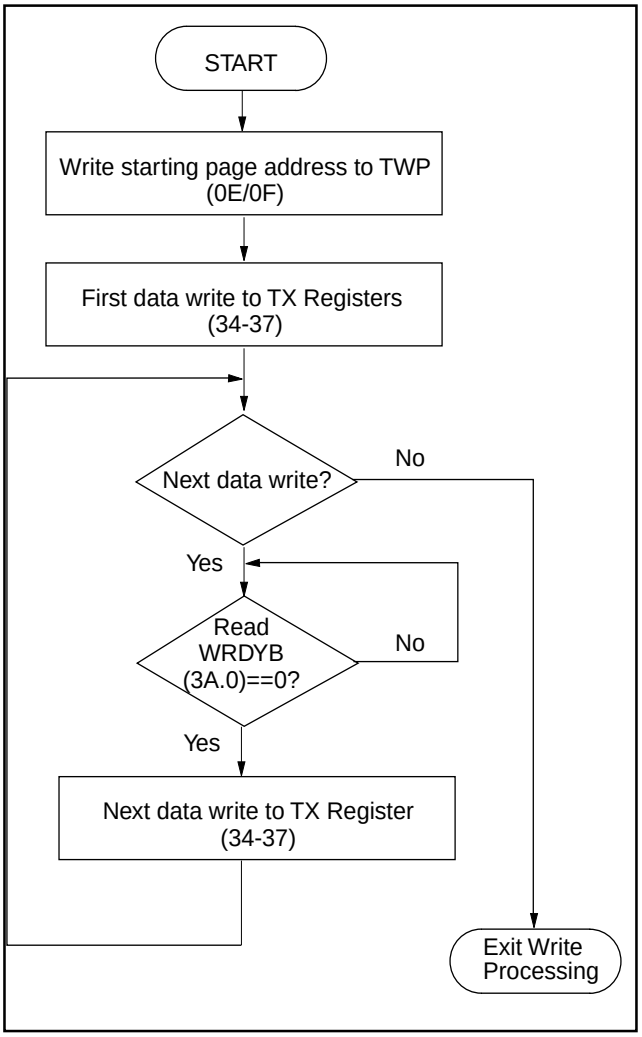
When ST1 and ST0 bits are both 0, the host can write a packet no longer than 1518 bytes through an IO port register located in 4Bh to 48h. It is called the "WRTXFIFOD" port. GMAC will record the byte count. Since the register WRTXFIFOD is a write only port, it can not be read. Before the entire packet is completely inside the FIFO, the host is allowed to do other operations except activating the TX local DMA. When TX byte count is not multiple of host bus width, TXFIFOCNT and TXFIFOCNTEN should be set. Issuing the TX DMA poll command before current direct FIFO write operations or the TX FIFO send completion will "corrupt" the current packet inside the TX FIFO. When the entire packet is in the FIFO, the host can issue ST1=1 and ST0=0 (the TX FIFO send command ). When this packet is sent out completely, the transmit status will be recorded in register 04h and both ST1 and ST0 are cleared to 0 to indicate the IDLE state.

**Prior to the transmission in the TX local DMA mode**

The transmit descriptor located at the beginning of the first page of the desired packet in the packet memory must be properly set by the device driver prior to a transmit command. By using TWP ( Transmit Write Page Pointer ) and the TWD data port , the device driver can fill up packet(s) in the transmit buffer ring. For the single packet transmission, the Next Packet Page Pointer field of the transmit descriptor should be equal to the TRP page pointer which links to the current packet itself. If multiple packets are to be transmitted, then the Next Packet Page Pointer field of the transmit descriptor should be set to the start page of the next packet. The Current Packet Length field ( in bytes ) is set to indicate the size of the current packet. Transmit Status bit 7 ( the OWN

bit ) of the descriptor needs to be set to 1 to indicate that the device driver has finished preparing the current packet. Then the packet can be transferred to GMAC for transmission. At this point, the TX DMA poll command can be issued by setting Reg00h.ST1=0, ST0=1 to activate the transmit operation. ST1 and ST0 bits will be cleared to 0 and TXDMA[3:0]=1h when the transmission is done.

During the process of filling up packet(s) in the transmit buffer ring, the current write address to the TX buffer ring is controlled by GMAC using TWP and TWPBC to form packet memory's address lines. TWP is updated by the driver only and TWP checked against TRP,BP,TLBP by both GMAC and the driver to maintain TX buffer ring's integrity. TWP serves as the start page of non-ready packet(s) which is still being prepared by the driver. The following flow chart shows the typical way of preparing a packet in the packet buffer. (for systems without the SRDY pin support).




**Conditions required to begin transmission**

1. Register 00h.ST1=0 and Reg00h.ST0=1 in the TX local DMA mode or register 00h.ST1=1 and ST0=0 in the direct FIFO mode
2. The interframe gap timer has timed out.
3. The TX FIFO is filled with a complete packet or is full.
4. If a collision has been detected and the backoff timer has expired.

After the packet starts to go out to the network, TTHD[1:0] will begin to affect the packet memory's arbitration if the FIFO needs more data from the packet memory( TTHD is not used in the direct FIFO mode ). In the TX local DMA mode, the advantage of the smaller threshold is to reduce the risk of a potential transmit FIFO underrun error for large packets beyond 1518 bytes. Such underrun error occurs when all the data in the FIFO is transmitted while the local DMA still has not filled in more data to be transmitted. Since the TX FIFO is large enough for the largest normal packet ( 1518 bytes ), the TTHD and FIFO underrun applies to packets larger than 1518 bytes in the TX local DMA mode. The larger the TTHD, the less aggressive the TX DMA is in the packet memory arbitration. Therefore the host and the RX DMA may have more bandwidth in the packet memory.

When this underrun occurs, the packet will be aborted and an interrupt will be asserted to get the host's attention. The FIFOEI ( register 09h bit 5 ) interrupt bit will be set when the underrun occurs and an interrupt to the host is asserted if the FIFOEIM bit (register 08h bit 5 ) is also set.

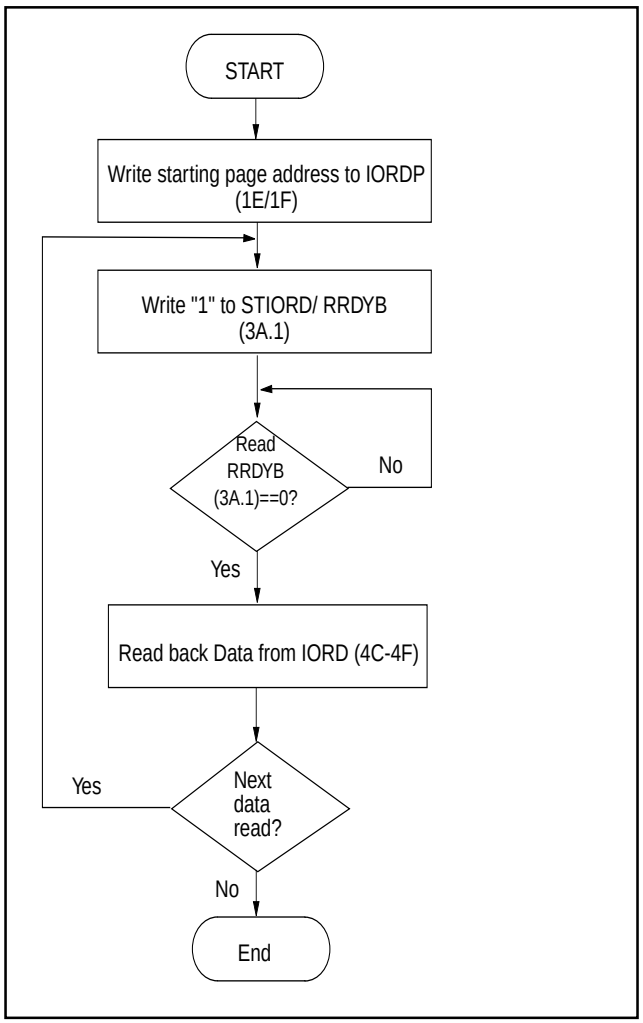
**Collision recovery**

During transmission, if a collision is detected before the first 64 bytes of the the packet has been transmitted, the FIFO will restore the necessary FIFO pointers to retransmit the same packet without fetching the transmitted data from the packet memory. An out-of-window collision is a collision occured after 64 bytes of data transmitted. If the out-of-window collision occurred, the packet will be aborted with an interrupt asserted. The OWC bit of the transmit descriptor is set and the device driver needs to resolve such a situation and reissue a transmit command so that GMAC can fetch the entire packet from the packet memory again for retransmission.

The collision count will be recorded for the current packet in register 04h.CC[3:0] bits. If all 15 retransmissions result in collisions, the transmission is aborted and the collision count CC[3:0]=1111 and an interrupt will be asserted and the TEI interrupt bit is set to indicate such an excessive collision error. If the TI interrupt bit is set, then the packet is successfully transmitted with the collision count=CC[3:0].

**After a single packet transmission**

When a packet(s) transmission is completed, register 00h.ST1 and ST0 are both cleared to 0 automatically by GMAC. Whenever the first packet is sent out, an interrupt is asserted for the host attention. The device driver can process this packet's status. In the TX local DMA mode, the first thing to check is making sure the OWN bit in the status field bit 7 is 0, which indicates that GMAC has completed the transmission of this packet and the status is valid. Or in the direct FIFO mode, check ST1 and ST0 for both 0, which indicates completion of the previous transmission. At this point, the device driver can proceed with the transmit status ( on the register or in the descriptor ) and other book keeping tasks. If host system does not support SRDY pin, the following flow chart provides a way to fetch transmit status of any transmitted packet in the packet memory in TX DMA mode. This is useful when multiple packets are transmitted in a single command and multiple transmit status needed to be checked.




For a successful transmission, an interrupt is caused by the interrupt register bit TI ( bit 2 of register 09h ) of the interrupt register IR, provided that the corresponding enable bit TIM ( bit 2 of register 08h ) of the interrupt enable register IMR is set. In case that an error occurred during the transmission, the interrupt register bit TEI will be set instead of TI. The register 09h bit 4 ( TEIM ) is the interrupt enable bit for TEI. Set TEIM will enable the TEI interrupt. The transmission error can be read from register 04h ( the LTPS register ) which records the transmit status of the last packet transmitted. If bit 7 ( TERR ) of register 04h is set, then TEI will be set as well. TERR is a logical OR of the underrun error( UF bit ), the out-of-window collision error ( OWC bit ), the carrier lost error ( CRSLOST bit ) and the excessive collision error ( CC[3:0]=1111 and TEI = 1).

The IORD port and the IORDP page pointer together can be used to access all the previous packet transmission status. Since the IORD port will read data from the packet memory, the SRDY pin must be used for possible wait states caused by the packet memory's arbitration. If the system application does not support the SRDY pin, then register 3A.1 ( STIORD/RRDYB ) can be used to read data from the IORD port in a handshake manner.

### Multiple packets transmission ( TX local DMA mode only )

If more packets are prepared in the packet memory and all transmit descriptors are set properly ( i.e. next packet page pointer, packet length, OWN bit = 1, etc), then a TX DMA poll command can be used to send out all these packets at once. As soon as the first packet transmission is done, an interrupt will be asserted to get the host attention. The device driver can serve this interrupt by processing all the packets that have the OWN bit set to zero in this multiple packets list in the packet memory. The device driver can "peek" the OWN bit of the next packet's descriptor to see if there are more packet(s) transmitted completely at that point. If the OWN bit of the next packet's descriptor is zero, then the device driver can proceed to the next packet after finishing the current packet. When all packets are transmitted successfully or aborted, register 00h. ST1 and ST0 bits are internally reset. This way, packets can be sent out in a burst with a single transmit command.

### Transmit packet assembly format in the packet memory

**For the 16 bit SRAM interface :**

| D15 D8 | D7 D0 |
|---|---|
| Descriptor Byte 1 | Descriptor Byte 0 |
| Descriptor Byte 3 | Descriptor Byte 2 |
| Destination Address Byte 1 | Destination Address Byte 0 |
| Destination Address Byte 3 | Destination Address Byte 2 |
| Destination Address Byte 5 | Destination Address Byte 4 |
| Source Address Byte 1 | Source Address Byte 0 |
| Source Address Byte 3 | Source Address Byte 2 |
| Source Address Byte 5 | Source Address Byte 4 |
| Type/Length byte 1 | Type/Length byte 0 |
| Data byte 1 | Data byte 0 |

**For the 8 bit SRAM interface :**

| D7 D0 |
|---|
| Descriptor Byte 0 |
| Descriptor Byte 1 |
| Descriptor Byte 2 |
| Descriptor Byte 3 |
| Destination Address Byte 0 |
| Destination Address Byte 1 |
| Destination Address Byte 2 |
| Destination Address Byte 3 |
| Destination Address Byte 4 |
| Destination Address Byte 5 |
| Source Address Byte 0 |
| Source Address Byte 1 |
| Source Address Byte 2 |
| Source Address Byte 3 |
| Source Address Byte 4 |
| Source Address Byte 5 |
| Type/Length byte 0 |
| Type/Length byte 1 |
| Data byte 0 |

**Transmit descriptor format**

There are 4 bytes in a descriptor structure for the transmit packet. The transmit descriptor is prepared by the device driver before transmitting the packet and is defined as follows :

| bit 7 | bit 0 |
|---|---|
| Next Packet Page Pointer ( bit 7-4 ) | Next Packet Page Pointer ( bit 3-0 ) |
| Packet Length ( bit 3-0 ) | Next Packet Page Pointer( bit 11-8 ) |
| Packet Length ( bit 11-8 ) | Packet Length ( bit 7-4 ) |
| Transmit Status ( bit 7-4 ) | Transmit Status ( bit 3-0 ) |

| Bit | Symbol | Description |
|---|---|---|
| 0 | CC0 | Collision Count Bit 0 : |
| 1 | CC1 | Collision Count Bit 1 : |
| 2 | CC2 | Collision Count Bit 2 : |
| 3 | CC3 | Collision Count Bit 3 : When CC[3:0] = 1111 and the TEI interrupt bit is set, it is called an excessive collision error which will abort the current packet. If the TI interrupt bit is set, CC[3:0] is the collision count and the packet is transmitted successfully. |
| 4 | CRSLOST | Carrier Sense Lost : The network carrier signal was lost at some point during the transmission or lost during the entire duration of the transmission. |
| 5 | UF | TX FIFO Underflow : The TX FIFO is exhausted before the TX DMA fills in more data for the transmission. |
| 6 | OWC | Out of Window Collision : A collision occurred after 64 bytes of data had been transmitted. This packet will be aborted. |
| 7 | OWN | Packet Buffer Ownership indicator:<br>1: indicates GMAC has access right to the current packet's buffer<br>0: indicates the host has access right to the current packet's buffer |

### 4.2 Packet Reception

The local DMA receive channel uses a receive buffer ring structure comprised of a series of contiguous fixed length 256-byte ( 128 word ) buffers for storage of received packets. The location of this receive buffer ring is programmed in two page pointers, the Boundary Page pointer and the Receive High Boundary Page pointer. Ethernet packets consist of a distribution of shorter link control packets and longer data packets, the 256-bytes buffer length provides a good compromise between different packet sizes to best utilize the memory. The receive buffer ring provides storage for back-to-back packets in a loaded network. The assignment of buffers for storing packets is managed by the GMAC's receive DMA logic. Three basic functions are provided by the receive DMA logic : linking receive buffers for long packets, recovery of buffers when a packet is rejected and recirculation of buffer pages that has been read by the host.

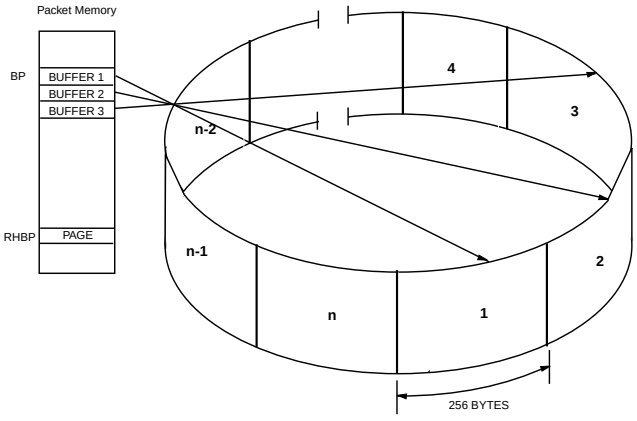



Figure 4.2.1 GMAC Receive Buffer Ring

**Initialization of the receive buffer ring**

Two static page pointer and two working page pointers control the operation of the receive buffer ring . These are the Boundary Page ( BP ) pointer, the Receive High Boundary Page ( RHBP ) pointer, the Receive Read Page ( RRP ) pointer and the Receive Write Page ( RWP ) pointer. The BP register points to the first buffer ( page ) of the receive buffer ring. RHBP points to the last page of the receive buffer ring. The RWP register points to the page in which the receive DMA logic is storing the incoming network data. The RRP register points to the page from which the host will read the next network data. A receive descriptor structure is located at the beginning of the start page of a received packet. If GMAC ever reaches the page pointed to by the RHBP register, it will link the page pointed to by the BP register as the next page, thus forms a ring buffer structure.

The size of the receive buffer ring is the total buffer space between the BP and the RHBP registers. An internal 8 bit byte counter ( RWPBC ) accounts for MA[7:0] will be used with the RWP register to form a physical memory address during the receive DMA write operation. This RWPBC counter will track the actual location within a page. After GMAC is initialized, BP, RWP and RRP should all point to the same page. These registers must be properly initialized before setting the register 00h SR ( bit 3 ) bit to 1 which enables the receive channel for the DMA function.

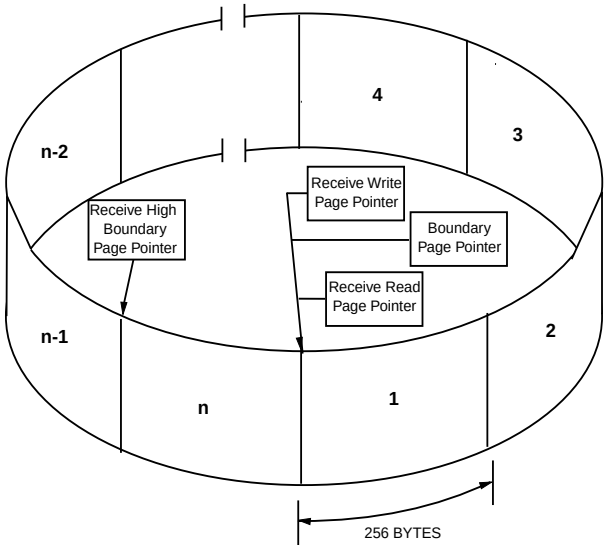



Figure 4.2.2 GMAC Receive Buffer Ring at Initialization

**Beginning of reception**

After all four page pointers are properly set by the device driver ( the host ), the register 00h SR bit can be set to enable the reception of packets. When the first packet arrives, the GMAC begins storing the packet at the location pointed to by the RWP register. 4 bytes ( descriptor ) are saved in this first page to store receive status corresponding to this packet. Whenever the internal byte counter reaches FFh indicating the end of a page, RWP will be increment by 1 automatically if more data of the packet is arriving.

The incoming network address is examined by GMAC to determine whether to accept or reject. If GMAC decides to reject the packet, then the receive FIFO will restore all spaces used by the rejected packet ( called restore ). If the packet should be accepted and the RX FIFO contains data up to a threshold level which can be programmed by RTHD[1:0] ( register 33h bits [3:2] ). The smaller the threshold, the faster the receive DMA logic removing data from FIFO, thus may has lower risk in running into a FIFO overrun situation. The disadvantage of a smaller threshold is that the host and the transmit channel may have less bandwidth of the packet memory. So RTHD threshold should be chosen to tune for the best network throughput. The default value of the receive FIFO threshold is 00, meaning 50% of the FIFO is filled up before any receive local DMA can start removing data out of the FIFO.

**Linking receive buffer pages**

If the packet exhausts the first 256-bytes buffer, the receive DMA logic will perform a forward link to the next buffer to store the remainder of the packet. For a maximum length packet , up to 6 buffers can be linked together. Buffers can not be skipped when linking. Therefore a packet will always be stored in contiguous buffers. Before the next page can be linked, the receive DMA logic does two comparisons.

The first comparison tests the equality between the content of the RWP register + 1 and the content of RRP register. If equal, the reception is aborted. This is called the receive buffer full error. Second comparison tests the equality between the RWP register and the RHBP register. If equal, the receive DMA will restore RWP to the first buffer in the receive buffer ring pointed to by the BP register if the receive buffer ring is not full.

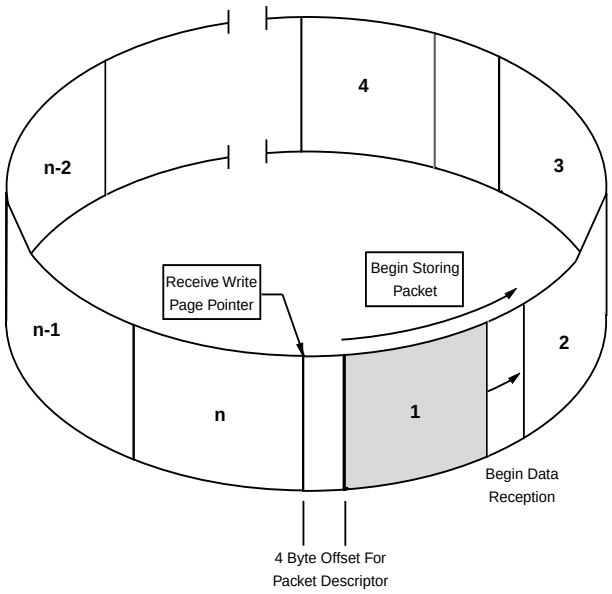



Figure 4.2.3 Received Packet Enters the Receive Buffer Pages

**Receive buffer ring full**

In a heavily loaded network which may cause overflow of the receive buffer ring, when the last available page is exhausted and more data needs to be stored for the current packet then the receive buffer ring is full but GMAC will continue receiving until RX FIFO is also overflow. At this point, GMAC will do the following actions :

1. Close current received packet with the FO bit ( bit 3 ) and the BF bit ( bit 0 ) of the receive descriptor being set if a minimum of one page is used by this packet.

2. An interrupt may be asserted if the RBFI ( register 09h bit 7 ) interrupt bit is set and the RBFIM bit ( register 08h bit 7 ) is also set.

3. If AUTORCVR is set, then the last packet with FO, BF error will be discarded from the packet memory and from RX FIFO as well and receiving is resumed for next packet.

4. If AUTORCVR is reset, then GMAC can not receive any more packet. All following packets will be lost and MPC ( Missed Packet Counter ), registers 07h and 06h, will be increment automatically. MPC can be reset by the device driver.

If device driver choose AUTORCVR = 0, the following procedure is suggested for the device driver to recover from such an error situation manually.

1. Issue the SR=0 ( NCRA register bit 3 ) which will stop RX channel to prevent new data from coming into RX FIFO.

2. Issue RX FIFORST to clean RX FIFO.

3. Remove all the received packets in the packet memory. When buffer ring is empty, RRP=RWP.

4. Clear all receive related interrupt flags and then set the SR bit=1 to resume the receive operation.

**Successful reception**

Based on the network address filtering modes set up by the device driver, GMAC will determine whether to receive a packet or to reject it. It either branches to a routine to store the packet or to another routine to reclaim the buffers used to store the packet. If a packet is successfully received, GMAC will store the receive status , the packet length and the next packet pointer in the receive descriptor located at the beginning of the first page of the packet and the status in the LRPS ( register 05h ) register. Note that the remaining bytes in the last page are discarded and reception of the next packet begins on the next empty 256-byte page boundary. The RWP is then set by GMAC to the next available page in the buffer ring.

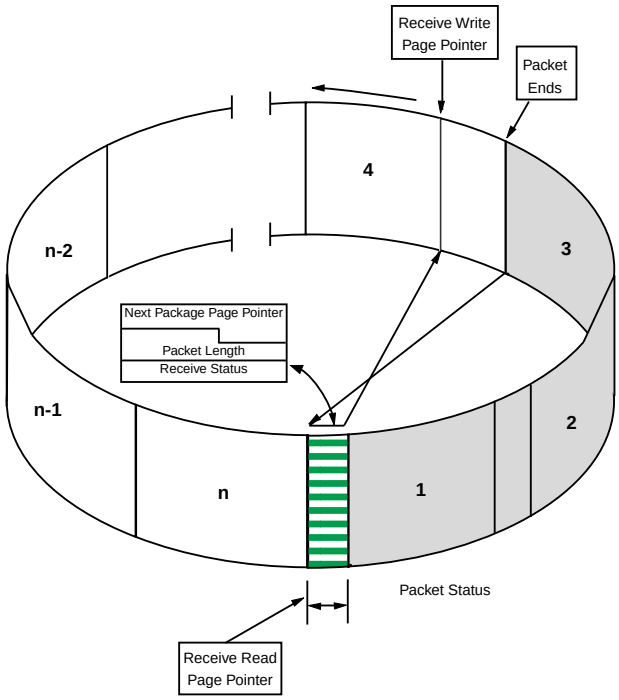



Figure 4.2.4 Termination Of Received Packet-Packet Accepted

**Rejected packets**

If the packet is a runt packet and the PB bit ( Pass Bad option, register 01h, bit 3 ) is 0, then it is rejected. The buffer previously used by this rejected packet is reclaimed by resetting the internal byte counter to zero automatically by GMAC. Packets with at least 64 or 60 bytes defined by register 50.2 ( RUNTSIZE ) are always received and stored regardless of the CRC error status.

**Removing packets from the buffer ring**

Packets are removed from the buffer ring inside the packet memory by the host through two ways, namely, host DMA and IO mode. The host DMA uses DACKB and DREQB signals to conduct read or multiple reads ( burst reads ) on the chip. The other way is so called IO mode read or burst reads to register 43h-40h of the chip. This 32 bit port is also called RRD data port. When DREQB = 0, the host can still do both read and write accesses to GMAC's internal registers.

DREQB is asserted by the chip whenever there is at least one receive packet inside the buffer ring and at least one burst transfer is ready inside the chip's on chip fast buffer. Host can issue DACKB or IO read at RRD port to read out the data whenever the DREQB = 0. The chip will keep track of the DMA byte count automatically and issue an interrupt at the end of host DMA depending on the set up of receive interrupt conditions.

The actual packet memory address contains two parts, the higher address lines consists of RRP register bit [11:0] and the lower address lines are provided by the RRPBC counter. By reading the descriptor, the device driver will know the size of the packet and it can move data up to the last page without updating the RRP register. The RRP register will be automatically updated by GMAC (if AUTOPUB bit=0) whenever a page is exhausted. GMAC also will properly link the RRP to the next page pointed to by the BP register if the RHBP page is exhausted. The device driver does have the right to "overwrite" the content of the RRP register at any time.

The configuration register GCA (32h) bit 5 is "AUTOPUB", when 0 meaning all page registers for the host side will be updated by GMAC automatically. The content of GCA can be loaded by GMAC from EEPROM automatically right after the system hardware reset. If AUTOPUB is 1, it means no automatic update of these host page registers ( RRP, TWP ). Default is 0 for the automatic host page registers update. So both the automatic and the manual RRP pointer updates are available for the device driver. The following is a suggested method for maintaining the receive buffer ring pointers :

1. At initialization, set up BP= RRP=RWP and RHBP to a higher memory page. At this point, the receive buffer is empty.
2. Setup a software address counter and a byte counter to keep track of the packet being removed from the packet memory to the host. After a packet is removed, the RRP is increment by GMAC so that RWP will not overwrite a page which is part of an unprocessed packet.
3. After a packet is stored in the receive buffer ring, GMAC may assert an interrupt.The device driver will start moving data beginning from the page pointed to by the RRP register. It reads the packet length and advanced the address counter the same as the DMA. Care should be taken when the RHBP page is exhausted or the buffer is full if the manual page pointer update is used .

**Possible junk data of burst transfer**

Burst read length can be programmed through register 50.1 and 50.0 bit. Length can be 1 , 2 or 4. It is possible to have extra junk bytes in the last burst transfer.

When H16_32=1 (16 bit host), regardless of burst length, all burst transfer will end at 8 bytes boundary. Therefore, possible junk bytes could be 1 byte to 7 bytes.

When H16_32=0 (32 bit host), regardless of burst length, all burst transfer will end at 16 bytes boundary. Therefore, possible junk bytes could be 1 byte to 15 bytes.

**Receive packet assembly format in the packet memory**

For the 16 bit SRAM interface :

| D15 D8 | D7 D0 |
|---|---|
| Descriptor Byte 1 | Descriptor Byte 0 |
| Descriptor Byte 3 | Descriptor Byte 2 |
| Destination Address Byte 1 | Destination Address Byte 0 |
| Destination Address Byte 3 | Destination Address Byte 2 |
| Destination Address Byte 5 | Destination Address Byte 4 |
| Source Address Byte 1 | Source Address Byte 0 |
| Source Address Byte 3 | Source Address Byte 2 |
| Source Address Byte 5 | Source Address Byte 4 |
| Type/Length byte 1 | Type/Length byte 0 |
| Data byte 1 | Data byte 0 |

**For the 8 bit SRAM interface :**

| D7 D0 |
|---|
| Descriptor Byte 0 |
| Descriptor Byte 1 |
| Descriptor Byte 2 |
| Descriptor Byte 3 |
| Destination Address Byte 0 |
| Destination Address Byte 1 |
| Destination Address Byte 2 |
| Destination Address Byte 3 |
| Destination Address Byte 4 |
| Destination Address Byte 5 |
| Source Address Byte 0 |
| Source Address Byte 1 |
| Source Address Byte 2 |
| Source Address Byte 3 |
| Source Address Byte 4 |
| Source Address Byte 5 |
| Type/Length byte 0 |
| Type/Length byte 1 |
| Data byte 0 |

**Receive status in the descriptor**

Notes : This staus byte of last received packet is also copied to register 5 ( LRPS ).

| bit # | Symbol | Description |
|---|---|---|
| 0 | BF | RX Packet Buffer Full Error : 1 indicates the RX packet buffer is full. |
| 1 | CRC | CRC error : caused by the corrupted data or dribble byte (s). |
| 2 | FAE | Frame Alignment Error : Dribble nibble (s). An FAE error might not cause a CRC error (e.g. only a dribble nibble is detected by GMAC). An FAE error will not set the RERR bit. |
| 3 | FO | FIFO Overrun |
| 4 | RW | Receive Watchdog : Set to indicate the frame length exceeds 2048 bytes. |
| 5 | MF | Multicast Frame address : Set to indicate the current frame has multicast address. |
| 6 | RF | Runt Frame : Set to indicate a frame length less than 64 or 60 bytes as defined by register 50.2 ( RUNTSIZE) , only meaningful when Reg00h.4 (PB bit) is set. |
| 7 | RERR | Receive Error : a logical OR of CRC, FO, BF, RW and RF bits. |

There are 4 bytes in a descriptor structure for both the transmit and the receive packets.The receive descriptor is prepared by GMAC and is defined as follows :

| bit 7 | bit 0 |
|---|---|
| Next Packet Page Pointer ( bit 7-4 ) | Next Packet Page Pointer ( bit 3-0 ) |
| Packet Length ( bit 3-0 ) | Next Packet Page Pointer( bit 11-8 ) |
| Packet Length ( bit 11-8 ) | Packet Length ( bit 7-4 ) |
| Receive Status ( bit 7-4 ) | Receive Status ( bit 3-0 ) |

### 4.3 Packet Structure and 802.3 conformance

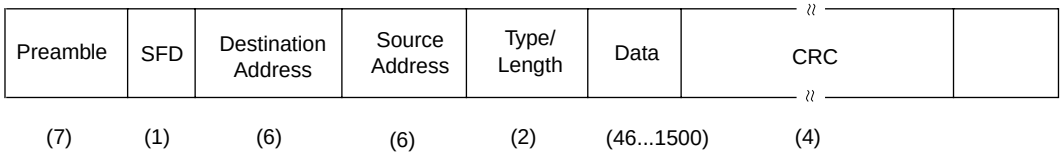
The network speed may be 10 MBPS or 100 MBPS. Further more, GMAC supports the full duplex mode where the transmit and the receive processes are running independently. A typical Ethernet frame structure is shown below.

**Ethernet and IEEE 802.3 Frames**

An Ethernet frame format consists of the following:

| Field | Description |
|---|---|
| Preamble | A 7-byte field of 56 alternating 1s and 0s, beginning with a 0. |
| SFD | Start Frame Delimiter. A 1-byte field that contains the value 10101011; the MSB is transmitted and received first. |
| Destination | A 6-byte field that contains the specific station address, the broadcast address, or a multicast address where this frame is directed. |
| Source | A 6-byte field that contains the specific station address where this frame was sent from. |
| Type/Length | A 2-byte field that indicates whether the frame is in IEEE 802.3 format or Ethernet format. A field greater than 1500 is interpreted as a type field, which defines the type of protocol of the frame. A field smaller than or equal to 1500 is interpreted as a length field, which indicates the No. of data bytes in the frame. |
| Data | A data field consists of 46 to 1500 bytes that is fully transparent. Shorter than 46 bytes is allowed. |
| CRC | A frame check sequence is a 32-bit cyclic redundancy check(CRC) value that is computed as a function of the destination address field, source address field, type field and data field. The FCS is appended to each transmitted frame, and used at reception to determine if the receive frame is valid. The figure shows the Ethernet frame format. |

Ethernet Frame Format




*Numbers in parentheses indicate field length in bytes.

The CRC polynomial, as specified in the Ethernet specification, is as follows:

$$FCS(X) = X^{31} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X^1 + 1$$

The 32 bits of the CRC value are placed in the FCS field so that the $X^{31}$ term is the right-most bit of the first octet, and the $X^0$ term is the left-most bit of the last octet. The bits of the CRC are transmitted in the order $X^{31}, X^{30}, \ldots X^1, X^0$.

### 4.4 Network Address Filtering

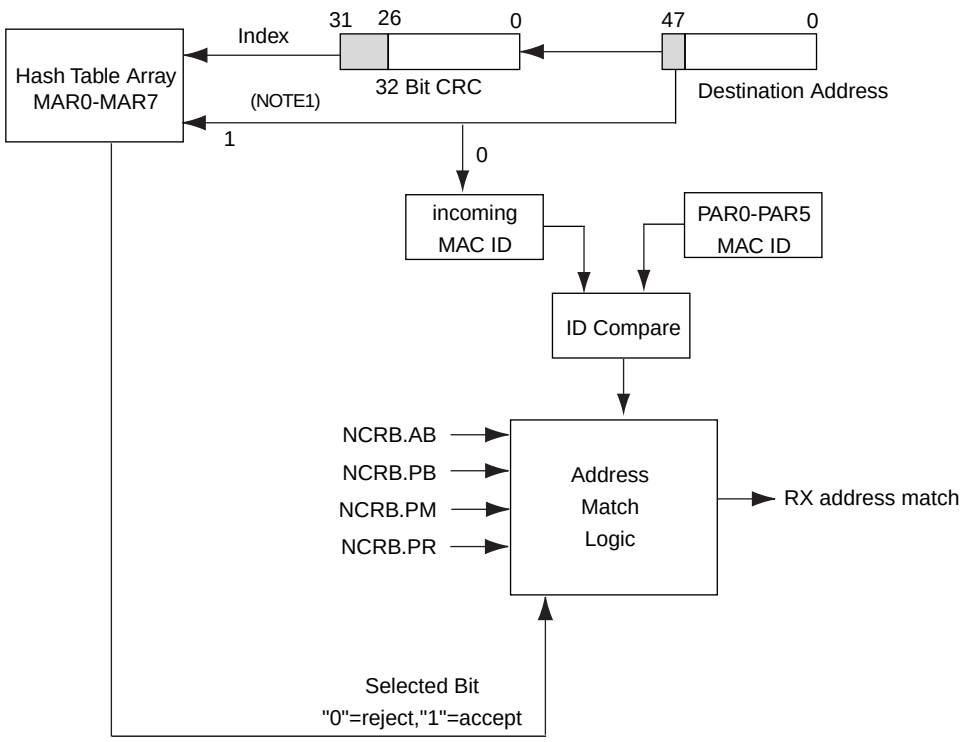
The first bit of the destination address signifies whether it is a physical address or a multicast address. The receive MAC filters the frame based on the address filtering option described below. Register 01h ( NCRB ) bit 0 is PR ( Promiscuous mode ) and bit 2 is PM ( Pass Multicast ). They are used to control the desired address filtering options.

Possible Address Filtering Options ( all independent of each other )

| Option | Description |
|---|---|
| 1 | One physical address perfect filtering , always enabled. |
| 2 | Unlimited multicast addresses imperfect filtering using the hash table. |
| 3 | Pass all multicast addresses. |
| 4 | Promiscuous Ethernet reception. When set, all valid frames are received. |
| 5 | Length field redefined as to be match against all broadcast packets. If matched, this broadcast packet is received. |

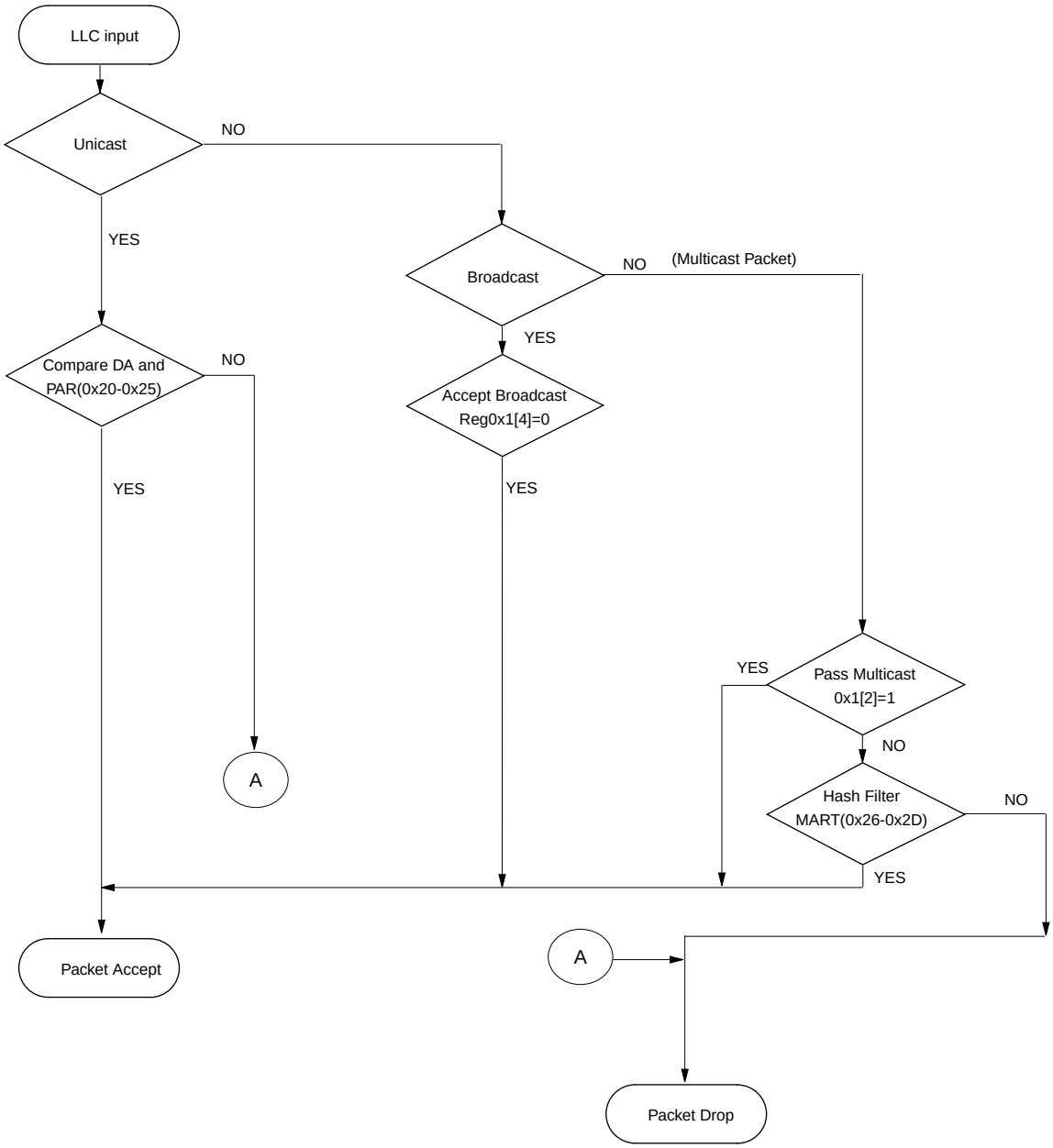
If the frame address passes the network address filter, the receive MAC removes the preamble and delivers the frame to the host processor memory. However, if the address does not pass the filter when mismatch is recognized, the receive MAC terminates this reception.

**GMAC Network Address Filtering**

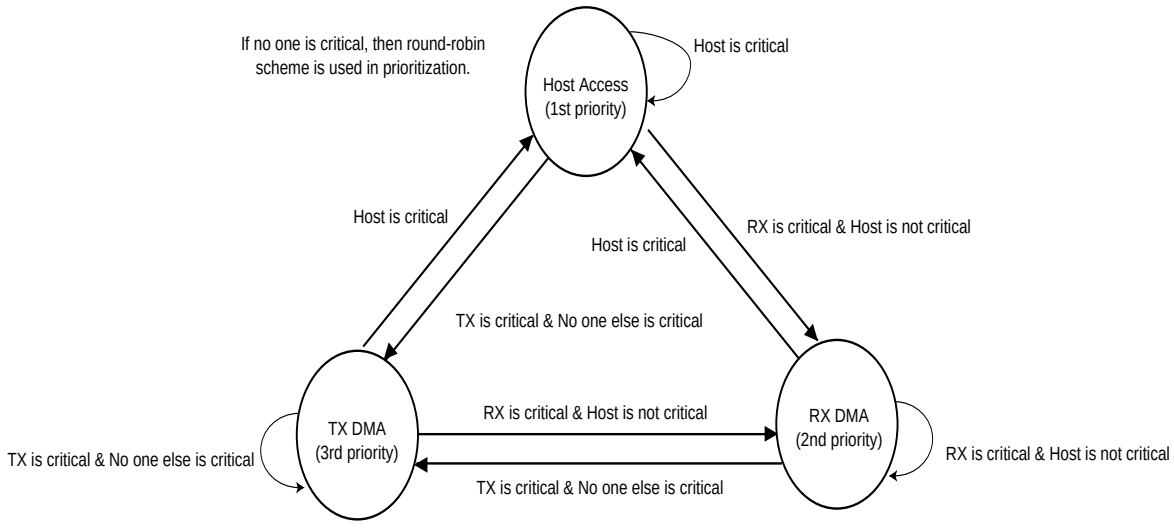



(NOTE1) Broadcast packet is not filtered by hash table array.

## GMAC's Network Address Filtering Flow Chart



## 5.0 Host/Local DMAs and the packet memory bus arbitration




Packet Memory Bus Arbitration State Diagram

**Rules of the packet memory access prioritization**

Rule 1: The TX local DMA is said to be "critical" if the TX FIFO counter falls below the TTHD level.
If the TX packet is in the "stored and forward" mode (TTHD[1:0]=11 ), the TX local DMA is never critical.

Rule 2 : The RX local DMA is said to be "critical" if the RX FIFO counter rises above the RTHD level.

Rule 3 : The host access is said to be "critical" if the DINTVAL timer is timed out.

Rule 4 : If all three accesses are critical, the host has the 1st priority. The RX local DMA has the 2nd priority and the TX local DMA has the last priority. If no one is critical, round-robin is used.

### 5.1 Host Accesses to the Packet Memory

**Host Burst Read**

Receive packet is removed by host through a high speed burst read buffer which is 32 bits x 4 or 16 bits x 4 depending on H16_32 pin. The Burst Read buffer can be accessed by two methods : DACKB and DREQB based protocol or IO based access ( RRD port ) to registers located at 43h-40h. Before any packet buffer read can be issued, the RX buffer must be initialized with proper page pointers set up at appropriate locations. Any read access to the Burst Read buffer, using DACKB/DREQB protocol or through IO register 43h-40h, will get data from the current location within the receive buffer ring pointed to by the RRP page pointer and the RRPBC byte counter. When the RRPBC reaches the boundary of a page, it will increment the RRP page pointer by 1 and reset RRPBC itself automatically. Of course, the software can always overwrite the RRP pointer. This write will also reset the RRPBC counter.

A burst read access can be issued only when either the DREQB pin is asserted low or the register 3A.2 bit ( DREQB status bit ) is low which indicates 4 consecutive data transfers are ready inside the GMAC's Burst Read Buffer for a burst read transfer. The host can read the RRD data port or issue DACKB in any length less than or equal to 4 reads. When the host have finished reading the entire packet and there might be junk data in the Burst Read Buffer, the host can issue a RRP page pointer update (e.g. RRP+1), which will automatically reset the Burst Read Buffer and the related control circuit. After the RRP page pointer update, the Burst Read buffer will fetch 4 consecutive double word from the new page if there are more data available.

Note : The current read physical location in the packet memory = the RRP pointer ( mapped to MA[19:8] ) cascaded with the RRPBC byte counter ( mapped to MA[7:0] ).

**Host Write**

The TWD data port ( offset 37H - 34H ) is used for write accesses to the transmit buffer ring. The current write position within the transmit buffer ring is pointed to by the TWP page pointer and the TWPBC byte counter. Since a write access to the transmit buffer ring involves the packet memory arbitration, the SRDY pin or the register 3A.0 ( WRDYB ) bit can be used for the wait state purpose. For system that supports the SRDY pin for wait states, a write to the TWD port can be issued at any time. This write will be treated as the top priority in the packet memory's arbitration. If no SRDY pin is supported in the system, inquire the register 3A.0 bit ( WRDYB ) for 0 to see if a new write can be issued. Otherwise, if WRDYB is 1 which means the previous write to TWD is still pending inside GMAC, a new write must not be issued. When the TWPBC counter reaches the boundary of a page, it will increment the TWP page pointer and reset the TWPBC byte counter automatically. Of course, software can always overwrite the TWP pointer which also reset the internal TWPBC byte counter.

Note : The current write physical location in the packet memory = the TWP pointer ( mapped to MA[19:8] ) cascaded with the TWPBC byte counter ( mapped to MA[7:0] ).

A write cycle is completed by the assertion of the SRDY signal high to indicate that GMAC has secured the write data. Or reading the register 3A.0 bit ( WRDYB ) for 0 which indicates that the previous write was done and a new write can be issued to GMAC. No burst is supported for any write access. A write access is independent of the status of the DREQB pin or the DREQB register bit. Due to the arbitration for the packet memory access, a write cycle ( without first reading a 0 from the WRDYB bit ) may encounter some "Wait state" which delays the assertion of SRDY for certain time. In any case, Bus Integrity Check Timer ( BICT ) can be pre-programmed to "terminate" any write cycle that runs over BICT time-out period. Such a time-out can both generate an interrupt to the software and flash LED0 and LED1 at identical low visible frequency to resolve a potential bus hang, bus dead lock problem.

### 5.2 Local DMA

**Receive FIFO threshold of the Receive DMA**

The receive FIFO threshold is defined by register 33h bit [3:2] (RTHD[1:0]). It is used to control the aggressiveness of the receive DMA request in the packet memory bus arbitration. For example, the default value of RTHD=1/2 depth of the receive FIFO means whenever the contents of the FIFO are over 1/2 of the FIFO space, it becomes "critical" since the FIFO may soon be full or overrun. When the receive FIFO is "critical", the receive DMA will have higher priority over the transmit DMA (regardless of whether the transmit FIFO is critical or not). If the FIFO is not over the RTHD level, it is not critical. The transmit DMA may have equal priority as the receive DMA or higher priority over the receive DMA if the transmit FIFO is critical. The larger the receive threshold, the less aggressive the receive DMA because it takes more time for the receive DMA to become critical. It also presents a higher risk to become FIFO full or to overrun the FIFO space. The smaller the RTHD, the more aggressive the receive DMA is and less risk in running into a FIFO full condition, but it also blocks other accesses from the host and the transmit DMA. Since the packet memory bandwidth is shared by the host, the transmit DMA and the receive DMA, "tuning" the RTHD threshold may be necessary for the best network/system throughput.

**Receive DMA**

The receive DMA normally has higher priority over the host and the transmit DMA. This is due to the receive data can not be reproduced locally. Therefore it is more urgent than others. The physical address of the receive DMA is formed by cascading a page address RWP register and the RWPBC counter for the receive DMA. RWP [11:0] is mapped to MA[19:8] while the RWPBC counter is mapped to MA[7:0]. Thus a 20 bit MA address is derived. RWP will be automatically updated by GMAC whenever a page is exhausted. If RHBP is reached, GMAC will set RWP as BP if the BP page is available.

**Transmit FIFO threshold of the transmit DMA**

The transmit FIFO threshold is defined by Register 33h bits [1:0] (TTHD [1:0]). TTHD is used to control the aggressiveness of the transmit DMA request for the packet longer than 1518 bytes in the packet memory bus arbitration. For example, the default value of TTHD=1/2 depth of the transmit FIFO means whenever the content of FIFO falls below 1/2 of the FIFO space, the transmit DMA will have higher prority over the receive DMA if the receive FIFO is not critical. If the transmit FIFO is over the TTHD level, then transmit may have equal priority as receive DMA or lower priority to the receive DMA if the receive FIFO is critical. The larger the TTHD threshold, the more aggressive the transmit DMA and it takes more time for the transmit DMA to become critical of running empty. The small TTHD will result in less aggressive transmit DMA but then it is also more critical of running the FIFO empty (underrun error). Since the packet memory bandwidth is shared by the host, the transmit DMA and receive DMA, "tuning" TTHD may be necessary for the best network/system throughput.

**Transmit DMA**

Transmit DMA normally has higher priority over the host but lower than the receive DMA. The physical address of receive DMA is formed by cascading a page address RWP register and the RWPBC counter for the receive DMA. RWP [11:0] is mapped to MA[19:8] while the RWPBC counter is mapped to MA[7:0]. Thus a 20 bit MA address is derived. RWP will be automatically updated by GMAC whenever a page is exhausted. If RHBP is reached, GMAC will link BP as the next available page into RWP if the BP page is free.

### 5.3 Receive interrupt

Normally the interrupt will be asserted after a packet is received. Either RI or REI will be set to indicate such an event. Sometimes, it is desirable not to report every single reception using the interrupt. GMAC has incorporated a receive packet counter and an interrupt timer ( RXINTT) to control the receive interrupt condition. By these two logic, we can issue the receive interrupt based on the receive packet count or the RXINTT time out, whichever comes first. So the receive interrupt logic can be expressed as follows:

Assert RI ( or REI ) interrupt if ( RXINTC is reached ) or ( RXINTT has timed out )

Receive Interrupt Timer : Register 15h and 14h forms a 16 bit timer running at 25Mhz. Default is 0000h, meaning no time-out is used on the RI or REI interrupt assertion. Reg15h.7 is the RXINTT.15 bit and Reg14h.0 is the RXINTT.0 bit. Any non-zero value enables the time out function. The possible time-out period ranges from 40ns to 2621 us. The RXINTT timer will be started after the last packet ( within the RXINTC range ) is transfered to the packet memory (RINTSEL=0) or the host memory (RINTSEL=1) and the timer will be reset when the interrupt is generated. When the received packet count has not reached the RXINTC [1:0] before the RXINTT time-out, an interrupt will be generated by the RXINTT time-out alone.

Receive Interrupt Counter : Register 01h bit 7 and bit 6 define the number of packets received before the receive interrupt RI or REI can be asserted. This function is independent of the RXINTT timer's ( Reg.15h/14h ) time-out. Whenever either a time-out or a packet count is reached, a receive interrupt will be generated. Default is 00h after reset, meaning the normal receive interrupt operation which asserts RI or REI after a single packet received and no RXINTT timer is used. Non-zero value in these two bits will enable this special receive interrupt operation.

| RXINTC1 | RXINTC0 | Interrupt received packet count |
|---|---|---|
| 0 | 0 | 1 ( default ) |
| 0 | 1 | 2 |
| 1 | 0 | 4 |
| 1 | 1 | 8 |

### 5.4 Bus integrity check

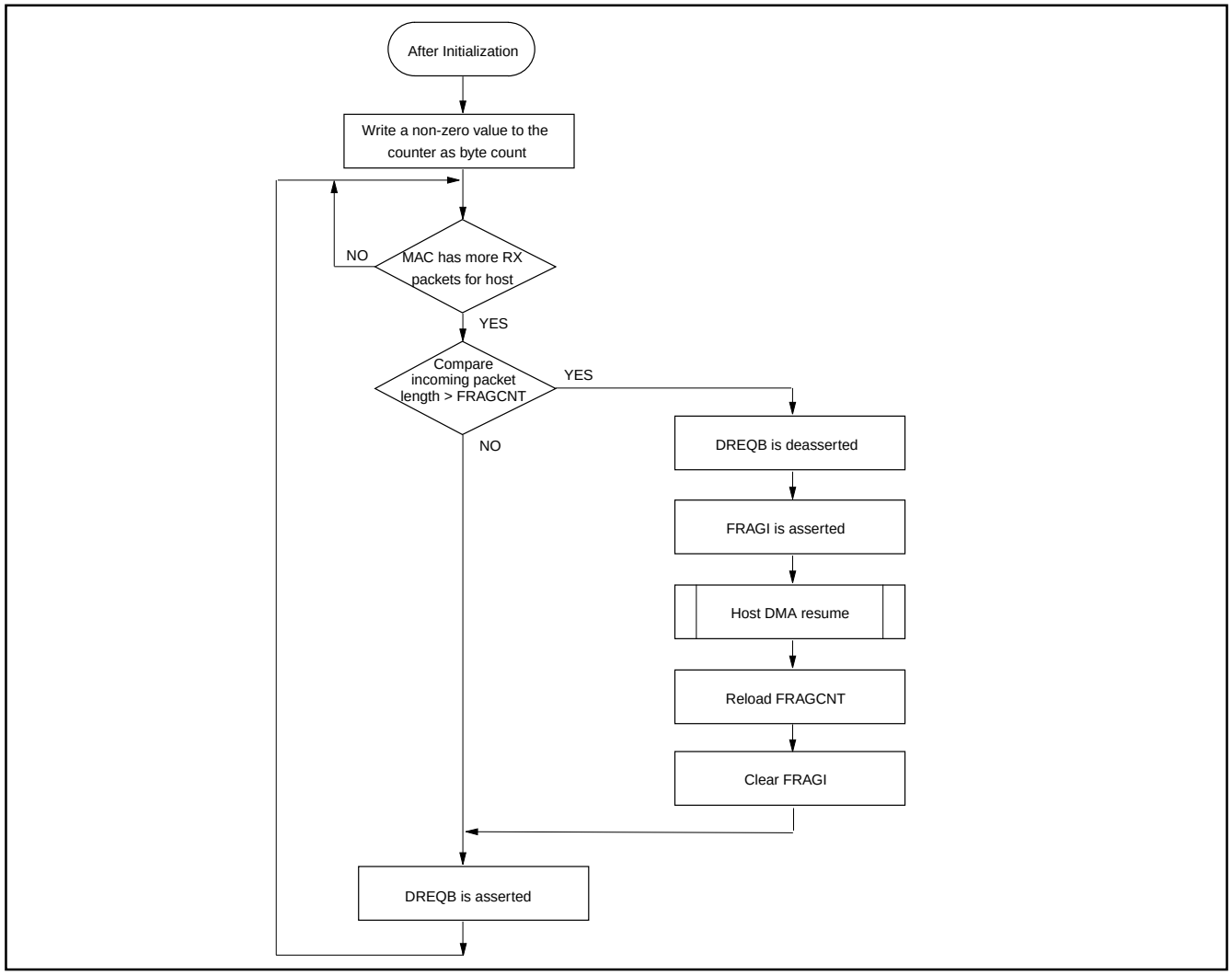
Sometimes, it is necessary to have a hardware checking mechanism which constantly monitoring the host activity for any abnormal situation.The host bus hang problem is sometimes seen in many systems. GMAC provides a monitoring logic that watches out for any abnormally long cycle on the host interface. A timer called the BICT ( register 1Dh ) timer is used, which is an 8 bit counter running at 25MHz or 40ns per clock. Default is 00h, meaning no bus integrity check is enabled. Value in this counter other than zero will enable the bus integrity check. Any bus cycle that longer than the time-out period defined in this timer will cause termination of the current bus cycle so that this abnormal bus hang and bus dead lock can be recovered. The BUSEI Interrupt ( register 09h bit 6 ) will be issued in this case. The possible time-out period ranges from 40ns to a maximum of 10.24us. As soon as a cycle is being processed by GMAC, this timer is started and the counter is reset when the cycle is normally finished before the time out.

### 5.5 Host Receive DMA Fragment Counter

In order to allow host to predict an insufficient host buffer problem before the actual host DMA takes place. The chip provide a fragment counter which can be used to "down count" the host DMA byte length and automatically compare the content to the length of the next receive packet. If the length fo the next receive packet is larger than the content of this counter then DREQB will be disabled temporarily until the count is programmed a new value which is larger than the length of next receive packet.

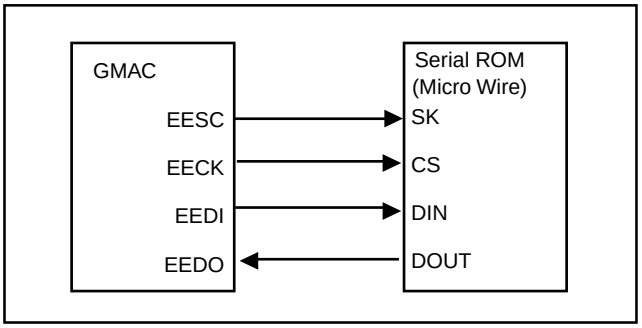
Typical application is that host set the initial counter value to indicate the amount of free host buffer for receive packets. When host buffer has been filled with packets and remaining free buffer might be smaller than the length of next receive packet then the chip can interrupt the host, if register 8.0 FRAGIM bit is set. Register 9.0 FRAGI will be set after host DMA of current packet is finished to indicate this interrupt and DMA is temporarily disabled so that host can allocate more free buffer to prevent "fragment" in the host buffer. Register 54h, 55h and 56h are defined as fragment counter which are all 0 after reset. When the counter is 0, this fragment counter logic is disabled, no down counting or interrupt will be valid.

**Flow Chart of Fragment Counter Programming**



## 6.0 Serial ROM ( EEPROM ) Interface

### Serial ROM Connection




EEDO - Serial ROM (EEPROM) Data Out = Register 1Ch, bit 3
EEDI - Serial ROM (EEPROM) Data In = Register1Ch, bit2
EECK - Serial ROM (EEPROM) Serial Clock = register 1Ch, bit 1
EECS - Serial ROM (EEPROM) Chip Select = register 1Ch, bit 0
EESEL - must be set to enable the EEPROM access by register 1Ch, bit 4

### Software Programming Interface

A read operation consists of three phases :
1. Command phase - 3 bits ( binary code of "110")
2. Address phase - 6 bits for 256- to 1K-bit ROMs ( C46/C66 pin is high), 8 bits for 2K- to 4K-bit ROMs ( C46/C66 is forced low )
3. Data phase - 16 bits for all type of EEPROMs.

These phases are generated through a sequence of writes to 1Ch. In certain action, the driver must wait until the minimum timing requirement for the serial ROM operation is met in order to advance to the next action.

The software sequence is available in the C source code from MXIC.

A typical read cycle can look like this(EESEL bit is set )

Write register 1Ch 10H ( >= 30ns )

Write register 1Ch 11H ( >= 50ns )
Write register 1Ch 13H ( >= 250ns )
Write register 1Ch 11H ( >= 100ns )

Write register 1Ch 15H ( >= 150ns )
Write register 1Ch 17H ( >= 250ns )
Write register 1Ch 15H ( >= 250ns )
Write register 1Ch 17H ( >= 250ns )
Write register 1Ch 15H ( >= 100 ns )
Write register 1Ch 11H ( >= 150 ns )
Write register 1Ch 13H ( >= 250 ns )
Write register 1Ch 11H ( >= 100ns )

Write register 1Ch 00H ( >= 150 ns )
Write register 1Ch 00H ( >= 250 ns )
Write register 1Ch 00H ( >= 100ns )

Write register 1Ch 03H ( >= 100ns )
Read register 1Ch.3 = DX ( >= 150ns )
Write register 1Ch 01H ( >= 250ns )
Write register 1Ch 00H ( >= 100ns )
END

A Write operation consist of three phases :
1. Command phase - 3 bits ( binary code of "110" )
2. Address phase - 6 bits for 256- to 1K-bit ROMs, 8 bits for 2K- to 4K-bit ROMs.
3. Data phase - 16 bits.

These phases are generated through a sequence of writes to 1Ch. In certain action, the driver must wait until the minimum timing requirement for the serial ROM operation is met in order to advance to the next action. A typical driver sequence can look like this

Write register 1Ch 00H ( >= 30ns )

Write register 1Ch 01H ( >= 50ns )
Write register 1Ch 03H ( >= 250ns )
Write register 1Ch 01H ( >= 100ns )

Write register 1Ch 05H ( >= 150ns )

Write register 1Ch 07H ( >= 250ns )
Write register 1Ch 05H ( >= 100ns )

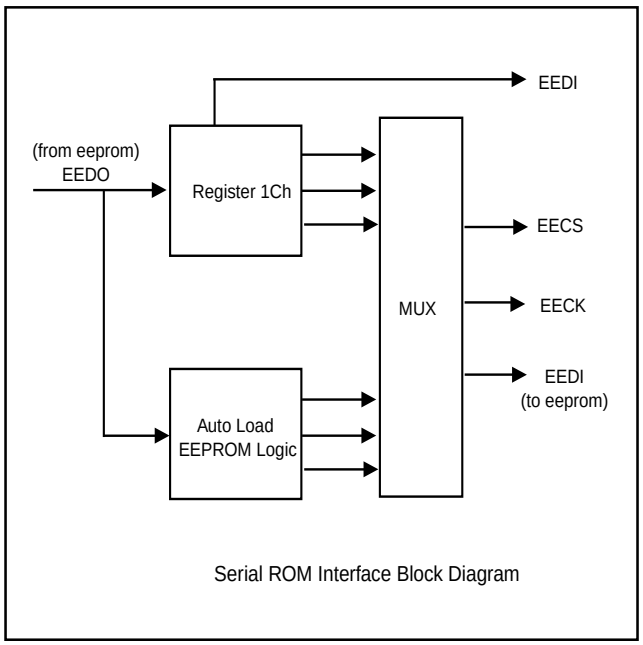
Write register 1Ch 01H ( >= 150ns )
Write register 1Ch 03H ( >= 250 ns )
Write register 1Ch 01H ( >= 100 ns )
Write register 1Ch 05H ( >= 150 ns )
Write register 1Ch 07H ( >= 250 ns )
Write register 1Ch 05H ( >= 100ns )

Write register 1Ch 00H ( >= 150 ns )
Write register 1Ch 00H ( >= 250 ns )
Write register 1Ch 00H ( >= 100ns )

Write register 1Ch 03H ( >= 150ns )
Write register 1Ch 0XH ( >= 250ns )
Write register 1Ch 0XH ( >= 100ns )

Write register 1Ch 00H ( >= 250ns )
Write register 1Ch 01H ( >= 250ns )

*Read register 1Ch.3
if register 1Ch.3 = 1 then go on
Write register 1Ch 00H ( >= 250ns )
else
Wait 1 ms then go to *Read register 1Ch.3
END




Serial ROM Interface Block Diagram

**Autoload Function**

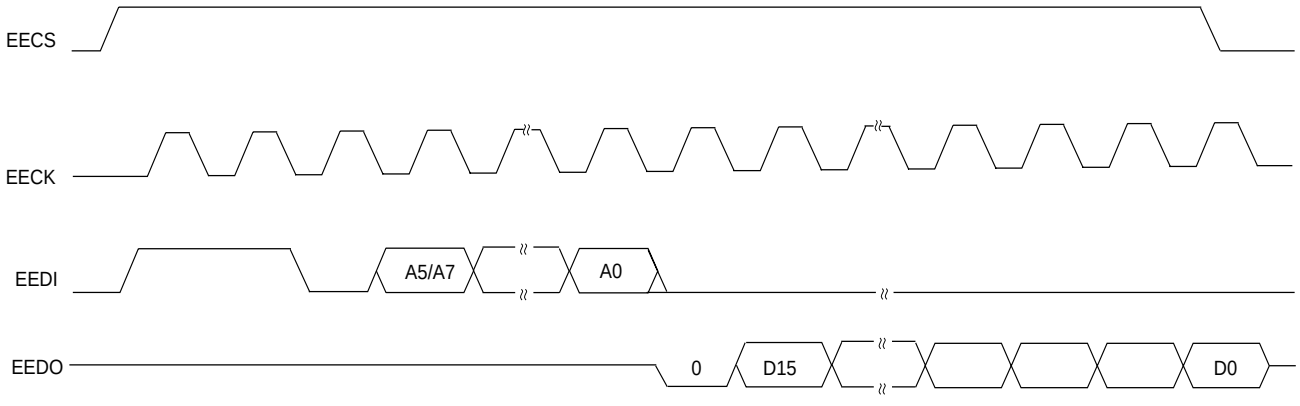
The Autoload Function is executed only once after the hardware reset pin RSTB from low to high. At that time the Serial ROM interface is driven by the internal circuit to load the data of the Serial ROM.

**EEPROM Content ( suggested )**

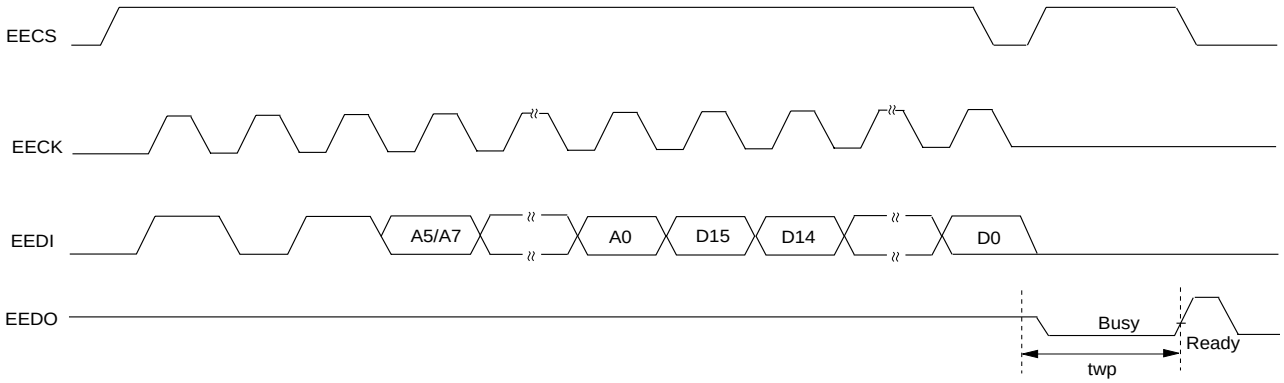
| Location | Content |
|---|---|
| 00H | Physical Address Byte 0 : PAR[7:0] ( MSB ) |
| 01H | Physical Address Byte 1: PAR[15:8] |
| 02H | Physical Address Byte 2 : PAR[23:16] |
| 03H | Physical Address Byte 3 : PAR[31:24] |
| 04H | Physical Address Byte 4 : PAR[39:32] |
| 05H | Physical Address Byte 5 : PAR[47:40] |
| 06H | GMAC Configuration A Register : GCA[7:0]<br>bit 0 : BPSCRM<br>bit 1 : PBW<br>bit 2 : SLOWSRAM<br>bit 3 : ARXERRB<br>bit 4 : MIISEL<br>bit 5 : AUTOPUB<br>bit 6 : TXFIFOCNTEN<br>bit 7 : RESERVED |
| 07H | reserved |
| 08H-END | Reserved for Software application |

## 6.1 On-Chip Transceiver vs MII Interface

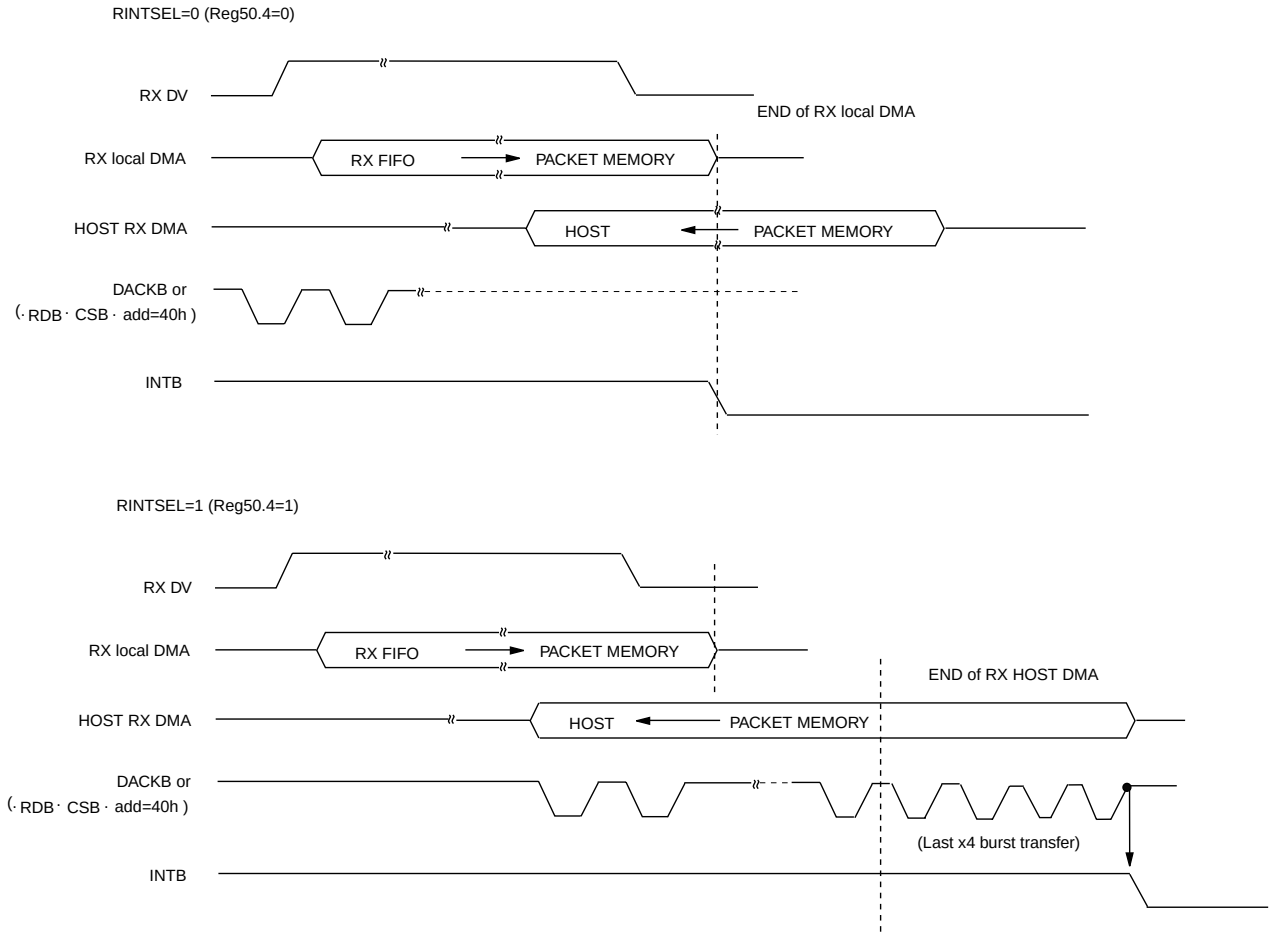
After system reset, GMAC enter its normal mode in which on chip 10/100 fast Ethernet tranceiver is used and immediately Nway auto negotiation will start setting up link in the network. The option of using a 3rd party tranceiver, such as 10/100 fast Ethernet tranceiver or HomePNA tranceiver is possible through the MII (Media Independent Interface) interface. Even if both fast Ethernet connection and HomePNA connection are desired, GMAC can allow user to switch between these two connection through register setup.
When MII mode is chosen, both Nway and on chip tranceiver are isolated from the internal MAC logic, so all data are from and to through the MII interface.



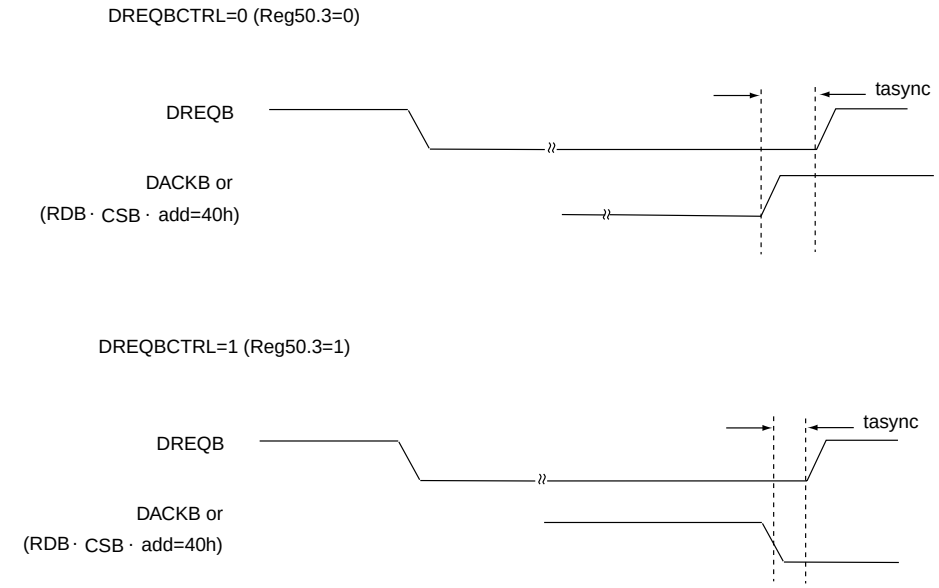

**EEPROM Read Cycle**




**EEPROM Write Cycle**



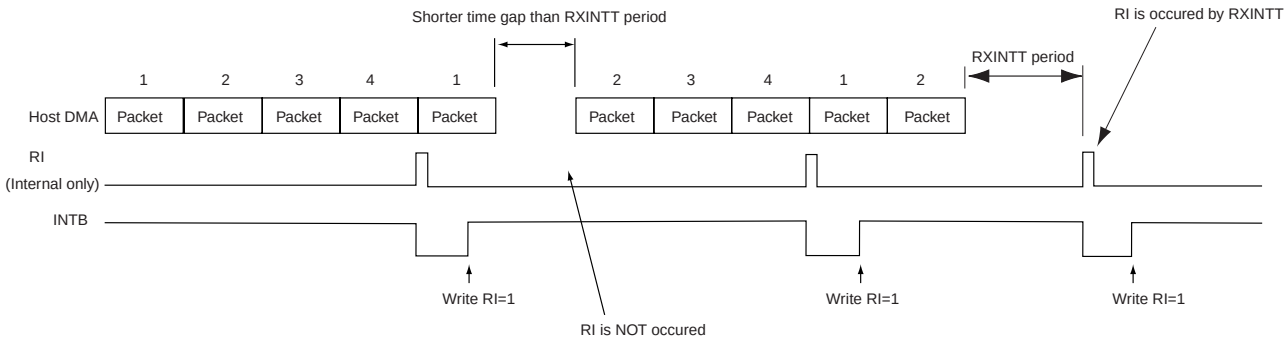

**RECEIVE INTERRUPT ASSERTION TIMING DIAGRAM**



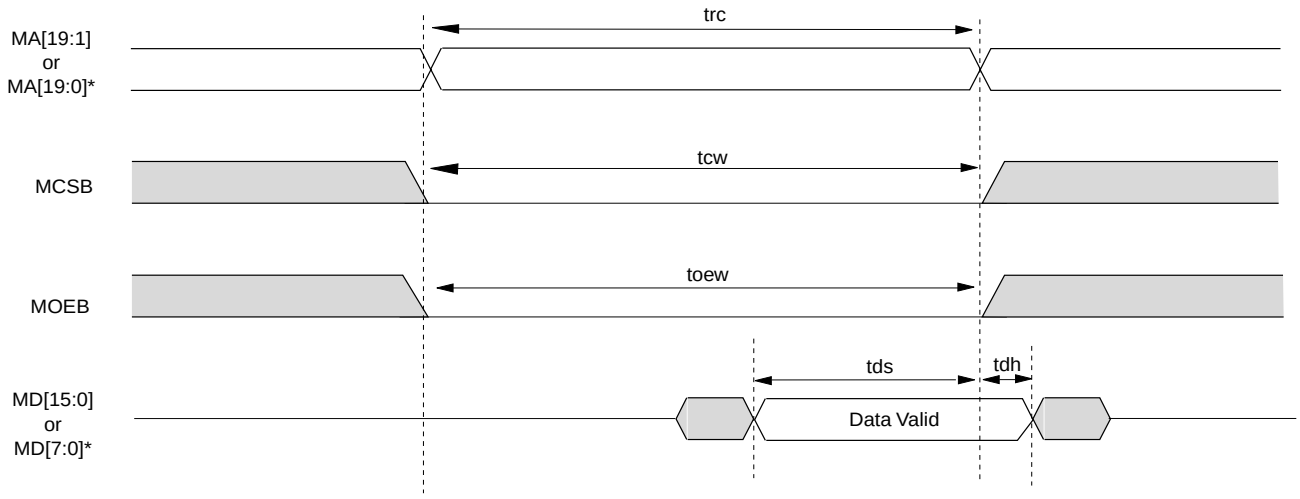

**DREQB TIMING CONTROL**

## DREQB TIMING CONTROL

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| DREQB deassertion delay | tasync | 5 | 7+1 Tclk | ns<br>Tclk=20ns |




RXINTT start time definition



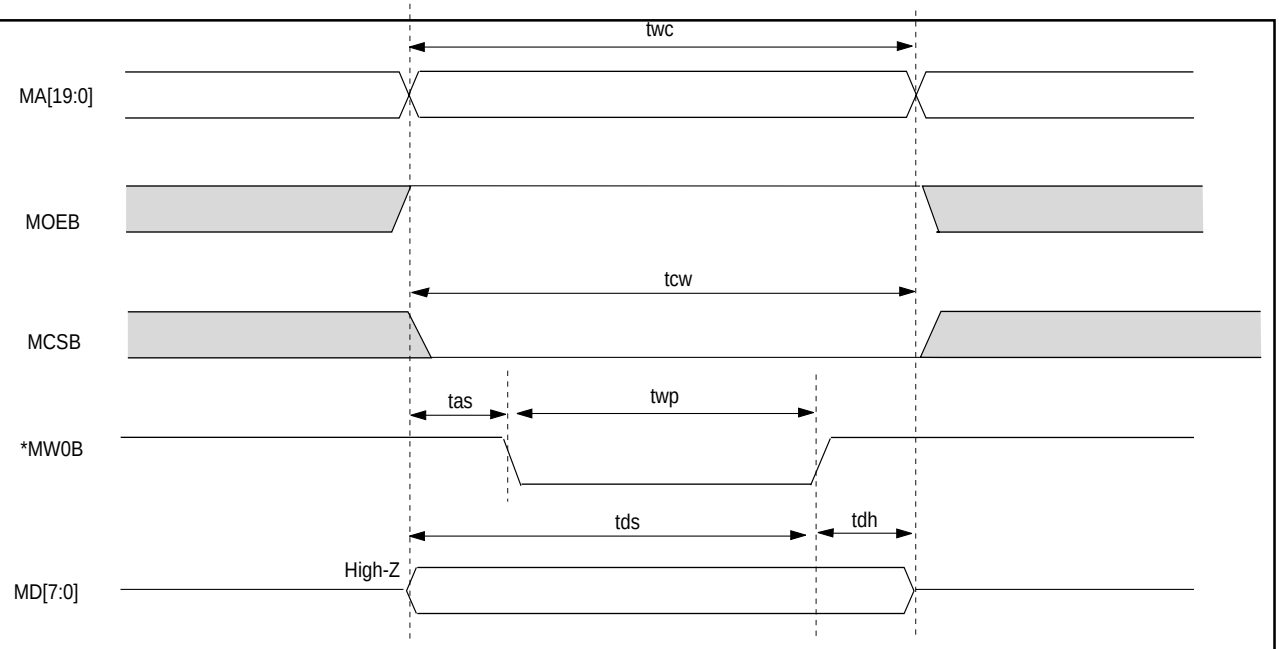

**16/8 BIT PACKET MEMORY READ CYCLE**

* 8-bit packet memory

## READ CYCLE

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Read Cycle Time | trc | 35 | 40 | ns |
| Chip Select Pulse Width | tcw | 35 | 40 | ns |
| Output Enable Pulse Width | toew | 35 | 40 | ns |
| Data Hold from Address Change | tdh | 0 | - | ns |
| Data Setup to MOEB Rising Edge | tds | 10 | - | ns |

**Note : MA[19:0], MOEB, MCSB are asserted at the same internal clock edge.**



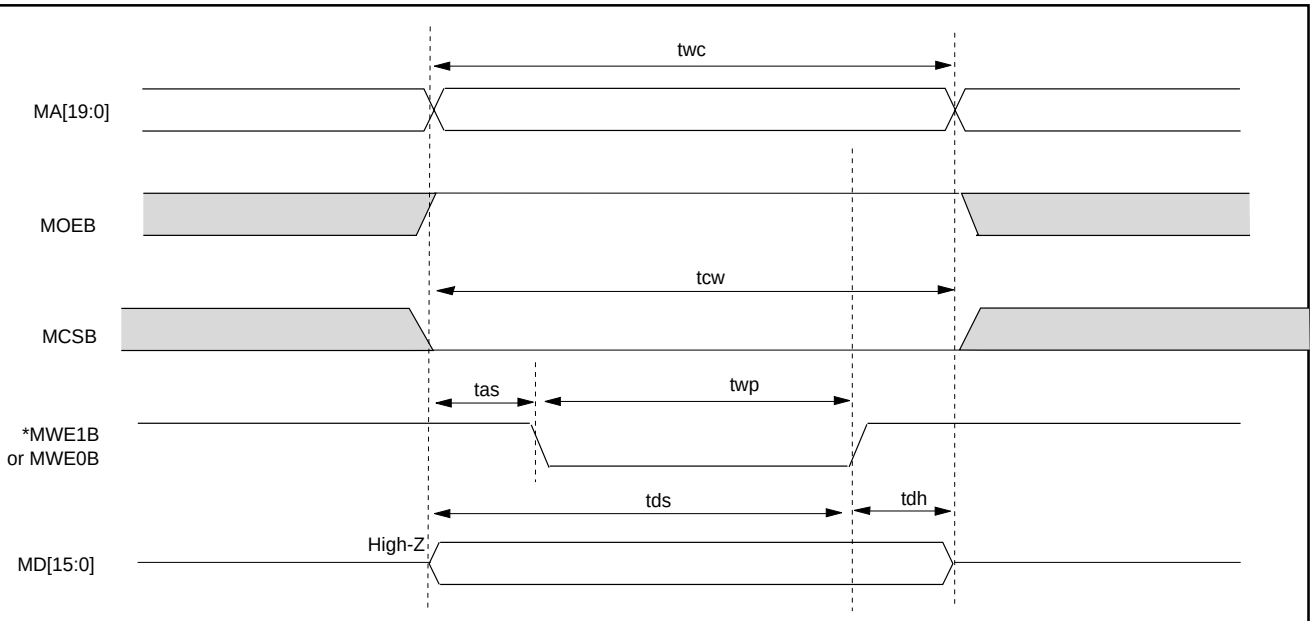

* In byte mode, only MWE0B is used.

**8 BIT PACKET MEMORY WRITE CYCLE**

## WRITE CYCLE

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Write Cycle Time | twc | 35 | 40 | ns |
| Chip Select Pulse Wdith | tcw | 35 | 40 | ns |
| Address Set-up Time | tas | 5 | - | ns |
| Write Pulse Width (OE-High) | twp | 18 | - | ns |
| Data Setup To Write Rising Edge | tds | 25 | 28 | ns |
| Data Hold from MWEB Deassertion | tdh | 10 | - | ns |

**Note : MA[19:0], MOEB, MCSB are asserted at the same internal clock edge.**

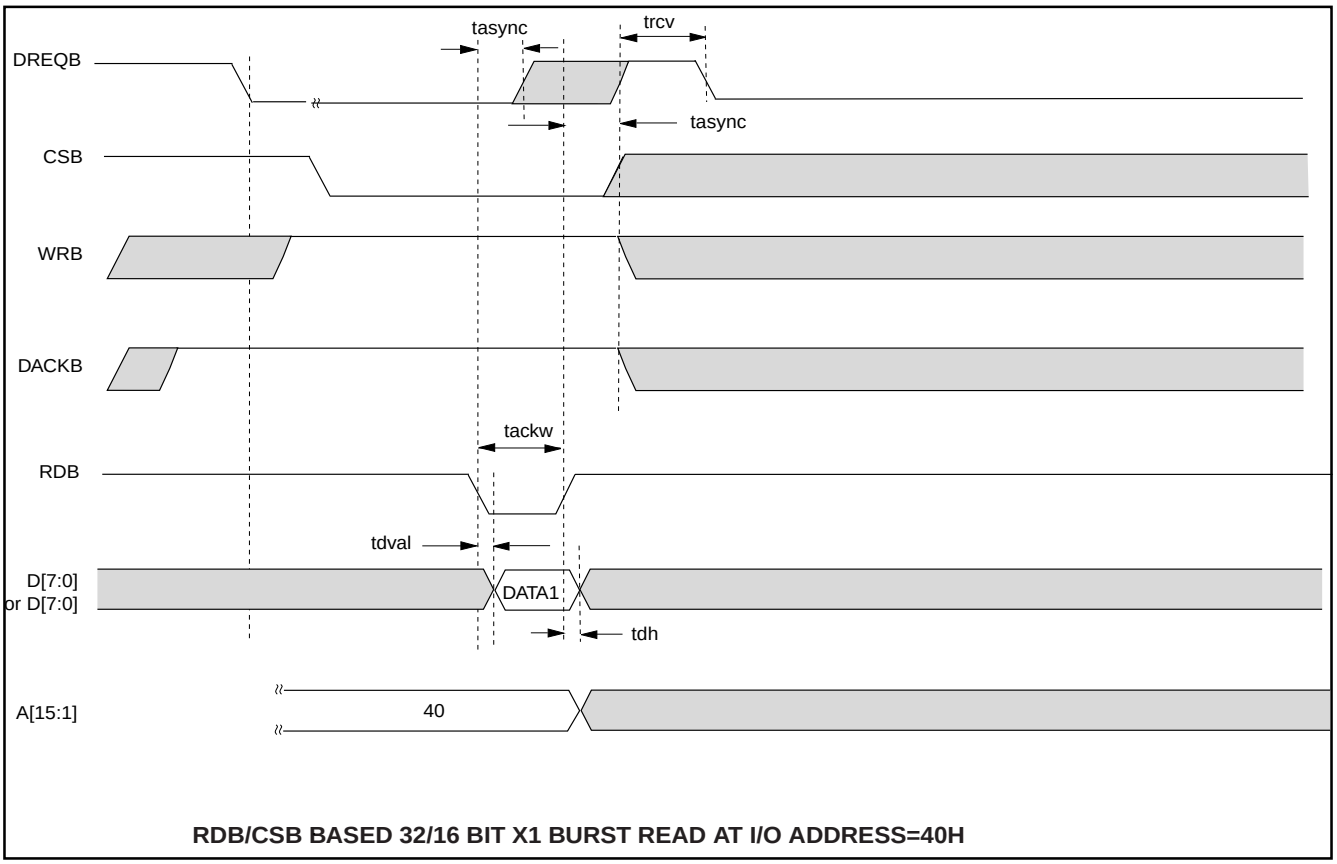



**16 BIT PACKET MEMORY WRITE CYCLE**

## WRITE CYCLE

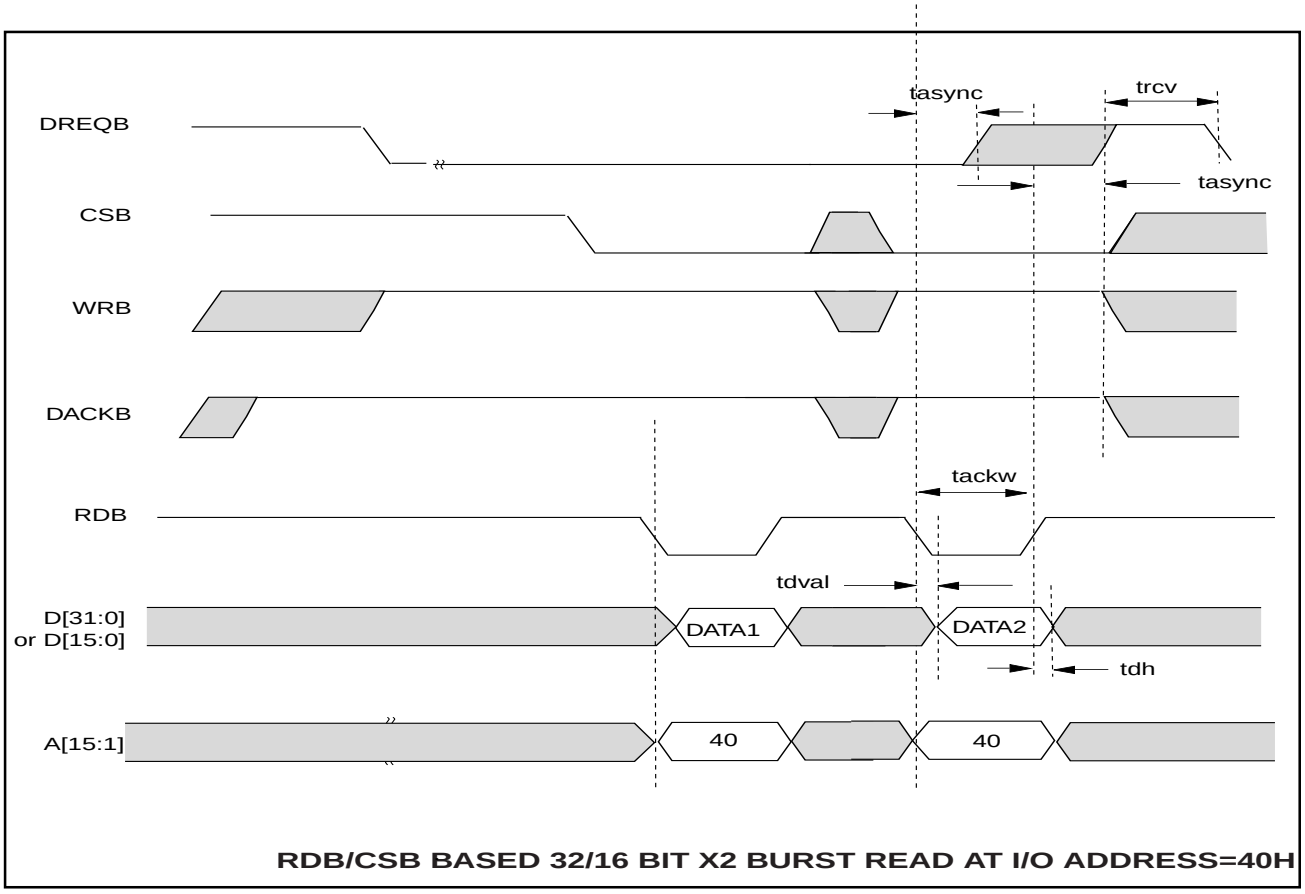
| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Write Cycle Time | twc | 35 | 40 | ns |
| Chip Select Pulse Wdith | tcw | 35 | 40 | ns |
| Address Set-up Time | tas | 5 | - | ns |
| Write Pulse Width (OE-High) | twp | 18 | - | ns |
| Data Setup To Write Rising Edge | tds | 25 | 28 | ns |
| Data Hold from MWEB Deassertion | tdh | 10 | - | ns |

**Note : MA[19:0], MOEB, MCSB are asserted at the same internal clock edge.**



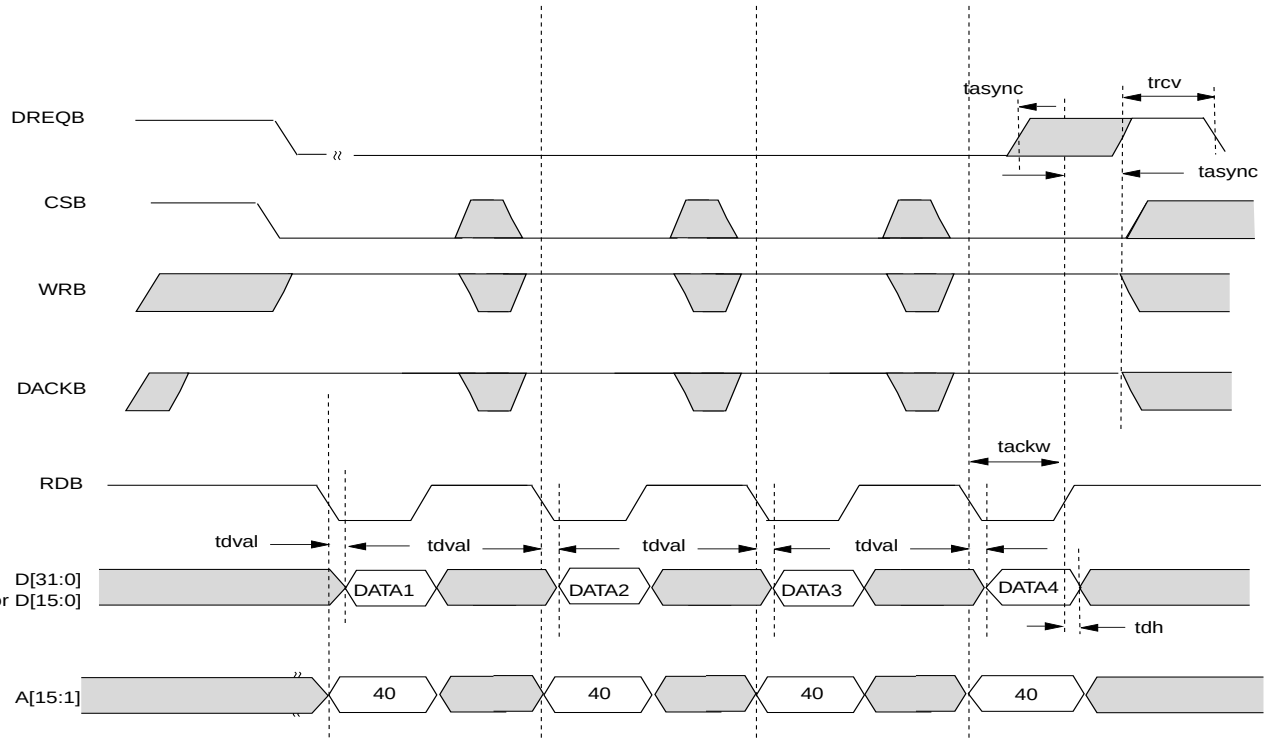

**RDB/CSB BASED 32/16 BIT X1 BURST READ AT I/O ADDRESS=40H**

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| DACKB Pulse Width | tackw | 30 | | ns |
| DREQB Recovery Time | trcv | 20 | | ns |
| Read Data Valid Delay | tdval | 7 | 10 | ns |
| Read Data Hold Time | tdh | 3 | | ns |
| DREQB deassertion delay | tasync | 5 | 7+1Tclk | ns, Tclk=20ns |



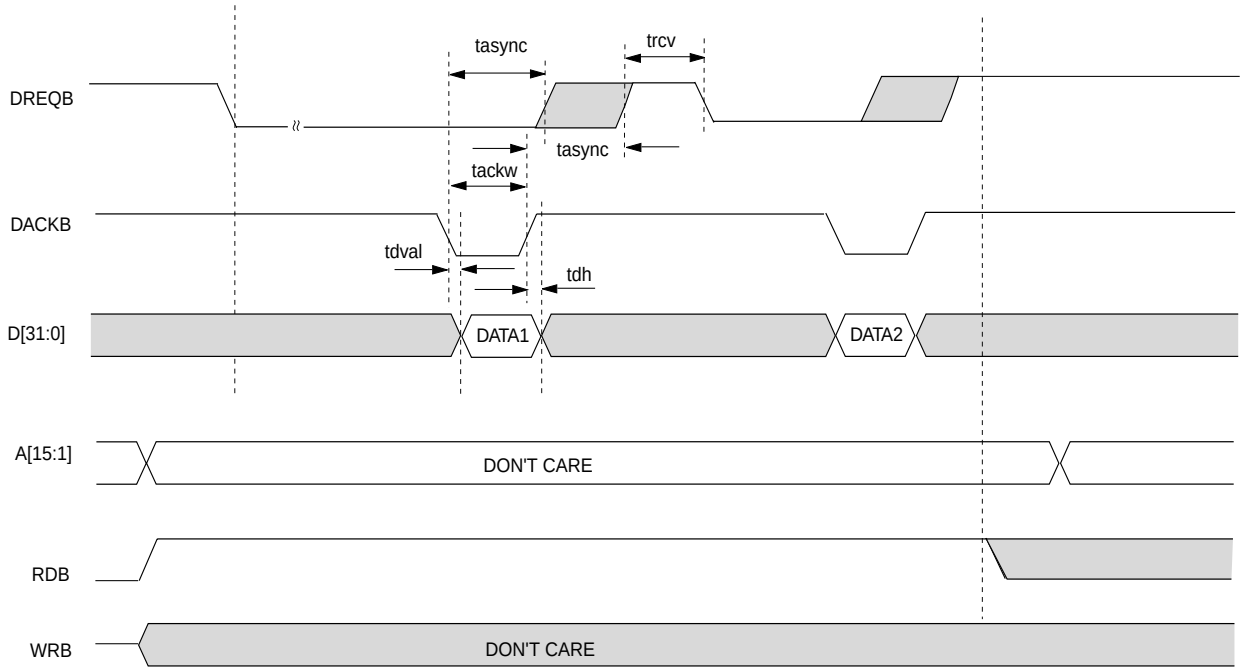

**RDB/CSB BASED 32/16 BIT X2 BURST READ AT I/O ADDRESS=40H**

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| DACKB Pulse Width | tackw | 30 | | ns |
| DREQB Recovery Time | trcv | 20 | | ns |
| Read Data Valid Delay | tdval | 7 | 10 | ns |
| Read Data Hold Time | tdh | 3 | | ns |
| DREQB deassertion delay | tasync | 5 | 7+1Tclk | ns, Tclk=20ns |



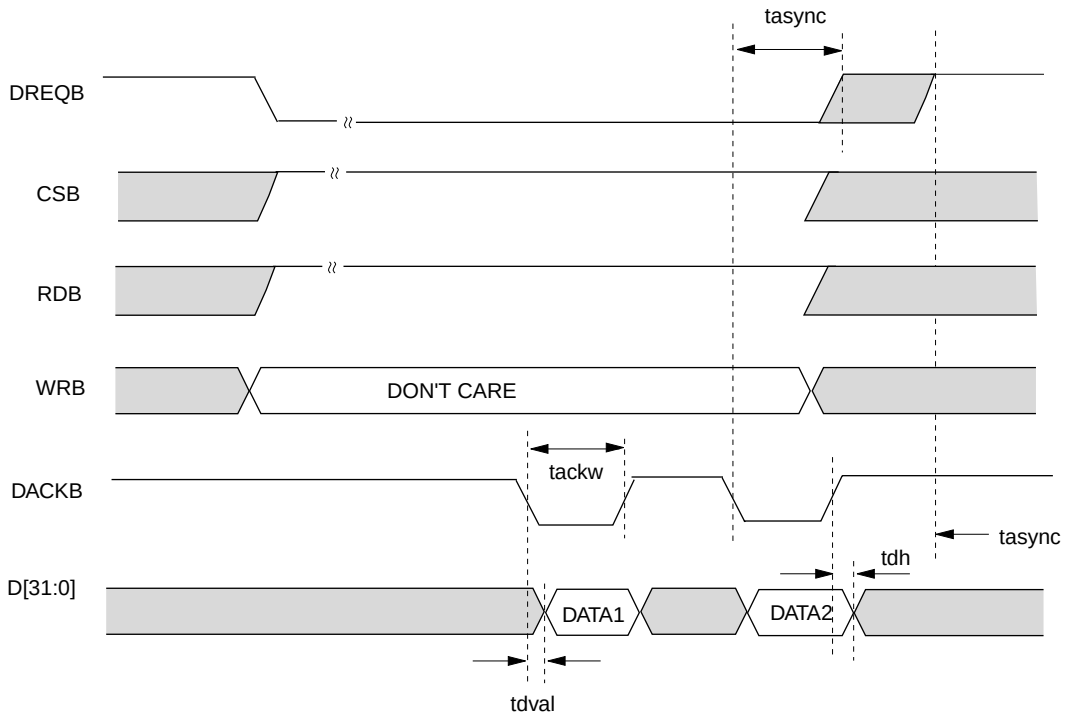

**RDB/CSB BASED 32/16 BIT X4 BURST READ AT I/O ADDRESS=40H**

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| DACKB Pulse Width | tackw | 30 | | ns |
| DREQB Recovery Time | trcv | 20 | | ns |
| Read Data Valid Delay | tdval | 7 | 10 | ns |
| Read Data Hold Time | tdh | 3 | | ns |
| DREQB deassertion delay | tasync | 5 | 7+1Tclk | ns, Tclk=20ns |



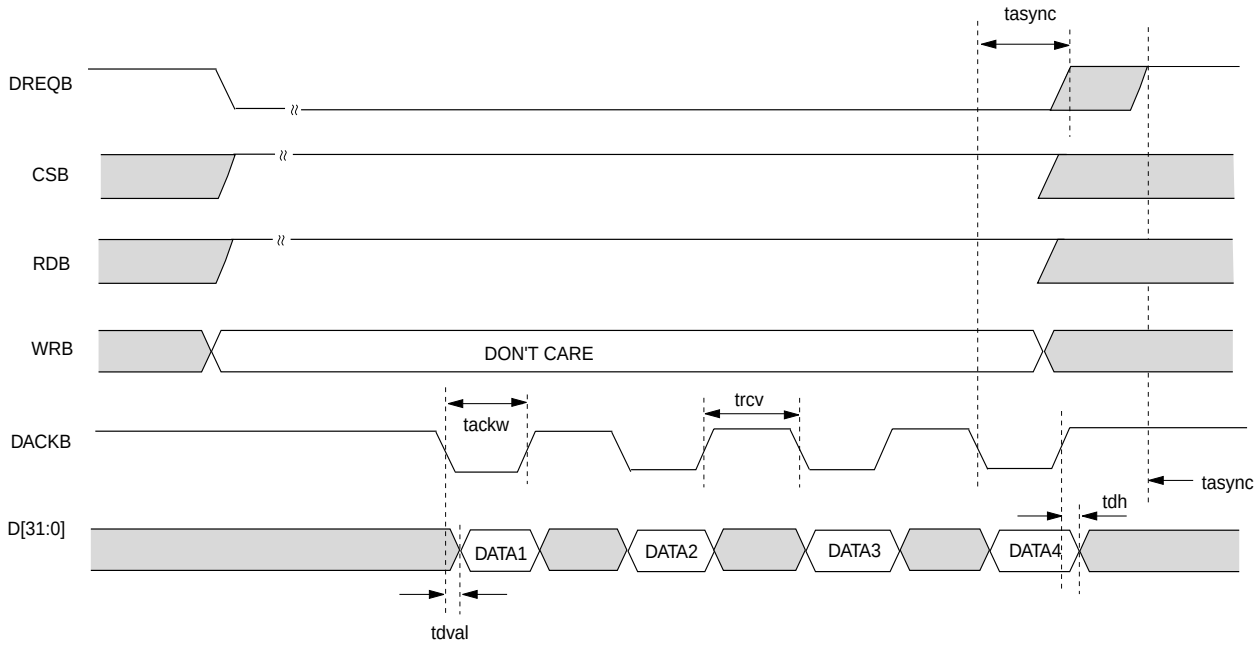

**DACKB BASED 32/16 BITS X1 BURST READ**

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| DACKB Pulse Width | tackw | 25 | | ns |
| DREQB Recovery Time | trcv | 20 | | ns |
| Read Data Valid Delay | tdval | 3 | 10 | ns |
| Read Data Hold Time | tdh | 3 | | ns |
| DREQB deassertion delay time | tasync | 5 | 7+1Tclk | ns, Tclk=20ns |



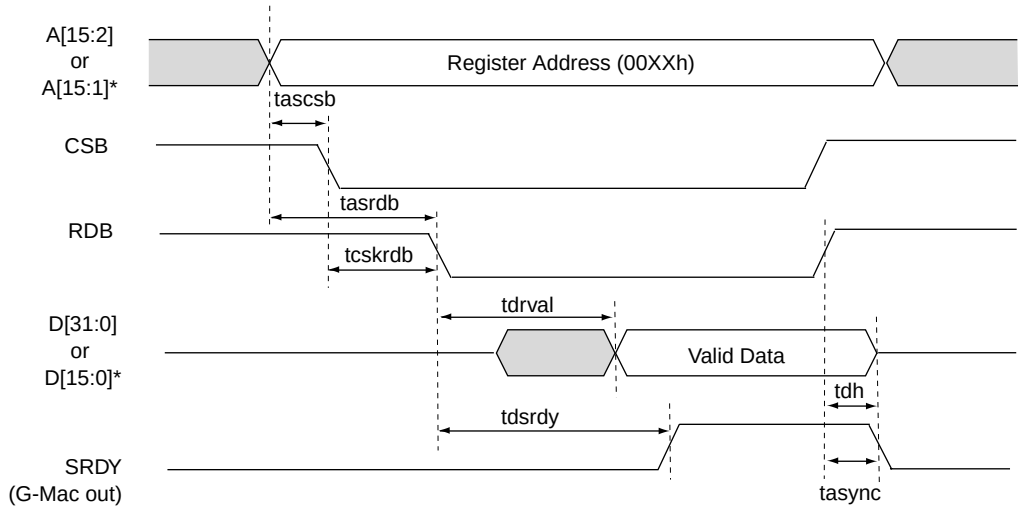

**DACKB BASED 32/16 BIT X2 BURST READ**

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| DACKB Pulse Width | tackw | 30 | | ns |
| DREQB Recovery Time | trcv | 20 | | ns |
| Read Data Valid Delay | tdval | 5 | 7 | ns |
| Read Data Hold Time | tdh | 3 | | ns |
| DREQB deassertion delay time | tasync | 5 | 7+1Tclk | ns, Tclk=20ns |




**DACKB BASED 32/16 BIT X4 BURST READ**

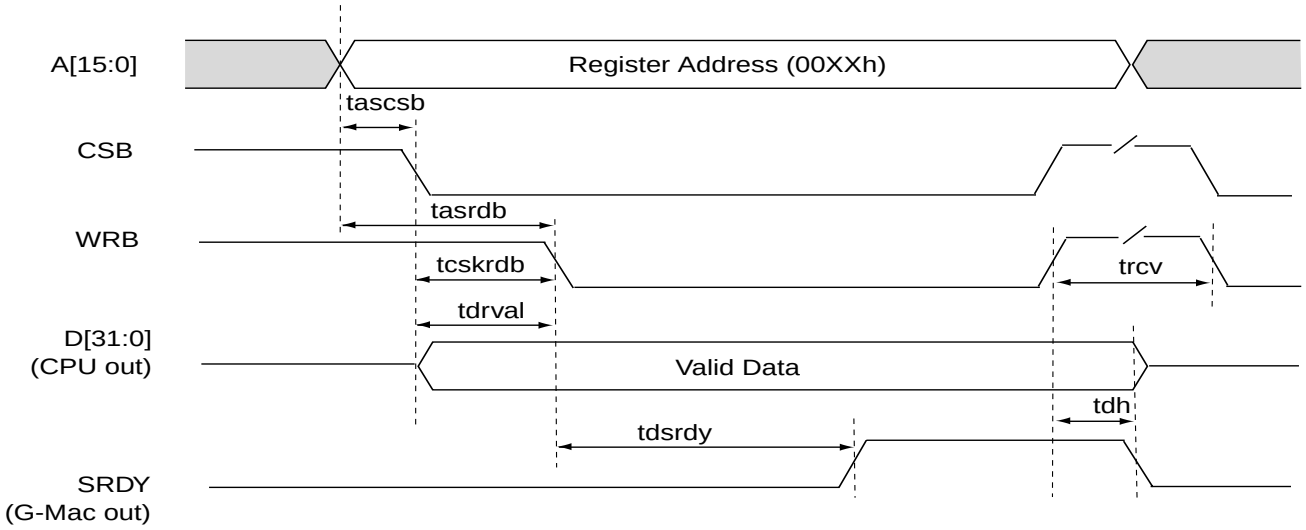
| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| DACKB Pulse Width | tackw | 30 | | ns |
| DREQB Recovery Time | trcv | 20 | | ns |
| Read Data Valid Delay | tdval | 5 | 7 | ns |
| Read Data Hold Time | tdh | 3 | | ns |
| DREQB deassertion delay time | tasync | 5 | 7+1Tclk | ns, Tclk=20ns |




**32/16 BIT HOST REGISTER ( non-IORD port ) READ**

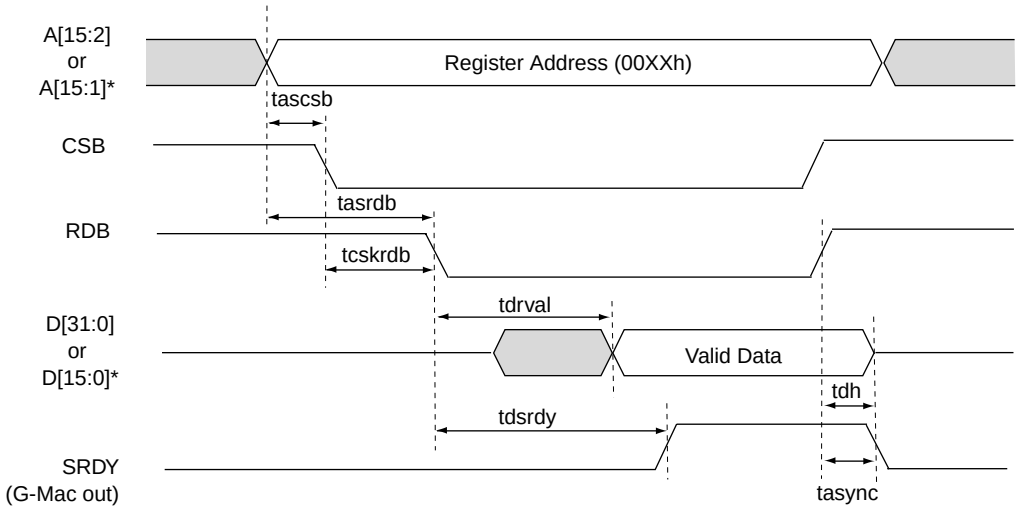
* 16-bit Host interface

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Address setup time (to CSB) | tascsb | 0 | | ns |
| Address setup time (to RDB) | tasrdb | 0 | | ns |
| CSB assert to RDB assert | tcskrdb | 0 | | ns |
| RDB assert to Valid Data output | tdval | 10 | 16 | ns |
| RDB assert to SRDY assert | tdsrdy | 7ns | 1Tclk+10ns | Tclk=20ns |
| Data hold time (from RDB) | tdh | 4 | 7 | ns |
| SRDY hold time (form RDB) | tasync | 0.5Tclk+7ns | 1.5Tclk+10ns | ns |




**32/16 BIT HOST REGISTER ( non-TWD PORT ) WRITE**

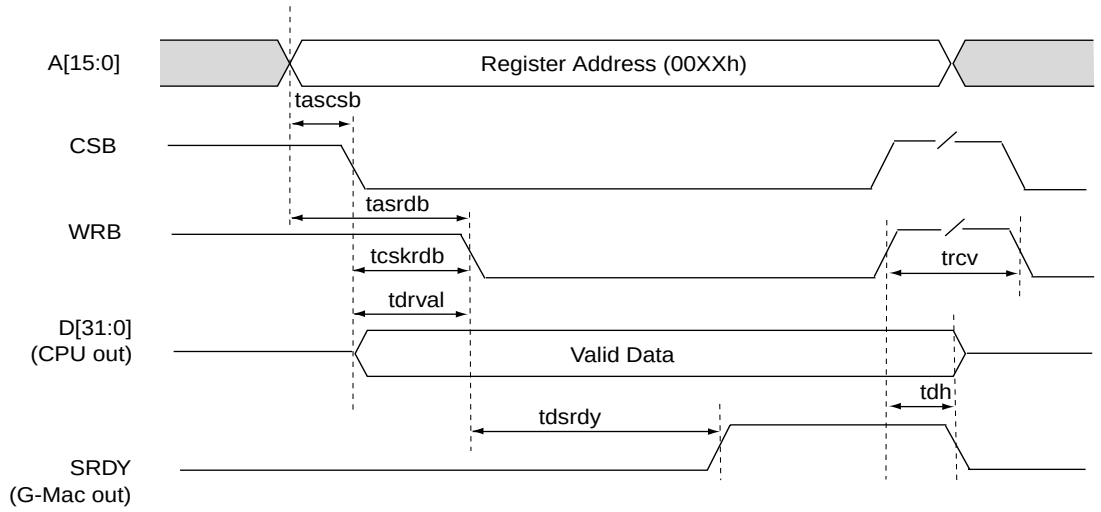
| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Address setup time (to CSB) | tascsb | 0 | | |
| Address setup time (to WRB) | tasrdb | 0 | | |
| CSB assert to WRD assert | tcskrdb | 0 | | |
| Data setup to WRB | tdval | 0 | | |
| WRB assert to SRDY assert | tdsrdy | 1.5Tclk+7ns | 2.5Tclk+10ns | Tclk=20ns |
| Data hold time (from WRB) | tasync | 0 | | |
| SRDY hold time (from WRB) | tdh | 0.5Tclk+7ns | 1.5Tclk+10ns | ns |
| WRB Recovery time | trcv | 1.5Tclk | | |




**32/16 BIT IORD PORT READ**

* 16-bit Host interface

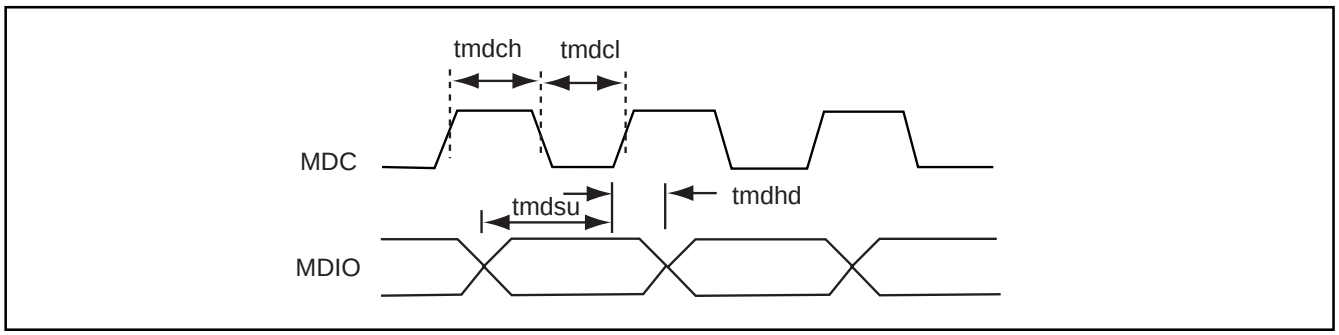
| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Address setup time (to CSB) | tascsb | 0 | | ns |
| Address setup time (to RDB) | tasrdb | 0 | | ns |
| CSB assert to RDB assert | tcskrdb | 0 | | ns |
| RDB assert to Valid Data output | tdval | 2Tclk+10 | 9Tclk+16ns | |
| RDB assert to SRDY assert | tdsrdy | 2Tclk+7ns | 9Tclk+10ns | Tclk=20ns |
| Data hold time (from RDB) | tdh | 4 | 7 | ns |
| SRDY hold time (form RDB) | tasync | 0.5Tclk+7ns | 1.5Tclk+10ns | ns |




**32/16 BIT HOST TWD PORT REGISTER WRITE**

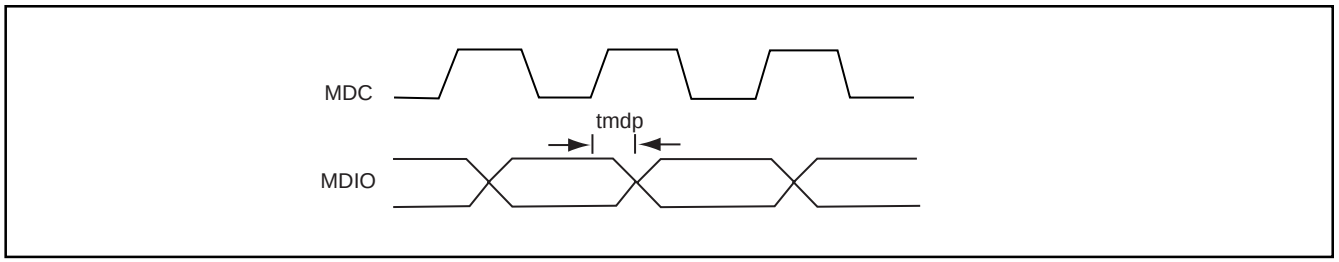
| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Address setup time (to CSB) | tascsb | 0 | | |
| Address setup time (to WRB) | tasrdb | 0 | | |
| CSB assert to WRD assert | tcskrdb | 0 | | |
| Data setup to WRB | tdval | 0 | | |
| WRB assert to SRDY assert | tdsrdy | 2Tclk+7ns | 9Tclk+10ns | Tclk=20ns |
| Data hold time (from WRB) | tasync | 0 | | |
| SRDY hold time (from WRB) | tdh | 0.5Tclk+7ns | 1.5Tclk+10ns | ns |
| WRB Recovery time | trcv | 1.5Tclk | | |

**MII management signal MDIO timing for GMAC :**




| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| tmdch | MDC high time | 200 | | ns |
| tmdcl | MDC low time | 200 | | ns |
| tmdsu | MDIO to MDC high setup time | 10 | | ns |
| tmdhd | MDIO to MDC high hold time | 10 | | ns |

**MII management signal MDIO timing sourced by PHY:**




| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| tmdp | MDC high to MDIO data valid | 2 | 300 | ns |

## 8.0 DC CHARACTERISTICS

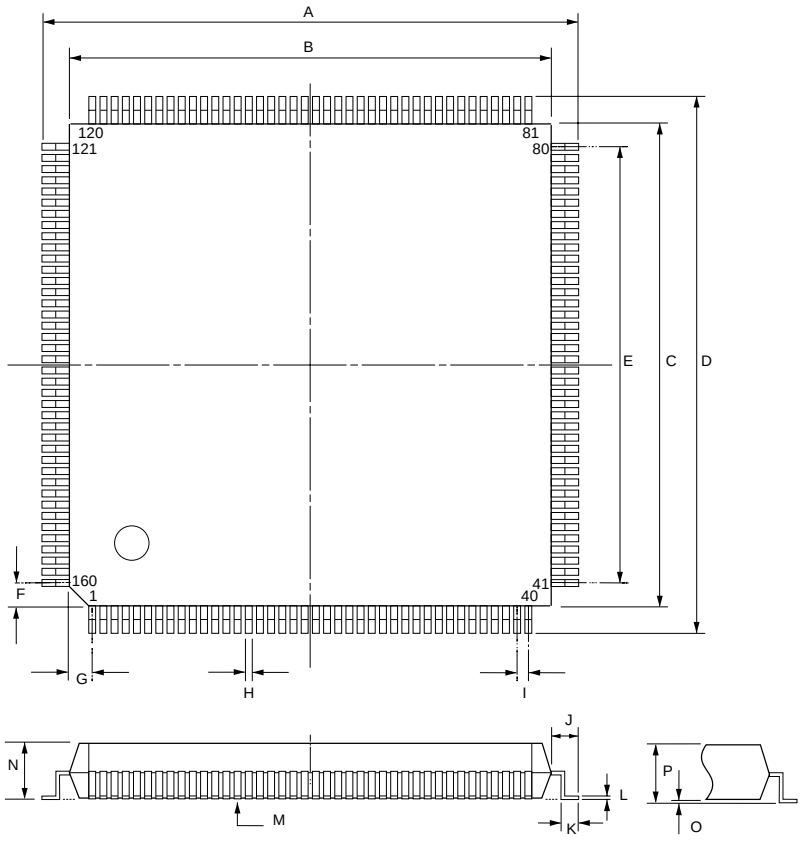
| Symbol | Parameter | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| TTL/PCI Input/Output | | | | | |
| Voh | Minimum High Level Output Voltage | Ioh=-4mA | 2.4 | | V |
| Vol | Maximum Low Level Output Voltage | Iol=+4mA | | 0.4 | V |
| Vih | Minimum High Level Input Voltage | | 2.0 | | V |
| Vil | Maximum Low Level Input Voltage | | | 0.8 | V |
| Iin | Input Current | Vi=VCC or GND | -1.0 | +1.0 | uA |
| Ioz | Minimum TRI-STATE Output Leakage Current | Vout=VCC or GND | -10 | +10 | uA |
| LED Output Driver | | | | | |
| Vlol | LED turn on Output Voltage | Iol=16mA | | 0.4 | V |
| Idd | Average Supply Current | CKREF=25MHz | 160 | 230 | mA |
| Ianalog | Average Analog Current | Full duplex | 120 | 160 | mA |
| Irx | Average RX Current | Full duplex | 50 | 70 | mA |
| Itx | TXOP, TXON Max Output Current | Max swing 1V/pin | 35 | 50 | mA |
| Vdd Average Supply Voltage | | | 4.75V | 5.25V | V |
| Clock | 25MHz±30ppm | | | | |

## 9.0 PACKAGE INFORMATION

### 160-Pin Plastic Quad Flat Pack

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 31.20 ± .30 | 1.228 ± .12 |
| B | 28.00 ± .10 | 1.102 ± .004 |
| C | 28.00 ± .10 | 1.102 ± .004 |
| D | 31.20 ± .30 | 1.228 ± .012 |
| E | 25.35 | .999 |
| F | 1.33 [REF.] | .052 [REF.] |
| G | 1.33 [REF.] | .052 [REF.] |
| H | .30 [Typ.] | .012 [Typ.] |
| I | .65 [Typ.] | .026 [Typ.] |
| J | 1.60 [REF.] | .063 [REF.] |
| K | .80 ± .20 | .031 ± .008 |
| L | .15 [Typ.] | .006 [Typ.] |
| M | .10 max. | .004 max. |
| N | 3.35 max. | .132 max. |
| O | .10 min. | .004 min. |
| P | 3.68 max. | .145 max. |

**NOTE:** Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



## REVISION HISTORY

| REVISION | DESCRIPTION | PAGE | DATE |
|---|---|---|---|
| 0.9.9 | contents modify MX98728OKI-->MX98728EC | | |
| | modify RESET, ST0, ST1 description | P8 | Apr/26/2000 |
| | modify HBD as reserved bit | P9 | |
| | modify FRAGIM, FIFOEIM description | P12 | |
| | modify RXINTT description | P15 | |
| | modify ANE description | P18 | |
| | modify TX FIFORST, RXFIFORST description | P22 | |
| | modify " prior to the transmission in the direct FIFO mode" paragraph | P29 | |
| | modify Receive buffer full description | P36 | |
| | modify Address filtering block diagram | P41 | |
| | modify Recerive interrupt section about RXINTT timer's function | P45 | |
| | modify Flow chart of fragment counter programming | p46 | |
| | modify Timing diagram for RINTSEL=1 | p51 | |
| | add RXINTT start time definition waveform | P52 | |
| | add Features | P1 | May/16/2000 |
| | modify block diagram | P2 | |
| | add combo application | P3 | |
| | modify pin definitions : 126~129, 144, 145, 43~46, 85, 86 | P4 | |
| | add host bus interface (pin126~129) | P5 | |
| | add packet memory interface (pin46~43) | P6 | |
| | modify miscellaneous (pin145, 144) | P8 | |
| | add VDD/GND Pins (85, 86) | P8 | |
| | modify GMAC Test Register A & B | P11,12 | |
| | modify GMAC Configuration A register (Bit 32.4) | P20 | |
| | modify MISC Control Register (Bit 3D.0) | P23 | |
| | add 6.1 On-chip Transceiver vs MII Interface | P50 | |
| | add Management Signal timing MDIO source by STA & PHY | P67 | |
| | add top side marking | P71 | |
| | modify FRAGCNT description, A11A8EN description | P26 | Jun/01/2000 |
| | enhance Reg54~Reg56 description | P27 | Jun/09/2000 |
| 1.0 | change Reg 0.1, 0.2 description | P9 | Jul/13/2000 |
| | add Reg 1C.6 and 1C.7 descriptions | P17 | |
| | change Reg 30.0 FD bit description | P19 | |
| | add Reg 33.4, 33.5 and 33.6 descriptions | P20 | |
| | enhance Reg 3D.6 description | P23 | |
| | enhance description of fragment counter | P47 | |

## TOP SIDE MARKING

| | |
|---|---|
| MX98728EC | line 1 : MX98728 is MXIC parts No.<br>"E" :PQFP<br>"C" : commercial grade |
| C9930 | line 2 : Assembly Date Code. |
| TA777001 | line 3 : Wafer Lot No. |
| 38BAX | line 4 : "38B" : revision code,<br>"A" : bonding option<br>"X" : no used |
| TAIWAN | line 5 : State |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