



# Complementary Silicon Plastic Power Transistors

... designed for use in general-purpose amplifier and switching applications.

- DC Current Gain Specified to 7.0 Amperes  
 $h_{FE} = 30-150 @ I_C$   
 = 3.0 Adc — 2N6111, 2N6288  
 = 2.3 (Min) @  $I_C = 7.0$  Adc — All Devices
- Collector-Emitter Sustaining Voltage —  
 $V_{CEO(sus)} = 30$  Vdc (Min) — 2N6111, 2N6288  
 = 50 Vdc (Min) — 2N6109  
 = 70 Vdc (Min) — 2N6107, 2N6292
- High Current Gain — Bandwidth Product  
 $f_T = 4.0$  MHz (Min) @  $I_C = 500$  mAdc — 2N6288, 90, 92  
 = 10 MHz (Min) @  $I_C = 500$  mAdc — 2N6107, 09, 11
- TO-220AB Compact Package

## \*MAXIMUM RATINGS

Rating	Symbol	2N6111 2N6288	2N6109	2N6107 2N6292	Unit
Collector-Emitter Voltage	$V_{CEO}$	30	50	70	Vdc
Collector-Base Voltage	$V_{CB}$	40	60	80	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0			Vdc
Collector Current — Continuous Peak	$I_C$	7.0 10			Adc
Base Current	$I_B$	3.0			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	40 0.32			Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150			$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	$^\circ\text{C/W}$

\*Indicates JEDEC Registered Data.

**PNP**  
**2N6107**  
**2N6109\***  
**2N6111**  
**NPN**  
**2N6288**  
**2N6292\***

\*ON Semiconductor Preferred Device

**7 AMPERE**  
**POWER TRANSISTORS**  
**COMPLEMENTARY**  
**SILICON**  
**30-50-70 VOLTS**  
**40 WATTS**

STYLE 1:  
 PIN 1. BASE  
 2. COLLECTOR  
 3. EMITTER  
 4. COLLECTOR

**CASE 221A-09**  
**TO-220AB**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

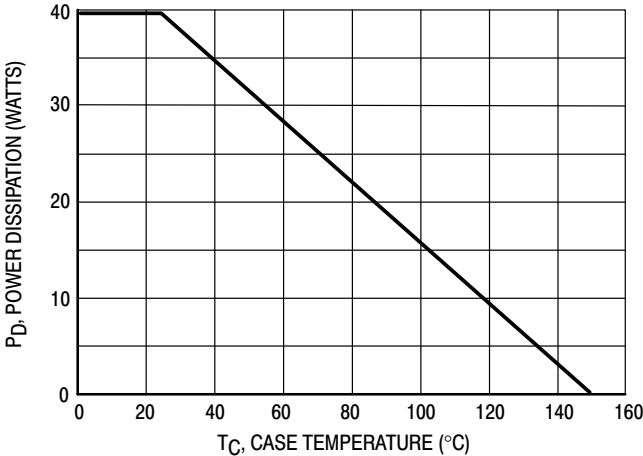


Figure 1. Power Derating

## 2N6107 2N6109 2N6111 2N6288 2N6292

\*ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 100\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	30 50 70	— — —	Vdc
				2N6111, 2N6288 2N6109 2N6107, 2N6292
Collector Cutoff Current ( $V_{CE} = 20\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 40\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 60\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	— — —	1.0 1.0 1.0	mAdc
				2N6111, 2N6288 2N6109 2N6107, 2N6292
Collector Cutoff Current ( $V_{CE} = 40\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 60\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 80\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 30\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ ) ( $V_{CE} = 50\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ ) ( $V_{CE} = 70\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	$I_{CEX}$	— — — — — —	100 100 100 2.0 2.0 2.0	$\mu\text{Adc}$   mAdc
				2N6111, 2N6288 2N6109 2N6107, 2N6292 2N6111, 2N6288 2N6109 2N6107, 2N6292
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	1.0	mAdc

### ON CHARACTERISTICS (1)

DC Current Gain ( $I_C = 2.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 2.5\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 7.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$h_{FE}$	30 30 30 2.3	150 150 150 —	—
				2N6107, 2N6292 2N6109 2N6111, 2N6288 All Devices
Collector–Emitter Saturation Voltage ( $I_C = 7.0\text{ Adc}$ , $I_B = 3.0\text{ Adc}$ )	$V_{CE(sat)}$	—	3.5	Vdc
Base–Emitter On Voltage ( $I_C = 7.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	—	3.0	Vdc

### DYNAMIC CHARACTERISTICS

Current Gain — Bandwidth Product (2) ( $I_C = 500\text{ mAdc}$ , $V_{CE} = 4.0\text{ Vdc}$ , $f_{test} = 1.0\text{ MHz}$ )	$f_T$	4.0 10	— —	MHz
				2N6288, 92 2N6107, 09, 11
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1.0\text{ MHz}$ )	$C_{ob}$	—	250	pF
Small–Signal Current Gain ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ , $f = 50\text{ kHz}$ )	$h_{fe}$	20	—	—

\*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

(2)  $f_T = |h_{fe}| \cdot f_{test}$ .

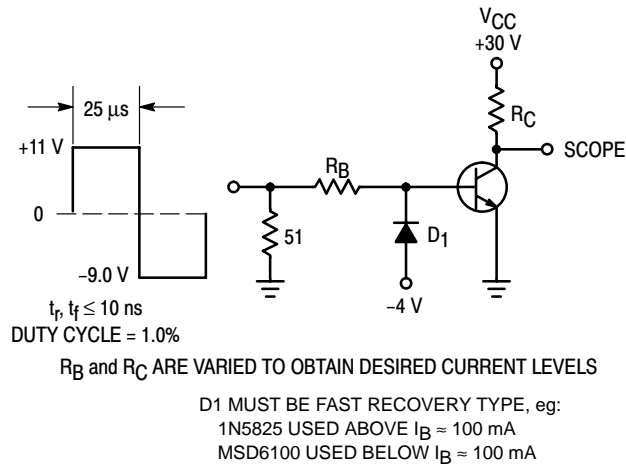


Figure 2. Switching Time Test Circuit

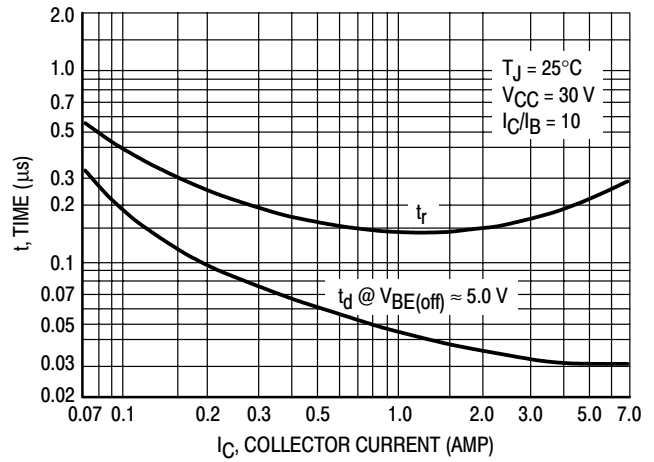


Figure 3. Turn-On Time

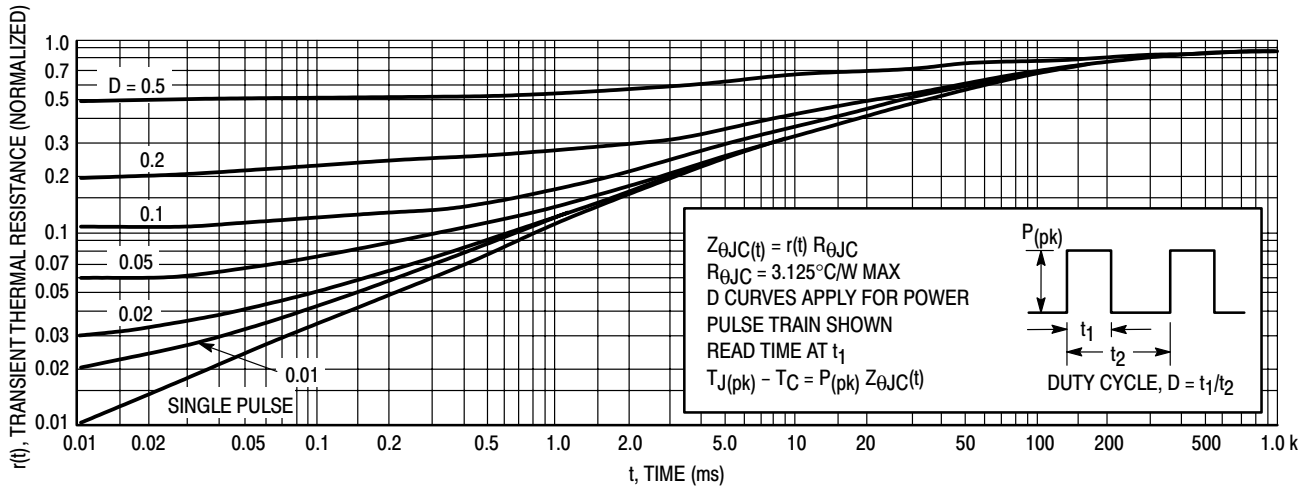


Figure 4. Thermal Response

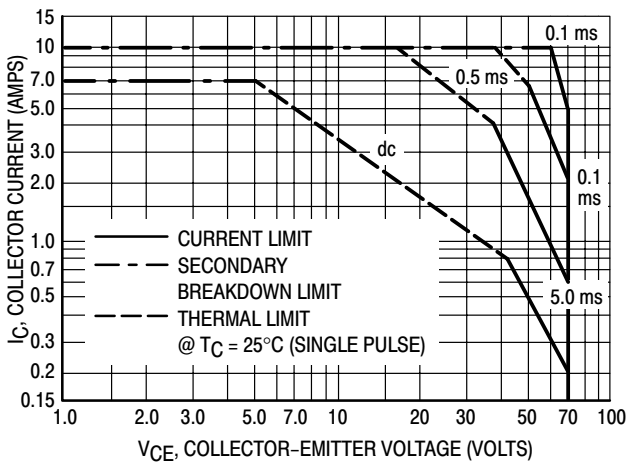


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

2N6107 2N6109 2N6111 2N6288 2N6292

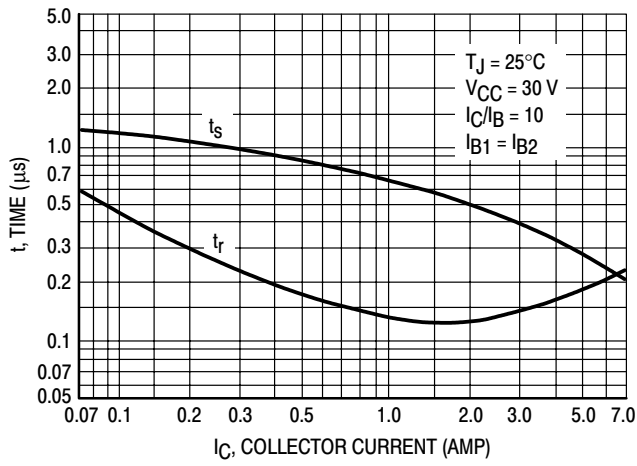


Figure 6. Turn-Off Time

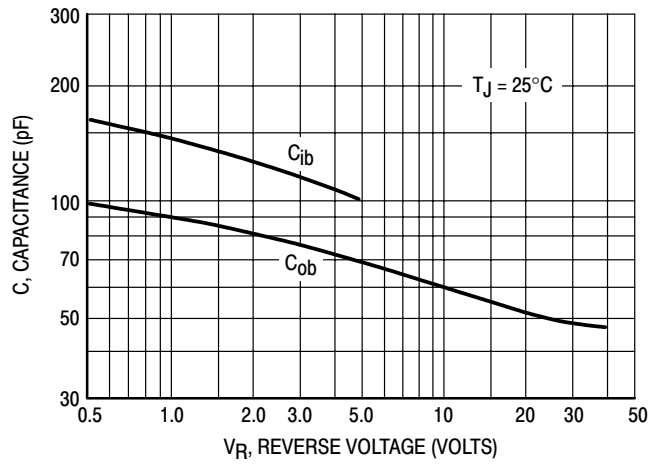
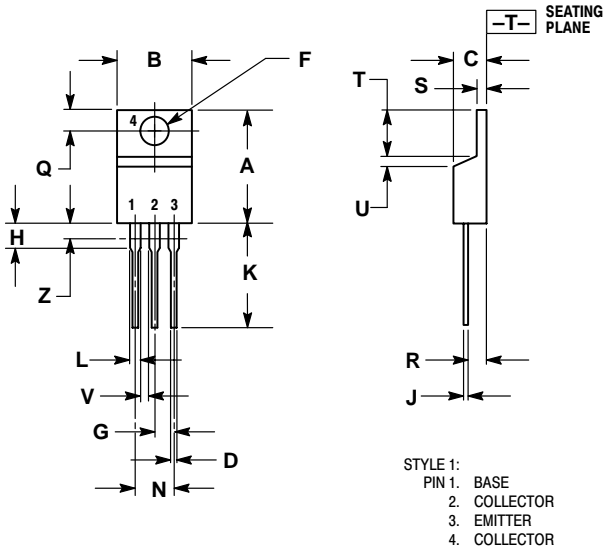


Figure 7. Capacitance

PACKAGE DIMENSIONS

TO-220AB  
CASE 221A-09  
ISSUE AA



- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.  
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

## Notes

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